Cat. No. W62-E1-2

OMRON USER'S MANUAL

Programmable Controller

Model SYSMAC-C120

OMRON TATEISI ELECTRONICS CO.

FEATURES

Package type small multi-function PC

Best suited for small- and medium-scale control

The SYSMAC-C120 is best suited for a small- and medium-scale control where 32 to 256 I/O Points are required.

Component type

Both the CPU and the expansion I/O rack are component type which are only 100mm in depth. They can be mounted on a DIN rail with a DIN rail attachment.

Instruction words compatible with either series products

The user program of the SYSMAC-C120 is compatible with programs of the SYSMAC-C250 and the SYSMAC-C500. The same user program can be used within the SYSMAC-C series products.

Wide variation of I/O units

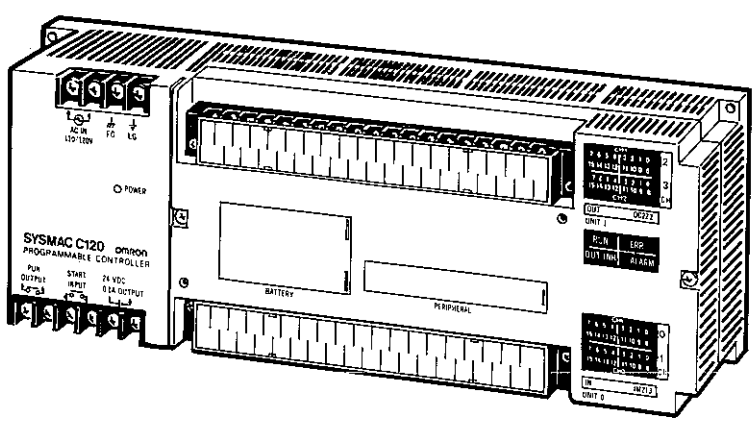
A wide variation of I/O specifications is available.

I/O unit easy to use

A terminal block type connector that can be easily connected/disconnected is employed in the I/O unit, allowing easy replacement of the unit. Additionally, each output relay can be replaced. With these features, maintainability of the I/O is significantly improved.

Same peripheral equipment usable

The same peripheral equipment can be used for all models of the SYSMAC-C series: SYSMAC-C120, SYSMAC-C250, and SYSMAC-C500.



CONTENTS

FEATURES

PART 1

CHAPTER 1 CONFIGURATION OF PC

1.1 Available types 1-1
1.2 Name of parts 1-2
1.3 System configuration 1-4
1.4 Dimensions 1-4
1.5 Wiring and power supply 1-5
1.6 Operating procedures of programmable controller 1-6

CHAPTER 2 SPECIFICATIONS

2.1 System specifications 2-1
2.2 I/O units specifications 2-2

CHAPTER 3 ASSIGNMENT OF RELAY NUMBERS

3.1 Explanation of special auxiliary relay numbers and temporary memory relay numbers 3-1
3.2 Free location concept and I/O channels 3-2

CHAPTER 4 INSTRUCTION WORDS

4.1 LOAD (LD)/AND (AND)/OR (OR)/OUTPUT (OUT) instructions 4-1
4.2 AND-LOAD (AND-LD) instruction 4-2
4.3 OR-LOAD (OR-LD) instruction 4-3
4.4 TIMER (TIM) instruction 4-3
4.5 COUNTER (CNT) instruction 4-5
4.6 TEMPORARY MEMORY RELAY (TR) instruction 4-6
4.7 END instruction 4-7
4.8 INTERLOCK [IL(FUN02)]/INTERLOCK CLEAR [ILC(FUN03)] instructions . 4-7
4.9 JUMP [JMP(FUN04)]/JUMP END [JME(FUN05)] instructions 4-8
4.10 DIAGNOSTIC [FAL(FUN06)]/FALS(FUN07)] instruction 4-9
4.11 SHIFT REGISTER [SFT(FUN10)] instruction 4-10
4.12 LATCHING RELAY [KEEP(FUN11)] instruction 4-11
4.13 UP-DOWN COUNTER [CNTR(FUN12)] instruction 4-12
4.14 DIFFERENTIATION UP [DIFU(FUN13)]/DIFFERENTIATION DOWN [DIFD(FUN14)] instructions 4-13
4.15 HIGH-SPEED TIMER [TIMH(FUN15)] instruction 4-14
4.16 WORD SHIFT [WSFT(FUN16)] instruction 4-14
4.17 COMPARE [CMP(FUN20)] instruction 4-15
4.18 MOVE [MOV(FUN21)]/MOVE NOT [MVN(FUN22)] instructions 4-16
4.19 BCD-TO-BIN CONVERSION [BIN(FUN23)] instruction 4-17
4.20 BIN-TO-BCD CONVERSION [BCD(FUN24)] instruction 4-18
4.21 ARITHMETIC SHIFT LEFT [ASL(FUN25)] instruction 4-19

4.22 ARITHMETIC SHIFT RIGHT [ASR(FUN26)] instruction 4-20
4.23 ROTATE LEFT [ROL(FUN27)] instruction 4-20
4.24 ROTATE RIGHT [ROR(FUN28)] instruction 4-21
4.25 COMPLEMENT [COM(FUN29)] instruction 4-22
4-26 ADD [ADD(FUN30)] instruction 4-22
4.27 SUBTRACT [SUB(FUN31)] instruction 4-23
4.28 MULTIPLY [MUL(FUN32)] instruction 4-24
4.29 DIVIDE [DIV(FUN33)] instruction 4-25
4.30 AND WORD [ANDW(FUN34)] instruction 4-26
4.31 OR WORD [ORW(FUN35)] instruction 4-27
4.32 EXCLUSIVE OR WORD [XORW(FUN36)] instruction 4-27
4.33 EXCLUSIVE OR NOT WORD [XNRW(FUN37)] instruction 4-28
4.34 INCREMENT [INC(FUN38)] instruction 4-29
4.35 DECREMENT [DEC(FUN39)] instruction 4-30
4.36 SET CARRY [STC(FUN40)]/CLEAR CARRY [CLC(FUN41)] instructions .. 4-31
4.37 BLOCK MOVE (FUN70) instruction 4-31
4.38 BLOCK SET (FUN71) instruction 4-32
4.39 SQUARE ROOT (FUN72) instruction 4-32
4.40 DATA EXCHANGE (FUN73) instruction 4-33
4.41 ONE DIGIT SHIFT LEFT (FUN74) instruction 4-34
4.42 ONE DIGIT SHIFT RIGHT (FUN75) instruction 4-35
4.43 4-TO-16 DECODER (FUN76) instruction 4-36
4.44 16-TO-4 ENCODER (FUN77) instruction 4-37
4.45 7-SEGMENT DECODER (FUN78) instruction 4-39
4.46 FLOATING-POINT DIVIDE (FUN79) instruction 4-40
4.47 DATA DISTRIBUTION (FUN80) instruction 4-42
4.48 DATA EXTRACTION (FUN81) instruction 4-43
4.49 BIT TRANSFER (FUN82) instruction 4-44
4.50 DIGIT TRANSFER (FUN83) instruction 4-45
4.51 LEFT/RIGHT SHIFT (FUN84) instruction 4-46
4.52 TABLE COMPARE (FUN85) instruction 4-48
4.53 WATCHDOG TIMER SETTING (FUN94) instruction 4-49
4.54 RUN STOP (FUN99) instruction 4-49

CHAPTER 5 INSTALLATION AND WIRING

5.1 Mounting locations and environmental conditions 5-1
5.2 Mounting positions within control panels 5-1
5.3 How to install within control panels 5-2

5.4 Processing of wiring within control panels 5-3
5.5 Operation at power failure 5-4
5.6 External wiring 5-4
5.7 Notes on output 5-5

CHAPTER 6 MAINTENANCE AND INSPECTION

6.1 Inspection 6-1
6.2 Troubleshooting 6-3
6.3 Abnormal symptom, possible cause, and corrective action 6-6
6.4 Diagnostic functions 6-7

PART 2

CHAPTER 7 SPECIAL I/O UNITS

7.1 Available types 7-1
7.2 Names of parts 7-2
7.3 Dimensions 7-4
7.4 A/D conversion input unit 7-5
7.5 D/A conversion output unit 7-12
7.6 High-speed counter unit 7-15
7.7 Remote I/O units 7-24
7.8 Optical transmitting I/O unit 7-26
7.9 Operation, diagnostic functions, and failure detection of remote I/O unit and optical transmitting I/O unit 7-34
7.10 Handling fiber optics cable 7-46

CHAPTER 8 GUIDE FOR SYSTEM

8.1 Host computer linkage system configuration 8-1
8.2 Programmable controller linkage configuration 8-2
8.3 I/O linkage system configuration 8-3

CHAPTER 9 PERIPHERAL EQUIPMENT

9.1 Available types 9-1
9.2 Appearance 9-2
9.3 Connection 9-3
9.4 Available functions 9-4

APPENDIXES

Appendix A List of relay numbers A-1
Appendix B List of instructions B-1

This user's manual mainly describes the programmable controller and special I/O units. For detailed information on the programming console, graphic programming console (CRT), or other peripheral equipment, please refer to each user's manual.

CHAPTER 1
CONFIGURATION OF PC

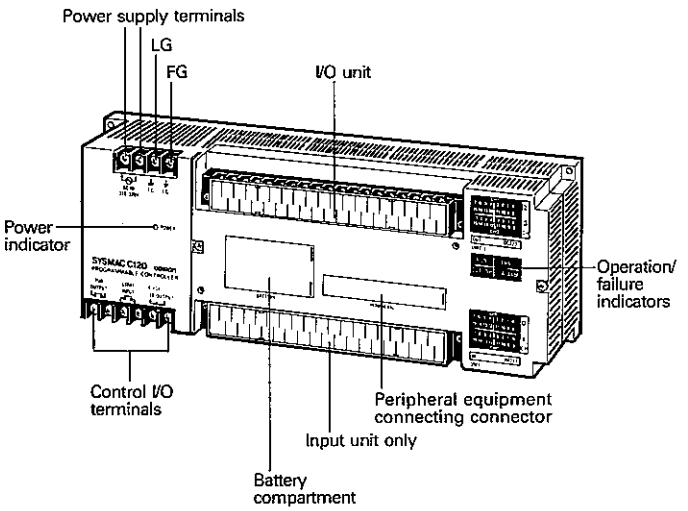
1.1 AVAILABLE TYPES

Classification		Specification	Weight	Type name
CPU rack		AC 110/120V RAM	2.5 kg max.	3G2C4-SC021-E
		AC 220/240V RAM	2.5kg max.	3G2C4-SC022-E
		AC 110/120V ROM/RAM *4	2.5kg max.	3G2C4-SC023-E
		AC 220/240V ROM/RAM *4	2.5kg max.	3G2C4-SC024-E
Expansion I/O rack		AC 110/120V for mounting I/O unit	2.5kg max.	3G2C4-SI021
		AC 220/240V for mounting I/O unit	2.5kg max.	3G2C4-SI022
		AC 110/120V for mounting I/O linkage unit	2.5kg max.	3G2C4-SI023
		AC 220/240V for mounting I/O linkage unit	2.5kg max.	3G2C4-SI024
		AC 110/120V for mounting A/D conversion input, D/A conversion output, or high-speed counter unit	2.5kg max.	3G2C4-SI025
		AC 220/240V for mounting A/D conversion input, D/A conversion output, or high-speed counter unit	2.5kg max.	3G2C4-SI026
		AC 110/120V for mounting remote I/O unit	2.5kg max.	3G2C4-SI027
		AC 220/240V for mounting remote I/O unit	2.5kg max.	3G2C4-SI028
I/O connecting cable		Cable length: 50cm	300g max.	3G2A5-CN511
		Cable length: 100cm	400g max.	3G2A5-CN121
I/O unit	Input unit	AC 100 to 120V 10mA, 16 points *1	450g max.	3G2A6-IA121
		AC 200 to 240V 10mA, 16 points *1	450g max.	3G2A6-IA222
		AC/DC 12 to 24V 10mA, 16 points, PNP/NPN input *2	450g max.	3G2A6-IM211
		AC/DC 12V 7mA, 32 points, PNP/NPN input *2	500g max.	3G2A6-IM111
		AC/DC 24V 7mA, 32 points, PNP/NPN input *2	450g max.	3G2A6-IM213
		DC 5 to 12V 16mA, 16 points, NPN input *3	450g max.	3G2A6-ID112
		DC 12 to 24V 10mA, 16 points, NPN input *3	450g max.	3G2A6-ID213
		DC 24V 7mA, 32 points, NPN input *3	450g max.	3G2A6-ID217
		DC 24V 10mA, 64 points, dynamic scan method	450g max.	3G2A6-ID212
	Output unit	Relay contact AC 250V/DC 24V 2A, 16 points (with relay socket)	450g max.	3G2A6-OC221
		Relay contact AC 250V/DC 24V 2A, 24 points (without relay socket)	500g max.	3G2A6-OC222
		Triac AC 85 to 250V 1A, 16 points	500g max.	3G2A6-OA222
		Transistor DC 12 to 48V 1A, 16 points	500g max.	3G2A6-OD411
		Transistor DC 12 to 48V 0.3A, 32 points	530g max.	3G2A6-OD412
		Transistor DC 24V 0.1A, 64 points, dynamic scan method	450g max.	3G2A6-OD211
	Dummy I/O unit	I/O 16, 32, 64 points (common)	450g max.	3G2A6-DUM01
Optional products	EPROM chip	64 bits (2764)	50g max.	ROM-H
	RAM chip	64 bits (6264)	50g max.	RAM-H
	Battery		100g max.	3G2A9-BAT08
	Cover plate	Covers vacant slot on SYSMAC-C120	50g max.	3G2A6-COV01
	DIN rail attachment	For mounting SYSMAC-C120 to DIN rail	500g max.	3G2A9-DIN01

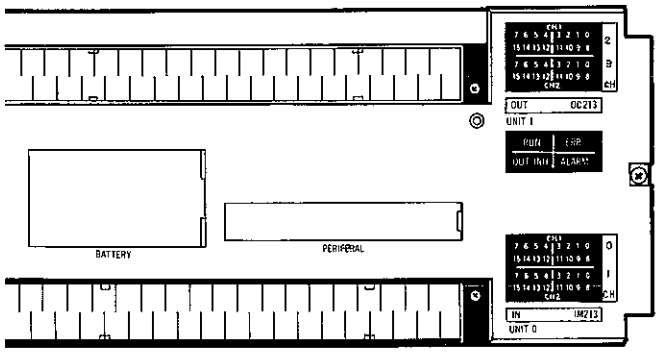
NOTES: *1 ON-delay time: 35ms, OFF-delay time: 55ms
*2 ON-delay time: 15ms, OFF-delay time: 15ms
*3 ON-delay time: 1.5ms, OFF-delay time: 1.5ms
*4 The EPROM and RAM chips are optional.

1.2 NAME OF PARTS

1.2.1 CPU rack and associated units



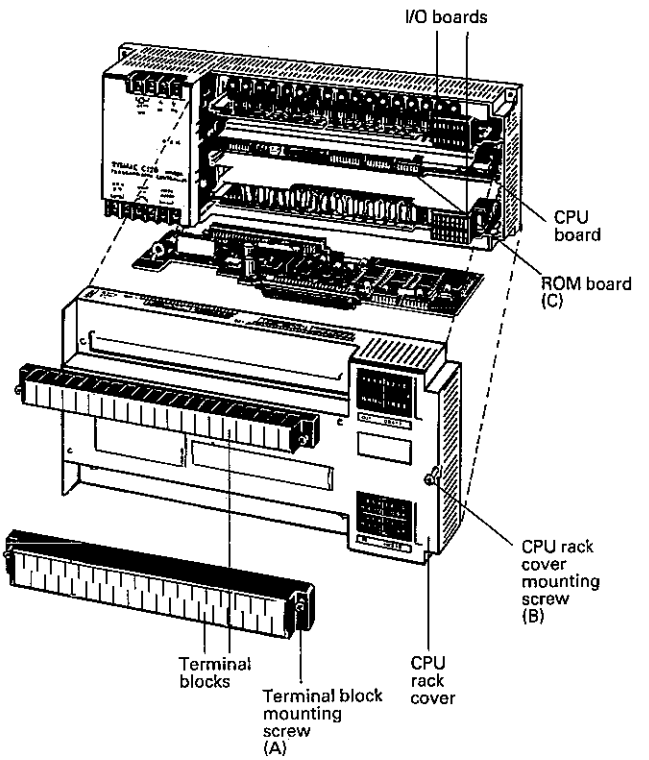
CPU FRONT INDICATION



USER MEMORY MOUNTING FOR 3G2C4-SC023-E/ -SC024-E

No user memory is mounted in the CPU rack of the SYSMAC-C120. Select the RAM-H (6264 or equivalent) or ROM-H (2764 or equivalent) and mount the memory in the CPU rack in accordance with the following procedures.

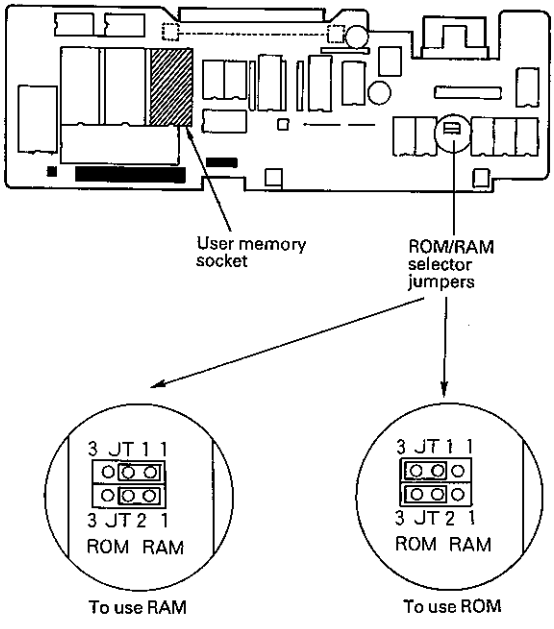
1. Turn off the power.
2. Remove the terminal block mounting screws (A) with a screwdriver to detach the terminal blocks from the CPU rack.
3. Remove the CPU rack cover mounting screws (B) to detach the cover.
4. Pull the ROM board (C) out of the CPU rack.
5. To exchange RAM with ROM
   (1) Short-circuit the JT2 and 3 pins of the ROM/RAM selector jumpers.
   (2) Pull out the RAM chip from the user memory socket.
   (3) Insert the ROM chip into the socket.
6. To exchange the ROM with RAM
   (1) Pull out the ROM chip from the socket.
   (2) Insert the RAM chip into the socket.
   (3) Short-circuit the JT2 and 3 pins of the ROM/RAM selector jumpers.



NOTE:

1. *Replacing the ROM chip with the RAM chip will cause memory failure to occur. To prevent this, perform the memory all clear operation after the replacement.*
2. *When the JT2 and 1 pins of the ROM/RAM selector jumpers are short-circuited, inserting or pulling out the ROM or RAM chip into or from the socket will cause the contents of the I/O table, and data of the data memories, holding relays, and timers/counters to be lost. Therefore, avoid doing so.*
3. *Be sure to short-circuit the pins of both the two ROM/RAM selector jumpers.*

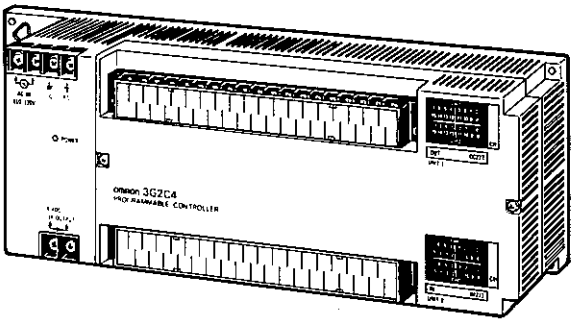
ROM board



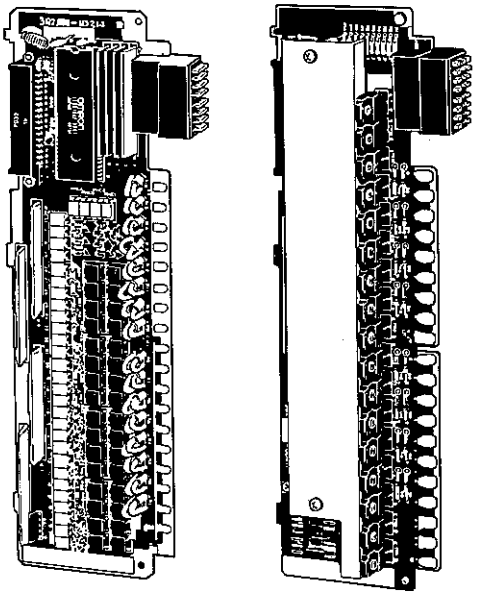
ROM/RAM selector jumpers

4. *For the RAM-type CPUs: Types 3G2C4-SC021-E and 3G2C4-SC022-E, user memory mounting is not required.*

1.2.2 Expansion I/O rack



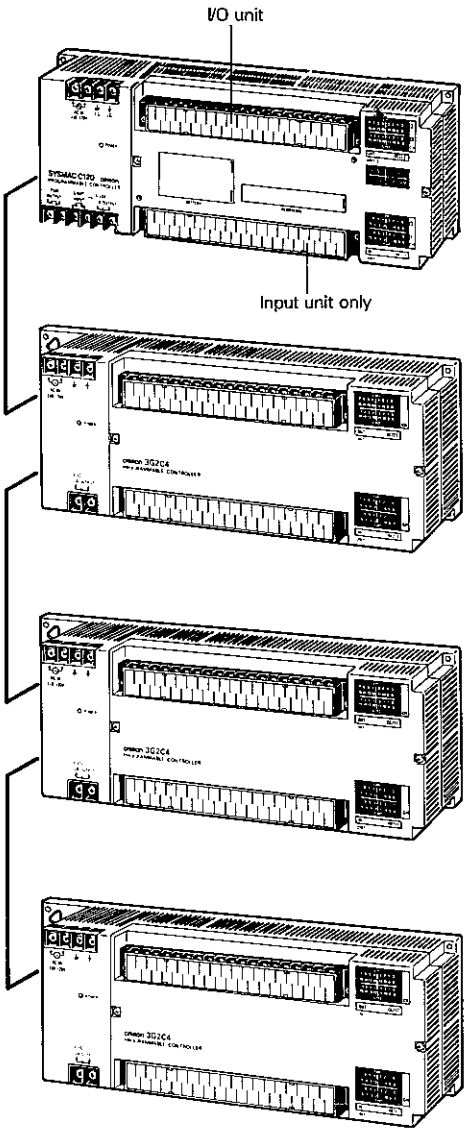
1.2.3 I/O unit



1.3 SYSTEM CONFIGURATION

BASIC SYSTEM

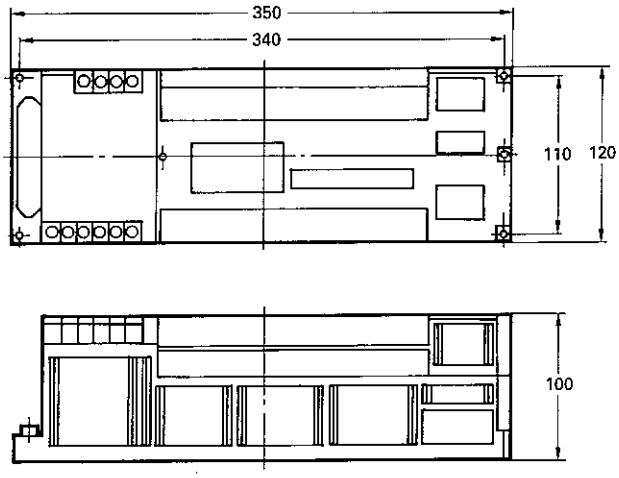
For the type of I/O units, refer to 1.1, Available types when placing your order.



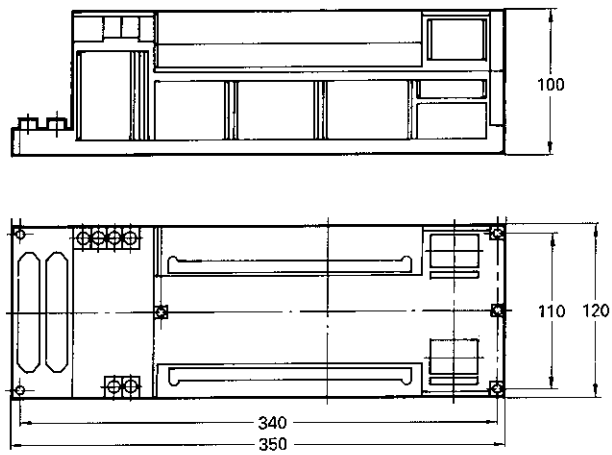
NOTES:
1. * A maximum of 2 I/O units can be mounted in the CPU rack.
2. ** A maximum of 2 I/O units can be mounted on an expansion I/O rack.
3. The PC allows additional connections of up to 3 expansion I/O units.
4. Any combination of I/O units can be made on an expansion I/O rack 3G2C4-SI021 or 3G2C4-SI022.

1.4 DIMENSIONS

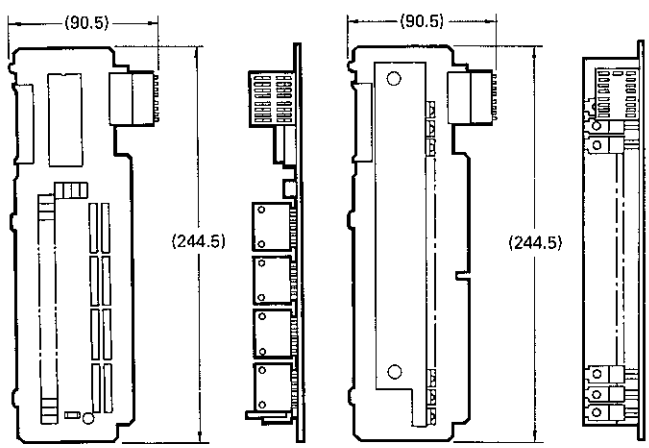
1.4.1 CPU rack



1.4.2 Expansion I/O rack



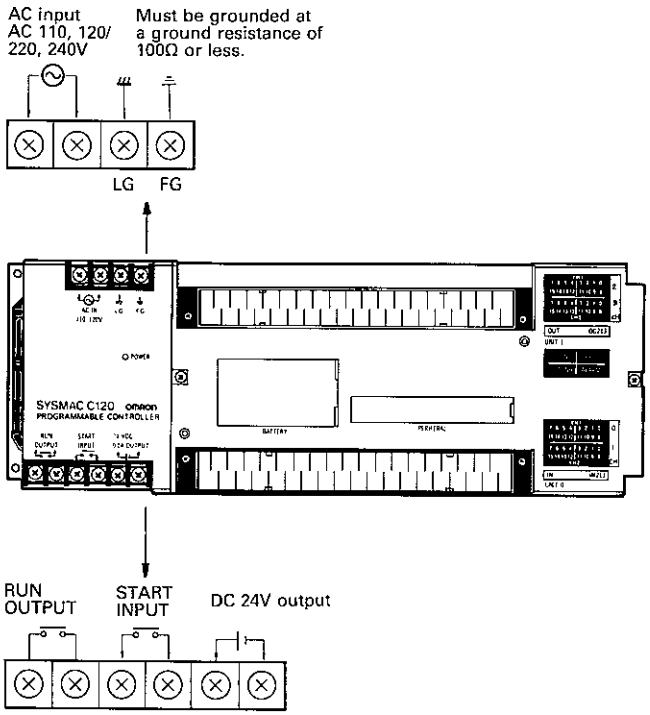
1.4.3 I/O unit



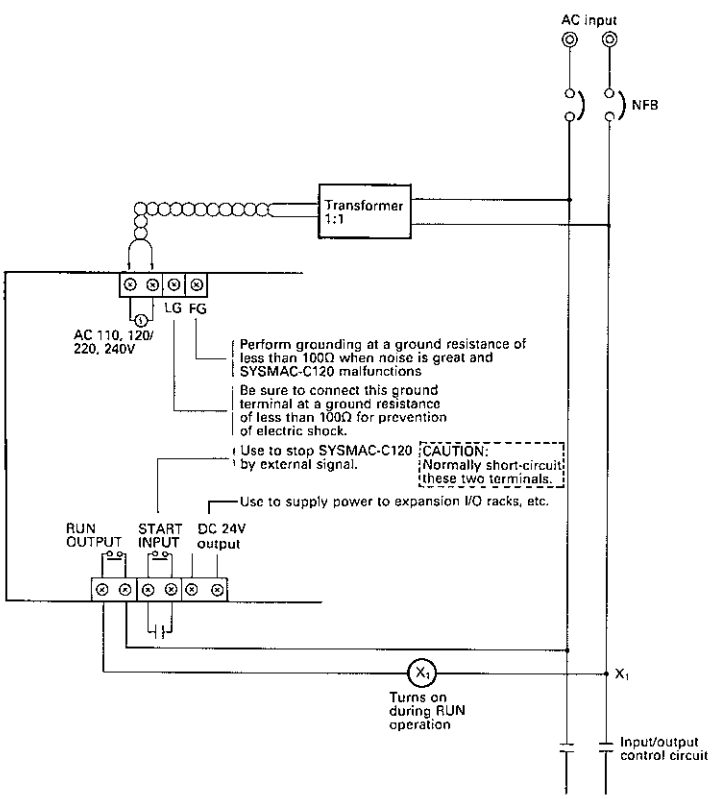
1.5 WIRING AND POWER SUPPLY

1.5.1 CPU rack

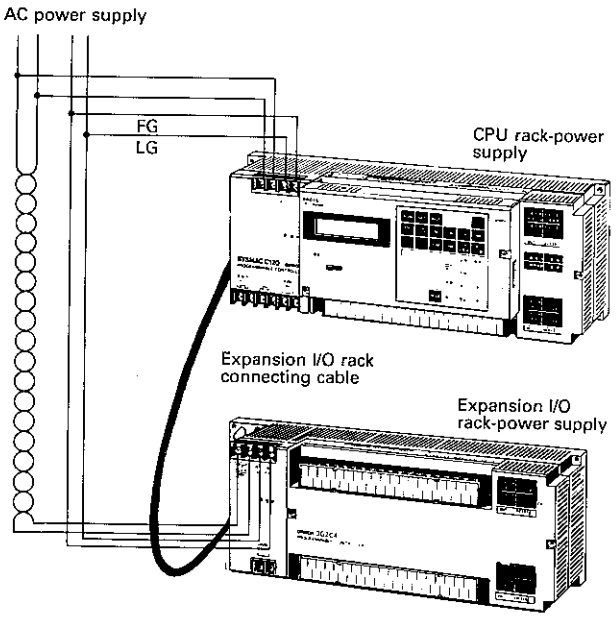
EXTERNAL INPUT TERMINAL



WIRING AND POWER SUPPLY OF CPU



1.5.2 I/O rack

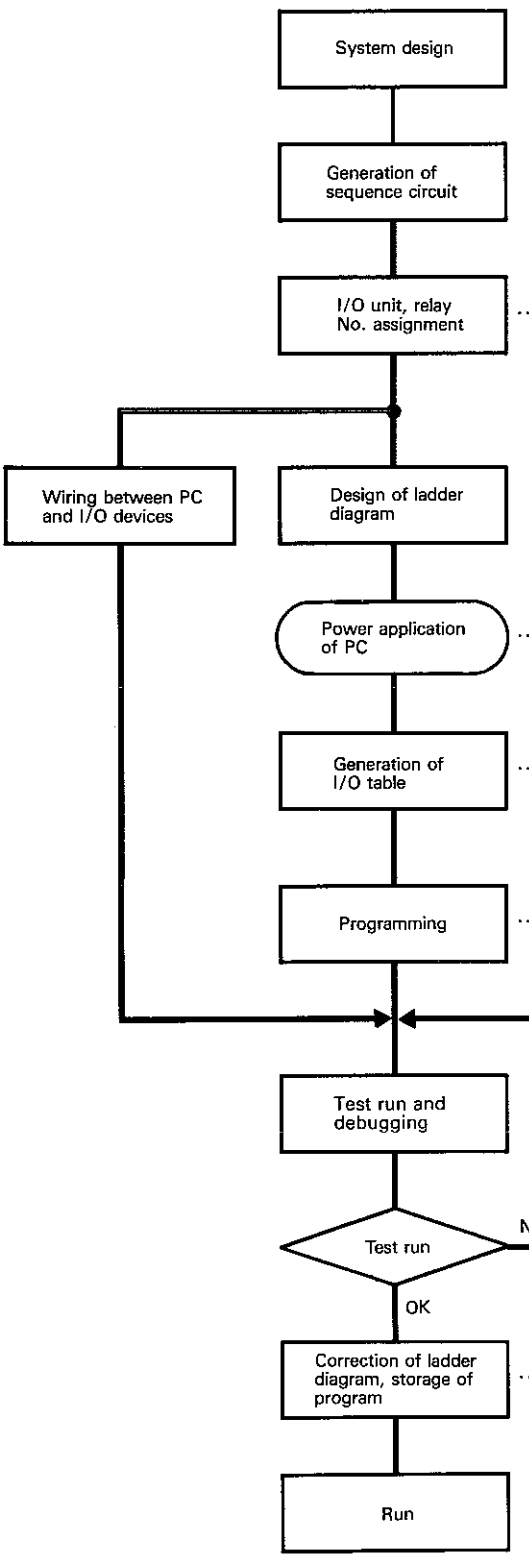


The following three I/O connecting cables are available.
50cm (Type 3G2A5-CN511),
1m (Type 3G2A5-CN121).

NOTE: Refer to 5.4, Processing of wiring within control panels, for details on wiring.

1.6 OPERATING PROCEDURES OF PROGRAMMABLE CONTROLLER

Here are the procedures from the designing of the sequence circuit to RUN operation of the PC.



- I/O unit, relay No. assignment: Refer to Chapter 3 and Appendix A.
- Power application of PC: *1 Set the PC in PROGRAM mode and connect the programming console to the PC. Apply power to the PC.
- Generation of I/O table: *1 First, the message "I/O VER ERR" will appear on the LCD of the programming console. Clear it by generating an I/O table with the programming console. (Refer to 3.2 for details.)
- Programming: Clear all memory contents by performing Program Clear operation before programming.
  NOTE: I/O table generation is not necessary each time the power is applied to the PC unless I/O unit location will change later.
- Test run and debugging: *1 Correct the program
- Correction of ladder diagram, storage of program: *2
  - Ladder diagrams can be printed out with a printer.
  - Programs can be recorded on a cassette tape or an EPROM chip.

NOTES:
*1 Refer to the user's manual of programming console for details.
*2 Refer to the user's manual of printer interface unit for details.

OPERATING MODE OF PC

The following operation modes of the PC are set on power application or when the PC is connected on-line to peripheral device(s).

Peripheral equipment	On power application	ON-LINE connection *2
Programming console, programming console adapter	According to the mode selector switch position of programming console *1	Current operation mode is continued. *3
Peripheral interface unit, printer interface unit, and PROM writer	PROGRAM	Current operation mode is continued.
None	RUN	—

*1 The operation mode of the PC will be PROGRAM if the mode selector switch of the programming console is set to PROGRAM position.

*2 ON-LINE connection is to connect the peripheral device(s) to the PC while the power supply to the PC is ON.

*3 For example, if the peripheral device is connected to the PC while the operation mode of the PC is RUN, the PC continues to be in RUN state.

CHAPTER 2
SPECIFICATIONS

2.1 SYSTEM SPECIFICATIONS

RATINGS

Supply voltage	AC 110, 120/220, 240V, 50/60Hz
Operating voltage range	85 to 110% of rated voltage *
Power consumption	CPU rack: 50VA max. Expansion I/O rack: 35VA max.
Insulation resistance	5MΩ min. at DC 500V (between external terminal and outer casing)
Dielectric strength	AC 1,500V, 50/60Hz for 1 minute (between external terminal and outer casing)
Noise immunity	1,000Vp-p Rise time: 1nsec; Pulse width: 50n to 1μsec
Vibration	16.7Hz, 3mm double amplitude, (in X, Y, Z directions, respectively 30 min)
Shock	10G (in X, Y, Z directions, respectively 3 times)
Ambient temperature	Operating : 0 to +50°C Storage : −20°C to +65°C
Humidity	35 to 80% RH (without condensation)
Atmosphere	Must be free from corrosive gases
Structure	Module type
Coating	Ivory white
Weight	See Section 1.1, Available Types.
Degree of protection	IP30 (IEC Publ-529)

NOTE: * A momentary power failure of less than 10ms is ignored by the programmable controller, and it will continue operation.

CHARACTERISTICS

Control system	Stored program system
Main control element	LSI, TTL, C-MOS
Programming system	Ladder diagram
Instruction word length	3 to 10 byte/address (1 address/instruction)
Number of instructions	68
Execution time/address	5 to 10μs/address (basic instruction)
Programming capacity	Approx. 2.2K address (RAM/EPROM)*1 (8K bytes)
Number of input/output points	256 (Relay Nos. 0000 to 1515)
Number of internal auxiliary relays	459 points (Relay Nos. 3200 to 6010)
Number of holding relays	512 points (Relay Nos. HR0000 to 3115) *3
Number of timers and counters	128 points Timer : 0 to 999.9s Counter : 0 to 9999 counts
Number of temporary memory relays	8 points (Relay Nos. 0 to 7)
Number of special auxiliary relays	45 points (Relay Nos. 6011 to 6315)*2
Number of data memory relays	512 points (16 bits/point)
Control input signal	START INPUT: In RUN mode, PC operates when contact is closed and stops when contact is opened.
Control output signal	RUN OUTPUT: Contact is closed while PC is RUN.
DC power supply	DC 24V, 0.1A (incorporated)
Memory protective function against power failure	Status data of respective holding relays, counters, and data memories before power failure is retained in memory.
Battery	Service life of built-in battery is about 5 years at a temperature of 25°C. If ambient temperature at which battery is to be used exceeds 25°C, battery life will be shortened. Replace battery within one week after battery low indicator illuminates and within approximately 5 minutes after turning off power switch.
Diagnostic function	RUN mode • CPU failure (watchdog timer) • Battery failure • Scan time failure • Memory error • I/O bus failure PROGRAM mode (program check) • Coil duplication check • END instruction check • Circuit error check • IL/ILC error check • JMP/JME error check • DIF instruction over error check

NOTES: *1

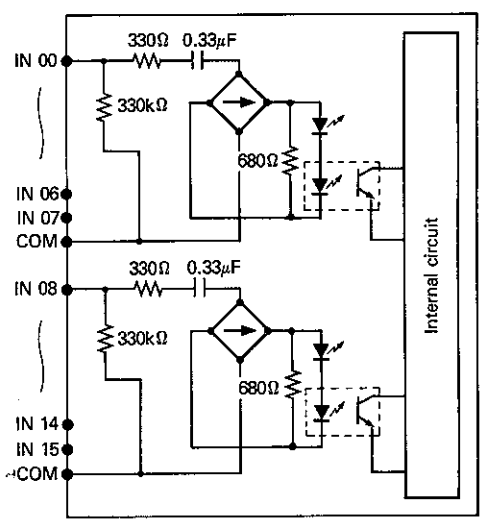
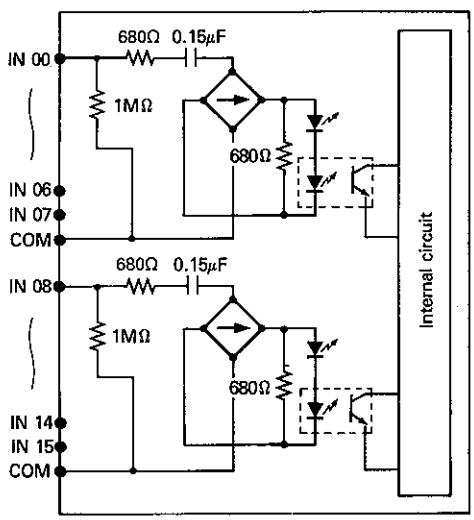
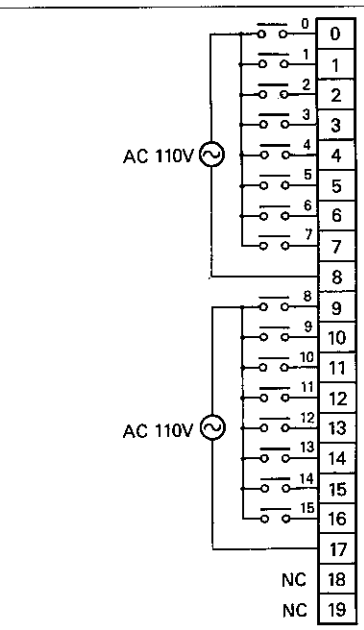
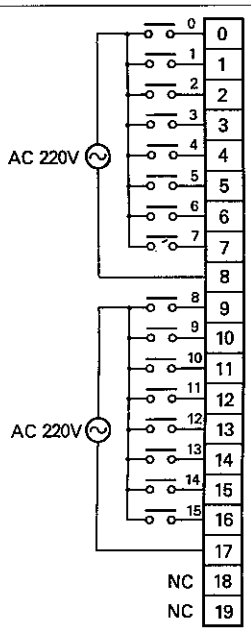
- Programming capacity
  - The user program memory of the PC is 8K bytes.
  - The programming capacity (i.e., number of addresses) is calculated on the assumption that one address is 3.6 bytes on the average.
- Address
  - The length of instruction words for the PC is variable within the range from 3 to 10 bytes. Each instruction has a respective length.
  - Because instruction words are variable in length, a maximum number of addresses that can be written in a specific program varies depending on the instructions used in that program.

*2
Refer to 3.1, Explanation of special auxiliary relay numbers and temporary memory relay numbers, for details on the description of the special auxiliary relays.

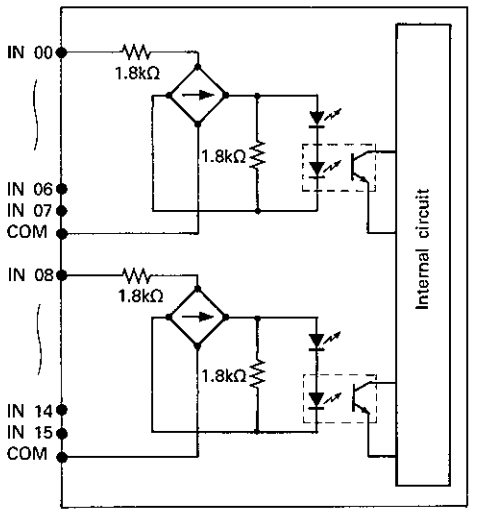
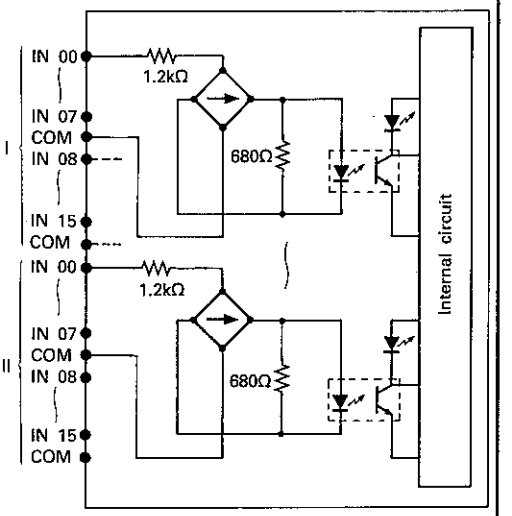
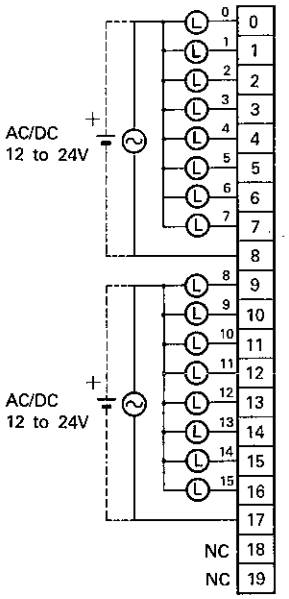
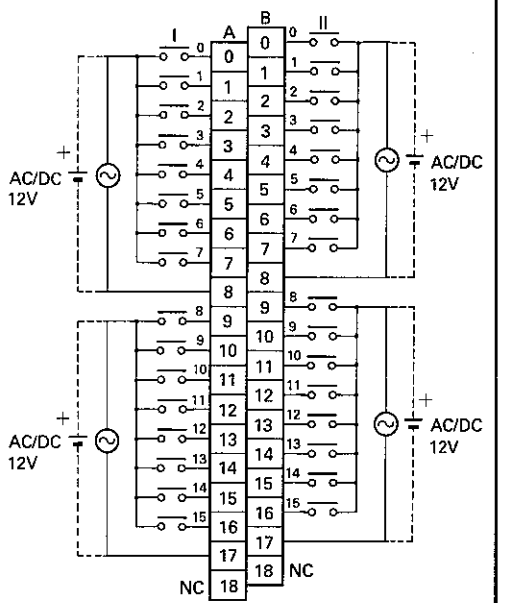
*3
The link relays of the SYSMAC-C250 and SYSMAC-C500 are used when linking the PC to another PC. The link relays of the SYSMAC-C120, however, are used only as auxiliary relays.

2.2 I/O UNITS SPECIFICATIONS

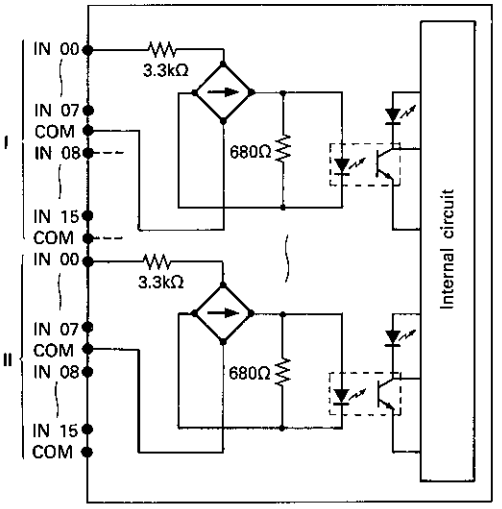
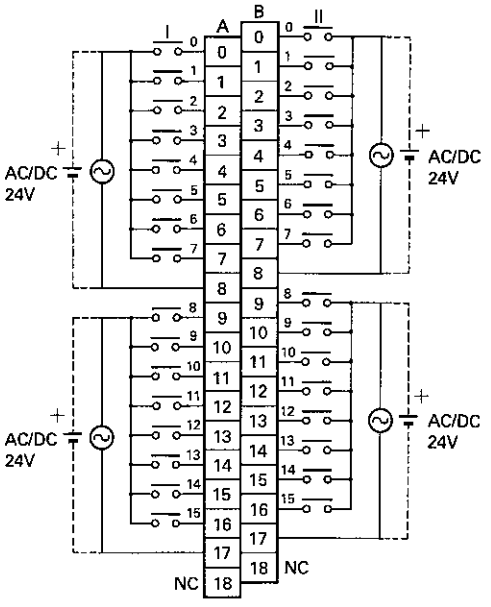
2.2.1 Input units

Item \ Type	AC input unit	
	Type 3G2A6-IA121	Type 3G2A6-IA222
Input voltage	AC 100 to 120V +10%, −15%, 50/60Hz	AC 200 to 240V +10%, −15%, 50/60Hz
Input impedance	9.7kΩ (50Hz), 8kΩ (60Hz)	22kΩ (50Hz), 18kΩ (60Hz)
Input current	10mA TYP. (AC 100V)	10mA TYP. (AC 200V)
ON-delay time*	35ms max.	35ms max.
OFF-delay time**	55ms max.	55ms max.
Number of circuits	16 points (8 points/common)	16 points (8 points/common)
Weight	450g max.	450g max.
ON voltage	AC 60V max.	AC 120V max.
OFF voltage	AC 20V min.	AC 40V min.
Current consumption of internal constant-voltage circuit	DC 5V 10mA max.	DC 5V 10mA max.
Circuit configuration		
Terminal connections***		

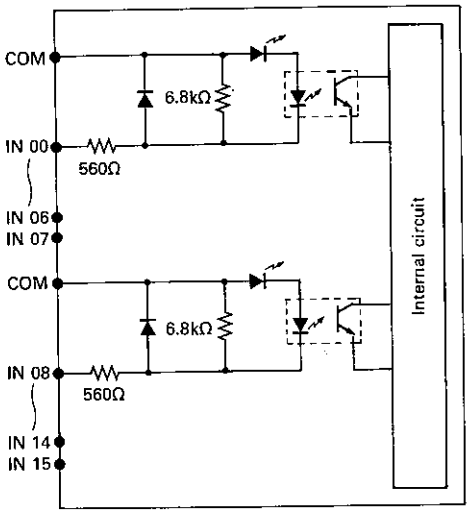
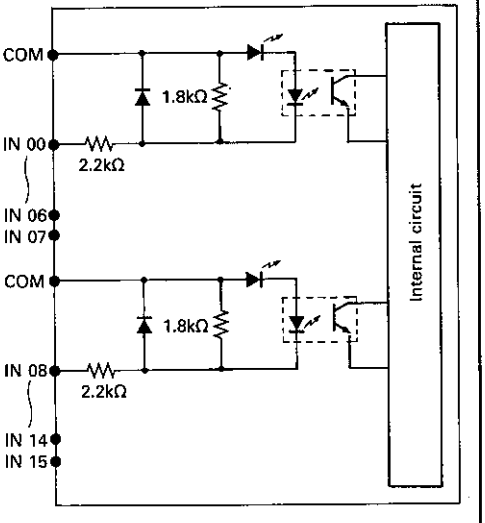
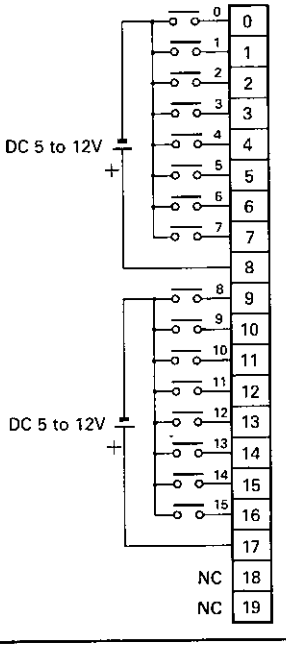
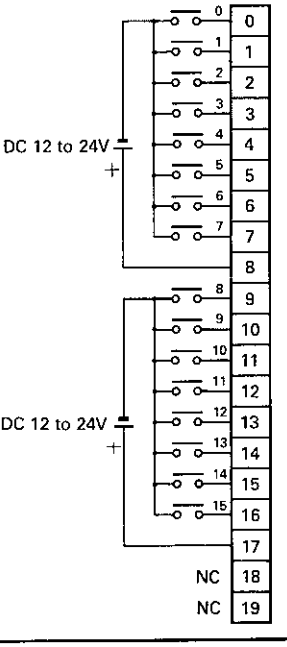
NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item \ Type	AC/DC input unit (for PNP/NPN input)	
	Type 3G2A6-IM211	Type 3G2A6-IM111
Input voltage	AC/DC 12 to 24V +10%, –15%	AC/DC 12V +10%, –15%
Input impedance	1.8kΩ	1.2kΩ
Input current	10mA TYP. (DC 24V)	7mA TYP. (DC 12V)
ON delay time	15ms max.	15ms max.
OFF delay time	15ms max.	15ms max.
Number of circuits	16 points (8 points/common)	32 points (8 points/common)
Weight	450g max.	500g max.
ON voltage	DC 10.2V max.	DC 8V max.
OFF voltage	DC 3.0V min.	DC 3.0V min.
Current consumption of internal constant-voltage circuit	DC 5V 10mA max.	DC 5V 200mA max.
Circuit configuration		
Terminal connections		

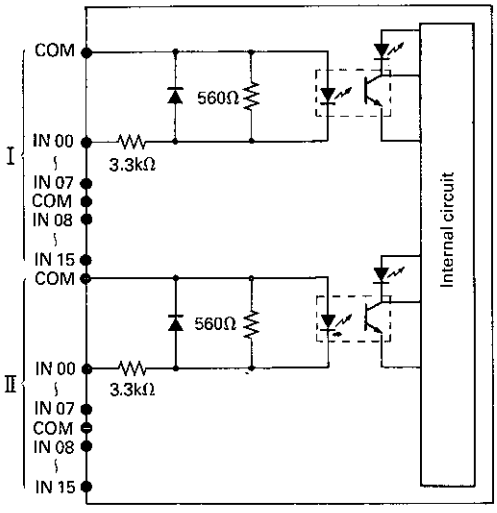
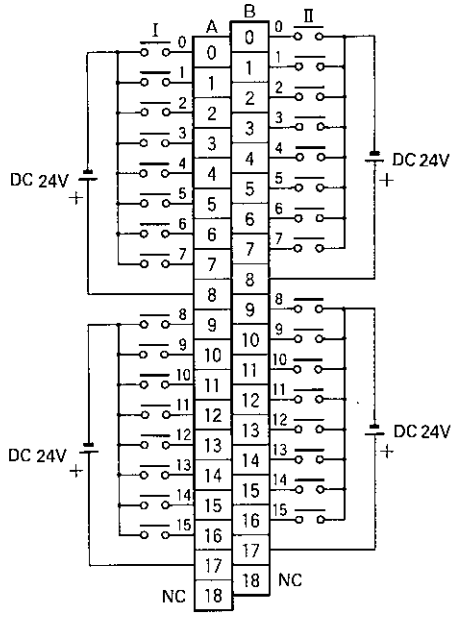
NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item \ Type	AC/DC input unit (for PNP/NPN input) Type 3G2A6-IM213
Input voltage	AC/DC 24V +10%, –15%
Input impedance	3.3kΩ
Input current	7mA TYP. (DC 24V)
ON delay time*	15ms max.
OFF delay time**	15ms max.
Number of circuits	32 points (8 points/common)
Weight	500g max.
ON voltage	DC 16.0V max.
OFF voltage	DC 5.0V min.
Current consumption of internal constant voltage circuit	DC 5V 200mA max.
Circuit configuration	
Terminal connections***	

NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The termfinal numbers and I/O channel relay numbers of an I/O unit are changed according to the position of the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item \ Type	DC input unit (for NPN input)	
	3G2A6-ID112	3G2A6-ID213
Input voltage	DC 5 to 12V +10%, –5%	DC 12 to 24V +10%, –5%
Input impedance	560Ω	2.2kΩ
Input current	16mA TYP. (DC 12V)	10mA TYP. (DC 24V)
ON-delay time*	1.5ms max.	1.5ms max.
OFF-delay time**	1.5ms max.	1.5ms max.
Number of circuits	16 points (8 points/common)	16 points (8 points/common)
Weight	450g max.	450g max.
ON voltage	DC 4.0V max.	DC 10.2V max.
OFF voltage	DC 1.5V min.	DC 3.0V min.
Current consumption of internal constant-voltage circuit	DC 5V 10mA max.	DC 5V 20mA max.
Circuit configuration	 NOTE: Tow-wire system sensor cannot be used with this imput unit.	
Terminal connections		

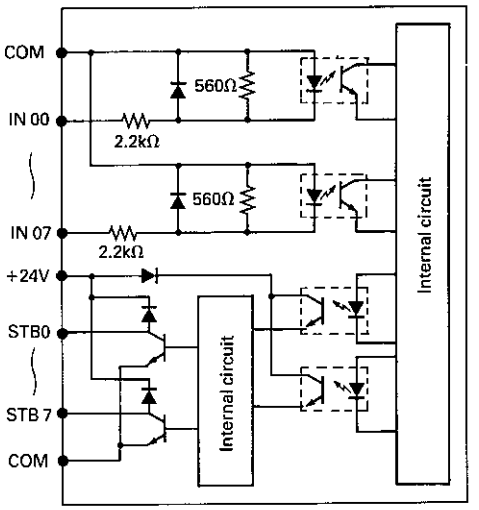
NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item \ Type	DC input unit (for NPN input) 3G2A6-ID217
Input voltage	DC 24V +10%, −15%
Input impedance	3.3kΩ
Input current	7mA TYP. (DC 24V)
ON delay time*	1.5ms max.
OFF delay time**	1.5ms max.
Number of circuits	32 points (8 points/common)
Weight	450g max.
ON voltage	DC 16.0V max.
OFF voltage	DC 5.0V min.
Current consumption of internal constant-voltage circuit	DC 5V 160mA max.
Circuit configuration	
Terminal connections***	

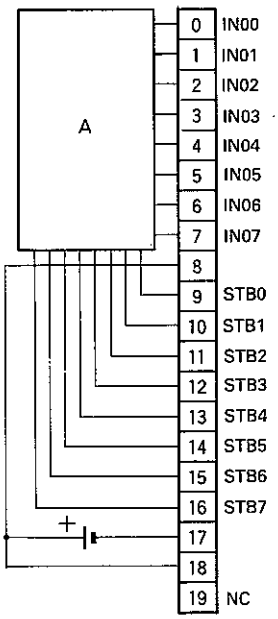
NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item	Type	DC input unit (for NPN input) 3G2A6-ID212
Input section	Input voltage	DC 24V +10%, −15%
	Input impedance	2.2kΩ
	Input current	10mA TYP. (DC 24V)
	ON delay time*	1.5ms max.
	OFF delay time**	1.5ms max.
	ON voltage	DC 10.2V max.
	OFF voltage	DC 3.0V max.
Strobe output section	Max. switching capacity	DC 24V +10%, −15% 0.1A
	Leakage current	100μA max.
	Saturation voltage	1.5V max.
	ON delay time	0.2ms max.
	OFF delay time	3.0ms max.
	Fuse capacity	No fuse
	Supply voltage to internal constant voltage circuit	DC 24V ±10%
Common section	Number of circuits	64 points
	Weight	450g max.
	Current consumption of internal constant voltage circuit	DC 5V 300mA max.

Circuit configuration

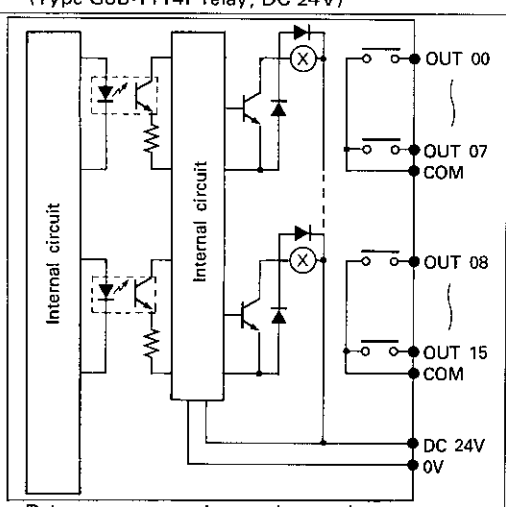
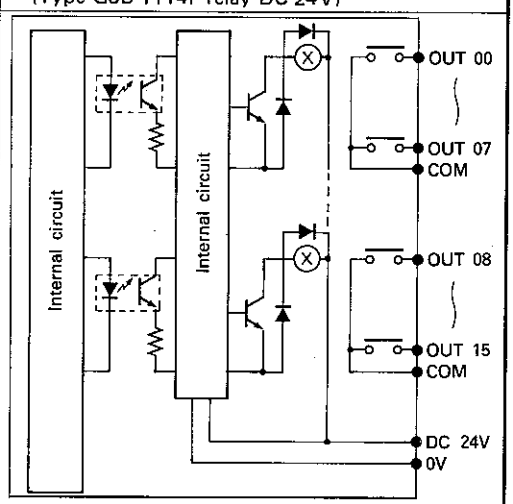
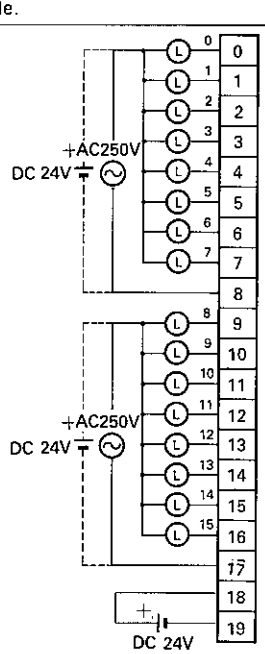
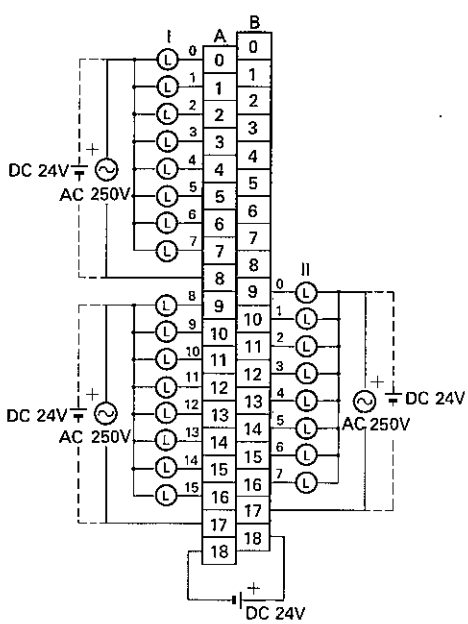


Terminal connection

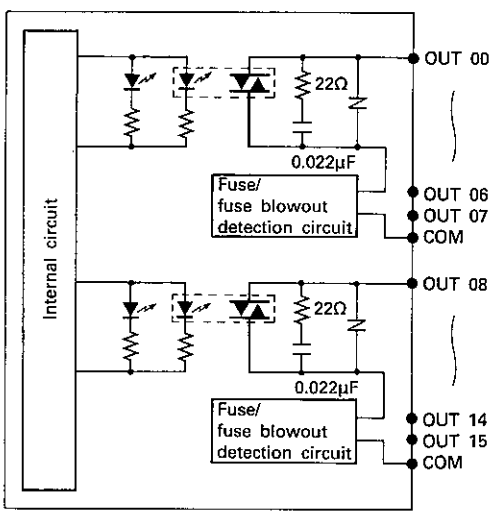
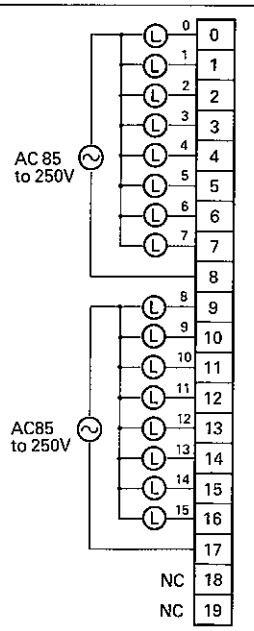


NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

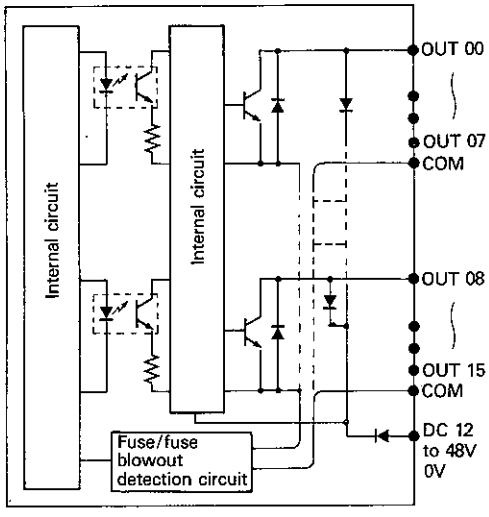
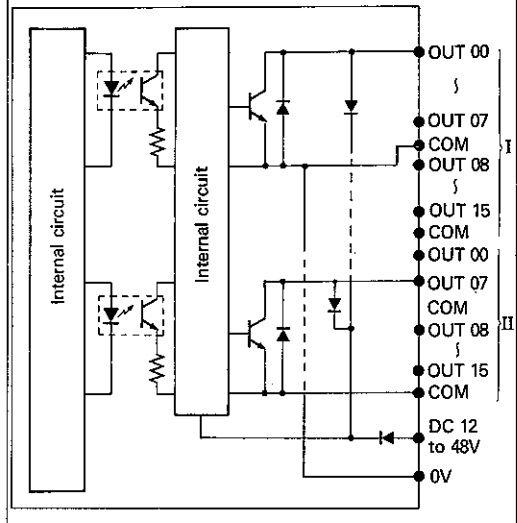
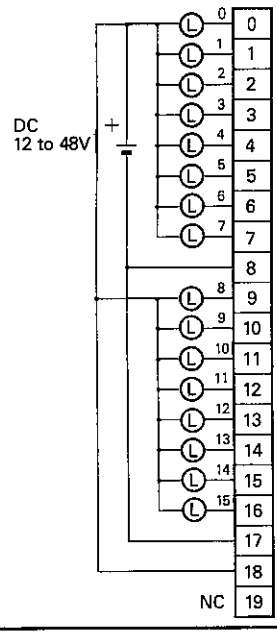
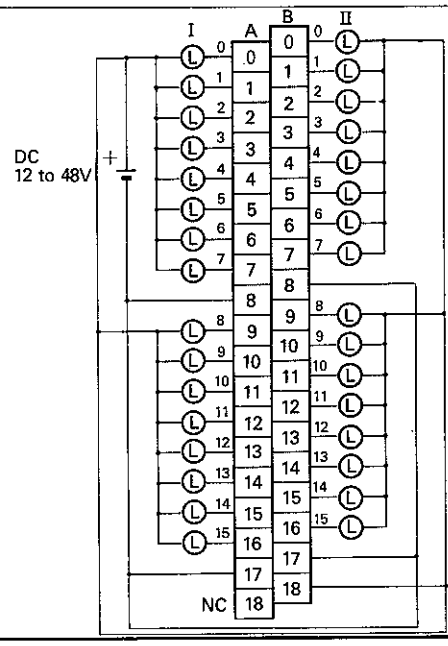
2.2.2 Output units

Item \ Type	Contact output unit	
	Type 3G2A6-OC221	Type 3G2A6-OC222
Max. switching capacity	AC 250V/2A (p.f.=1), DC 24V/2A (8A/common, 16A/unit)	AC 250V/2A (p.f.=1), DC 24V/2A (8A/common, 24A/unit)
Min. switching capacity	DC 5V 100mA	DC 5V 100mA
Supply voltage to internal constant-voltage circuit (for relay driving)	Voltage: DC 24V ±10% Current: 10mA/point, 160mA/unit	Voltage: DC 24V±10% Current: 10mA/point, 160mA/unit
ON-delay time*	15ms max.	15ms max.
OFF-delay time**	15ms max.	15ms max.
Number of circuits	16 points (8 points/common)	24 points (8 points/common)
Weight	450g max.	500g max.
Current consumption of internal constant-voltage circuit	DC 5V ±5% 100mA max. DC 24V ±10% 160mA max.	DC 5V ±5% 180mA max., DC 24V ±10% 240mA max.
Service life	Electrically: 300,000 operations Mechanically: 20,000,000 operations (Type G6B-1114P relay, DC 24V)	Electrically: 300,000 operations Mechanically: 20,000,000 operations (Type G6B-1114P relay DC 24V)
Circuit configuration	 Relays are mounted on sockets and are replaceable.	
Terminal connections ***		

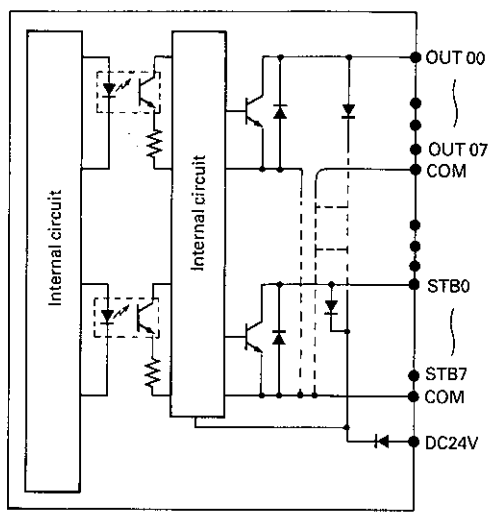
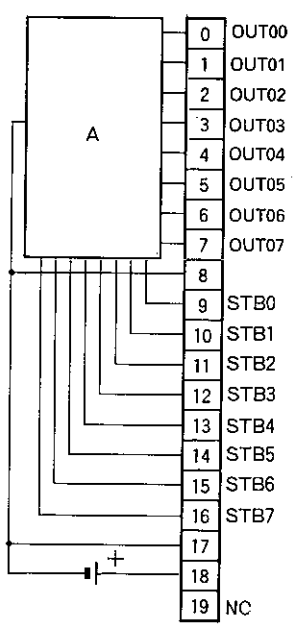
NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item \ Type	Triac output unit
	Type 3G2A6-OA222
Max. switching capacity	AC 85 to 250V +10%, −15%, 1A 50/60Hz (4A/common, 5A/unit)
Min. switching capacity	10mA/AC 100V, 20mA/AC 200V
Leakage current	3mA max./AC 100V, 6mA max./AC 200V
Saturation voltage	1.2V max.
ON-delay time*	1.5ms max.
OFF-delay time**	1/2 of load frequency max. (zero crossing circuit incorporated)
Number of circuits	16 points (8 points/common)
Weight	500g max.
Current consumption of internal constant-voltage circuit	DC 5V 280mA max.
Fuse capacity	5A/8 points
Circuit configuration	
Terminal connections***	

NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item \ Type	Transistor output unit	
	Type 3G2A6-OD411	Type 3G2A6-OD412
Max. switching capacity	DC 12 to 48V +10%, −15%, 1A (4A/common, 5A/unit)	DC 12 to 48V +10%, −15%, 0.3A (2.4A/common, 4.8A/unit)
Leakage current	100μA max.	100μA max.
Saturation voltage	1.4V max.	1.5V max.
ON-delay time*	0.2ms max.	0.2ms max.
OFF-delay time**	0.3ms max.	0.3ms max.
Number of circuits	16 points (8 points/common)	32 points (8 points/common)
Weight	500g max.	530g max.
Current consumption of internal constant-voltage circuit	DC 5V 160mA max.	DC 5V 230mA max.
Fuse capacity	5A/8 points	No fuse
Supply voltage to internal constant-voltage circuit	DC 12 to 48V +10%, −10%, 50mA max.	DC 12 to 48V +10%, −10%, 80mA max.
Circuit configuration		
Terminal connections***		

NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of an input signal until the inactivation of the output terminal of the unit.
*** The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position on the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

Item \ Type	Transistor output unit 3G2A6-OD211
Max. switching capacity	DC 24V +10% −15%, 0.1A
Leakage current	100μA max.
Saturation voltage	1.5V max.
ON-delay time	0.2ms max.
OFF-delay time	0.3ms max.
Number of circuits	64 points
Weight	450g max.
Internal current consumption	DC 5V 300mA max.
Fuse capacity	No fuse
Power supply to internal constant-voltage circuit	DC 24V ±10%, 50mA max.
Circuit configuration	
Terminal connections	

NOTE: The terminal numbers and I/O channel relay numbers of an I/O unit are changed according to the position of the CPU (or expansion I/O) rack on which the I/O unit is mounted. The terminal connections shown above are for when the I/O unit is mounted on the UNIT 1 position. For details, refer to 2.2.4, Terminal numbers and I/O channel relay numbers.

2.2.3 Dummy I/O unit

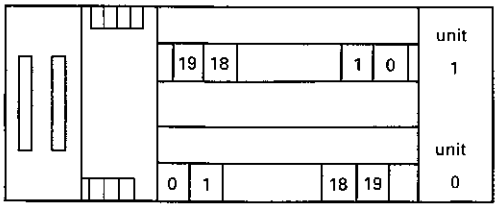
Item \ Type	Dummy input/output unit Type 3G2A6-DUM01	
Selection function	Unit designation	Input/output
	Point designation	16/32/64 points
Weight	450g max.	
Current consumption of internal constant-voltage circuit	DC 5V 35mA max.	
Supply voltage to internal constant-voltage circuit	DC 24V ±10%, 30mA max.	
Circuit configuration	—	
Terminal connections	Short circuit: input Open : output 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 + DC 24V	

Terminal No. / I/O points	3-4	4-5
16 points	Open	Open
32 points	Short-circuit	Open
64 points	Open	Short-circuit

2.2.4 Terminal numbers and I/O channel relay numbers

When mounting an I/O unit on the CPU or expansion I/O rack, the relation between the terminal numbers and I/O channel relay numbers of the I/O unit will be as follows, according to the mounting position of the I/O unit.

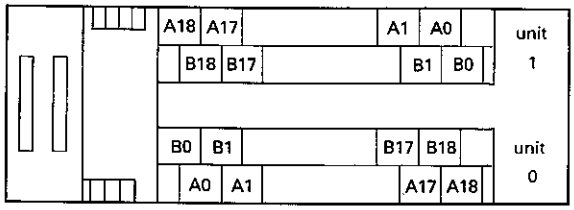
When mounting 16-point I/O units



← Terminal number 0 is bit 00 of channel 01.
Terminal numbers 17 and 8 are common terminals.

← Terminal number 19 is bit 00 of channel 00.
Terminal numbers 11 and 2 are common terminals.

When mounting 32-point I/O units



← Terminal number A0 is bit 00 of channel 02.
Terminal numbers A8 and A17 are common terminals.

← Terminal number B0 is bit 00 of channel 03.
Terminal numbers B8 and B17 are common terminals.

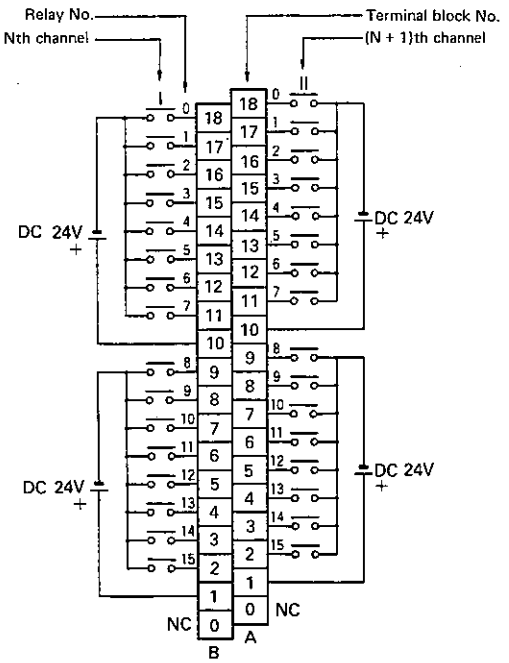
← Terminal number B18 is bit 00 of channel 00.
Terminal numbers B10 and B1 are common terminals.

← Terminal number A18 is bit 00 of channel 01.
Terminal numbers A10 and A1 are common terminals.

The terminal connections shown in 2.2 I/O unit specifications are when the I/O unit is mounted on the UNIT 1 position of the CPU or expansion I/O rack.
The terminal connections are as follows when the I/O unit is mounted on the UNIT 0 position.

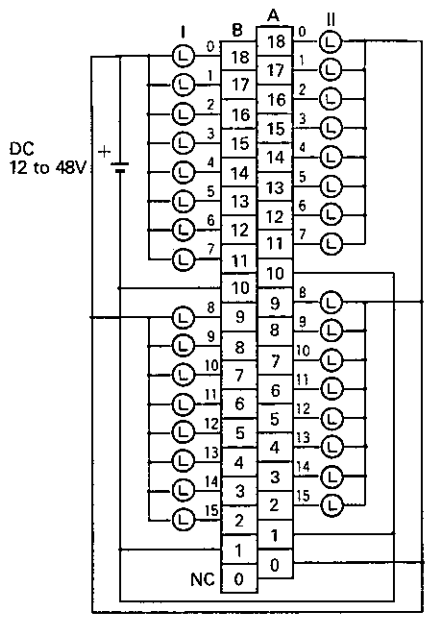
32-point input unit

3G2A6-ID217
3G2A6-IM111
3G2A6-IM213



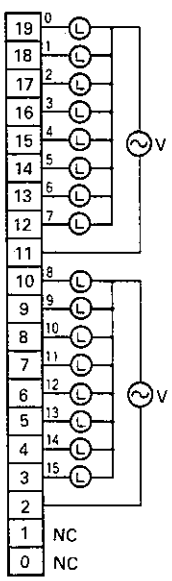
32-point output unit

3G2A6-OD412



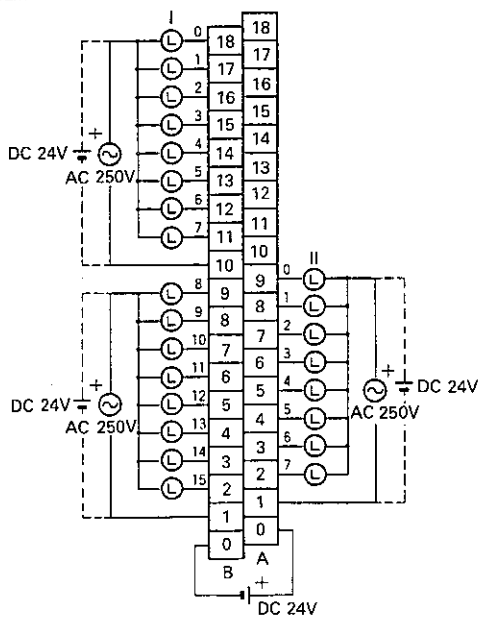
16-point I/O unit

3G2A6-IA121
3G2A6-IA222
3G2A6-ID112
3G2A6-ID213
3G2A6-IM211
3G2A6-OC221
3G2A6-OD411
3G2A6-OA222



24-point output unit

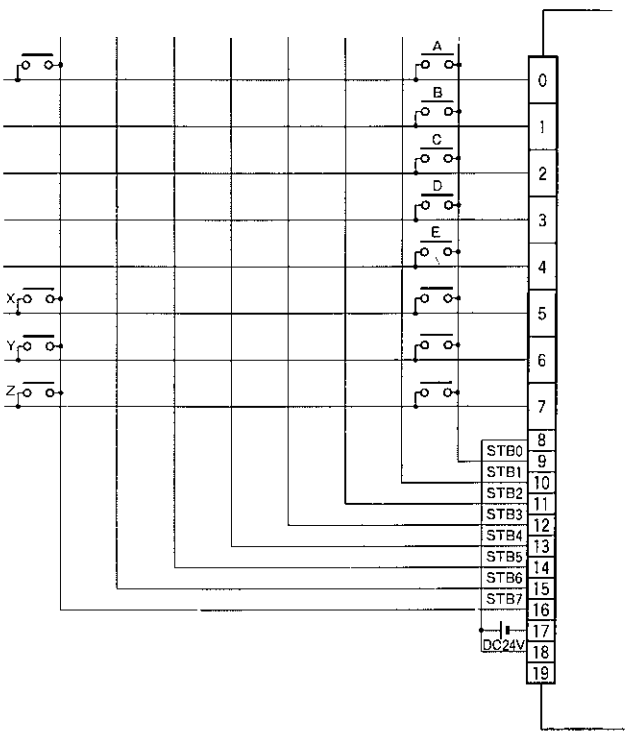
3G2A6-OC222



2.2.5 DC input (64-point) unit

Since this unit is of dynamic input type, a maximum of 16 digits of data can be input to the programmable controller from thumbwheel switches or a keyboard with the wiring simplified.

CONNECTION EXAMPLE (1)



Relay No.

	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00
n CH		··· E D C B A
n+1 CH		
n+2 CH		
n+3 CH	z y x ···	

When the key corresponding to "A" is depressed, relay 00 of the channel n turns ON (i.e., becomes logical 1).

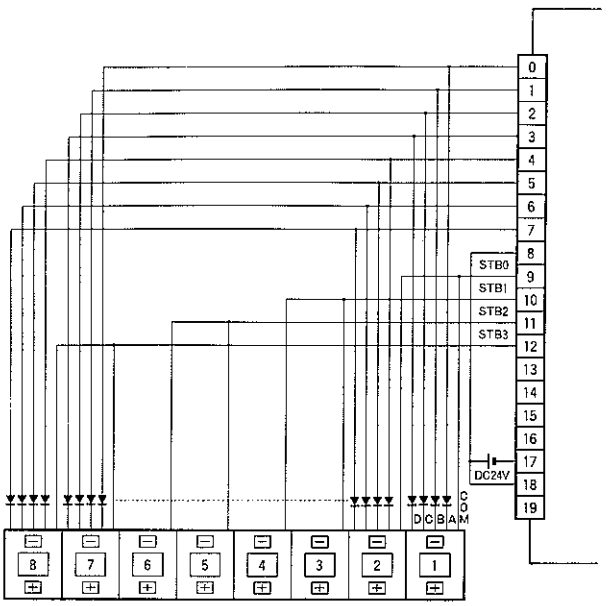
NOTE:

1. Channel n is determined according to the sequence in which the DC input unit is mounted to the SYSMAC-C500. Refer to 3.2, Free location concept and I/O channels.
2. Insert a diode to each key as follows if more than one key is depressed at the same time.

CAUTION FOR HANDLING

Since the DC input unit is operated by an extremely small current, provide an adequate distance between the wires of the unit and high-tension equipment or power lines when performing wiring; otherwise, use shielded cables. Also, keep the length of the wires within 10m.

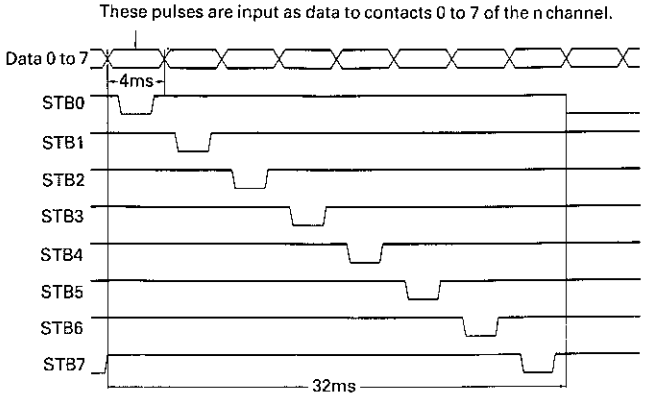
CONNECTION EXAMPLE (2)



Relay No.

	07	06	05	04	03	02	01	00	15	14	13	12	11	10	09	08
n CH	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1
n+1 CH	1	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1
n+2 CH																
n+3 CH																

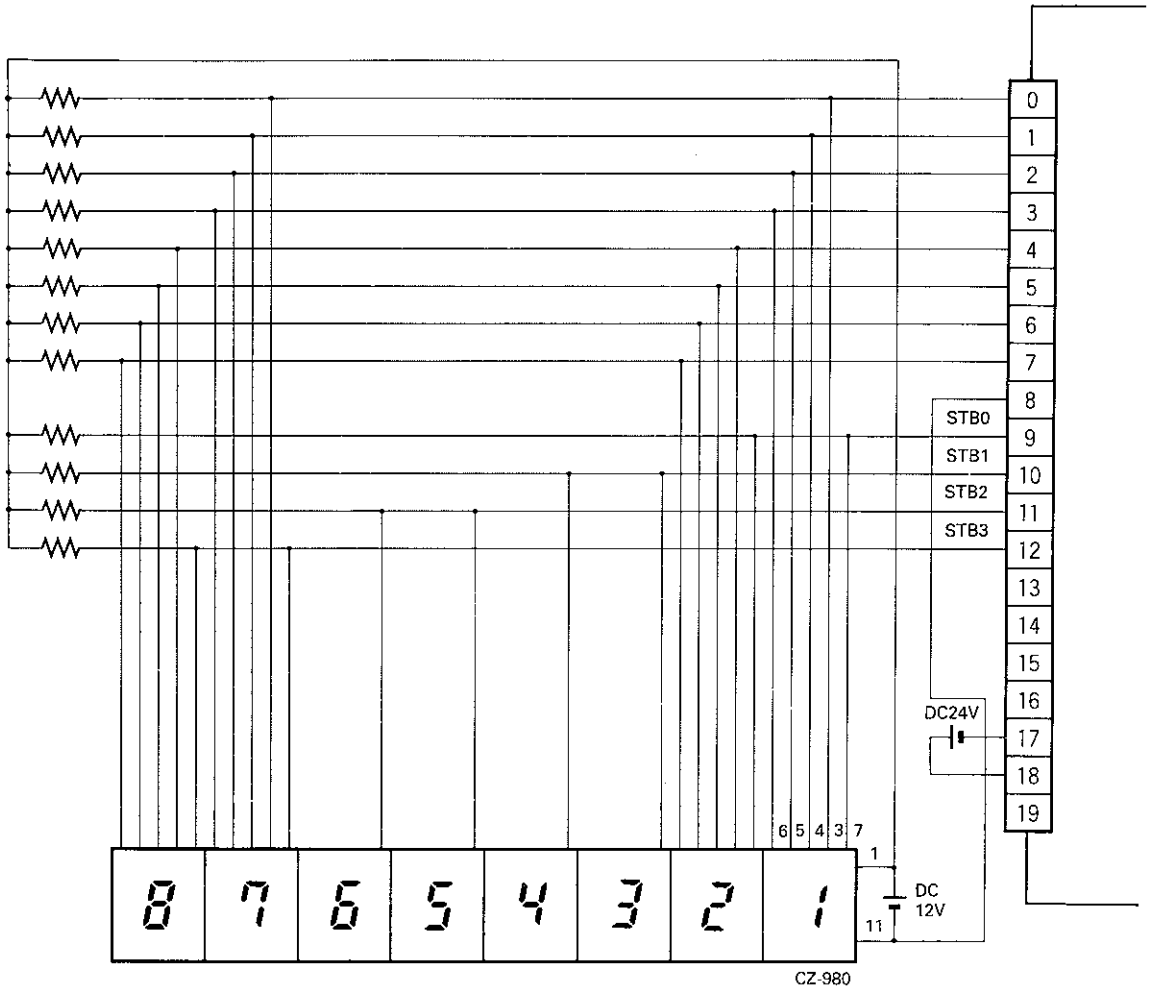
TIMING



2.2.6 DC output (64-point) unit

Since this unit is of dynamic output type, the wiring of a device to be connected to it (such as a numeric display device) can be simplified.

CONNECTION EXAMPLE



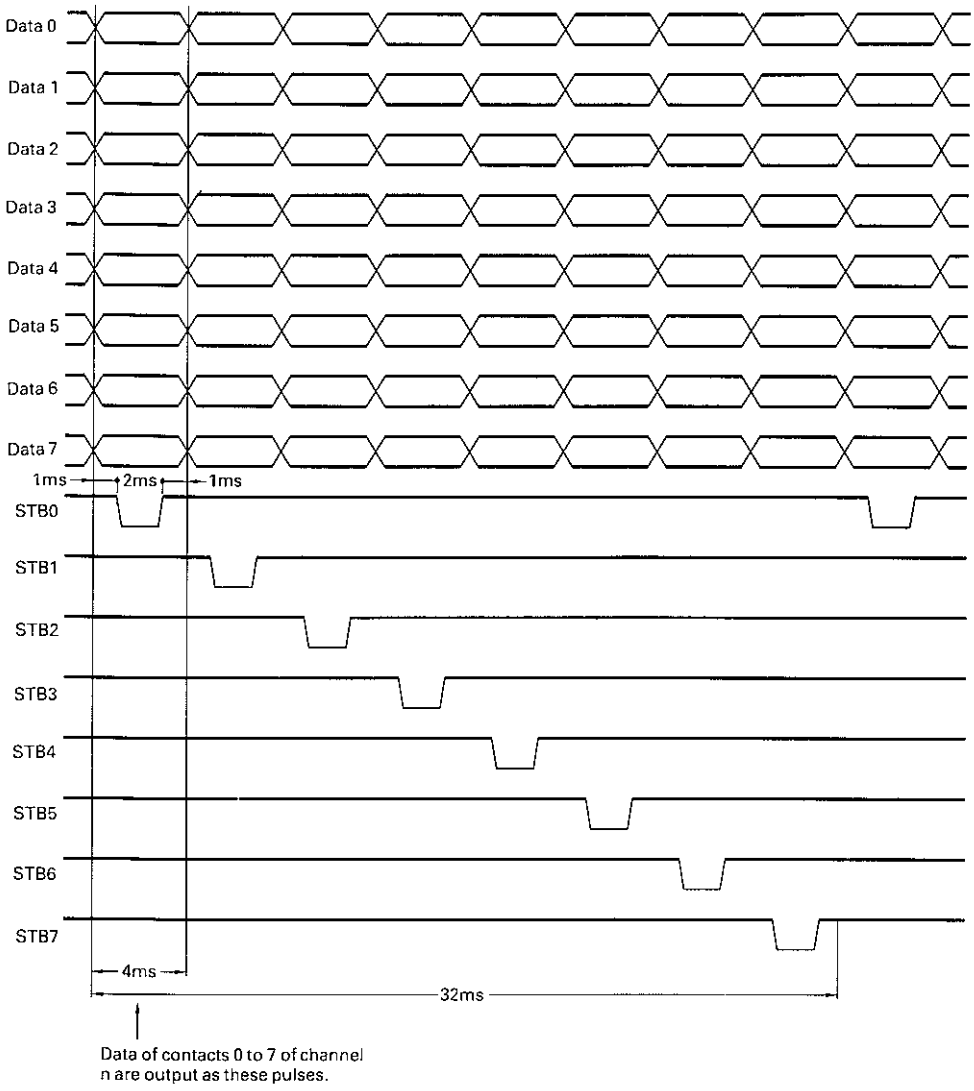
Relay No.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
n CH	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1
n+1 CH	1	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1
n+2 CH																
n+3 CH																

NOTE:
Channel n is determined according to the sequence in which the DC output unit is mounted to the SYSMAC-500. Refer to 3.2, Free location concept and I/O channels.

CAUTION FOR HANDLING
Since the DC output unit is operated by an extremely small current, provide an adequate distance between the wires of the unit and high-tension equipment or power lines when performing wiring; otherwise, use shielded cables. Also, keep the length of the wires within 10m. In the above diagram, supply voltage of DC 24V must be applied at the same time or before applying the supply voltage of DC 12V. The DC 24V supply voltage must be turned off at the same time or after turning off the DC 12V supply voltage.

TIMING


Data 0
Data 1
Data 2
Data 3
Data 4
Data 5
Data 6
Data 7
1ms
2ms
1ms
STB0
STB1
STB2
STB3
STB4
STB5
STB6
STB7
4ms
32ms
Data of contacts 0 to 7 of channel n are output as these pulses.

CHAPTER 3
ASSIGNMENT OF RELAY NUMBERS

Relay numbers correspond to the data memory areas, and the operating state (ON/OFF) of each relay is stored in the corresponding memory area. See list of relay numbers in **Appendix A.**

3.1 EXPLANATION OF SPECIAL AUXILIARY RELAY NUMBERS AND TEMPORARY MEMORY RELAY NUMBERS

The programmable controller has 45 special auxiliary relays. Some operate or release according to internal conditions controlled by the hardware, regardless of the conditions of I/O devices. The operations of the others are controlled by the software (FAL instruction).

Relay No. 6011:
This relay turns ON when the FUN99 (RUN stop) instruction is executed and indicates a power failure in the input power supply.

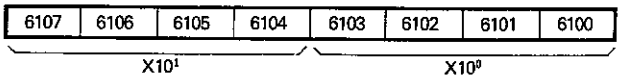
Relay No. 6012:
This relay serves as a data retention flag that can be turned ON by an OUT instruction and OFF by an OUT-NOT instruction. If the flag is turned OFF, all the data in the I/O, internal auxiliary, and link relay areas are cleared on starting the RUN operation. When this flag is turned ON, the previous data in those relay areas are retained.

NOTE: When a power failure occurs, this flag will retain the data stored earlier.

Relay No. 6015:
This relay serves as a LOAD OFF flag that can be turned ON by an OUT instruction and OFF by an OUT-NOT instruction. If this flag is turned OFF, the contents of the I/O relays are newly output to the output units. If the flag is turned ON, all output units are turned OFF, and the OUT INH indicator (LED) on the front panel of the CPU illuminates.

NOTE: When a power failure occurs, the LOAD OFF flag retains the data stored earlier.

Relay Nos. 6100 to 6107:
When Diagnostic (FAL, FALS) instruction is executed, an FAL No. (01 to 99) is output in BCD to each of the 6100 to 6107 relay numbers.



Further, the FAL No. is output to this area should an abnormal alarm output occur, such as one caused by battery failure.
In that event, the abnormal state will be reset through execution of the FAL 00 instruction or by means of the abnormal clear procedure, using the programming console.

NOTE: FAL No. 00 output to this area indicates the normal state.

Relay No. 6108:
This relay operates when a battery failure occurs and releases when the battery is returned to normal. To transmit the BATTERY FAILURE signal externally, prepare and program a circuit using the contacts of this relay.

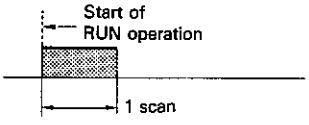
Relay No. 6109:
This relay operates when the scan time exceeds a predetermined period (or when the processing time of a user program exceeds 100msec).

Relay No. 6110:
This relay operates when the number of I/O units actually mounted disagrees with those registered by means of a free-location concept.

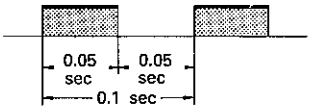
Relay No. 6113:
This relay is normally ON.

Relay No. 6114:
This relay is normally OFF.

Relay No. 6115:
This relay serves as an initial cycle ON flag. It operates only one scan time on start of the RUN operation. One scan time is the time required to execute a user program once starting from step 0000 to the END instruction of the program.

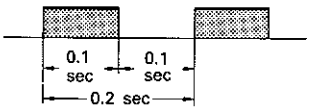


Relay No. 6300:
This relay is used to generate a 0.1-sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure.

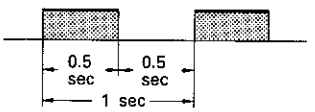


NOTE: The ON time of a 0.1-sec clock is 50msec. Therefore note that if the program execution time is prolonged, the CPU may fail to read the clock.

Relay No. 6301:
This relay is used to generate a 0.2-sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure or as a long-time timer.



Relay No. 6302:
This relay is used to generate a 1-sec clock. In conjunction with a counter, it functions as a timer for memory retention during a power failure or as a long-time timer. The relay output can also be used as a flicker signal.



Relay No. 6303:
This relay operates (ON) when the result of an arithmetic operation is not output in BCD, or when an address higher than 511 is specified in indirectly addressing the data memory.

Relay No. 6304:
This relay serves as a carry flag and operates or releases (ON or OFF) according to the result of an arithmetic operation. It is forcibly turned ON by an STC (Set Carry) instruction and OFF by a CLC (Clear Carry) instruction.

Relay No. 6305:
This relay operates if the result of a Compare operation (CMP instruction) executed is more than (>).

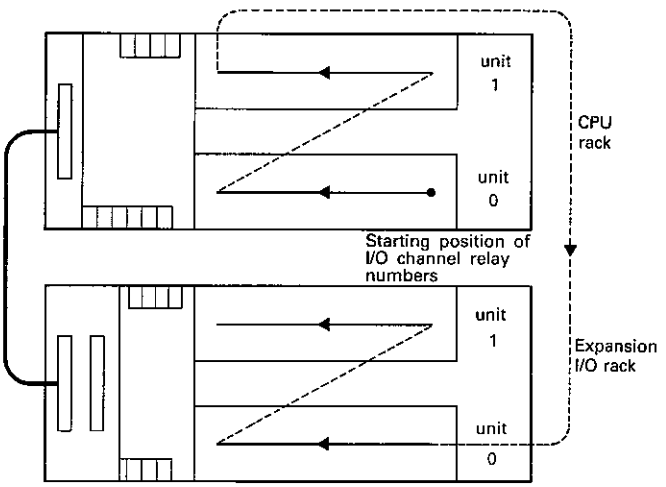
Relay No. 6306:
This relay operates if the result of a Compare operation (CMP instruction) executed is equal (=). It may operate if the result of an arithmetic operation is 0.

Relay No. 6307:
This relay operates if the result of a Compare operation (CMP instruction) executed is less than (<).

Relay Nos. TR 0 to TR 7:
- Relay numbers 0 to 7 may not necessarily be assigned consecutively.
- Temporary memory relay coil numbers cannot be used in duplication within the same block. With two or more blocks, they can be used in duplication.
- When using a temporary memory relay, the letters "TR" must be prefixed to the relay number (e.g., TR0).

3.2 FREE LOCATION CONCEPT AND I/O CHANNELS

The PC employs a free-location concept for I/O unit mounting. Any type of I/O unit can be mounted to the CPU rack in any order, and I/O channel relay numbers are assigned serially according to the mounting order of the I/O units.



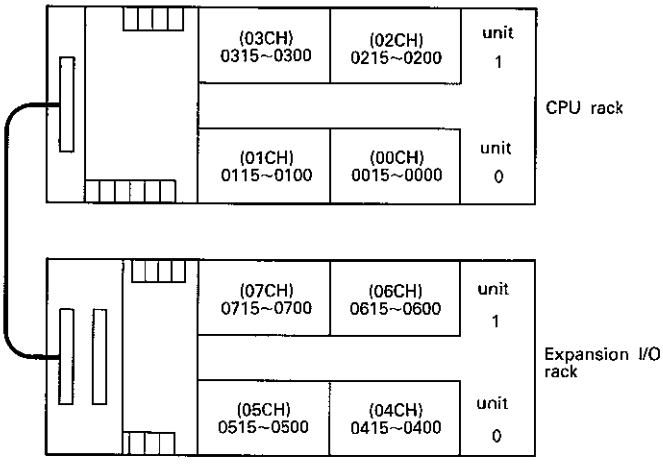
The rightmost point (0000: channel 00, bit 00) of the I/O unit mounted on the lower I/O unit mounting position of the CPU rack is regarded as the starting point of the assignment. The serial relay channel numbers are assigned from the right to the left starting from this point. The assignment continues in the same manner from the lower to the upper I/O unit mounting position on the CPU rack. The I/O unit(s) mounted on an expansion I/O rack connected to the CPU rack is also assigned with serial I/O channel relay numbers in exactly the same manner.

NOTES:
1. The I/O channel relay numbers are determined by registering the status of the mounted I/O unit(s) in the CPU memory. This registration is performed by using the programming console. For details, refer to I/O table generation procedures described in the user's manual for the programming console. The registered contents can be confirmed.

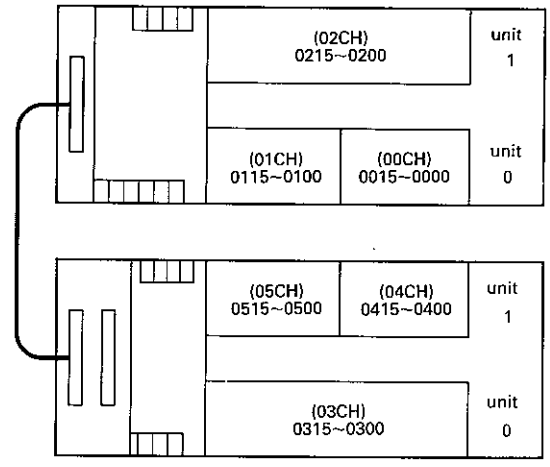
2. The vacant space is not registered as a channel.
3. *If an I/O unit is later mounted additionally to a vacant position, the I/O unit location will disagree with the registered location and cause an I/O verify error to occur. If this happens, register the I/O unit location again by following the procedure described in Note 1.*

WHEN I/O UNITS ARE FULLY MOUNTED IN ORDER

When only 32-point I/O units are mounted on the CPU and the expansion I/O rack, the relation between the I/O unit mounting positions and I/O channel relay numbers is as follows:



When 16-point I/O units and 32-point I/O units are mounted to the CPU rack in combination, the relation between I/O unit locations and channel relay numbers is as follows:



NOTES:

1. *If a mounted I/O unit is replaced with one having a different number of points, or if an additional I/O unit is mounted, the relay numbers assigned to the I/O unit already mounted to the right of the new I/O unit will be reassigned in sequence. The same applies when a mounted I/O unit is removed from the CPU rack, resulting in a vacancy. The relay numbers will not be changed, however, if a new I/O unit is mounted to the right of the unit that has been mounted on the right-most position of the existing I/O unit row. After the replacement, addition, or removal of an I/O unit, the relay numbers will not be modified unless the statuses of the mounted I/O units have been registered in the CPU memory. At this point, however, an I/O verify error or I/O setting error occurs.*
2. If a vacant position(s) is required to mount additional I/O unit(s) in the future because of possible modifications in design, use a dummy I/O unit(s) (3G2A6-DUM01) to reserve desired channels so that no program modification will be required.

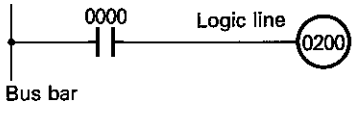
CHAPTER 4
INSTRUCTION WORDS

See Appendix for List of instructions.

4.1 LOAD(LD)/AND(AND)/OR(OR)/ OUTPUT(OUT) INSTRUCTIONS

4.1.1 LOAD(LD) & OUTPUT(OUT) instructions

If each logic line starts with an NO contact, use the LD instruction.
Use the OUT instruction for relay coil.

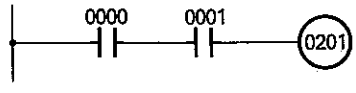


Coding

Address	OP	Data
0000	LD	0000
0001	OUT	0200

4.1.2 AND instruction

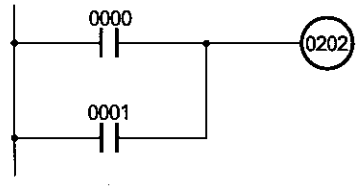
NO contacts in series are processed by the AND instruction.



Address	OP	Data
0003	LD	0000
0004	AND	0001
0005	OUT	0201

4.1.3 OR instruction

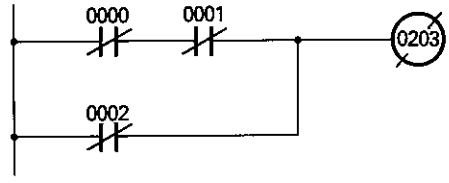
NO contacts in parallel are processed by the OR instruction.



Address	OP	Data
0006	LD	0000
0007	OR	0001
0008	OUT	0202

4.1.4 LOAD NOT (LD-NOT) instruction

If each logic line starts with an NC contact, use the LD-NOT instruction in place of the LD instruction.



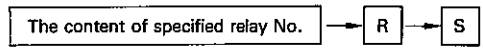
Address	OP	Data
0009	LD-NOT	0000
0010	AND-NOT	0001
0011	OR-NOT	0002
0012	OUT-NOT	0203

Contents of data

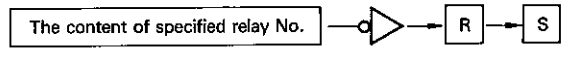
	LD	LD-NOT, AND, AND-NOT, OR, OR-NOT	OUT	OUT NOT
I/O relay, internal auxiliary relay	0000 to 6307		0000 to 6015	
Link relay	LR 0000 to 3115			
Holding relay	HR 0000 to 3115			
Timer, counter	TIM, CNT000 to 127			
Temporary memory relay	TR 0 to 7	–	TR 0 to 7	–

OPERATION OF EACH REGISTER

LD . . . . . The LD instruction causes the content (ON or OFF state) of the specified relay number to be stored in the RESULT REGISTER (hereafter referred to as "R register"). It also causes the previous result in the R register to be transferred to the STACK REGISTER (hereafter referred to as "S register").

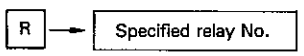


LD-NOT.. The LD-NOT instruction causes the content of the specified relay number to be inverted and then stored in the R register.

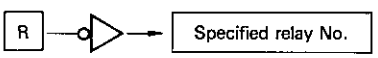


Like the LD instruction, this instruction causes the previous result in the R register to be transferred to the S register.

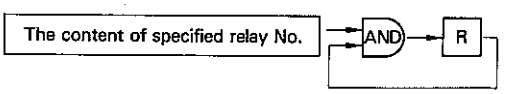
OUT..... The OUT instruction causes the content of the R register to be output to the specified relay number. In this case the content of the R register will remain unchanged.



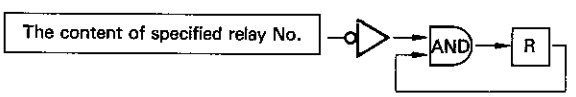
OUT-NOT. The OUT-NOT instruction causes the content of the R register to be inverted and then output to the specified relay number. In this case the content of the R register will remain unchanged.



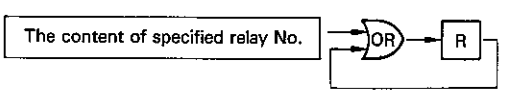
AND..... The AND instruction causes the logical AND operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical AND operation will be newly stored in the R register.



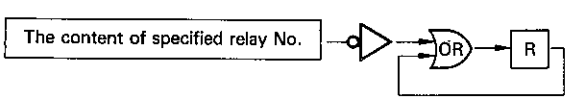
AND-NOT. The AND-NOT instruction causes the content of the specified relay number to be inverted and then ANDed with the content of the R register. The result of the logical AND operation will be newly stored in the R register.



OR..... The OR instruction causes the logical OR operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical OR operation will be newly stored in the R register.



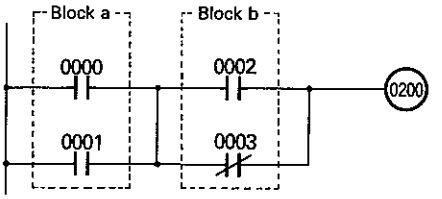
OR-NOT.. The OR-NOT instruction causes the content of the specified relay number to be inverted and then ORed with the content of the R register. The result of the logical OR operation will be newly stored in the R register.



NOTE: The number of contacts in series or parallel is not limited for use on a logic line within a program capacity.

4.2 AND-LOAD (AND-LD) INSTRUCTION

For interblock AND operation between two or more blocks, use the AND-LD instruction.



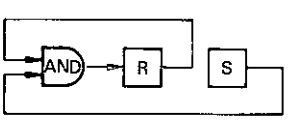
Coding

Address	OP	Data
0200	LD	0000
0201	OR	0001
0202	LD*	0002
0203	OR-NOT	0003
0204	AND-LD**	—
0205	OUT	0200

NOTES: * Use this instruction as the first instruction for the next block to be ANDed with the preceding block.
** Use the AND-LD instruction for series connection of two blocks (blocks a and b).

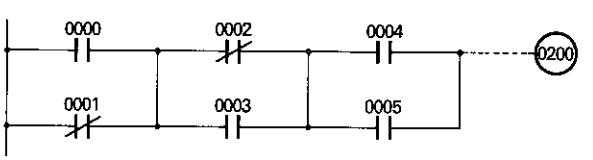
OPERATION OF EACH REGISTER

1. By the LD0000 and OR0001 instructions, the result of the logical OR operation in block a is stored in the R register.
2. By the LD0002 instruction in block b, the result of the operation in block a is transferred in the S register, and the result of the logical operation by instructions LD0002 and OR-NOT0003 in block b is stored in the R register.
3. The AND-LD instruction causes a logical AND operation to be performed between the R register and the S register. The result of the logical AND operation will be newly stored in the R register.



NUMBER OF BLOCKS

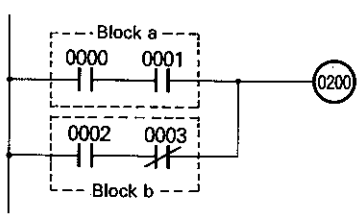
The number of blocks is not limited for AND-LD operation of a logic line. As many blocks as required can be continued for series connection by means of LD to AND-LD keys.



OP	Data
LD	0000
OR-NOT	0001
LD-NOT	0002
OR	0003
AND-LD	–
LD	0004
OR	0005
AND-LD	–
OUT	0200

4.3 OR-LOAD (OR-LD) INSTRUCTION

For interblock OR operation between two or more blocks, use the OR-LOAD instruction.



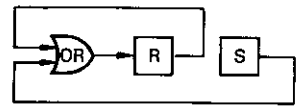
Coding

Address	OP	Data
0200	LD	0000
0201	AND	0001
0202	LD*	0002
0203	AND-NOT	0003
0204	OR-LD**	–
0205	OUT	0200

NOTES: * Use this LD instruction as the first instruction of the next block to be ORed with the preceding block.
** Use the OR-LD instruction for parallel connection of two blocks (blocks a and b).

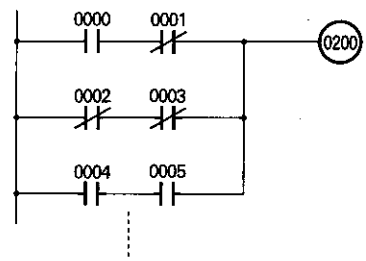
OPERATION OF EACH REGISTER

1. By the LD0000 and AND0001 instructions, the result of the logical AND operation in block a is stored in the R register.
2. By the LD0002 instruction in block b, the result of the operation in block a is transferred into the S register, and the result of the logical operation by instructions LD0002 and AND-NOT0003 in block b is stored in the R register.
3. The OR-LD instruction causes a logical OR operation to be performed between the R register and the S register. The result of the logical OR operation will be newly stored in the R register.



NUMBER OF BLOCKS

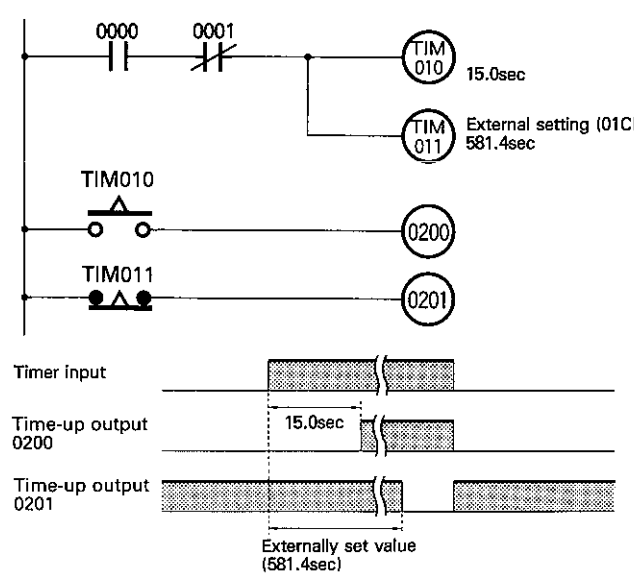
The number of blocks is not limited for OR-LD operation on a logic line. As many blocks as required can be continued for parallel connection by means of LD to OR-LD keys.



OP	Data
LD	0000
AND-NOT	0001
LD-NOT	0002
AND-NOT	0003
OR-LD	–
LD	0004
AND	0005
OR-LD	–
OUT	0200

4.4 TIMER (TIM) INSTRUCTION

The TIM instruction can be used as an ON-delay timer in the same manner as a relay circuit.



Coding

Address	OP	Data	
0200	LD		0000
0201	AND-NOT		0001
0202	TIM		010*
		#	0150**
0203	TIM		011
			01
0204	LD	TIM	010
0205	OUT		0200
0206	LD-NOT	TIM	011
0207	OUT		0201

NOTES:
1. * Timer number 000 to 127.
   ** Time setting value 0000 to 9999 x 0.1sec.
2. *Timer numbers are shared by both timers and counters. Therefore a number already assigned to a timer must not be used for any other timer or counter.*

Externally set channel

Input/output relay, internal auxiliary relay	00 to 63
Link relay	LR00 to 31
Holding relay	HR00 to 31

OPERATION OF EACH REGISTER

The timer starts when the content of the R register is logical 1 and resets when the content of the R register is logical 0.

NUMBER OF CONTACTS

A time-up contact designates the timer number itself. Both NO and NC contacts can be used in the required quantity.

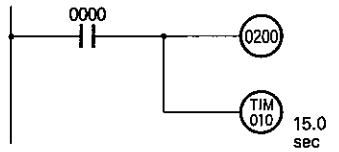
TIMER IS DECREMENTING TYPE

The timer is a decrementing type that produces an output when the present value (time remaining) becomes "0000". When the timer input is turned off, the present value of the timer returns to the preset value. The timer output is transmitted externally through an output relay as shown in the above circuit example.

TIMER IS RESET AT THE TIME OF A POWER FAILURE

If a power failure occurs, the timer is reset and the present value returns to the preset value. Therefore, if retaining the present value of the timer in the memory is required, a memory retentive type timer circuit, as shown below, must be used for programming.

CONSECUTIVE OUT INSTRUCTION AND TIM INSTRUCTION



OP		Data
LD		0000
OUT		0200
TIM		010
	#	0150

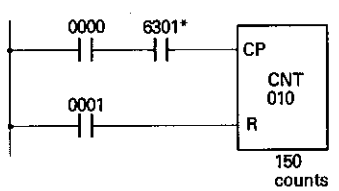
When the NO contact 0000 turns ON, output relay 0200 is energized and at the same moment timer 010 starts operating.

EXTERNALLY SET TIMER DATA

Externally set timer data must be in four BCD digits, and the CPU checks whether it is or not. If it is not, special auxiliary relay 6303 is turned ON, indicating an error. In this case the program can still be executed, but the time-up operation may not be accurate.

MEMORY RETENTIVE TYPE TIMER

A circuit to retain the present value of the timer during a power failure is configured using a combination of clock instruction and counter (CNT) instruction.

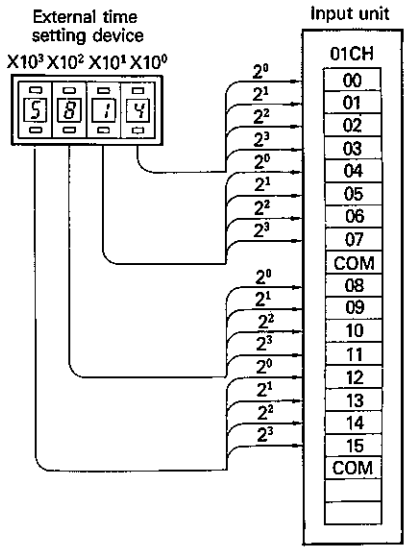


OP		Data
LD		0000
AND		6301*
LD		0001
CNT		010
	#	0150

NOTE: * Special auxiliary relay 6301 is used to generate a 0.2sec clock pulse.

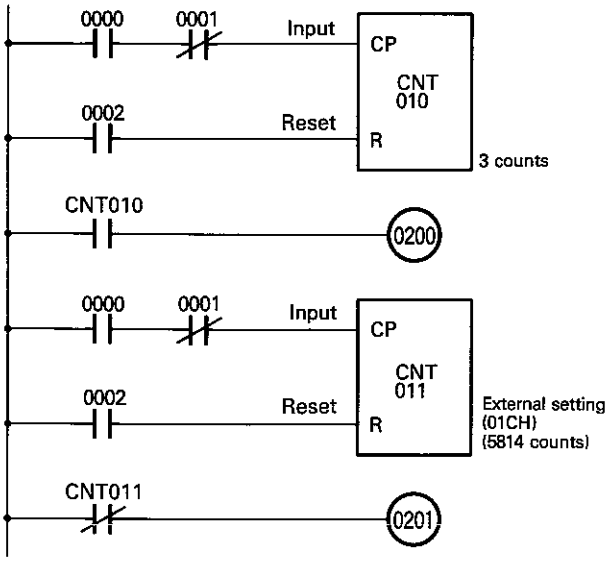
USE OF AN EXTERNALLY SET TIMER

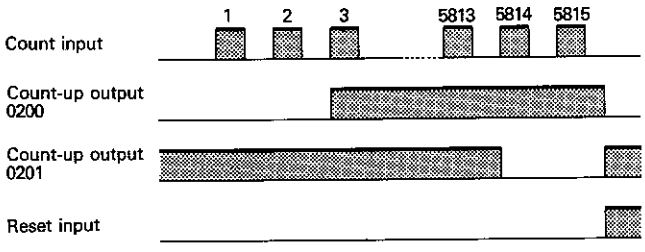
In the above example, the timer 011 of the other system is used for external time setting. An external time setting device is connected to channel No. 01 (C I/O input unit) of its own system so that the timer operation will be up after the lapse of 581.4sec set by the external time setting device.



4.5 COUNTER (CNT) INSTRUCTION

The CNT instruction can be used as a preset counter in the same manner as a relay circuit.





Coding

Address	OP		Data
0200	LD		0000
0201	AND-NOT		0001
0202	LD		0002
0203	CNT		010
		#	0003
0204	LD	CNT	010
0205	OUT		0200
0206	LD		0000
0207	AND-NOT		0001
0208	LD		0002
0209	CNT		011
			01
0210	LD-NOT	CNT	011
0211	OUT		0201

NOTES:
1. A counter program must be entered in the order of a count input circuit, a reset input circuit, and a counter coil.
2. Counter number 000 to 127.
3. Counter setting value 0000 to 9999.
4. *Counter numbers are shared by both counters and timers. Therefore, a number already assigned to a counter must not be used for any other timer or counter.*

Externally set channel

Input/output relay Internal auxiliary relay	00 to 63
Link relay	LR00 to 31
Holding relay	HR00 to 31

OPERATION OF EACH REGISTER

The counter resets when the content of the R register is logical 1 and is enabled to count when the content of the R register is logical 0. A count input is provided from the S register.

NUMBER OF CONTACTS

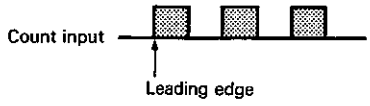
A count-up contact designates the counter number itself. Both NO and NC contacts can be used in the required quantity.

COUNTER IS DECREMENTING TYPE

The counter is a decrementing type that produces an output when the count value becomes "0000". The present value of the counter returns to the preset value when a reset input is applied. The counter output is transmitted externally through an output relay as shown in the circuit example.

After the preset count is up, subsequent count inputs are ignored.

At the leading edge (i.e., from OFF to ON) of a count input signal, the counter decrements the count value by 1.



When both a count input and a reset input are applied simultaneously, the reset input takes precedence. Even if the reset input is removed after this, the counter performs no counting operation.

EXTERNALLY SET COUNTER DATA

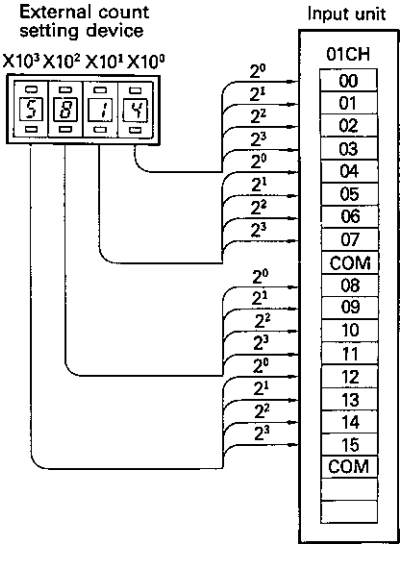
Externally set counter data must be in four BCD digits. The CPU checks whether the externally set counter data is in four BCD digits or not. If not in BCD digits, special auxiliary relay 6303 is turned ON, indicating an error. In this case the program can still be executed, but the count-up operating may not be accurate.

MEMORY RETAINING DURING A POWER FAILURE

The present value of the counter is retained in memory during a power failure. If a power failure occurs, the counter is not reset and the present value (i.e., count remaining) of the counter is retained in the memory.

USE OF AN EXTERNALLY SET COUNTER

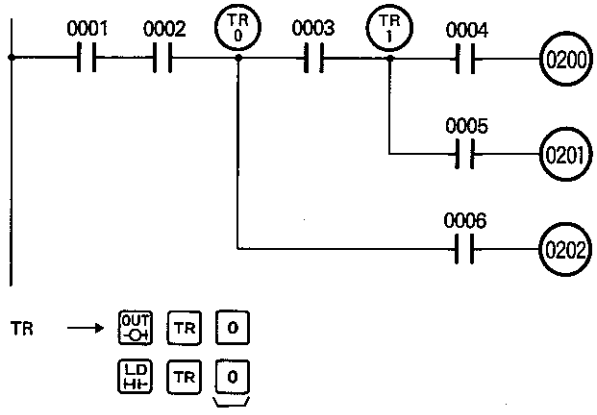
In the example, the counter 011 of the other system is used for external count setting. An external count-setting device is connected to channel No. 01 (C I/O input unit) of its own system so that the counter operation will be up when the value (5814 counts) set by the external count-setting device has been counted.



4.6 TEMPORARY MEMORY RELAY (TR) INSTRUCTION

The TR instruction can be used as a temporary memory relay.

To program a temporary memory relay, the TR instruction must be used with an OUT or LD instruction.



Relay numbers are 0 to 7.

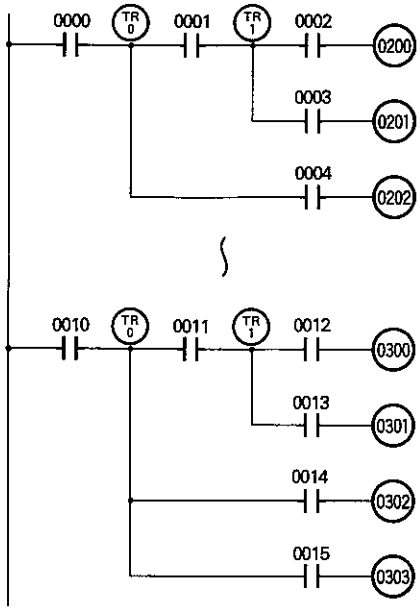
Coding

Address	OP	Data	
0200	LD		0001
0201	AND		0002
0202	OUT	TR	0
0203	AND		0003
0204	OUT	TR	1
0205	AND		0004
0206	OUT		0200
0207	LD	TR	1
0208	AND		0005
0209	OUT		0201
0210	LD	TR	0
0211	AND		0006
0212	OUT		0202

The TR instruction is used when a ladder diagram cannot be programmed with interlock (IL/ILC) instructions.

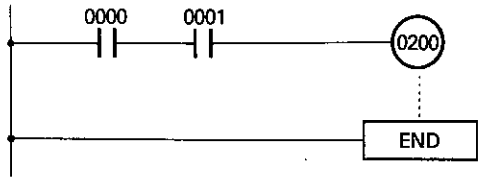
In an output branching circuit consisting of multiple blocks, temporary memory relay numbers are used at each point, but they cannot be used in duplication in the same block.

Example



4.7 END (FUN01) INSTRUCTION

Insert this instruction at the end of a program.

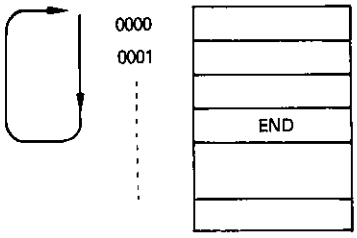


END → FUN 0 1

Coding

Address	OP	Data
0000	LD	0000
0001	AND	0001
0002	OUT	0200
⋮	⋮	⋮
0700	END(01)	—

The CPU scans program data from address 0000 to the address with an END instruction according to the sequence diagram.

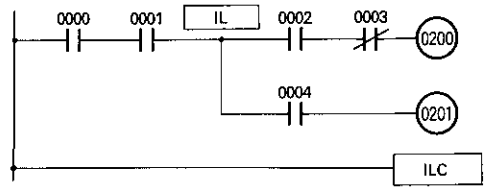


When performing a test run, insert an END instruction at each end of a sequence circuit, and then delete the END instruction after confirming each circuit. In this manner, the test run can be executed smoothly.

NOTE: If an attempt is made to operate the PC without inserting an END instruction at the end of the program, the RUN indicator on the front panel of the CPU does not illuminate and the PC will not operate. In this case the ERR indicator will illuminate.
If such an attempt is made with the programming console connected to the PC, the error message "NO END INSTR" will appear on the LCD of the programming console.

4.8 INTERLOCK [IL(FUN02)] /INTERLOCK CLEAR [ILC(FUN03)] INSTRUCTIONS

The IL and ILC instructions are used in pairs when branching a circuit to plural OUT instructions.



IL → FUN 0 2

ILC → FUN 0 3

Coding

Address	OP	Data
0200	LD	0000
0201	AND	0001
0202	IL(02)	—
0203	LD	0002
0204	AND-NOT	0003
0205	OUT	0200
0206	LD	0004
0207	OUT	0201
0208	ILC(03)	—

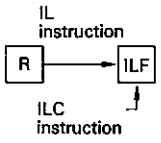
NOTE: When the IL condition is OFF (i.e., when input 0000 or 0001 is OFF in the above example), the state of each relay between the IL and ILC instructions is:

Output relay, internal auxiliary relay	OFF
Timer	Reset
Counter, shift register, holding relay	Holds present state

However, when the IL condition is ON, the state of each relay is the same as that in an ordinary relay circuit without IL/ILC instructions.

OPERATION OF EACH REGISTER

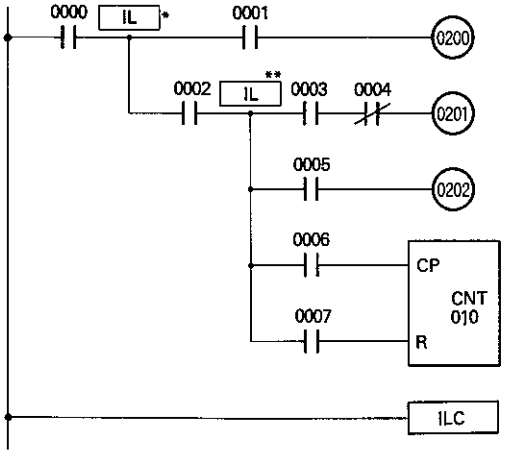
When the interlock flip-flop (ILF) in the CPU is "0", the content of the R register is fixed to "0". Therefore, until the ILF is set to "1", the output relay will remain OFF.



The IL instruction causes the content of the R register to be transferred to the ILF. Therefore, the ILF is set to "0" if the content of the R register is "0". The ILC instruction causes the ILF to be set to "1", regardless of the content of the R register.

NOTE: The invert output relay is also turned OFF.

IL-ILC ERROR

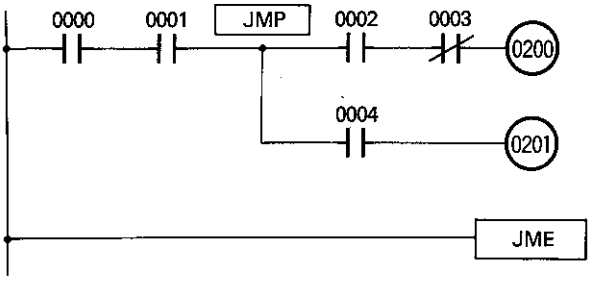


If IL and ILC instructions are not used in pairs (as IL/IL/ILC in the above example), this is judged as an IL-ILC error during the program check. The operation of the circuit in this case will be as programmed, which is shown below.

1. If the condition of IL* is OFF, output relays 0200, 0201, and 0202 are all OFF, and counter CNT010 retains its present count value.
2. If the conditions of both IL* and IL** are OFF, the state of each relay is the same as 1.
3. If the condition of IL* is ON and that of IL** is OFF, output relay 0200 turns ON or OFF if input 0001 is ON or OFF, and output relays 0201 and 0202 remain in the OFF state. Counter CNT010 retains its present count value.
4. If the condition of IL* is OFF and that of IL** is ON, the state of each relay is the same as 1 and 2.

4.9 JUMP [JMP(FUN04)]/JUMP END [JME(FUN05)] INSTRUCTIONS

The JMP instruction is used in conjunction with the JME instruction and causes the contents of a program between these two instructions to be ignored or executed according to the result immediately before the JMP instruction.



JMP → FUN 0 4

JME → FUN 0 5

Coding

Address	OP	Data
0200	LD	0000
0201	AND	0001
0202	JMP(04)	—
0203	LD	0002
0204	AND-NOT	0003
0205	OUT	0200
0206	LD	0004
0207	OUT	0201
0208	JME(05)	—

NOTE: When the JMP condition is OFF (i.e., when input 0000 or 0001 is OFF in the above example), the state of each relay between the JMP and JME instructions is:

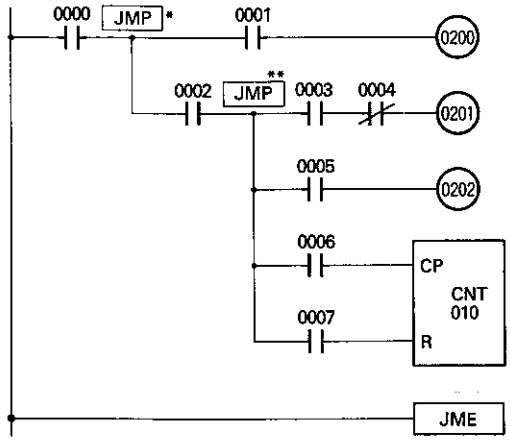
Output relay, internal auxiliary relay	Holds present state
Timer	ditto
Counter, shift register	ditto

However, if the JMP condition is ON, the state of each relay is the same as that in an ordinary relay circuit without JMP/JME instructions.

OPERATION OF EACH REGISTER

If the content of the R register is "0", the program steps between the JMP and JME instructions are not executed. In other words, the states of output relays, internal auxiliary relays, timers, and counters remain unchanged. If the content of the R register is "1", the program steps between the two instructions are executed.

JMP-JME ERROR

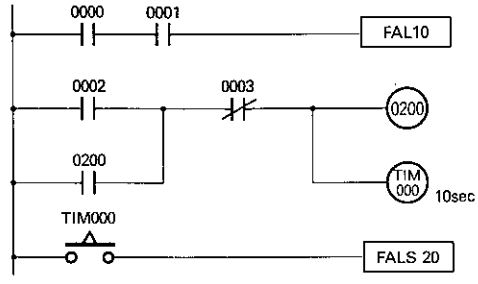


If JMP and JME instructions are not used in pairs (as JMP/JMP/JME in the above example), this is judged as a JMP-JME error during the program check. The operation of the circuit in this case will be as programmed, which is shown below.

1. If the condition of JMP* is OFF, output relays 0200, 0201, and 0202 remain in their present ON/OFF states, and counter CNT010 retains its present count value.
2. If the conditions of both JMP* and JMP** are OFF, the state of each output relay is the same as 1.
3. If the condition of JMP* is ON and that of JMP** is OFF, output relay 0200 turns ON or OFF if input 0001 is ON or OFF, and output relays 0201 and 0202 remain in their present ON/OFF state. Counter CNT010 retains its present count value.
4. If the condition of JMP* is OFF and that of JMP** is ON, the state of each output relay is the same as 1 and 2.

4.10 DIAGNOSTIC [FAL(FUN06)/FALS (FUN07)] INSTRUCTION

The FAL and FALS instructions are used to output the failure or abnormal mode to the FAL area, indicating the occurrence of a failure or abnormality in the internal circuit during the operation of the PC.



FAL → FUN 0 6

FALS → FUN 0 7

Coding

Address	OP		Data
0200	LD		0000
0201	AND		0001
0202	FAL(06)		10
0203	LD		0002
0204	OR		0200
0205	AND-NOT		0003
0206	OUT		0200
0207	TIM		000
0208		#	0100
0208	LD	TIM	000
0209	FALS(07)		20

NOTES: 1. FAL No. is 01 to 99.
2. Use FAL00 instruction to reset FAL area display.
3. Note that the FAL number is commonly used by FAL and FALS instructions.

OPERATION OF EACH REGISTER

The FAL or FALS instruction is executed only when the content of the R register is logical 1 and is not executed when the content of the R register is logical 0.

When the FAL instruction is executed, the FAL number applicable to the failure is output to the FAL area, and the ALARM indicator (LED) on the front panel of the CPU illuminates. The CPU continues program execution, however.

	6107	6106	6105	6104	6103	6102	6101	6100
FAL area (FAL10)	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"
	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
	X10				X1			

A maximum of two FAL errors can be stored in memory when another FAL error is detected before the first FAL error has been removed.

To reset the FAL area output, remove the cause of the FAL error and then execute a FAL00 instruction.
If the programming console is connected to the PC, FAL area outputs can also be reset by performing a FAILURE READ operation.

Each time the FAL00 instruction is executed, the FAL area output is reset and another FAL error retained in the memory is output.

Other alarms and failures, such as battery error and remote I/O error, are also output to the FAL area in addition to FAL and FALS instructions.

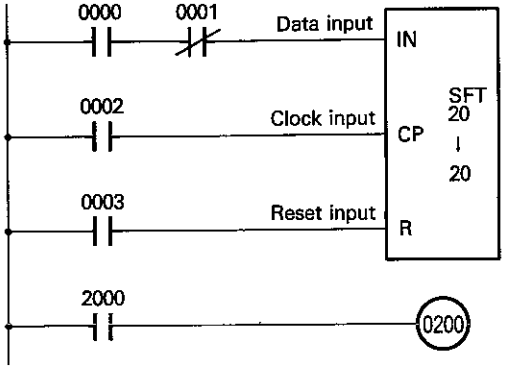
CAUTION
When the FALS instruction is executed, a FALS number is output to the FAL area and the ERR indicator (LED) on the front panel of the CPU illuminates. Then the PC stops.

To reset the FALS output, remove the cause of the FALS errors, and then perform a FAILURE READ operation using the programming console with the program mode set by its mode selector switch.
The FALS output can also be reset by restarting the PC using the mode selector switch (RUN to PROGRAM to RUN) after removing the cause of the FALS error.
If a FALS error or any other error that causes the PC to stop has occurred while a FAL error is being detected, that FALS or failure number is output in place of the FAL number.

Priority of output:
The output of the FALS or the failures that cause the PC to stop take precedence over the FAL or those that do not.

4.11 SHIFT REGISTER [SFT(FUN10)] INSTRUCTION

The SFT instruction can be used as a serial input shift register.



SFT → FUN 1 0 — Start channel number / End channel number

Coding

Address	OP		Data
0200	LD		0000
0201	AND-NOT		0001
0202	LD		0002
0203	LD		0003
0204	SFT(10)		20
			20
0205	LD		2000
0206	OUT		0200

Contents of data (start channel and end channel numbers)

Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31

NOTE: A shift register must be programmed in the order of data input, clock input, reset input, and an SFT instruction (from the start channel to the end channel).

Each SFT instruction must be specified in units of 16 bits. In the above example, 16 bits from 2000 to 2015 are transferred.

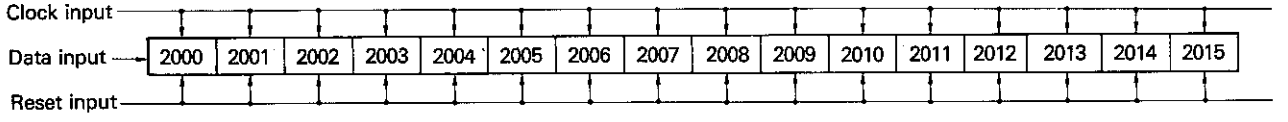
The 16-bit contents (2000 to 2015 in the above example) of the shift register can be output bit by bit using an LD instruction.

When a reset input is applied to the shift register, 16 bits are reset together.

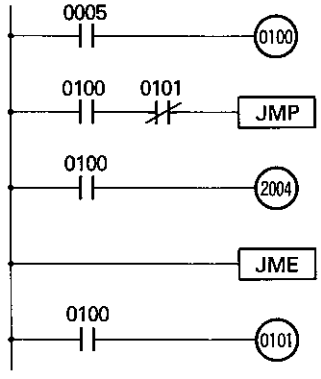
The data are shifted at the leading edge of an input clock.

DATA RETAINING DURING A POWER FAILURE

If the holding relay area is used, the data are retained during power failure until a clock or reset input is applied.



ANY OF THE 16 BITS CAN BE SET OR RESET BY FORCE

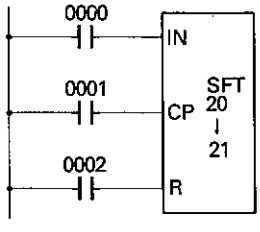


OP	Data
LD	0005
OUT	0100
LD	0100
AND-NOT	0101
JMP(04)	—
LD	0100
OUT	2004
JME(05)	—
LD	0100
OUT	0101

With a circuit arranged as shown above, a bit in 2004 can be set forcibly when NO contact 0005 is turned ON. Use the NC contact of 0100 to reset the SFT bit forcibly.

SHIFT REGISTER EXCEEDING 16 BITS

In this case, a shift register circuit can be configured by combining two or more stages of 16-bit shift registers.



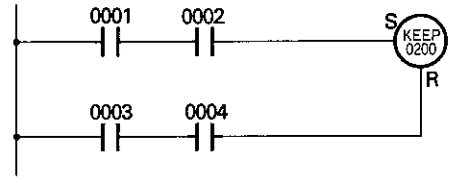
Address	OP	Data
0200	LD	0000
0201	LD	0001
0202	LD	0002
0203	SFT(10)	20
		21

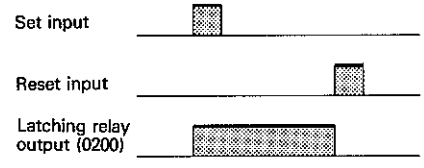
The above circuit configuration shows a 32-bit shift register from 2000 to 2115.

The data for the SFT instruction must be input with the upper-stage SFT data less than or equal to the lower-stage SFT data and within the same relay area.

4.12 LATCHING RELAY [KEEP(FUN11)] INSTRUCTION

The KR instruction can be used as a latching relay in the same manner as a relay circuit.





KEEP → FUN 1 1

Coding

Address	OP	Data
0200	LD	0001
0201	AND	0002
0202	LD	0003
0203	AND	0004
0204	KEEP(11)	0200

Contents of data

Input/output relay, internal auxiliary relay	0000 to 6015
Link relay	LR0000 to 3115
Holding relay	HR0000 to 3115

NOTE: A latching relay program must be entered in the order of a set input circuit, a reset input circuit, and a latching relay coil.

OPERATION OF EACH REGISTER

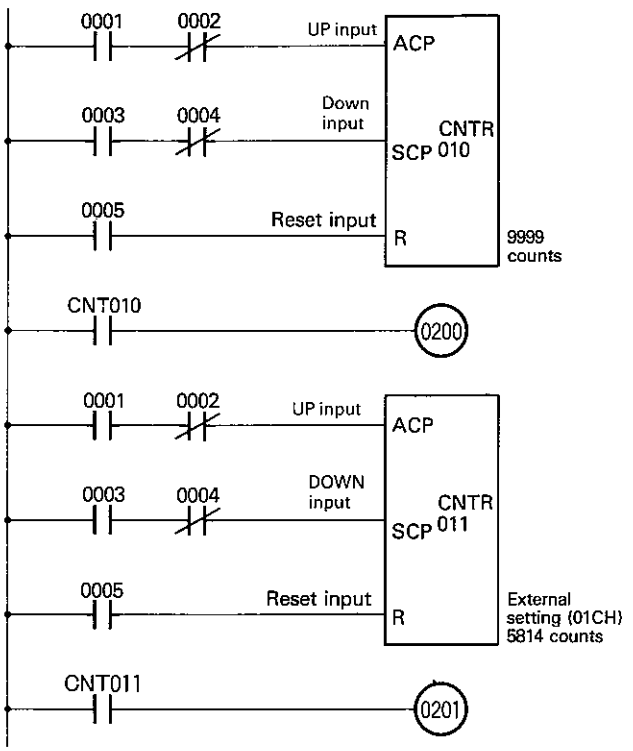
The latching relay operates when the content of the R register is logical 0 and the content of the S register is logical 1. The relay releases when the content of the R register is logical 1.

When both a set input and a reset input are applied simultaneously, the reset input takes precedence.

If a holding relay (HR) is used as a latching relay, data in the memory are retained during power failure until a set or reset input is applied.

4.13 UP-DOWN COUNTER [CNTR(FUN12)] INSTRUCTION

The CNTR(FUN12) instruction can be used as an up-down (reversible) counter in the same manner as a relay circuit.



CNTR → FUN 1 2

Coding

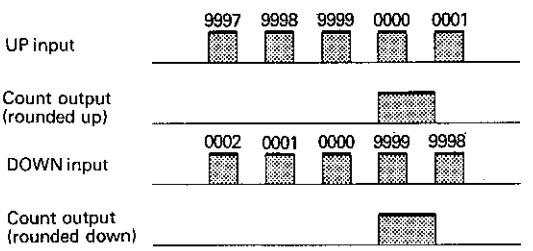
Address	OP		Data
0200	LD		0001
0201	AND-NOT		0002
0202	LD		0003
0203	AND-NOT		0004
0204	LD		0005
0205	CNTR(12)		010
		#	9999
0206	LD	CNT	010
0207	OUT		0200
0208	LD		0001
0209	AND-NOT		0002
0210	LD		0003
0211	AND-NOT		0004
0212	LD		0005
0213	CNTR(12)		011
			01
0214	LD	CNT	011
0215	OUT		0201

Externally set channel

Input/output relay, internal auxiliary relay	00 to 63
Link relay	LR00 to 31
Holding relay	HR00 to 31

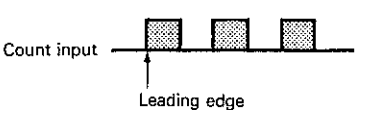
NOTES: 1. An externally set up-down counter program must be entered in the order of an UP input circuit, a DOWN input circuit, a reset input circuit, and a counter coil.
2. *Externally set up-down counter numbers are shared with timers, high-speed timers, down counters, and up-down counters. Therefore, a number already assigned to an externally set up-down counter cannot be used by any other counter or timer.*

COUNT OUTPUTS (CARRY AND BORROW)



The present value of the counter is retained in memory during a power failure. The present value of the counter is reset to "0000" when a reset input is applied.

At the leading edge (i.e., from OFF to ON) of an UP or DOWN input, the counter increments or decrements the count value by 1.



When both an UP/DOWN input and a reset input are applied simultaneously, the reset input takes precedence. Even if the reset input is removed after this, the counter performs no counting operation until the UP/DOWN input has been removed once.

When both an UP input and a DOWN input rise simultaneously, the counter performs no counting operation.

When a reset input is applied, the present value of the counter is reset to "0000". However, no count output is generated.

The up-down counter performs a ring counter operation according to the ring value.

UP → 9998, 9999, 0000, 0001 . . . . .
DOWN → 0001, 0000, 9999, 9998 . . . . .

Therefore, note that the count output (carry or borrow) is different from the count.

NUMBER OF CONTACTS

A count output contact designates the same number as the counter number. Both NO and NC contacts can be used in the required quantity.

EXTERNALLY SET UP-DOWN COUNTER DATA MUST BE 4-DIGIT BCD

The CPU checks whether the externally set data is in four BCD digits. If not, special auxiliary relay 6303 is turned ON, indicating an error. In this case the program can still be executed, but count-down operation may not be accurate.

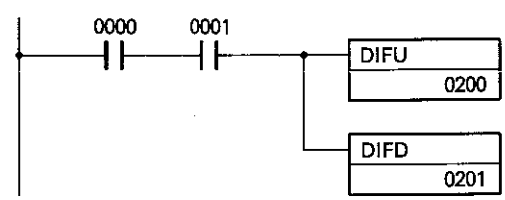
USE OF EXTERNALLY SET UP-DOWN COUNTER

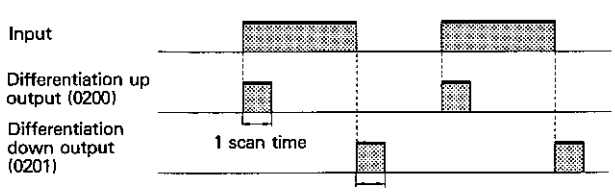
In the above circuit example, counter 011 is used for external up-down count setting. An external count-setting device is connected to channel No. 01 of its own system, and the number of counts (ring value) is determined by the set value of the setting device.
Because the ring value is 5814, the up-down counter repeats its operation in this way.

When performing add operation
..... 5813, 5814, 0000, 0001 .....
When performing subtract operation
..... 0001, 0000, 5814, 5813 .....

4.14 DIFFERENTIATION UP [DIFU (FUN13)] /DIFFERENTIATION DOWN [DIFD(FUN14)] INSTRUCTIONS

The DIFU and DIFD instructions are used to output the differentiation of an input condition to a specified relay for 1 scan time.





DIFU → FUN 1 3
DIFD → FUN 1 4

Coding

Address	OP	Data
0200	LD	0000
0201	AND	0001
0202	DIFU(13)	0200
0203	DIFD(14)	0201

Contents of data

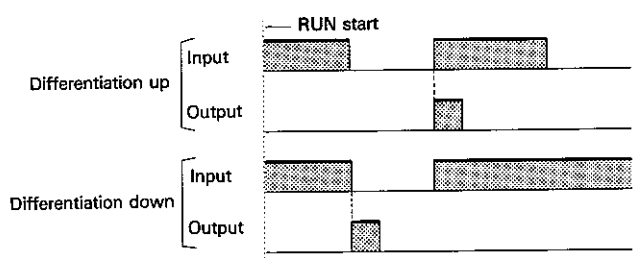
Input/output relay	0000 to 6015
Link relay	LR0000 to 3115
Holding relay	HR0000 to 3115

OPERATION OF EACH REGISTER

The DIFU instruction must be set so that the output is issued for 1 scan time at the leading edge of the R register, that is, at the point when the R register's level turns from 0 to 1. Conversely, the DIFD instruction must be set so that the output is issued at the trailing edge of the R register (1 to 0).

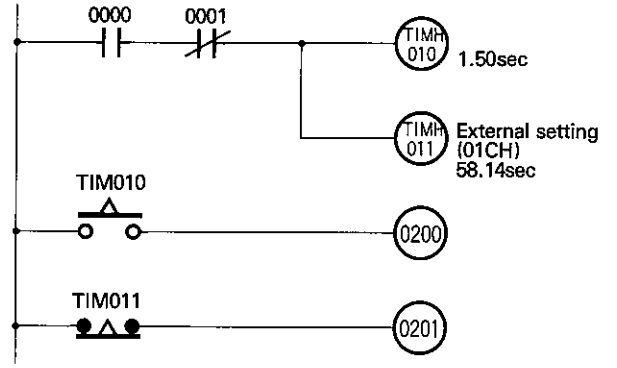
NOTE: The maximum number of DIFU and DIFD instructions that can be programmed together is 128. The 129th or later differentiation instructions are regarded as NOP (no operation).

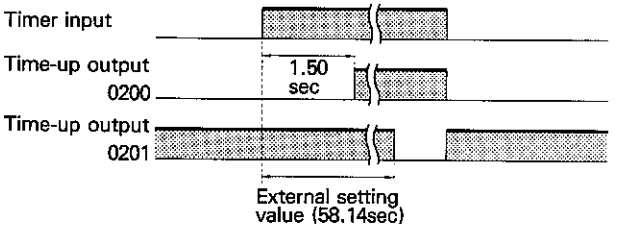
The differentiation instructions perform their operations in response to changes in input after the PC starts operating.



4.15 HIGH-SPEED TIMER [TIMH(FUN15)] INSTRUCTION

The TIMH(FUN15) instruction can be used as a high-speed timer in the same manner as a relay circuit.





TIMH → FUN 1 5

Coding

Address	OP		Data
0200	LD		0000
0201	AND-NOT		0001
0202	TIMH(15)		010*
		#	0150**
0203	TIMH(15)		011
			01
0204	LD	TIM	010
0205	OUT		0200
0206	LD-NOT	TIM	011
0207	OUT		0201

NOTES: 1. * Timer numbers 000 to 127 can be assigned to a TIMH instruction.
2. ** The time setting of the TIMH instruction can be performed in units of 0.01sec, from 00.00sec to 99.99sec.
3. *High-speed timer numbers are shared by timers, counters, and up-down counters. Therefore, a number already assigned to a high-speed timer cannot be used for any other timer or counter.*

Externally set channel

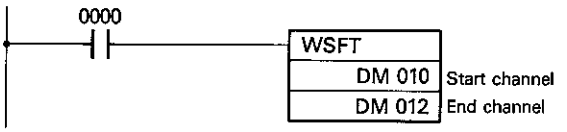
Input/output relay, internal auxiliary relay	00 to 63
Link relay	LR00 to 31
Holding relay	HR00 to 31

The operating conditions and contents of the operation are the same as the timer instruction.

Note that if the cycle time exceeds 10msec, the timing operation may be inaccurate.

4.16 WORD SHIFT [WSFT(FUN16)] INSTRUCTION

The WSFT instruction is used to shift words in I/O channel data units (i.e., 16 bits).



WSFT → FUN 1 6

D1: Start channel number

D2: End channel number

Coding

Address	OP		Data
0200	LD		0000
0201	WSFT(16)		—
0202		DM	010
0203		DM	012

Contents of data (D_1, D_2)

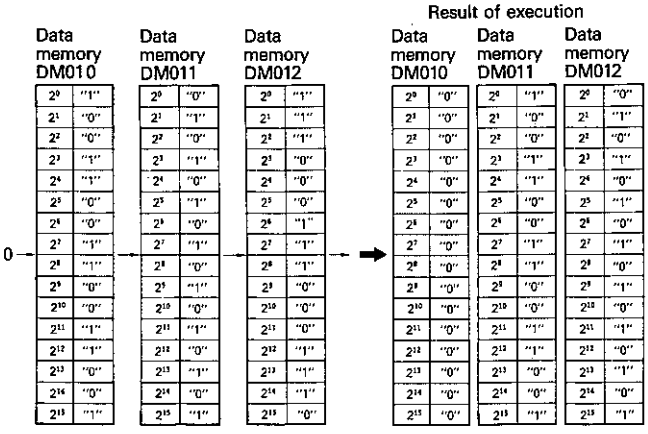
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTE: When the R register is logical 1, word shifting of 16-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the data between the start and the end channels are shifted in units of 16 bits.

In the above program, the 16-bit contents of DM010 to DM012 are shifted in units of 16 bits, and 0000 is input to the start channel.



DATA OF WSFT INSTRUCTION

The data for the WSFT instruction contain a start channel number and an end channel number by which the range of word shifting can be specified. The start channel must be less than or equal to the end channel, and both the channel numbers must be within the same data area. Note that a WSFT instruction cannot be programmed, and special auxiliary relay 6303 turns ON if this condition is not satisfied.

WORD SHIFTING OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

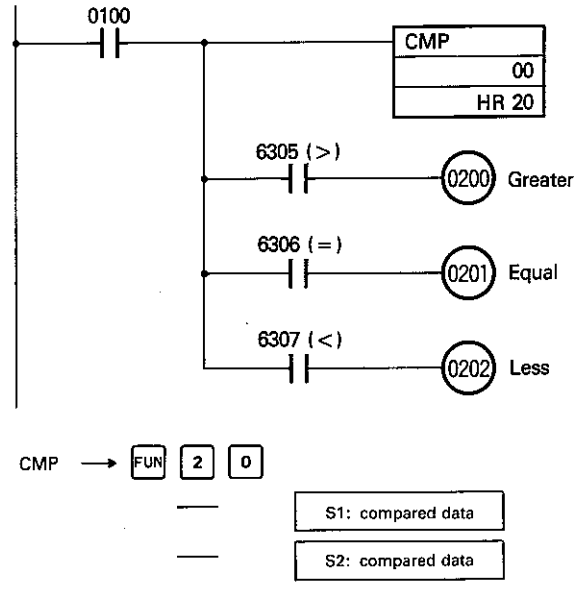
Use the data memory area for start and end channels when addressing relays indirectly.

If the contents of the indirectly addressed area are not in BCD, if the abovementioned condition is not satisfied, or if a data memory number greater than 512 is addressed, an error will occur, causing special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.17 COMPARE [CMP(FUN20)] INSTRUCTION

The CMP instruction is used to compare a 16-bit channel data or a hexadecimal 4-digit (16-bit binary) constant against another 16-bit channel data.

As a result of the comparison:
6305 turns ON if the S1 is greater than the S2;
6306 turns ON if the S1 is equal to the S2;
6307 turns ON if the S1 is less than the S2.



Coding

Address	OP		Data
0200	LD		0100
0201	OUT	TR	0
0202	CMP(20)		—
0202			00
0202		HR	20
0203	LD	TR	0
0204	AND		6305
0205	OUT		0200
0206	LD	TR	0
0207	AND		6306
0208	OUT		0201
0209	LD	TR	0
0210	AND		6307
0211	OUT		0202

Contents of data (S1, S2)

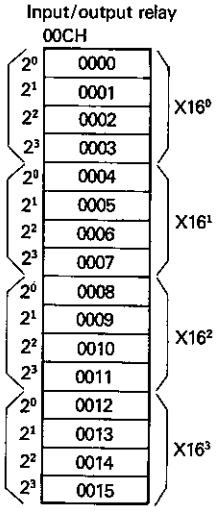
Input/output relay, internal auxiliary relay	00 to 63
Link relay	LR00 to 31
Holding relay	HR00 to 31
Timer, counter	TIM, CNT000 to 127
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511
Constant	#0000 to FFFF

NOTE: When the R register is logical 1, a CMP instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. Therefore, the compare result area of special auxiliary relays 6305 to 6307 holds the previous status, and on execution of an END instruction, all these relays are cleared to "0". When the content of the R register is logical 1, the CMP instruction is executed.

When the above program is executed, the 16-bit data of 00CH (0000 to 0015) are compared with the 16-bit data of HR20CH (HR2000 to 2015), and the results are output to the result area of special auxiliary relays 6305 to 6307.



Result of comparison

	6305	6306	6307
00CH>HR20CH	"1"	"0"	"0"
00CH = HR20CH	"0"	"1"	"0"
00CH<HR20CH	"0"	"0"	"1"

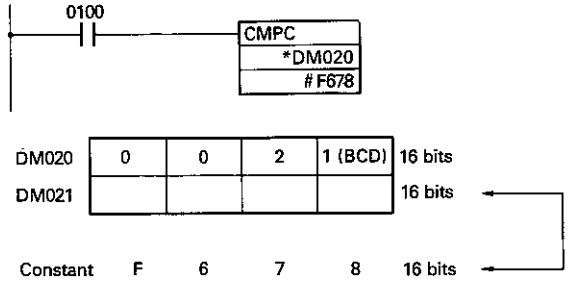
Constant is compared with the 4-digit hexadecimal (binary 16-bit) data.

COMPARISON OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to 511.

The contents of indirectly addressed data are BCD data 0000 to 0511, and they indicate the channel number of the data memory.

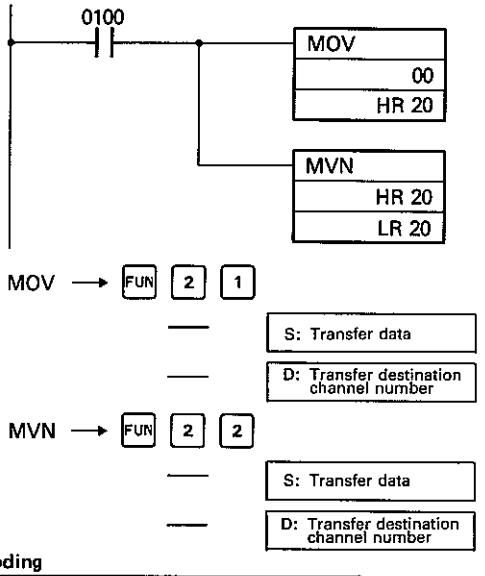
If the contents of the indirectly addressed data are not in BCD or if they are greater than 0511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.



The above program is executed when the NO contact of 0100 is ON. Because *DM020 is indirectly addressed, the data 21 (decimal) in DM020 specifies DM021, and the contents of DM021 are compared with the 4-digit constant F678 (16 bits).

4.18 MOVE [MOV(FUN21)]/MOVE NOT [MVN(FUN22)] INSTRUCTIONS

The MOV instruction is used to transfer 16-bit channel data or hexadecimal 4-digit (16-bit binary) constant to a specified channel.



Coding

Address	OP	Data	
0200	LD		0100
0201	MOV(21)		—
			00
		HR	20
0202	MVN(22)		—
		HR	20
		LR	20

Contents of data

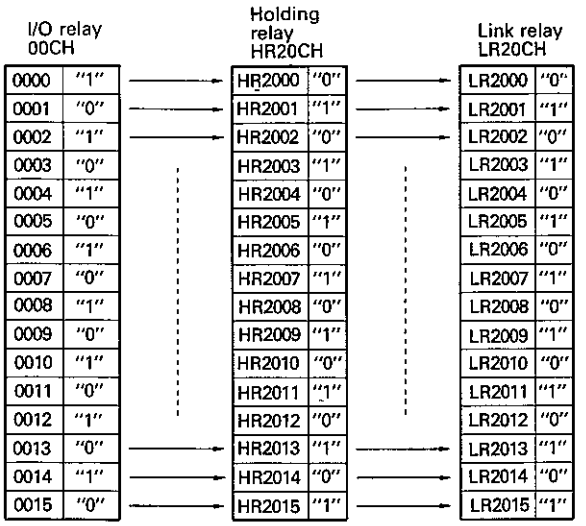
	S	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to FFFF	—

NOTES: 1. If the transferred data are all 0, special auxiliary relay 6306 (=) turns ON.
2. When the R register is logical 1, a MOV or MVN instruction is executed at each scanning. To execute it only once, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, transfer of data or of inverted data is performed.

When the above program is executed, the 16-bit data of 00CH (0000 to 0015) is transferred to HR20CH (HR2000 to HR2015), then inverted to be further transferred to LR20CH (LR2000 to LR2015).



The result of the transfer will be:

HR20CH = 0 → 6306 = 1

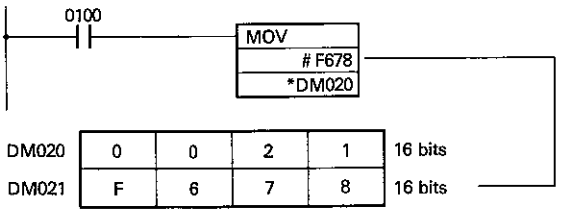
(LR20CH) ≠ 0 → 6306 = 0

In constant designation, hexadecimal 4-digit (binary 16-bit) data is either transferred or inverted and then transferred.

TRANSFER OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are not in BCD, or if they are greater than 511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

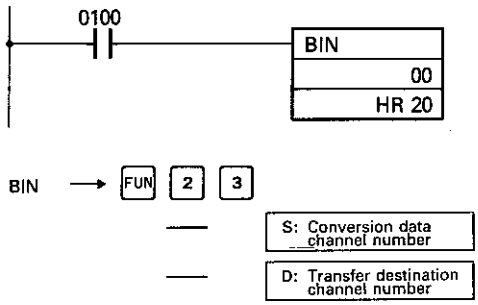


The above program is executed when the NO contact of 0100 is ON.

Because *DM020 is indirectly addressed, the data 21 (decimal) in DM020 specifies DM021, and a 4-digit constant (F678) is transferred to DM021. As a result, the contents of DM021 become F678. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.19 BCD-TO-BIN CONVERSION [BIN (FUN23)] INSTRUCTION

The BIN instruction is used to convert 4-digit decimal data into 16-bit binary data and to output the converted data to a specified channel.



Coding

Address	OP		Data
0200	LD		0100
0201	BIN(23)		—
			00
		HR	20

Contents of data

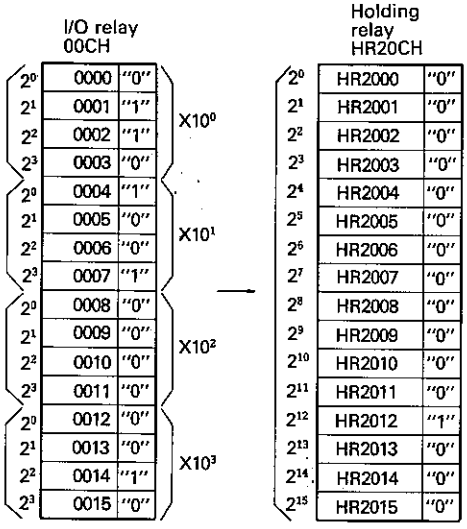
	S	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer/counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	

NOTES: 1. If the converted data are all 0, special auxiliary relay 6306 (=) turns ON.

2. When the R register is logical 1, a BIN instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the 4-digit decimal data in the specified channel is converted into 16-bit binary data. In the above program, the 16-bit contents of the 4-digit decimal data in 00CH (0000 to 0015) are converted into 16-bit binary data, then output to the 16-bit locations of HR20CH (HR2000 to HR2015).



The result of the conversion will be:

HR20CH = 0 → 6306 = 1
≠ 0 → 6306 = 0

The CPU will check whether the data to be converted is in four-digit BCD. If not, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

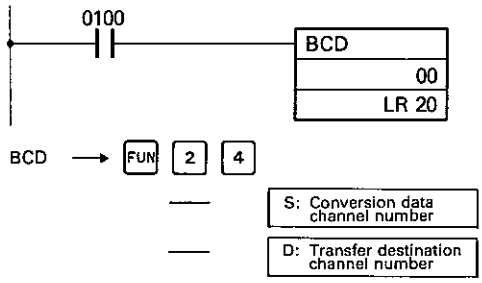
BCD-TO-BINARY CONVERSION OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are greater than DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.20 BIN-TO-BCD CONVERSION [BCD (FUN24)] INSTRUCTION

The BCD instruction is used to convert 16-bit binary data into 4-digit decimal data and to output the converted data to a specified channel.



Coding

Address	OP		Data
0200	LD		0100
0201	BCD(24)		—
			00
		LR	20

Contents of data

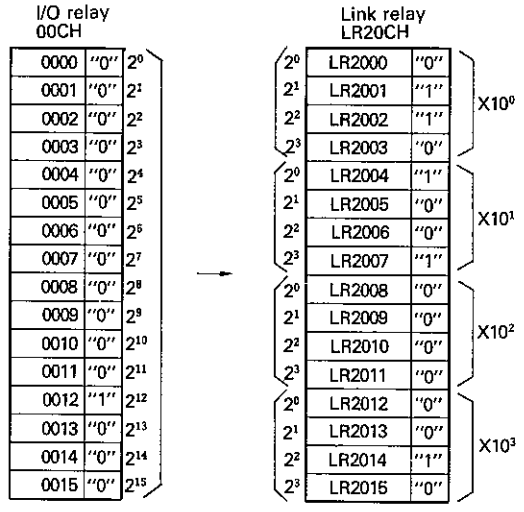
	S	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	

NOTES: 1. If the converted data are all 0, special auxiliary relay 6306 (=) turns ON.
2. When the R register is logical 1, a BCD instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the 16-bit binary data in the specified I/O channel is converted into a 4-digit decimal data.

In the above program, the 16-bit binary data in 00CH (0000 to 0015) is converted into a 4-digit decimal data and then output to the 16-bit locations of LR20CH (LR2000 to 2015).



The result of the conversion will be:

LR20CH = 0 → 6306 = 1
≠ 0 → 6306 = 0

If the converted decimal data exceeds 9999, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

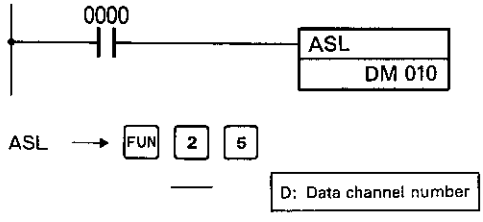
BINARY-TO-BCD CONVERSION OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relay DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.21 ARITHMETIC SHIFT LEFT [ASL (FUN25)] INSTRUCTION

The ASL instruction is used to shift to the left 16-bit data, including a carry.



Coding

Address	OP	Data	
0200	LD		0000
0201	ASL(25)		—
		DM	010

Contents of data (D)

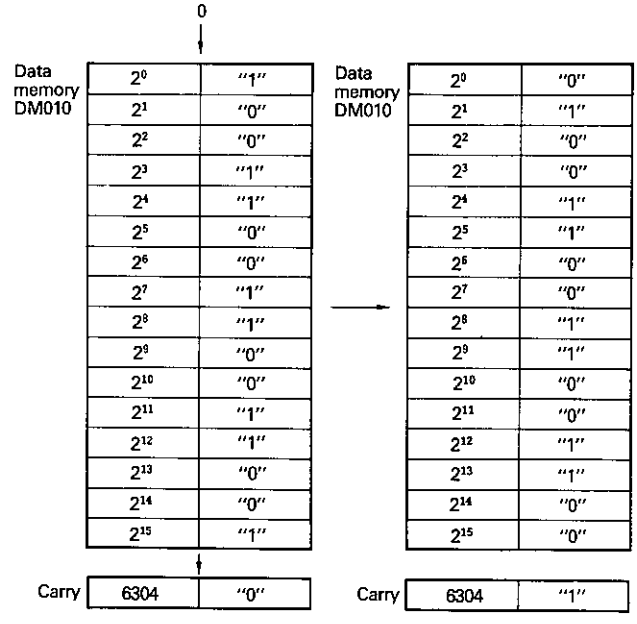
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTES: 1. Two addresses must be used to program an ASL instruction.
2. When the R register is logical 1, shifting left of 16-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 16-bit data, including a carry, is shifted to the left.

In the above program, all the 16-bit contents of DM010 including a carry (6304) are shifted one bit to the left. If the result of the operation is "0000", special auxiliary relay 6306 is turned on.



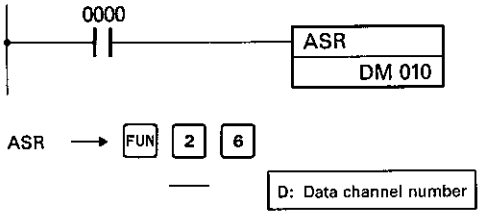
ARITHMETIC SHIFT LEFT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.22 ARITHMETIC SHIFT RIGHT [ASR(FUN26)] INSTRUCTION

The ASR instruction is used to shift to the right 16-bit data, including a carry.



Coding

Address	OP	Data	
0200	LD		0000
0201	ASR(26)		—
		DM	010

Contents of data (D)

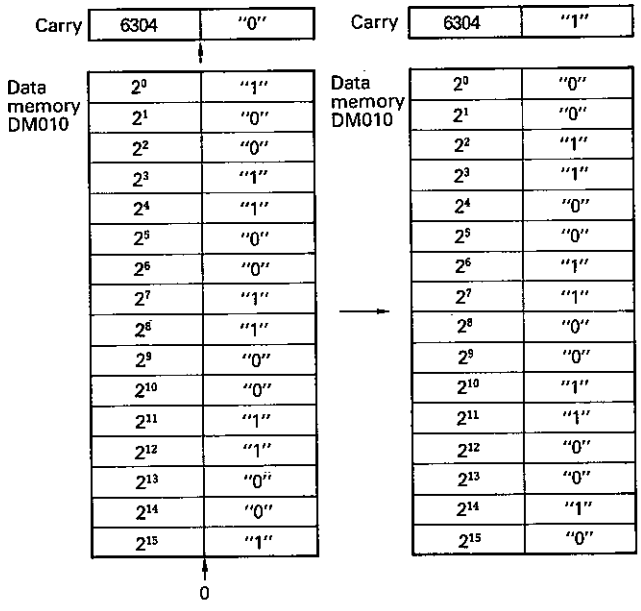
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTES: 1. Two addresses must be used to program an ASR instruction.
2. When the R register is logical 1, shifting right of 16-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 16-bit data, including a carry, is shifted to the right.

In the above program, all the 16-bit contents of DM010, including a carry (6304), are shifted one bit to the right. If the result of the operation is "0000," special auxiliary relay 6306 is turned ON.



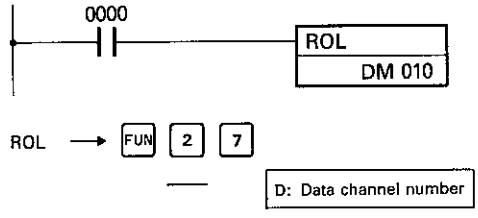
ARITHMETIC SHIFT RIGHT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.23 ROTATE LEFT [ROL(FUN27)] INSTRUCTION

The ROL instruction is used to rotate to the left 16-bit data, including a carry.



Coding

Address	OP	Data	
0200	LD		0000
0201	ROL(27)		—
		DM	0010

Contents of data (D)

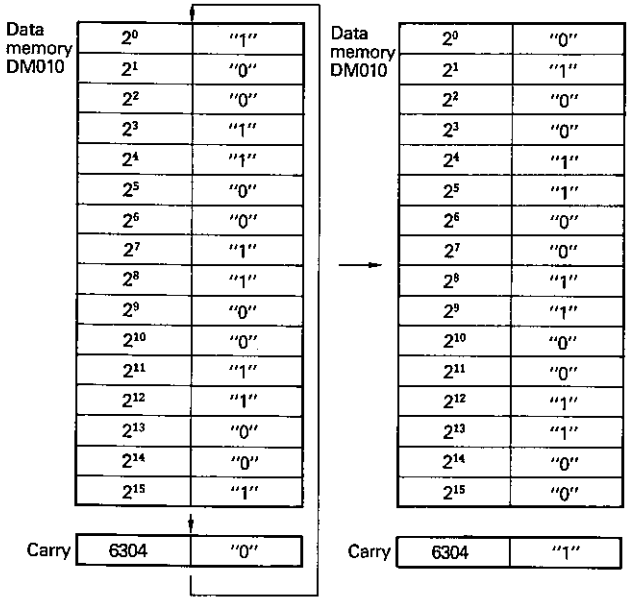
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTE: When the R register is logical 0, rotating left of 16-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 16-bit data, including a carry, is rotated to the left.

In the above program, all the 16-bit contents of DM010, including a carry (6304), are rotated one bit to the left. If the result of the operation is "0000", special auxiliary relay 6306 is turned ON.



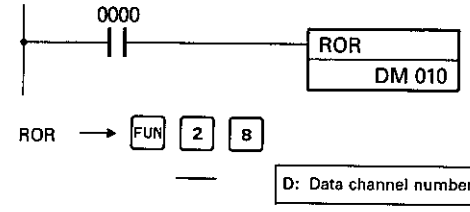
ROTATING LEFT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.24 ROTATE RIGHT [ROR(FUN28)] INSTRUCTION

The ROR instruction is used to rotate to the right 16-bit data, including a carry.



Coding

Address	OP	Data	
0200	LD		0000
0201	ROR(28)		—
		DM	010

Contents of data (D)

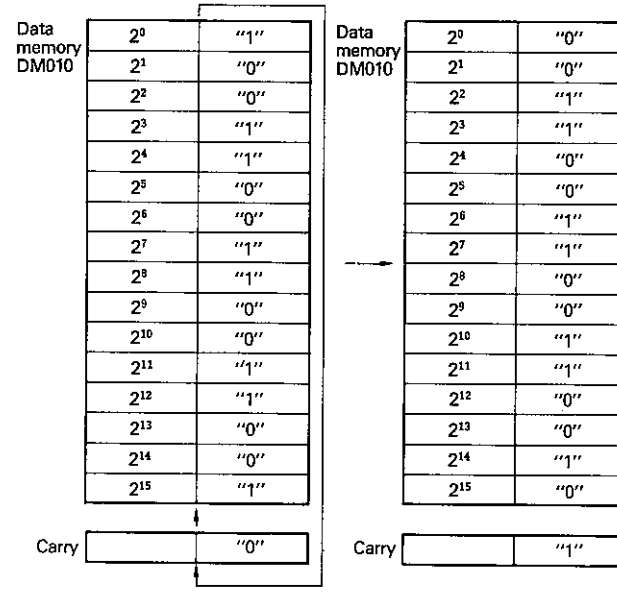
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTE: When the R register is logical 0, rotating right of 16-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content is logical 1, 16-bit data, including a carry, is rotated to the right.

In the above program, all the 16-bit contents of DM010, including a carry (6304), are rotated one bit to the right. If the result of the operation is "0000", special auxiliary relay 6306 is turned ON.



ROTATING RIGHT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

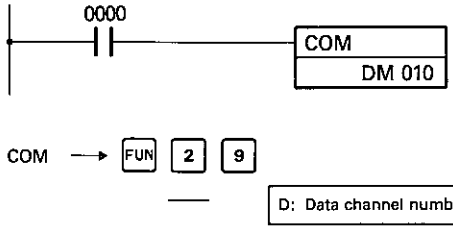
Data memory DM010		
	2^0	"1"
	2^1	"0"
	2^2	"0"
	2^3	"1"
	2^4	"1"
	2^5	"0"
	2^6	"0"
	2^7	"1"
	2^8	"1"
	2^9	"0"
	2^{10}	"0"
	2^{11}	"1"
	2^{12}	"1"
	2^{13}	"0"
	2^{14}	"0"
	2^{15}	"1"

→

Data memory DM010		
	2^0	"0"
	2^1	"1"
	2^2	"1"
	2^3	"0"
	2^4	"0"
	2^5	"1"
	2^6	"1"
	2^7	"0"
	2^8	"0"
	2^9	"1"
	2^{10}	"1"
	2^{11}	"0"
	2^{12}	"0"
	2^{13}	"1"
	2^{14}	"1"
	2^{15}	"0"

4.25 COMPLEMENT [COM(FUN29)] INSTRUCTION

The COM instruction is used to invert 16-bit data.



Coding

Address	OP	Data	
0200	LD		0000
0201	COM(29)		—
		DM	010

Contents of data (D)

Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTE: When the R register is logical 1, complementing 16-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the 16-bit data in the specified data memory is inverted.

In the above program, the 16-bit contents of DM010 are inverted, and the result of the COMPLEMENT operation is stored in the 16-bit locations of DM010. If the result of the operation is "0000", 6306 is turned ON.

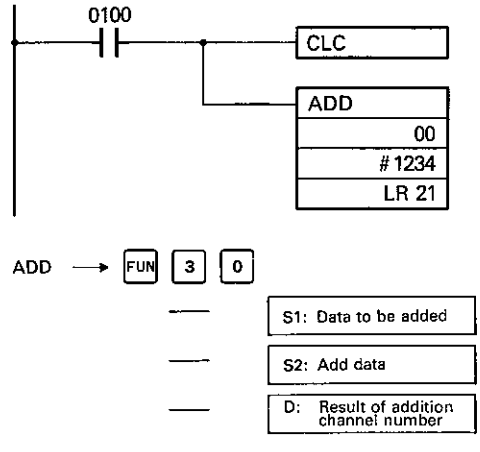
COMPLEMENTING OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.26 ADD [ADD(FUN30)] INSTRUCTION

The ADD instruction is used to execute the addition between two specified 4-digit BCD data.



Coding

Address	OP	Data	
0200	LD		0100
0201	CLC		—
0202	ADD(30)		—
			00
		#	1234
		LR	21

Contents of data

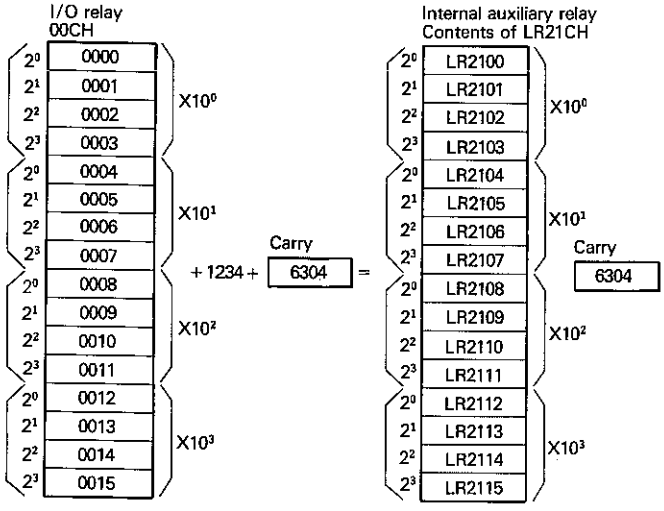
	S1 S2	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to 9999	—

NOTES: 1. Before an ADD instruction is executed, a CLC instruction must be programmed to clear the carry flag (6304).
2. When the R register is logical 1, a BCD addition is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, addition of a 4-digit BCD data to a 4-digit BCD data including a carry (6304) is executed. If the result of the addition is "0000", 6306 is turned ON, and if there is a carry in the result, 6304 is turned ON.

In the above program, the 16-bit contents of 00CH (0000 to 0015) are added in units of four BCD digits to the 16-bit contents of the 4-digit constant "1234", including a carry (6304), and the result of the addition is output to the 16-bit locations of LR21 CH (LR2100 to LR2115). If there is a carry in the result, 6304 is turned ON, and if the result of the addition is "0000", 6306 is turned ON.



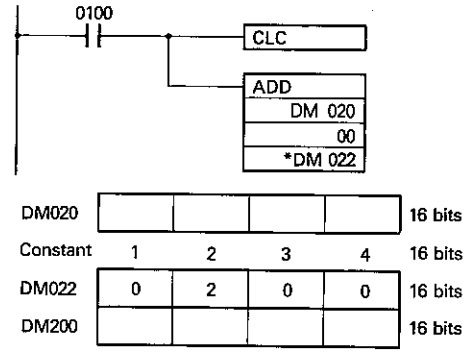
NOTE: Before executing an ADD instruction, the carry register (6304) must always be cleared using a CLEAR CARRY (CLC) instruction. (Execution of CLC is omitted in multistage addition.)

The CPU checks whether the data for BCD addition are in four BCD digits. If not, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

ADDITION OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

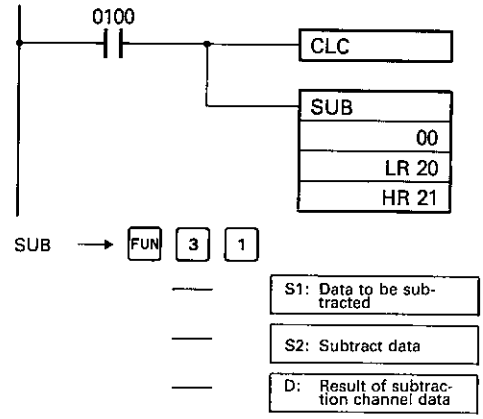
If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.



The program shown above is executed when the NO contact of 0100 turns ON. Because *DM022 is indirectly addressed, the data 200 (decimal) in DM022 specifies DM200, and the result of addition of the contents of DM020 to the 4-digit constant 1234 is output to DM200.

4.27 SUBTRACT [SUB(FUN31)] INSTRUCTION

The SUB instruction is used to execute BCD subtraction between two specified 4-digit data.



Coding

Address	OP	Data	
0200	LD		0100
0201	CLC		—
0202	SUB(31)		—
			00
		LR	20
		HR	21

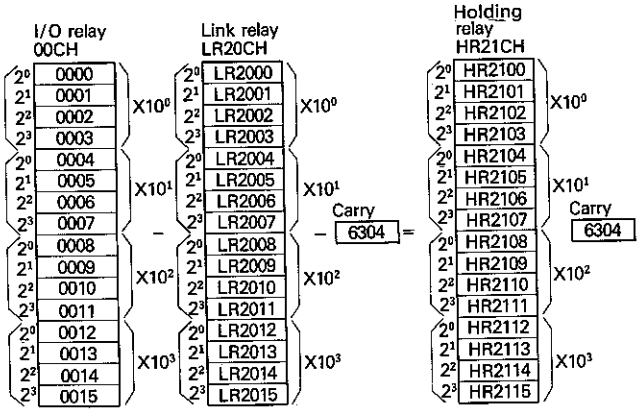
Contents of data

	S1, S2	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to 9999	—

NOTES: 1. Before executing a SUB instruction, a CLC instruction must be programmed to clear the carry flag (6304).
2. When the R register is logical 1, a BCD subtraction is executed at each scanning. To execute it only once, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content is logical 1, 4-digit BCD subtraction, including a carry (6304), is executed. If the result of the subtraction is "0000", 6306 is turned ON, and if there is a carry in the result, 6304 is turned ON. In the above program, the 16-bit contents of LR20CH (LR2000 to LR2015), including a carry (6304), are subtracted in units of four BCD digits from the 16-bit contents of 00CH (0000 to 0015), and the result of the subtraction is output to the 16-bit locations of LR20CH (LR2000 to 2015). If there is a carry in the result, 6304 is turned ON, and if the result of the subtraction is "0000", 6306 is turned ON.



NOTE: Before executing a SUB instruction, the carry register (6304) must always be cleared using a CLEAR CARRY (CLC) instruction. (Execution of CLC is omitted in multistage subtraction.)

The CPU checks whether the data for BCD subtraction are in four BCD digits. If not, an error will occur, causing special auxiliary relay 6303 to turn ON, and the program will not be executed.

SUBTRACTION OF INDIRECTLY ADDRESSED DATA

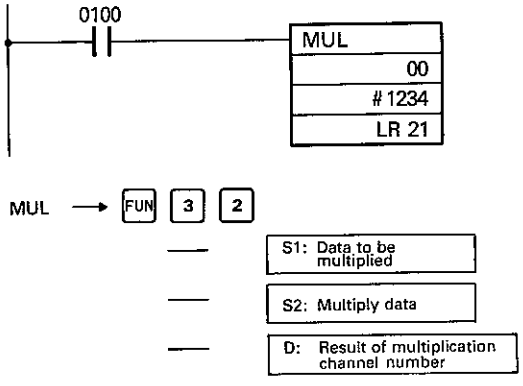
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.
If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

If the carry register 6304 is ON as the result of the subtraction, the result is output as tens complements.
To obtain a true complement, subtract the tens complement from "0000".

0000 — tens complement = true complement

4.28 MULTIPLY [MUL(FUN32)] INSTRUCTION

The MUL instruction is used to execute BCD multiplication between two specified 4-digit BCD data.



Coding

Address	OP		Data
0200	LD		0100
0201	MUL(32)		—
			00
		#	1234
		LR	21

Contents of data

	S1, S2	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 59
Link relay	LR00 to 31	LR00 to 30
Holding relay	HR00 to 31	HR00 to 30
Timer, counter	TIM, CNT000 to 127	–
Data memory relay	DM000 to 511	DM000 to 510
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to 9999	–

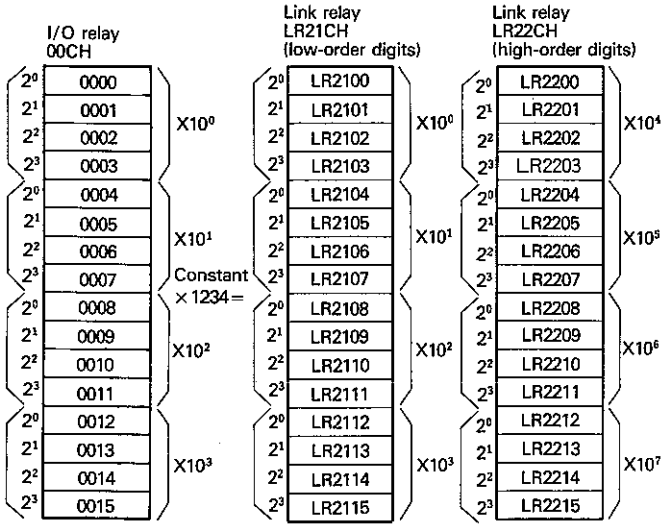
NOTES: 1. Two channels (16 bits x 2) must be used for the operation result area.
2. When the R register is logical 1, a BCD multiplication is executed at each scanning. To execute it only once, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, multiplication of 4-digit BCD data by 4-digit BCD data is executed. Two channels are required for the operation result area.

In the above program, the 16-bit contents of 00CH (0000 to 0015) are multiplied by the 16-bit contents of the 4-digit constant "1234" in units of four BCD digits; the result is output to the two 16-bit locations of LR21CH and LR22CH (LR2100 to LR2215).

If the result of the multiplication is "00000000", special auxiliary relay 6306 is turned ON.



The CPU checks whether the data for BCD multiplication is in four BCD digits. If not, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

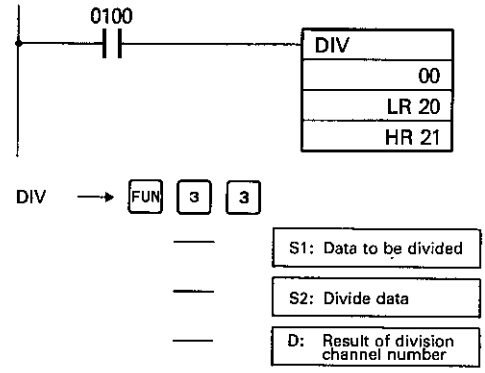
MULTIPLICATION OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.29 DIVIDE [DIV(FUN33)] INSTRUCTION

The DIV instruction is used to execute BCD division between two specified 4-digit BCD data.



Coding

Address	OP	Data	
0200	LD		0100
0201	DIV(33)		–
			00
		LR	20
		HR	21

Contents of data

	S1, S2	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 59
Link relay	LR00 to 31	LR00 to 30
Holding relay	HR00 to 31	HR00 to 30
Timer, counter	TIM, CNT000 to 127	–
Data memory relay	DM000 to 511	DM000 to 510
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to 9999	–

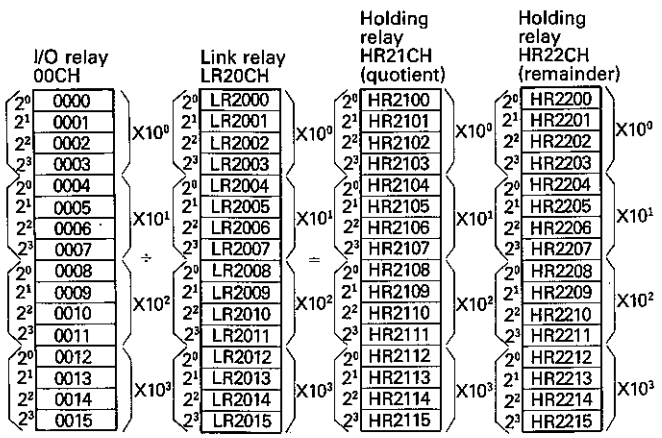
NOTES: 1. Two channels (16 bits x 2) are used for the operation result area.
2. When the R register is logical 1, a BCD division is executed at each scanning. To execute it only once, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 4-digit BCD division is executed. Two channels are required for the operation result area.

In the above program, the 16-bit contents of 00CH (0000 to 0015) are divided by the 16-bits of LR20CH (LR2000 to LR2015) in units of four BCD digits, and the result of the division is output to the two 16-bit locations of HR21CH and HR22CH (HR2100 to HR2215).

If the result of the division is "0000", special auxiliary relay 6306 is turned ON.



The CPU checks whether the data for BCD division are in four BCD digits. If not, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

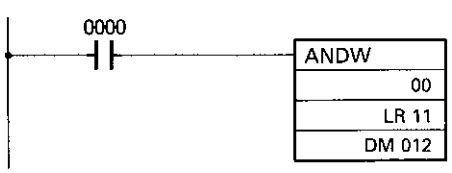
DIVISION OF INDIRECTLY ADDRESSED DATA

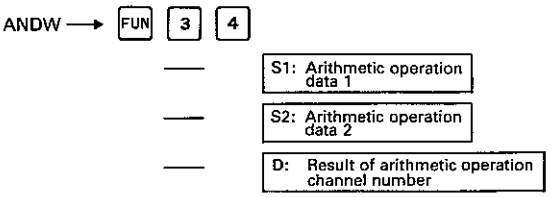
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

4.30 AND WORD [ANDW(FUN34)] INSTRUCTION

The ANDW instruction is used to perform a logical AND operation between two specified data (16 bits each).





Coding

Address	OP	Data	
0200	LD		0000
0201	ANDW(34)		—
			010
		LR	11
		DM	012

Contents of data

	S1, S2	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 59
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to FFFF	—

NOTE: When the R register is logical 1, an ANDW instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, a logical AND operation is executed between two 16-bit data.

In the above program, the 16-bit contents of 00CH are ANDed with the 16-bit contents of LR11, and the result of the AND operation is stored in the 16-bit locations of DM012. If the result of the operation is "0000", special auxiliary relay 6306 is turned ON.

I/O relay 00CH			Link relay LR11CH		Data memory DM012	
0000	2^0	"1"	2^0	"1"	2^0	"1"
0001	2^1	"0"	2^1	"0"	2^1	"0"
0002	2^2	"0"	2^2	"1"	2^2	"0"
0003	2^3	"1"	2^3	"0"	2^3	"0"
0004	2^4	"1"	2^4	"1"	2^4	"1"
0005	2^5	"0"	2^5	"0"	2^5	"0"
0006	2^6	"0"	2^6	"1"	2^6	"0"
0007	2^7	"1"	2^7	"0"	2^7	"0"
0008	2^8	"1"	2^8	"1"	2^8	"1"
0009	2^9	"0"	2^9	"0"	2^9	"0"
0010	2^{10}	"0"	2^{10}	"1"	2^{10}	"0"
0011	2^{11}	"1"	2^{11}	"0"	2^{11}	"0"
0012	2^{12}	"1"	2^{12}	"1"	2^{12}	"1"
0013	2^{13}	"0"	2^{13}	"0"	2^{13}	"0"
0014	2^{14}	"0"	2^{14}	"1"	2^{14}	"0"
0015	2^{15}	"1"	2^{15}	"0"	2^{15}	"0"

LOGICAL AND OPERATION OF INDIRECTLY ADDRESSED DATA

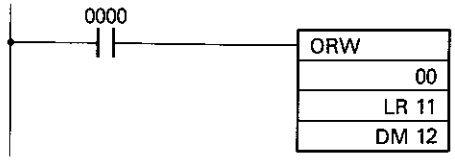
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

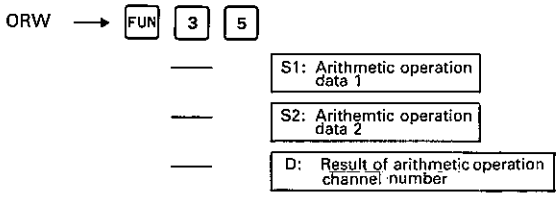
If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

The constant can be specified as a 4-digit hexadecimal (binary 16-bit) data.

4.31 OR WORD [ORW(FUN35)] INSTRUCTION

The ORW instruction is used to perform a logical OR operation between two specified data (16 bits each).





Coding

Address	OP	Data	
0200	LD		0000
0201	ORW(35)		—
			010
		LR	11
		DM	012

Contents of data

	S	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to FFFF	—

NOTE: When the R register is logical 1, an ORW instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, a logical OR operation is executed between two 16-bit data.

In the above program, the 16-bit contents of 00CH are ORed with the 16-bit contents of LR11, and the result of the OR operation is stored in the 16-bit locations of DM012. If the result of the operation is "0000", special auxiliary relay 6306 is turned ON.

I/O relay 00CH			Link relay LR11CH		Data memory DM012	
0000	2^0	"1"	2^0	"1"	2^0	"1"
0001	2^1	"0"	2^1	"0"	2^1	"0"
0002	2^2	"0"	2^2	"1"	2^2	"1"
0003	2^3	"1"	2^3	"0"	2^3	"1"
0004	2^4	"1"	2^4	"1"	2^4	"1"
0005	2^5	"0"	2^5	"0"	2^5	"0"
0006	2^6	"0"	2^6	"1"	2^6	"1"
0007	2^7	"1"	2^7	"0"	2^7	"1"
0008	2^8	"1"	2^8	"1"	2^8	"1"
0009	2^9	"0"	2^9	"0"	2^9	"0"
0010	2^{10}	"0"	2^{10}	"1"	2^{10}	"1"
0011	2^{11}	"1"	2^{11}	"0"	2^{11}	"1"
0012	2^{12}	"1"	2^{12}	"1"	2^{12}	"1"
0013	2^{13}	"0"	2^{13}	"0"	2^{13}	"0"
0014	2^{14}	"0"	2^{14}	"1"	2^{14}	"1"
0015	2^{15}	"1"	2^{15}	"0"	2^{15}	"1"

LOGICAL OR OPERATION OF INDIRECTLY ADDRESSED DATA

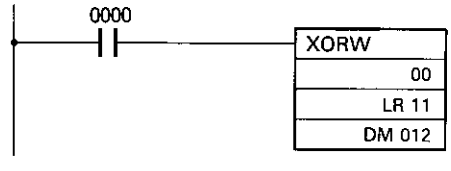
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

The constant can be specified as a 4-digit hexadecimal (binary 16-bit) data.

4.32 EXCLUSIVE OR WORD [XORW (FUN36)] INSTRUCTION

The XORW instruction is used to perform an exclusive logical OR operation between two specified data (16 bits each).



XORW → FUN 3 6

— S1: Arithmetic operation data 1

— S2: Arithmetic operation data 2

— D: Result of arithmetic operation channel number

Coding

Address	OP	Data	
0200	LD		0000
0201	XORW(36)		—
			010
		LR	11
		DM	012

Contents of data

	S	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to FFFF	—

NOTE: When the R register is logical 1, an exclusive logical OR operation is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, an exclusive logical OR operation is executed between two 16-bit data.

In the above program, the 16-bit contents of 00CH are exclusively ORed with the 16-bit contents of LR11, and the result of the OR operation is stored in the 16-bit locations of DM012.

If the result of the operation is "0000", special auxiliary relay 6306 is turned ON.

I/O relay 00CH			Link relay LR11CH		Data memory DM012	
0000	2^0	"1"	2^0	"1"	2^0	"0"
0001	2^1	"0"	2^1	"0"	2^1	"0"
0002	2^2	"0"	2^2	"1"	2^2	"1"
0003	2^3	"1"	2^3	"0"	2^3	"1"
0004	2^4	"1"	2^4	"1"	2^4	"0"
0005	2^5	"0"	2^5	"0"	2^5	"0"
0006	2^6	"0"	2^6	"1"	2^6	"1"
0007	2^7	"1"	2^7	"0"	2^7	"1"
0008	2^8	"1"	2^8	"1"	2^8	"0"
0009	2^9	"0"	2^9	"0"	2^9	"0"
0010	2^{10}	"0"	2^{10}	"1"	2^{10}	"1"
0011	2^{11}	"1"	2^{11}	"0"	2^{11}	"1"
0012	2^{12}	"1"	2^{12}	"1"	2^{12}	"0"
0013	2^{13}	"0"	2^{13}	"0"	2^{13}	"0"
0014	2^{14}	"0"	2^{14}	"1"	2^{14}	"1"
0015	2^{15}	"1"	2^{15}	"0"	2^{15}	"1"

EXCLUSIVE LOGICAL OR OPERATION OF INDIRECTLY ADDRESSED DATA

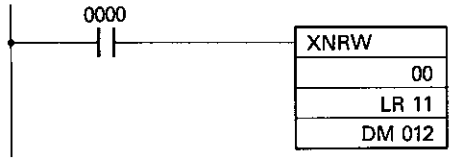
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than 000 to 511, an error will occur, causing special auxiliary relay 6303 to turn ON and the program to be not executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

The constant can be specified as a hexadecimal 4-digit (binary 16-bit) data.

4.33 EXCLUSIVE OR NOT WORD [XNRW(FUN37)] INSTRUCTION

The XNRW instruction is to perform an exclusive logical OR NOT operation between two specified data (16 bits each).



XNRW → FUN 3 7

— S1: Arithmetic operation data 1

— S2: Arithemtic operation data 2

— D: Result of arithmetic operation channel number

Coding

Address	OP	Data	
0200	LD		0000
0201	XNRW(37)		—
			010
		LR	11
		DM	012

Contents of data

	S	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to FFFF	—

NOTE: When the R register is logical 1, an exclusive logical OR NOT operation is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, an exclusive logical OR NOT operation is executed between two 16-bit data.

In the above program, the 16-bit contents of 00CH are exclusively ORed with the 16-bit contents of LR11, and the result of the OR operation is inverted and then stored in the 16-bit locations of DM012. If the result of the operation is "000", special auxiliary relay 6306 is turned ON.

I/O relay 00CH			Link relay LR11CH		Data memory DM012	
0000	2^0	"1"	2^0	"1"	2^0	"1"
0001	2^1	"0"	2^1	"0"	2^1	"1"
0002	2^2	"0"	2^2	"1"	2^2	"0"
0003	2^3	"1"	2^3	"0"	2^3	"0"
0004	2^4	"1"	2^4	"1"	2^4	"1"
0005	2^5	"0"	2^5	"0"	2^5	"1"
0006	2^6	"0"	2^6	"1"	2^6	"0"
0007	2^7	"1"	2^7	"0"	2^7	"0"
0008	2^8	"1"	2^8	"1"	2^8	"1"
0009	2^9	"0"	2^9	"0"	2^9	"1"
0010	2^{10}	"0"	2^{10}	"1"	2^{10}	"0"
0011	2^{11}	"1"	2^{11}	"0"	2^{11}	"0"
0012	2^{12}	"1"	2^{12}	"1"	2^{12}	"1"
0013	2^{13}	"0"	2^{13}	"0"	2^{13}	"1"
0014	2^{14}	"0"	2^{14}	"1"	2^{14}	"0"
0015	2^{15}	"1"	2^{15}	"0"	2^{15}	"0"

EXCLUSIVE LOGICAL OR NOT OPERATION OF INDIRECTLY ADDRESSED DATA

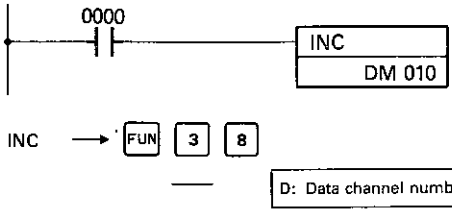
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than 000 to 511, an error will occur; this will cause special auxiliary relay 6306 to turn ON, and the program will not be executed. For details, refer to Comparison of indirectly addressed data in 4.17 Compare instruction.

The constant can be specified as a hexadecimal 4-digit (binary 16-bit) data.

4.34 INCREMENT [INC(FUN38)] INSTRUCTION

The INC instruction is used to increment a 4-digit BCD data by 1.



Coding

Address	OP	Data	
0200	LD		0000
0201	INC(38)		—
0202		DM	010

Contents of data (D)

Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTE: When the R register is logical 1, the increment of a 4-digit BCD data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the 4-digit BCD data in the specified data is incremented by 1.

In the above program, the 16-bit contents of DM010 are incremented by 1, and the result of the increment operation is stored in DM010. If the result of the operation is "0000", special auxiliary relay 6306 is turned ON.

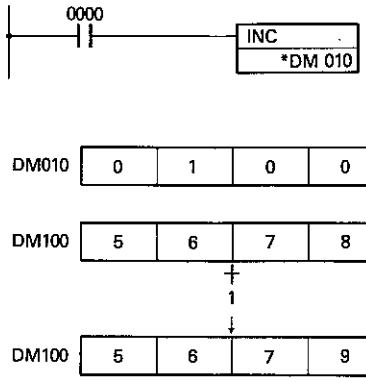
Data memory DM010 (1234)					Data memory DM010 (1235)			
$X10^0$	2^0	"0"			$X10^0$	2^0	"1"	
	2^1	"0"				2^1	"0"	
	2^2	"1"				2^2	"1"	
	2^3	"0"				2^3	"0"	
$X10^1$	2^0	"1"			$X10^1$	2^0	"1"	
	2^1	"1"				2^1	"1"	
	2^2	"0"				2^2	"0"	
	2^3	"0"				2^3	"0"	
$X10^2$	2^0	"0"	+1	→	$X10^2$	2^0	"0"	
	2^1	"1"				2^1	"1"	
	2^2	"0"				2^2	"0"	
	2^3	"0"				2^3	"0"	
$X10^3$	2^0	"1"			$X10^3$	2^0	"1"	
	2^1	"0"				2^1	"0"	
	2^2	"0"				2^2	"0"	
	2^3	"0"				2^3	"0"	

The CPU checks whether the data to be incremented is in four BCD digits. If not, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

INCREMENT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

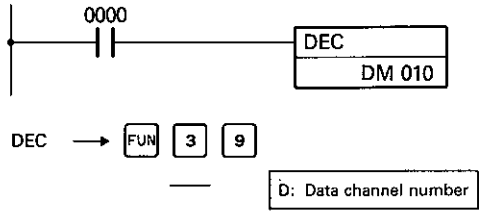
If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.



The above program is executed when the NO contact of 0000 turns ON. Because *DM010 is indirectly addressed, the data 100 in DM010 specifies DM100, and the 16-bit contents of DM100 (5678) are incremented by 1. The result of the increment operation (5679) is stored in the 16-bit locations of DM100.

4.35 DECREMENT [DEC(FUN39)] INSTRUCTION

The DEC instruction is used to decrement a 4-digit BCD data by 1.



Coding

Address	OP	Data	
0200	LD		0000
0201	DEC(39)		—
		DM	010

Contents of data (D)

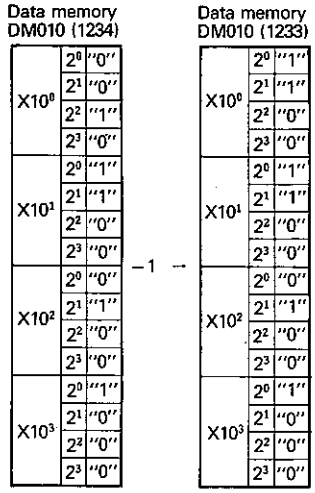
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTE: When the R register is logical 1, the increment of a 4-digit BCD data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

No operation is performed when the content of the R register is logical 0. When the content of the R register is logical 1, the 4-digit BCD data in the specified data is decremented by 1.

In the above program, the 16-bit contents of DM010 are decremented by 1, and the result of the decrement operation is stored in DM010. If the result of the operation is "0000", special auxiliary relay 6306 is turned on.

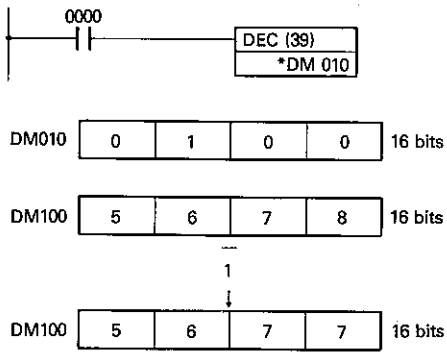


The CPU checks whether the data to be decremented are in four BCD digits. If not, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

DECREMENT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

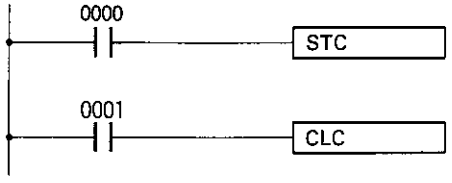
If the contents of the indirectly addressed area are other than BCD data or greater than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.



The above program is executed when the NO contact of 0000 turns ON. Because *DM010 is indirectly addressed, the data 100 in DM010 specifies DM100, and the 16-bit contents of DM100 (5678) are decremented by 1. The result of the decrement operation (5677) is stored in the 16-bit locations of DM100.

4.36 SET CARRY [STC(FUN40)] /CLEAR CARRY [CLC(FUN41)] INSTRUCTIONS

The STC instruction is used to set the carry register (6304) to "1", and the CLC instruction is used to reset the carry register (6304) to "0".



STC → FUN 4 0

CLC → FUN 4 1

Coding

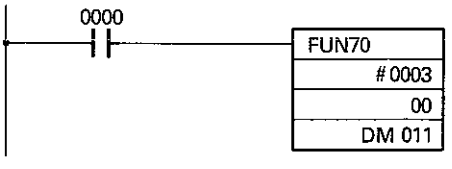
Address	OP	Data	
0200	LD		0000
0201	STC(40)		—
0202	LD		0001
0203	CLC(41)		—

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the STC instruction causes the carry register (6304) to be set to "1", and the CLC instruction causes the carry register (6304) to be reset to "0".

4.37 BLOCK MOVE (FUN70) INSTRUCTION

The BLOCK MOVE instruction is used to transfer channel data consecutively at one time.



FUN 7 0

— W: Number of channels (words)

— S: Start channel number of data to be transferred

— D: Start channel number of destination

Coding

Address	OP	Data	
0200	LD		0000
0201	FUN70		—
		#	0003
			00
		DM	011

Contents of data

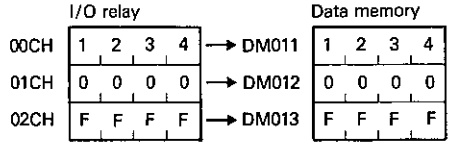
	W	S	D
Input/output relay, internal auxiliary relay	—	00 to 63	00 to 60
Link relay	—	LR00 to 31	
Holding relay	—	HR00 to 31	
Timer, counter		TIM, CNT000 to 127	
Data memory relay	—	DM000 to 511	
Indirectly addressed data	—	*DM000 to 511	
Constant	#0000 to 0511	—	

NOTE: When the R register is logical 1, a channel data transfer operation is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, channel data are consecutively transferred at one time.

In the above program, data of 3 channels (48 bits), 00CH to 02CH (0000 to 0215), are consecutively transferred to DM011 to 013 by channel unit.



The transfer operation is consecutively executed from the start channel to a specified channel.

NOTE: Be sure not to specify the same block in duplication, though both start channels and end can be specified within the same area.

BLOCK TRANSFER OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than 000 to 511, an error will occur, causing special auxiliary relay 6303 to turn ON and the program not to be executed.

DATA OF BLOCK MOVE INSTRUCTION

The data of a block transfer instruction that must be specified are the start channels of the source and destination of the transfer operation and the number of channels to be transferred. Any number of channels within the

limitation of the hardware can be specified for transference, and the data must satisfy these conditions.

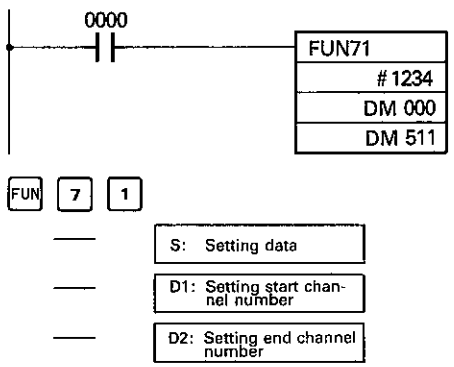
- Only BCD data are acceptable when specifying the number of channels.
- Block area must be within the same data area.
  (Start channel number + number of channels − 1 ≦ Start channel area maximum channel number)

If these data conditions are not satisfied, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.38 BLOCK SET (FUN71) INSTRUCTION

This instruction is used to transfer the same data to all consecutive channels.



Coding

Address	OP	Data	
0200	LD		0000
0201	FUN71		←
		#	1234
		DM	000
		DM	511

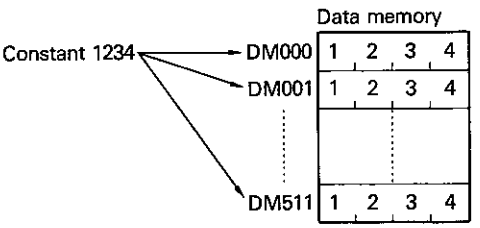
Contents of data

	S	D1, D2
Input/output relay, internal auxiliary relay	00 to 63	00 to 60
Link relay	LR00 to 31	
Holding relay	HR00 to 31	
Timer, counter	TIM, CNT000 to 127	
Data memory relay	DM000 to 511	
Indirectly addressed data	*DM000 to 511	
Constant	#0000 to FFFF	–

NOTE: When the R register is logical 1, a data transfer operation is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the same data is transferred to all consecutive channels.
In the above program, constant "1234" (16-bit data) is transferred to DM000 to 511.



BLOCK SET OF INDIRECTLY ADDRESSED DATA

The only data that can be indirectly addressed are data memory relays DM000 to DM511.
If the contents of the indirectly addressed area are other than 000 to 511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

DATA OF BLOCK SET INSTRUCTION

The data of a block setting instruction that must be specified are the start and end channels of the setting operation and the number of channels to be set. Any number of channels within the limitation of the hardware can be specified for setting, and the data must satisfy these conditions.

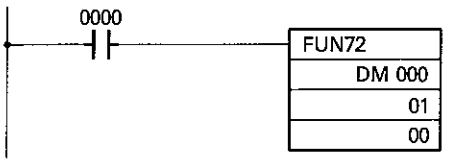
Start channel number ≦ End channel number and same data area

If these data conditions are not satisfied, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed. Any set data can be selected, and a hexadecimal 4-digit (binary 16-bit) data can be specified for the constant.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.39 SQUARE ROOT (FUN72) INSTRUCTION

The SQUARE ROOT instruction is used to compute the square root of an 8-digit BCD data.



FUN 7 2

—— S: Arithmetic operation data

—— D: Result of arithmetic operation channel number

—— —

Coding

Address	OP	Data	
0200	LD		0000
0201	FUN72		—
		DM	000
			01
			00

Contents of data

	S	D
Input/output relay, internal auxiliary relay	00 to 62	00 to 60
Link relay	LR00 to 30	LR00 to 31
Holding relay	HR00 to 30	HR00 to 31
Timer, counter	TIM, CNT000 to 126	—
Data memory relay	DM000 to 510	DM000 to 511
Indirectly addressed data	*DM000 to 511	

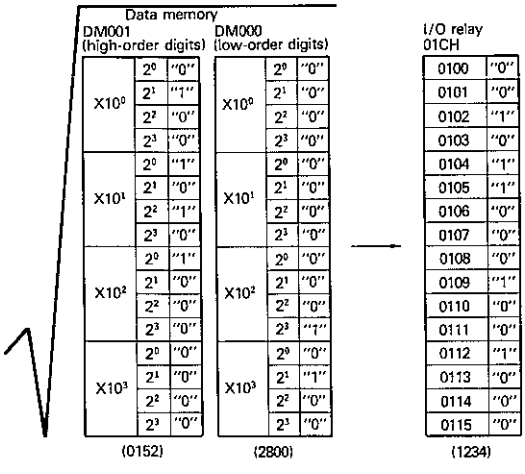
NOTES: 1. Two channels (16 bits x 2) are required for the operation data area.
2. The third data — is ignored when the instruction is executed.
3. When the R register is logical 1, computing the square root of an 8-digit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the square root of a BCD 8-digit integer is computed.

In the above program, the square root of BCD data (16 bits x 2) in the DM000 and DM001 is computed, and the result (BCD 4-digit integer) is output to the 01CH (16 bits).

If the result is 0000, special auxiliary relay 6306 turns ON.



Only a 4-digit integer is output as a result data, and a fraction is rounded off at the decimal point.

SQUARE ROOT OF INDIRECTLY ADDRESSED DATA

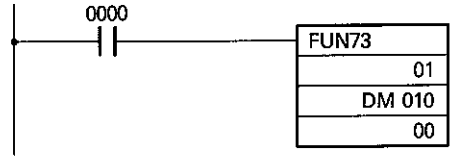
The only data that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.40 DATA EXCHANGE (FUN73) INSTRUCTION

The DATA EXCHANGE instruction is used to exchange one channel of (16 bits) data with another.



FUN 7 3

—— D1: Exchange channel number 1

—— D2: Exchange channel number 2

—— —

Coding

Address	OP	Data	
0200	LD		0000
0201	FUN73		—
			01
		DM	010
			00

Contents of data (D1, D2)

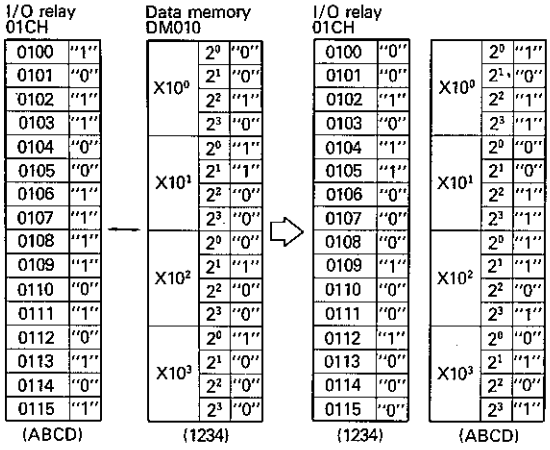
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Timer, counter	TIM, CNT000 to 127
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTES: 1. The third data [—] is ignored when the instruction is executed.
2. When the R register is logical 1, a data exchange operation is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 16-bit data of one channel is exchanged with another.

In the above program, the contents of 01CH (0100 to 0115) are exchanged with the 16-bit contents of DM010.



DATA EXCHANGE OPERATION OF INDIRECTLY ADDRESSED DATA

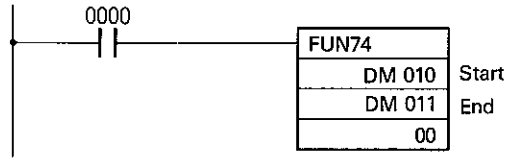
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

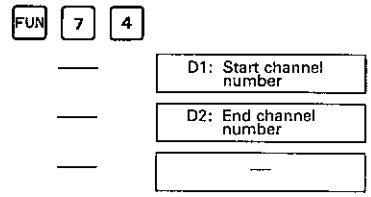
If the contents of the indirectly addressed area are other than BCD data or more than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.41 ONE DIGIT SHIFT LEFT (FUN74) INSTRUCTION

The ONE DIGIT SHIFT LEFT instruction is used to shift data between the start and end channels by four bits to the left.





Coding

Address	OP	Data	
0200	LD		0000
0201	FUN74		—
		DM	010
		DM	011
			00

Contents of data (D1, D2)

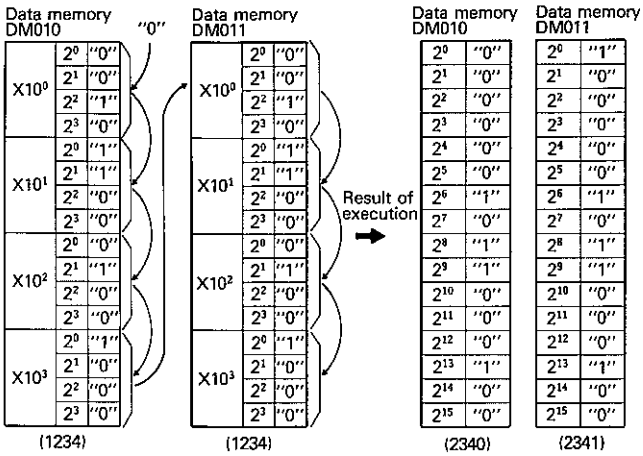
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTES: 1. The third data [—] is ignored when the instruction is executed.
2. When the R register is logical 1, data between the start and end channels are shifted to the left by four bits at each scanning. To execute the ONE DIGIT SHIFT LEFT instruction only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, data between the start and end channels are shifted by 4 bits to the left.

In the above program, the contents of DM010 to DM011 are shifted by 4 bits (1 bit x 4 times) to the left. In this case "0" is inserted as the first digit of the start channel.



The data shifting operation is performed starting from the least significant digit of the start channel to the most significant digit of the end channel.

DATA OF ONE DIGIT SHIFT LEFT

The data area for the ONE DIGIT SHIFT LEFT instruction is specified by a start channel number and an end channel number, both of which can be determined freely provided these conditions are satisfied.

Start channel number ≦ End channel number and same data area

If these data conditions are not satisfied, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

ONE DIGIT SHIFT LEFT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511. Use data memory area for the start and end channels.

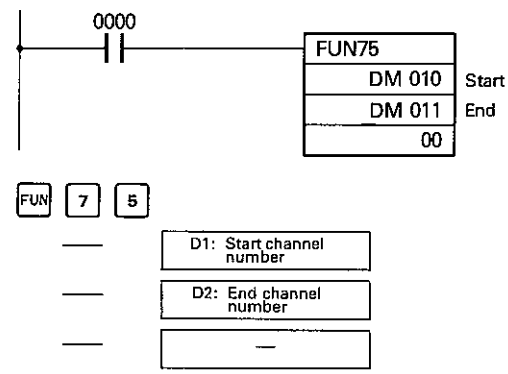
If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

NOTE: If the range of the data shift exceeds 50 channels (200 digits), a power failure may cause the execution of the shift operation to stop midway. Be sure to use no more than 50 channels.

4.42 ONE DIGIT SHIFT RIGHT (FUN75) INSTRUCTION

The ONE DIGIT SHIFT RIGHT instruction is used to shift data between the start and end channels by four bits to the left.



Coding

Address	OP	Data	
0200	LD		0000
0201	FUN75		—
		DM	010
		DM	011
			00

Contents of data (D1, D2)

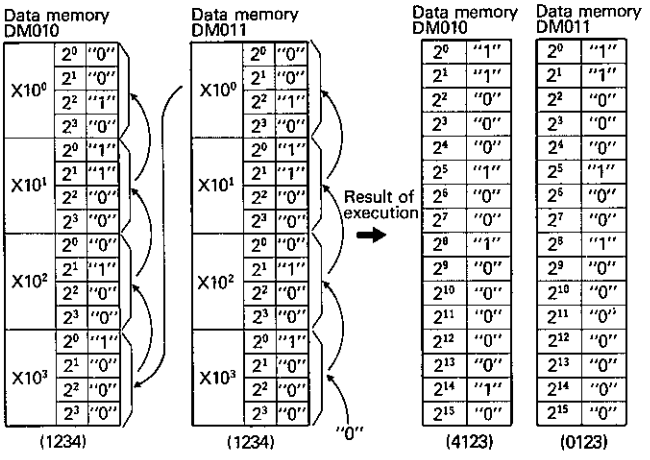
Input/output relay, internal auxiliary relay	00 to 60
Link relay	LR00 to 31
Holding relay	HR00 to 31
Data memory relay	DM000 to 511
Indirectly addressed data	*DM000 to 511

NOTES: 1. The third data [—] is ignored when the instruction is executed.
2. When the R register is logical 1, the ONE DIGIT SHIFT RIGHT instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, data between the start and end channels are shifted by four bits to the right.

In the above program, the contents of DM010 to DM011 are shifted by four bits (1 bit x 4 times) to the right. In this case "0" is inserted as the first digit of the start channel.



The data shifting operation is performed starting from the most significant digit of the end channel to the least significant digit of the start channel.

DATA OF ONE DIGIT SHIFT RIGHT

The data area for the ONE DIGIT SHIFT RIGHT instruction is specified by a start channel number and an end channel number, both of which can be determined freely provided these conditions are satisfied.

Start channel number $\leq$ End channel number and same data area

If these data conditions are not satisfied, an error will occur, causing special auxiliary relay 6303 to turn ON and the program not to be executed.

ONE DIGIT SHIFT RIGHT OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511. Use the data memory area for the start and end channels.

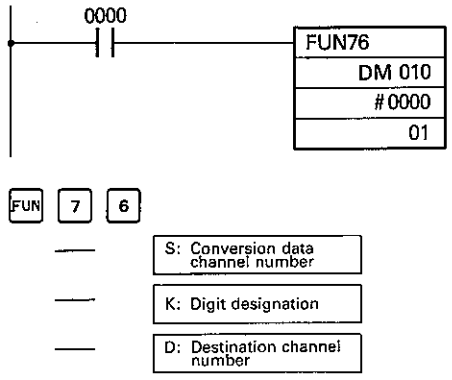
If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

NOTE: If the range of the data shift exceeds 50 channels (200 digits), a power failure may cause the execution of the shift operation to stop midway. Be sure to use no more than 50 channels.

4.43 4-TO-16 DECODER (FUN76) INSTRUCTION

The 4-TO-16 DECODER instruction is used to decode 4-bit binary data of 16 bits to 16-bit decimal data.



Coding

Address	OP	Data	
0200	LD		0000
0201	FUN76		—
		DM	010
		#	0000
			01

Contents of data

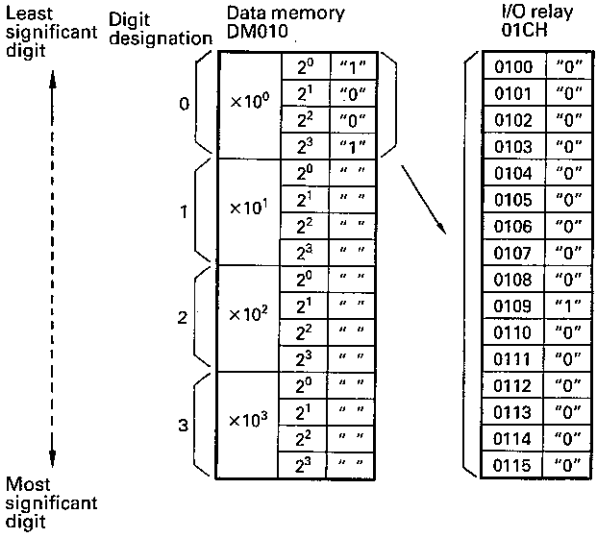
	S	D	K
Input/output relay, internal auxiliary relay	00 to 63	00 to 60	
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Timer, counter	TIM, CNT000 to 127	—	TIM, CNT000 to 127
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		
Constant	—		(See NOTE 1.)

NOTE: 1. The constant is determined according to the designated digit.
2. When the R register is logical 1, encoding 16-bit data into 4-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 1-digit (4 bits) binary data is decoded and transferred from the specified conversion data channel to the specified destination channel as 16-bit data by the specified number of digits.

In the above program, the least significant digit (4 bits 2^0 to 2^3) in the data memory is decoded to a decimal value (0 to 15) and transferred to the 01CH. Only the bits in the 01CH corresponding to the value are turned ON (logical 1), and other bits are turned OFF (logical 0).



4-TO-16 DECODING OF INDIRECTLY ADDRESSED DATA

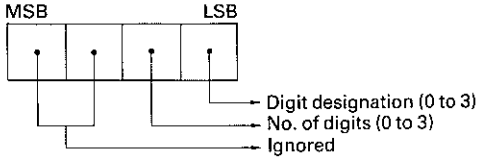
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or more than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

DIGIT DESIGNATION

Designate the digit and the number of digits to be decoded into 16-bit decimal data.

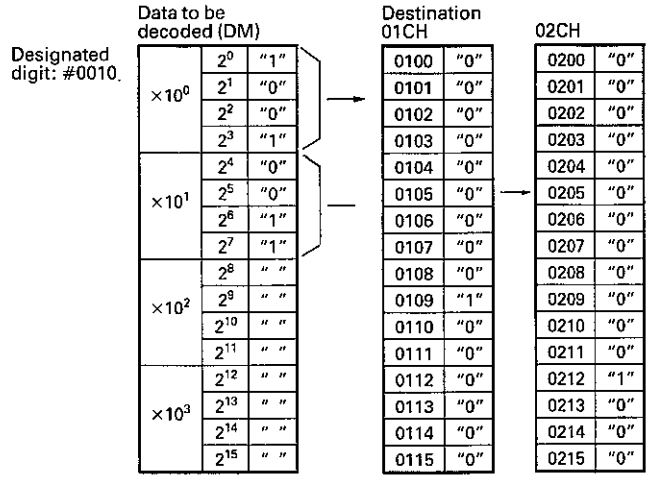


- Number of digits
  "0": One digit (4 bits) is decoded.
  "1": Two digits (8 bits) are decoded.
  "2": Three digits (12 bits) are decoded.
  "3": Four digits (16 bits) are decoded.

- Digit designation
  Designate the desired digit by using the digit designating number. (Refer to the figure appearing in "Operation of each register.")

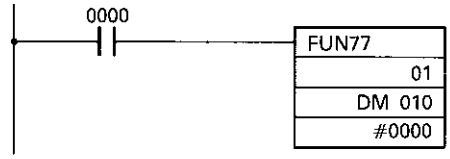
DECODING PLURAL DIGITS

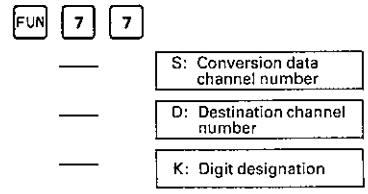
To decode plural digits, designate the lower-order digit as the digit designation.



4.44 16-TO-4 ENCODER (FUN77) INSTRUCTION

The 16-TO-4 ENCODER instruction is used to encode 16-bit decimal data into 4 bits of another 16-bit binary data.





Coding

Address	OP	Data	
0200	LD		0000
0201	FUN77		—
			01
		DM	010
		#	0000

Contents of data

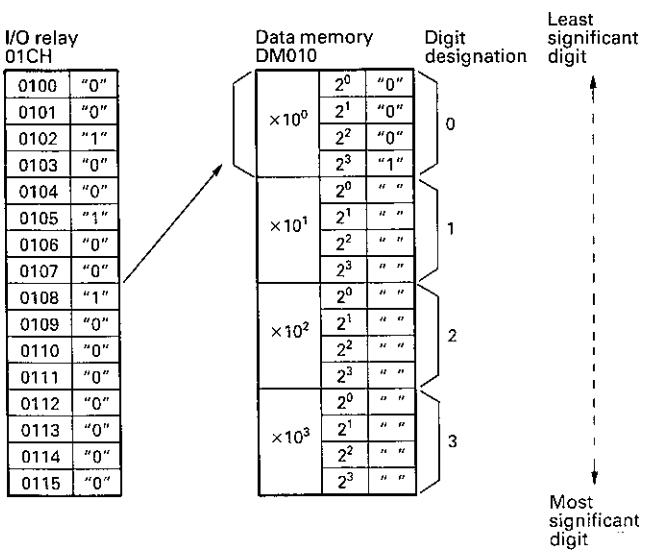
	S	D	K
Input/output relay, internal auxiliary relay	00 to 63	00 to 60	
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Timer, counter	TIM, CNT000 to 127	—	TIM, CNT000 127
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		
Constant	—		(See NOTE 1.)

NOTE: 1. The constant is determined according to the designated digit.
2. When the R register is logical 1, encoding 16-bit data into 4-bit data is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the 16-bit data in one channel is encoded to a 1-digit, 4-bit data, and transferred to specified digits of the data memory.

In the above program, the higher-order bit of 16-bit data of the 01CH (0100 to 0115) that is being turned ON is encoded to a 4-bit BCD value (expressed as decimal 0 to 15) and transferred to the least significant four bits (4 bits 2^0 to 2^3) in DM010.

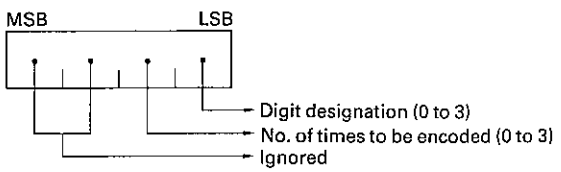


Of the ON bits of the 16-bit data to be encoded, the highest-order bit takes precedence over the lower-order bits when executing the instruction.

The data of all bits except the designated bits in the destination channel are not changed.

DIGIT DESIGNATION

Designate the number of times the data must be encoded and the destination digit to which the encoded data is to be transferred.

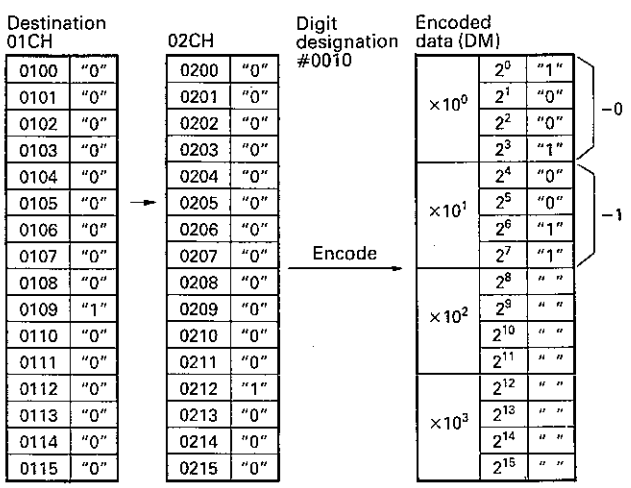


- No. of times the data is encoded
  "0": Once "2": Three times
  "1": Twice "3": Four times

- Digit designation
  Designate the desired digit by using the digit number of the digit. (Refer to the figure appearing in "Operation of each register.")

WHEN ENCODING PLURAL DIGITS

To encode plural digits, designate the lower-order digit as the digit designation.



16-TO-4 ENCODING OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

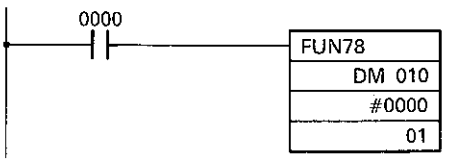
If the contents of the indirectly addressed area are other than BCD data or more than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

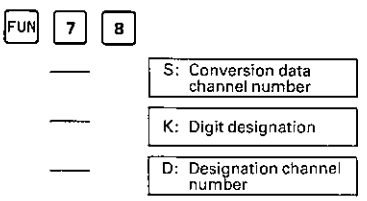
If all the bits of the input of a 16-TO-4 ENCODER instruction are "0000", an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.45 7-SEGMENT DECODER (FUN78) INSTRUCTION

The 7-SEGMENT DECODER instruction is used to convert 4 bits of 16-bit data into 8-bit data for 7-segment display.





Coding

Address	OP	Data	
0200	LD		0000
0201	FUN78		—
		DM	010
		#	0000
			01

Contents of data

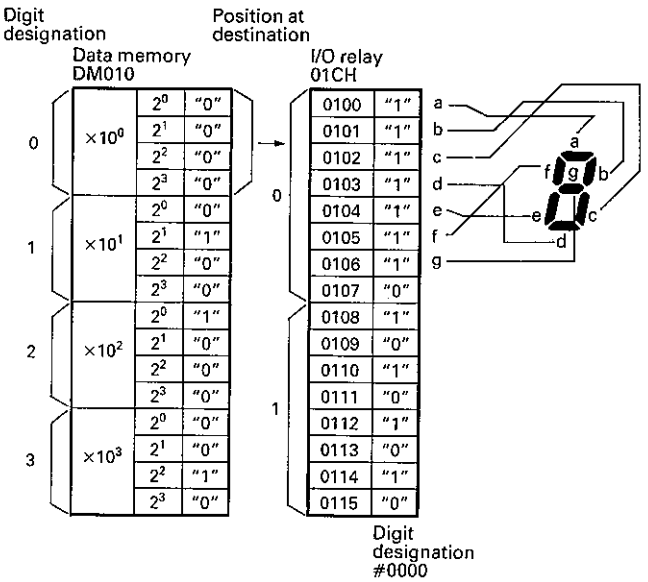
	S	D	K
Input/output relay, internal auxiliary relay	00 to 63	00 to 60	
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Timer, counter	TIM, CNT000 to 127	—	TIM, CNT000 to 127
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		
Constant	—		(See NOTE 1.)

NOTE: 1. The constant is determined according to the designated digit.
2. When the R register is logical 1, the conversion is executed at each scanning. To execute it only one time, program a differentaiting circuit for the input.

OPERATION OF EACH REGISTER

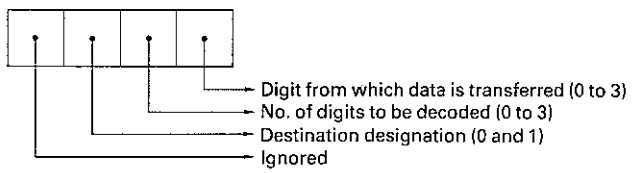
Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, specified 1-digit (4 bits) binary data in a channel is converted to 8-bit data for 7-segment display and transferred to the destination channel.

In the above program, the values of the four bits (expressed as hexadecimal 0 to F) of the least significant digit (2^0 to 2^3) are converted to 8-bit data for 7-segment display, transferred to the eight bits of I/O relay channel number 01 (0100 to 0107).



DIGIT DESIGNATION

Designate the destination, the number of digits to be decoded, and the digit from which the data is to be transferred.



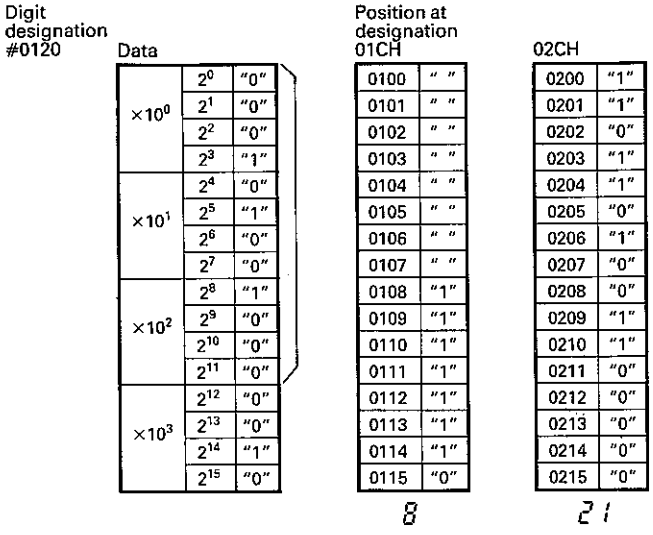
- Destination position
  "0": Lower two digits (8 bits)
  "1": Higher two digits (8 bits)

- Number of digits to be decoded
  "0": One digit is decoded.
  "1": Two digits are decoded.
  "2": Three digits are decoded.
  "3": Four digits are decoded.

- Designation of digit to be transferred
  Designate the digit from which data is transferred by using the digit number of that digit.

WHEN DECODING PLURAL DIGITS

To execute the 7-segment decoder instruction on plural digits, designate the lower-order digit as the digit destination.



7-SEGMENT DECODING OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

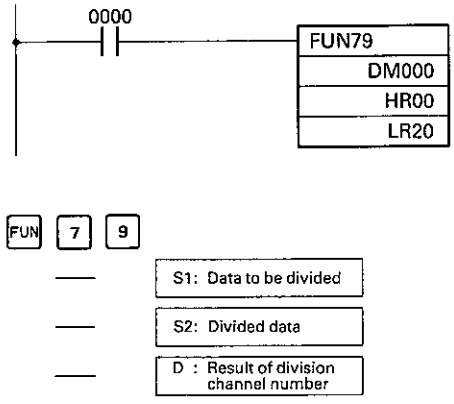
If the contents of the indirectly addressed area are other than BCD data or more than 512, an error will occur; this will cause special auxiliary relay 6303 to turn ON and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON and the program will not be executed.

Conversion input data					Conversion output data								7-segment display
2^3	2^2	2^1	2^0	(hexa-decimal)	g	f	e	d	c	b	a	
0	0	0	0	(0)	0	0	1	1	1	1	1	1	0
0	0	0	1	(1)	0	0	0	0	0	1	1	0	1
0	0	1	0	(2)	0	1	0	1	1	0	1	1	2
0	0	1	1	(3)	0	1	0	0	1	1	1	1	3
0	1	0	0	(4)	0	1	1	0	0	1	1	0	4
0	1	0	1	(5)	0	1	1	0	1	1	0	1	5
0	1	1	0	(6)	0	1	1	1	1	1	0	1	6
0	1	1	1	(7)	0	0	1	0	0	1	1	1	7
1	0	0	0	(8)	0	1	1	1	1	1	1	1	8
1	0	0	1	(9)	0	1	1	0	1	1	1	1	9
1	0	1	0	(A)	0	1	1	1	0	1	1	1	A
1	0	1	1	(B)	0	1	1	1	1	1	0	0	b
1	1	0	0	(C)	0	0	1	1	1	0	0	1	c
1	1	0	1	(D)	0	1	0	1	1	1	1	0	d
1	1	1	0	(E)	0	1	1	1	1	0	0	1	E
1	1	1	1	(F)	0	1	1	1	0	0	0	1	F

4.46 FLOATING-POINT DIVIDE (FUN79) INSTRUCTION

This instruction is used to divide 7-digit BCD data while automatically accounting for the position of the radix point (i.e., floating-point arithmetic operation). The result of the arithmetic operation is output as 7-digit data to two channels.



Coding

Address	OP	Data	
0200	LD		0000
0201	FUN79		—
		DM	000
		HR	00
		LR	20

Contents of data

	S1	S2	D
Input/output relay, internal auxiliary relay	00 to 62		00 to 59
Link relay	LR00 to 30		
Holding relay	HR00 to 30		
Timer, counter	TIM, CNT000 to 126		
Data memory relay	DM000 to 510		
Indirectly addressed data	*DM000 to 511		

NOTE: When the R register is logical 1, the floating-point divide instruction is executed at each scanning. To execute it only once, program a differentiating circuit for input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 7-digit BCD division is performed. The dividend, divisor, and quotient each require two channels.

In the above program, the contents of DM000 and DM001 of which each holds 16-bit data are divided by the contents of HR00CH and HR01CH (HR0000 to HR0115) of which each also has 16-bit data. The arithmetic operation is performed using 7-digit BCD data while automatically accounting for the position of the radix point. The results of the division are two 16-bit data and are output to LR20CH and LR21CH (LR2000 to LR2115). If the quotient is "0000" as a result of the operation, special auxiliary relay 6303 turns ON.

The following is an example when the division "$0.5670000 \times 10^{-2} \div 0.1234567 \times 10^{-3} = 0.4592703 \times 10^{2}$" is performed.

DM000

2^0	"0"
2^1	"0"
2^2	"0"
2^3	"0"
2^4	"0"
2^5	"0"
2^6	"0"
2^7	"0"
2^8	"0"
2^9	"0"
2^{10}	"0"
2^{11}	"0"
2^{12}	"0"
2^{13}	"0"
2^{14}	"0"
2^{15}	"0"

DM001

2^0	"1"
2^1	"1"
2^2	"1"
2^3	"0"
2^4	"0"
2^5	"1"
2^6	"1"
2^7	"0"
2^8	"1"
2^9	"0"
2^{10}	"1"
2^{11}	"0"
2^{12}	"0"
2^{13}	"1"
2^{14}	"0"
2^{15}	"1"

0.5670000×10^{-2}

÷

HR000

HR0000	"1"
HR0001	"1"
HR0002	"1"
HR0003	"0"
HR0004	"0"
HR0005	"1"
HR0006	"1"
HR0007	"0"
HR0008	"1"
HR0009	"0"
HR0010	"1"
HR0011	"0"
HR0012	"0"
HR0013	"0"
HR0014	"1"
HR0015	"0"

HR001

HR0100	"1"
HR0101	"1"
HR0102	"0"
HR0103	"0"
HR0104	"0"
HR0105	"1"
HR0106	"0"
HR0107	"0"
HR0108	"1"
HR0109	"0"
HR0110	"0"
HR0111	"0"
HR0112	"1"
HR0113	"1"
HR0114	"0"
HR0115	"1"

0.1234567×10^{-3}

||

LR20

LR2000	"1"
LR2001	"1"
LR2002	"0"
LR2003	"0"
LR2004	"0"
LR2005	"0"
LR2006	"0"
LR2007	"0"
LR2008	"1"
LR2009	"1"
LR2010	"1"
LR2011	"0"
LR2012	"0"
LR2013	"1"
LR2014	"0"
LR2015	"0"

LR21

LR2100	"1"
LR2101	"0"
LR2102	"0"
LR2103	"1"
LR2104	"1"
LR2105	"0"
LR2106	"1"
LR2107	"0"
LR2108	"0"
LR2109	"0"
LR2110	"1"
LR2111	"0"
LR2112	"0"
LR2113	"1"
LR2114	"0"
LR2115	"0"

0.4592703×10^{2}

The floating point is expressed as indicated by this example.

Ex. 0.5670000×10^{-2}

DM000

10^{-7}	2^0	"0"
	2^1	"0"
	2^2	"0"
	2^3	"0"
10^{-6}	2^4	"0"
	2^5	"0"
	2^6	"0"
	2^7	"0"
10^{-5}	2^8	"0"
	2^9	"0"
	2^{10}	"0"
	2^{11}	"0"
10^{-4}	2^{12}	"0"
	2^{13}	"0"
	2^{14}	"0"
	2^{15}	"0"

DM001

10^{-3}	2^0	"1"
	2^1	"1"
	2^2	"1"
	2^3	"0"
10^{-2}	2^4	"0"
	2^5	"1"
	2^6	"1"
	2^7	"0"
10^{-1}	2^8	"1"
	2^9	"0"
	2^{10}	"1"
	2^{11}	"0"
Floating point	2^{12}	"0"
	2^{13}	"1"
	2^{14}	"0"
	2^{15}	"1"

→ Virtual decimal point

→ Exponent (0 to 7)

→ Sign ("0"...+, "1"...−)

(0000)

The dividend, divisor, and quotient are set as shown above.

The floating point is indicated by the exponent and sign.

The virtual decimal point is at the most significant bit position.

The valid range of the divisor and dividend is 0.9999999×10^{7} to 0.0000001×10^{-7}.

The valid range of the quotient is 0.9999999×10^{7} to 0.1000000×10^{-7}.

The valid number of digits for the quotient is seven and digit exceeding this number will be rounded off.

If an attempt is made to execute this instruction with "0" as the dividend and the quotient exceeds the valid range, an error will occur and special auxiliary relay 6303 turns ON, disabling the instruction from being executed.

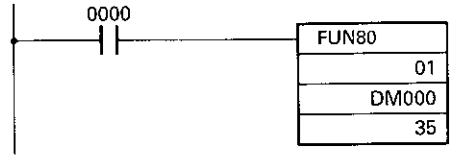
Since the arithmetic operation is performed with BCD data only, the data is checked. If the data is discovered not to be BCD, an error will occur. If the contents of the data are different from those in the above table, an error will also occur. Should an error occur, special auxiliary relay 6303 will turn ON and the instruction will not be executed.

FLOATING-POINT DIVIDE OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.
If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.47 DATA DISTRIBUTION (FUN80) INSTRUCTION

This instruction is used to distribute 16-bit data.



FUN 8 0

S: Data to be distributed

D1: Base address

D2: Offset data

Coding

Address	OP	Data	
0200	LD		0000
0201	FUN80		—
			01
		DM	000
			35

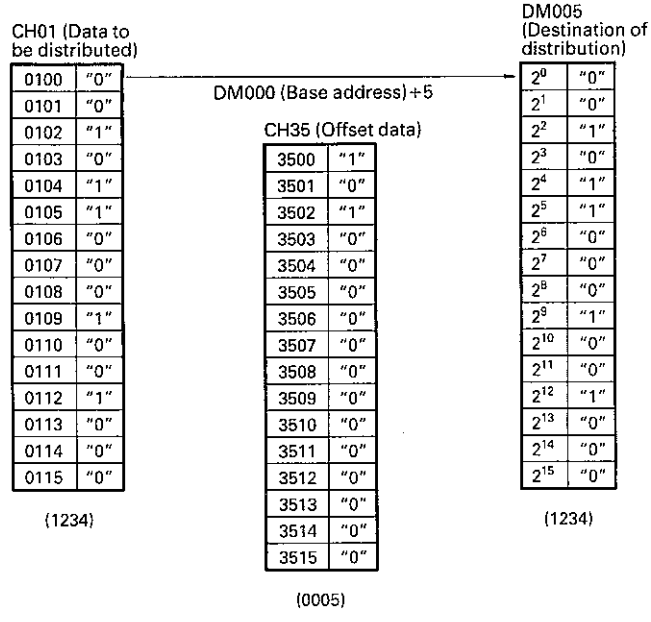
Contents of data

	S	D1	D2
Input/output relay, internal auxiliary relay	00 to 63	00 to 60	
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Timer, counter	TIM, CNT000 to 127		
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		
Constant	0000 to FFFF	—	—

NOTE: When the R register is logical 1, the DATA DISTRIBUTE instruction is executed at each scanning. To execute it only once, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, specified data is distributed to a channel that is a base address added with an offset. That is:
(S) → [D1 + (D2)]
In the above program, when the contents of CH35 that holds offset data are 0005, the contents of CH01 which are data to be distributed are distributed to DM005, the fifth channel from DM000 holding the base address. If the distributed data is "0000" as a result of the execution, special auxiliary relay 6306 turns ON.



CH01	
0100	"0"
0101	"0"
0102	"1"
0103	"0"
0104	"1"
0105	"1"
0106	"0"
0107	"0"
0108	"0"
0109	"1"
0110	"0"
0111	"0"
0112	"1"
0113	"0"
0114	"0"
0115	"0"

CH35	
3500	"1"
3501	"0"
3502	"1"
3503	"0"
3504	"0"
3505	"0"
3506	"0"
3507	"0"
3508	"0"
3509	"0"
3510	"0"
3511	"0"
3512	"0"
3513	"0"
3514	"0"
3515	"0"

DM005	
2^0	"0"
2^1	"0"
2^2	"1"
2^3	"0"
2^4	"1"
2^5	"1"
2^6	"0"
2^7	"0"
2^8	"0"
2^9	"1"
2^{10}	"0"
2^{11}	"0"
2^{12}	"1"
2^{13}	"0"
2^{14}	"0"
2^{15}	"0"

DATA DISTRIBUTION OF INDIRECTLY ADDRESSED DATA

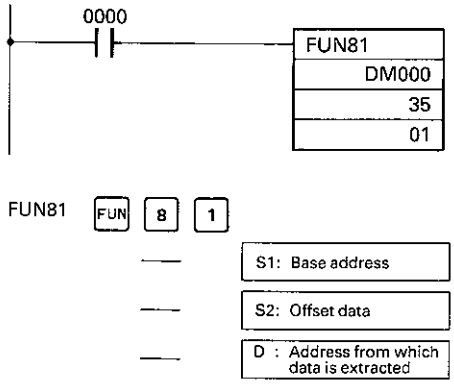
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.
If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the offset is not in BCD or exceeds the relay area within which it is specified, or data other than those in the above table will cause an error to occur. If an error occurs, special auxiliary relay 6303 turns ON and the instruction will not be executed.

NOTE: For details on base address and offset data, refer to 4.48, Data Extraction Instruction.

4.48 DATA EXTRACTION (FUN81) INSTRUCTION

This instruction is used to extract 16-bit data from a specified channel.



Coding

Address	OP	Data	
0200	LD		0000
0201	FUN81		–
		DM	000
			35
			01

Contents of data

	S1	S2	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60	
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Timer/counter	TIM, CNT000 to 127		
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		

NOTE: When the R register is logical 1, the DATA EXTRACTION instruction is executed at each scanning.
To execute it only one time, program a differentiating circuit for input.

OPERATION OF EACH REGISTER

Nothing is executed when the R register is logical 0. When the R register is logical 1, 16-bit data is extracted from a channel that is a base address added with an offset and is transferred to a specific channel. That is:

[S1 + (S2)] → (D)

In the above program, when the contents of CH35 that holds the offset data are 0005, the contents of DM005 that is the fifth channel from the base address DM000 are extracted and transferred to CH01. If the extracted data is 0000, special auxiliary relay 6303 turns ON.

DM000 (Base address)

CH35 (Offset data)

3500	"1"
3501	"0"
3502	"1"
3503	"0"
3504	"0"
3505	"0"
3506	"0"
3507	"0"
3508	"0"
3509	"0"
3510	"0"
3511	"0"
3512	"0"
3513	"0"
3514	"0"
3515	"0"

(0005)

DM005 (Data to be extracted)

2^0	"0"
2^1	"0"
2^2	"1"
2^3	"0"
2^4	"1"
2^5	"1"
2^6	"0"
2^7	"0"
2^8	"0"
2^9	"1"
2^{10}	"0"
2^{11}	"0"
2^{12}	"1"
2^{13}	"0"
2^{14}	"0"
2^{15}	"0"

(1234)

CH01 (Destination)

0100	"0"
0101	"0"
0102	"1"
0103	"0"
0104	"1"
0105	"1"
0106	"0"
0107	"0"
0108	"0"
0109	"1"
0110	"0"
0111	"0"
0112	"1"
0113	"0"
0114	"0"
0115	"0"

(1234)

DATA EXTRACTION OF INDIRECTLY ADDRESSED DATA

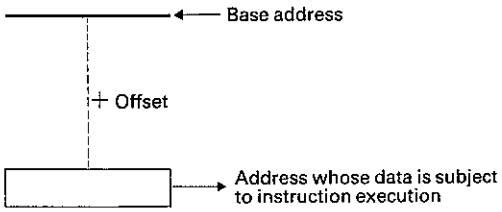
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.
If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the offset is not in BCD or exceeds the relay area within which it is specified, or data other than those in the above table is specified, an error occurs. If an error occurs, special auxiliary relay 6303 turns ON and the instruction will not be executed.

NOTE: For details on address and offset data, refer to the following description.

CONCEPT OF BASE ADDRESS AND OFFSET

Both the DATA DISTRIBUTION and DATA EXTRACTION instructions use a base address varied by the value of offset data within the same relay area.



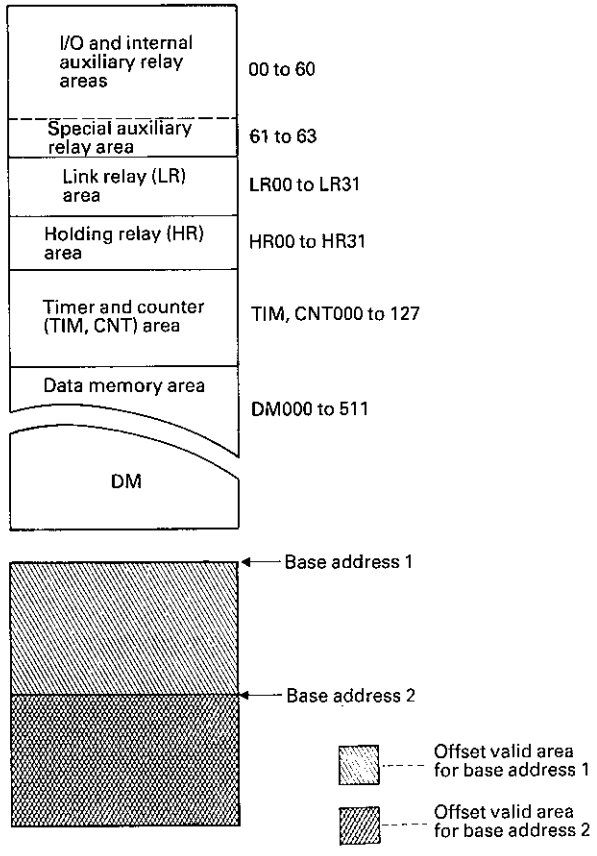
OFFSET DATA SETTING

Only BCD (binary coded decimal) data can be specified as the offset data. The valid range of the offset data is within the same relay area.

The "same relay area" can be any of five relay areas: I/O and internal auxiliary relay, link relay, holding relay, timer and counter, and data memory areas.

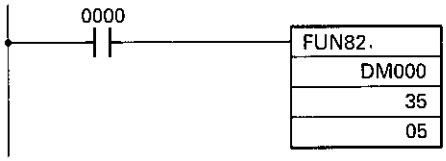
Since the special auxiliary relay area is used for data input only, this is an invalid area for the DATA DISTRIBUTION instruction. However, when the DATA EXTRACTION instruction is to be executed, the special auxiliary relay area can be used as part of the I/O and internal auxiliary relay area.

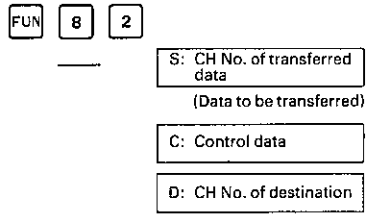
The valid range of the offset data is determined according to the base address. For example, if the base address is DM000, the maximum value of the offset data is 0511. If DM256 is set as the base address, however, the maximum value is 0255.



4.49 BIT TRANSFER (FUN82) INSTRUCTION

This instruction is used to transfer a specified bit data to a specified bit.





Coding

Address	OP	Data	
0200	LD		0000
0201	FUN82		—
		DM	000
			35
			05

Contents of data

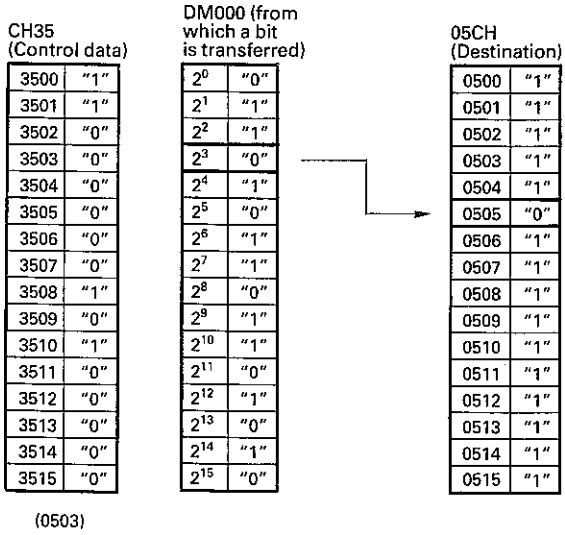
	S	C	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60	
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Timer, counter	—	TIM, CNT000 to 127	—
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		
Constant	0000 to FFFF	(See NOTE 1.)	—

NOTE: 1. The constant is determined according to the control data.
2. When the R register is logical 1, the BIT TRANSFER instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, a specified bit is transferred to a specified bit.

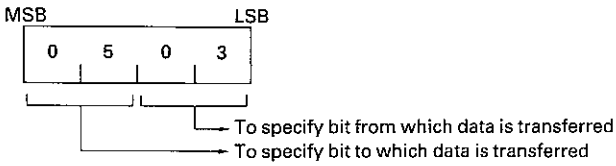
In the above program, when the contents of CH35 are 0503, the third least significant bit (bit 2^3) of DM000 is transferred to 0505.



SPECIFYING BIT BY CONTROL DATA

The bit from which data is to be transferred and the bit to which the data is transferred are specified by BCD data as follows.

The valid value is from 0 to 15.



BIT TRANSFER OF INDIRECTLY ADDRESSED DATA

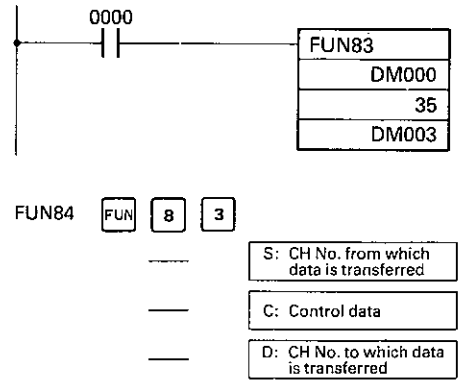
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

An invalid value of the control data, or data other than those in the above table will cause an error to occur. If an error occurs, special auxiliary relay 6303 turns ON and the instruction is not executed.

4.50 DIGIT TRANSFER (FUN83) INSTRUCTION

This instruction is used to transfer data in units of digits (4 bits).



Coding

Address	OP	Data	
0200	LD		0000
0201	FUN83		—
		DM	000
			35
		DM	003

Contents of data

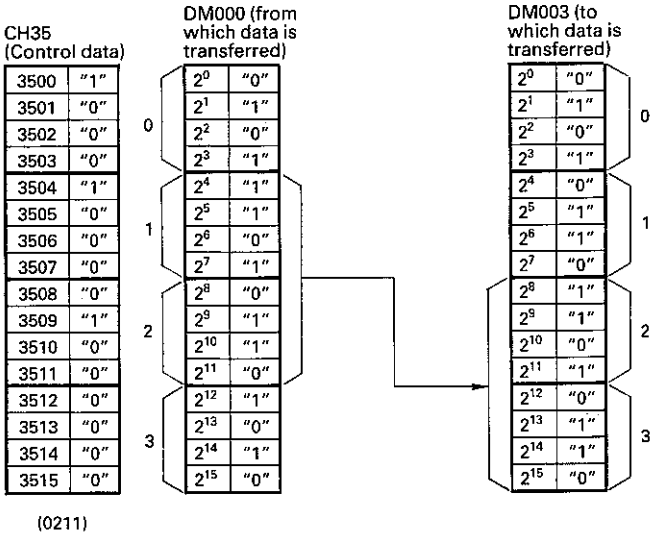
	S	C	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 60	
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Timer, counter	TIM, CNT000 to 127		
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		
Constant	0000 to FFFF	(See NOTE 1.)	—

NOTE: 1. The constant is determined according to the constants of the control data.
2. When the R register is logical 1, the DIGIT TRANSFER instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

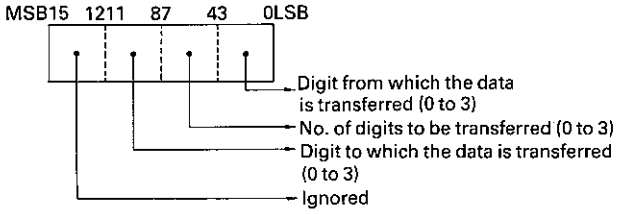
Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, data is transferred in units of 4 bits.

In the above program, when the contents of CH35 are 0211, 8 bits starting from bit 4 to bit 11 are transferred from DM000 to the most significant 8 bits of DM003.



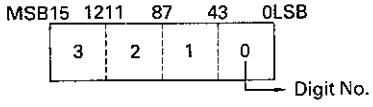
CONTROL DATA

In units of 4 bits, specify the digit from which the data is transferred, the number of digits to be transferred, and the digit to which the data is transferred.



SPECIFYING DIGIT

Specify the digit to or from which the data is transferred by using the digit number of that digit as follows:

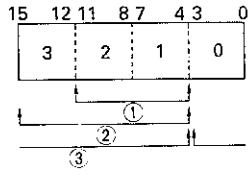


SPECIFYING NUMBER OF DIGITS

"0": One digit (4 bits) is transferred.
"1": Two digits (8 bits) are transferred.
"2": Three digits (12 bits) are transferred.
"3": Four digits (16 bits) are transferred.
If a number "4" or greater is specified, an error occurs.

TRANSFER OF PLURAL DIGITS

When transferring plural digits, specify the digit to which the data are transferred starting from the least significant bit of the destination digits.



For example, when digit 1 is specified in this figure, the data are transferred in this manner.

1. When the number of digits is specified as "1", the data are transferred to digit 1 and then 2.
2. When the number of digits is specified as "2", the data are transferred to digits 1, 2, and then 3.
3. When the number of digits is specified as "3", the data are transferred to digits 1, 2, 3, and then 0.

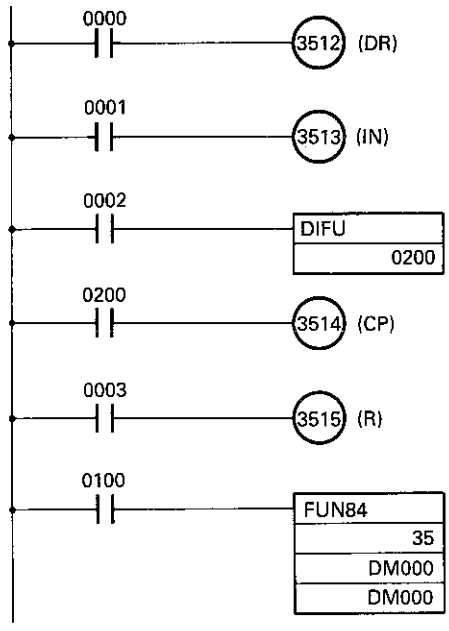
DIGIT TRANSFER OF INDIRECTLY ADDRESSED DATA

The only relays that can be indirectly addressed are data memory relays DM000 to DM511.
If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

An invalid value of the control data, or data other than those in the above table, causes an error to occur. If an error occurs, special auxiliary relay turns ON and the instruction will not be executed.

4.51 LEFT/RIGHT SHIFT (FUN84) INSTRUCTION

This instruction is used to shift specified 16-bit data either to the left or to the right by 1 bit.



FUN 8 4

— Control data
— Start CH No.
— End CH No.

Coding

Address	OP	Data	
0200	LD		0000
0201	OUT		3512
0202	LD		0001
0203	OUT		3513
0204	LD		0002
0205	DIFU(13)		0200
0206	LD		0200
0207	OUT		3514
0208	LD		0003
0209	OUT		3515
0210	LD		0100
0211	FUN84		—
			35
		DM	000
		DM	000

Contents of data

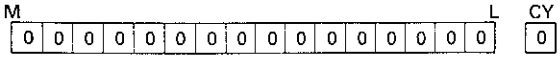
	Control data	Start CH No.	End CH No.
Input/output relay, internal auxiliary relay	00 to 60		
Link relay	LR00 to 31		
Holding relay	HR00 to 31		
Data memory relay	DM000 to 511		
Indirectly addressed data	*DM000 to 511		

NOTE: When the R register is logical 0, the LEFT/RIGHT SHIFT instruction is not executed at either clock input or reset input. When the R register is logical 1, the LEFT/RIGHT SHIFT instruction is executed at each scanning according to the control data.

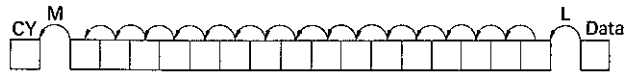
OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1 and a reset input is applied, all the specified 16 bits are reset (reset priority). When a clock input is applied, the 16 bits are shifted in the specified direction by 1 bit. When the instruction should be executed at the leading edge of the clock, program a differentiating circuit for the clock input. The instruction is executed as follows according to the contents of the control data.

1. When reset input is applied



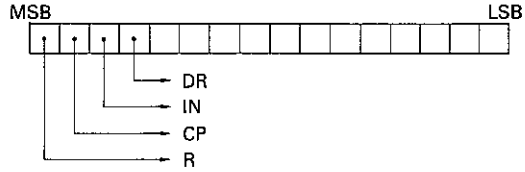
2. To shift from LSB to MSB



3. To shift from MSB to LSB

CONTROL DATA

To the control data, the direction of the shift (DR), data input (IN), clock input (CP), and reset input (R) are assigned.



DIRECTION OF SHIFT (D12)

"1": The data is shifted from the LSB to MSB.
"0": The data is shifted from the MSB to LSB.

DATA INPUT (D13)

The content of the data to be shifted

CLOCK INPUT (D14)

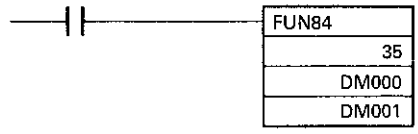
The data is shifted when the clock input turns ON.

RESET INPUT (D15)

All the 16 bits are reset when the reset input turns ON. The reset input takes precedence over the clock input.

SHIFTING MORE THAN 16 BITS

This instruction can also be used to shift more than 16 bits. To do so, specify channels according to the number of bits to be shifted to accommodate them.



In the above program, for example, 32 bits in data memories DM000 and DM001 are shifted by 1 bit.

When executing this instruction, make sure that the contents of the preceding data memory are equal to or less than those of the subsequent data memory, and that all the channels are within the same relay area. If these conditions are not satisfied, an error will occur causing special auxiliary relay 6303 to turn ON and the instruction to be not executed.

The contents of the carry flag (special auxiliary relay 6304) and the error flag (6303) are changed as follows:

	R register = 0	R register = 1		
		At reset	At data shift	At non-execution
Carry flag (6304)	•	"0"	↕	•
Error flag (6303)	•	↕	↕	↕

If the contents of the data are different from those in the table with the heading "Contents of data", an error occurs, causing special auxiliary relay 6303 to turn ON and the instruction to be not executed.

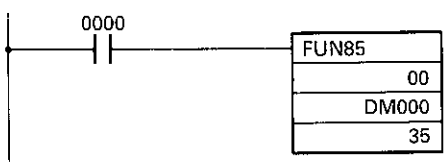
LEFT/RIGHT SHIFT OF INDIRECTLY ADDRESSED DATA

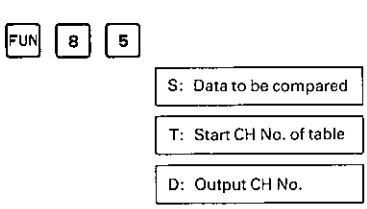
The only relays that can be indirectly addressed are data memory relays DM000 to DM511.

If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.52 TABLE COMPARE (FUN85) INSTRUCTION

This instruction is used to compare 16-bit data against data in 16 channels (table) and to output the results of the comparison to a specified channel.





Coding

Address	OP	Data
0200	LD	0000
0201	FUN85	—
		00
		DM000
		35

Contents of data

	S	T	D
Input/output relay, internal auxiliary relay	00 to 63	00 to 45	00 to 60
Link relay	LR00 to 31	LR00 to 16	LR00 to 31
Holding relay	HR00 to 31	HR00 to 16	HR00 to 31
Timer, counter	TIM, CNT000 to 127	TIM, CNT000 to 112	TIM, CNT000 to 127
Data memory relay	DM000 to 511	DM000 to 496	DM000 to 511
Indirectly addressed data	*DM000 to 511		
Constant	0000 to FFFF	—	—

NOTE: When the R register is logical 1, the TABLE COMPARE instruction is executed at each scanning. To execute it only one time, program a differentiating circuit for the input.

OPERATION OF EACH REGISTER

Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, 16-bit data is compared against data of each channel of the specified 16 channels. As a result of the comparison, when the 16-bit data is found to be in agreement with the data in the channels, "1" is sequentially output to the corresponding bits of a channel specified for the output starting from the least significant bit. In the same manner, "0" is output when the 16-bit data disagrees with the data in the 16 channels. If "0" is output to all the 16 bits of the output channel, special auxiliary relay 6306 turns ON.

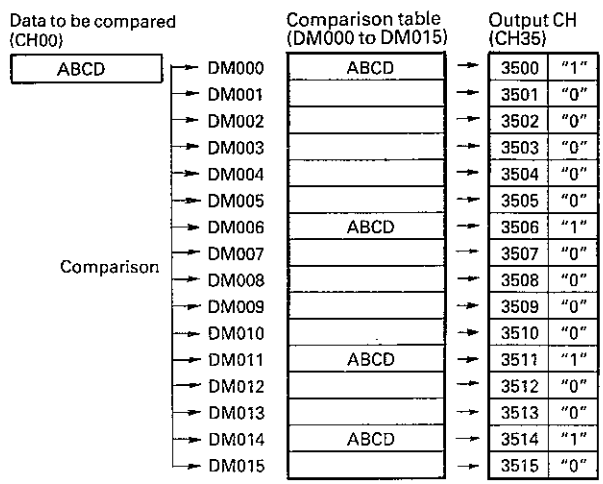


TABLE COMPARE OF INDIRECTLY ADDRESSED DATA

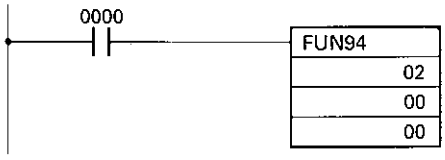
Data memories DM000 to 511 can be indirectly addressed for the data to be compared and the output channel number. For the start channel number of the table, DM000 to 495 can be indirectly addressed.

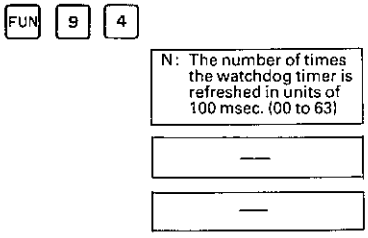
If the contents of the indirectly addressed area are other than BCD data or DM000 to DM511, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

If the contents of data are other than those in the above table, an error will occur; this will cause special auxiliary relay 6303 to turn ON, and the program will not be executed.

4.53 WATCHDOG TIMER SETTING (FUN94) INSTRUCTION

This instruction is used to refresh the time of the watchdog timer.





Coding

Address	OP	Data
0200	LD	0000
0201	FUN94	
		02
		00
		00

Contents of data

MAX	MIN
N=0 130 msec.	—
1 230 msec.	130 msec.
2 330 msec.	230 msec.
⋮	⋮
n 100 · n + 130 msec.	100 · (n − 1) + 130 msec.

NOTE:
1. Input the number of times the watchdog timer is to be refreshed in the same manner as setting channel number.
2. The second and third data are ignored.

OPERATION OF EACH REGISTER

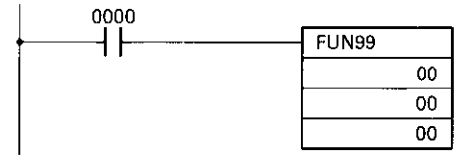
Nothing is executed when the content of the R register is logical 0. When the content of the R register is logical 1, the watchdog timer is refreshed.

Once the FUN94 instruction has been executed, the watchdog timer is refreshed the number of times specified by the instruction. This instruction can be used more than once.

Unless the FUN94 instruction exists in the program, the time of the watchdog timer is automatically set to 130msec.

4.54 RUN STOP (FUN99) INSTRUCTION

This instruction is used to stop the RUN operation of the programmable controller when the specified input relay is turned OFF. When the specified input relay is turned ON, the RUN operation is started from the initial state into which the programmable controller is set upon power application.



Coding

Address	OP	Data
0000	LD	0000
0001	FUN99	—

Be sure to specify a contact number of the input unit. By so doing, this instruction can be used to monitor the power supply to the input unit and thus to protect the system from damage in case of a power failure.

When the specified input relay is turned ON (i.e., when the R register is logical 1), this instruction is processed as NOP.

If the address immediately before that for this instruction holds any other instruction than the LD instruction, the error flag (special auxiliary relay 6303) is turned ON and the RUN STOP instruction is processed as NOP.

When the power supply to the specified relay has been restored after the relay was turned OFF, causing the programmable controller to stop the RUN operation, special auxiliary relay 6011 is turned ON to indicate that the RUN operation was temporarily stopped. The special auxiliary relay should be reset by the user program.

CHAPTER 5
INSTALLATION AND WIRING

The SYSMAC-C Series programmable controller is highly reliable and resistant to adverse environmental conditions. However, to permit the PC to exhibit its functions fully and to enhance its reliability, care must be exercised on the following points when installing the PC.

5.1 MOUNTING LOCATIONS AND ENVIRONMENTAL CONDITIONS

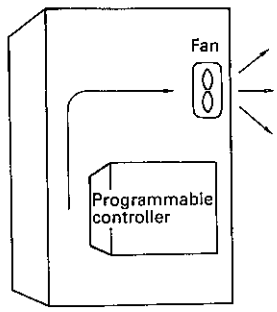
When installing the programmable controller, avoid these areas.

- Where the ambient temperature is beyond the range of 0 to 50°C.
- Where temperature changes abruptly, thus resulting in condensation.
- Where relative humidity exceeds the range of 35 to 85%.
- When subject to corrosive or flammable gas.
- When subject to excessive dust, salt, or iron particles.
- When subject to vibration or shock.
- When subject to direct sunlight.

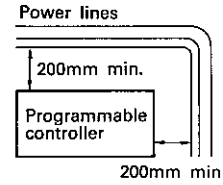
5.2 MOUNTING POSITIONS WITHIN CONTROL PANELS

When mounting the PC in a control panel, take into consideration the operability, maintainability, and environmental resistance of the PC.

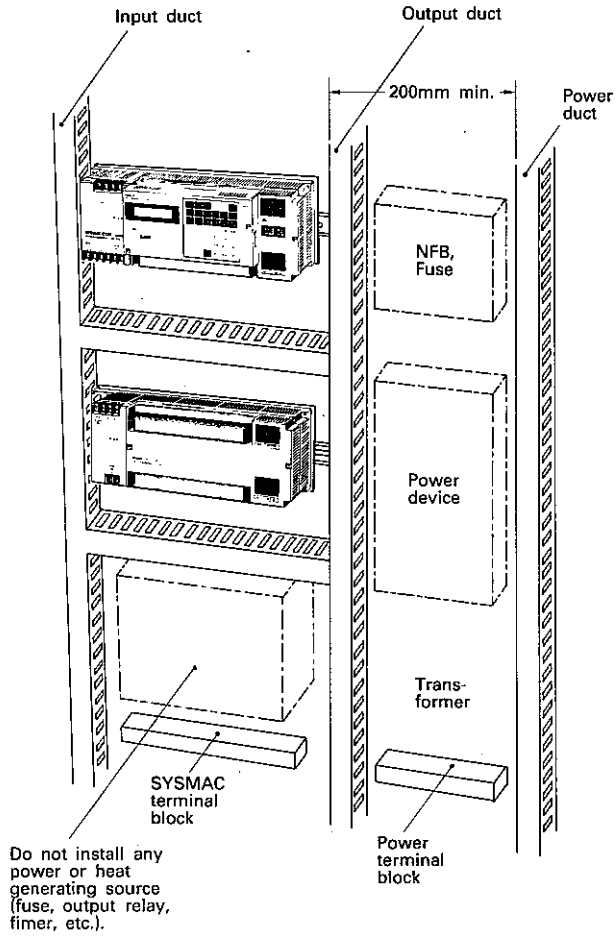
1. To permit the use of the PC within the ambient operating temperature range, pay attention to these points.
   a. Provide the programmable controller with adequate space for ventilation.
   b. Avoid mounting the controller directly above any heat generating sources (heater, transformer, resistor of high capacity).
   c. Install a fan for forced ventilation if the ambient temperature exceeds 50°C.



2. Avoid mounting the PC in a panel in which high-tension equipment is installed.
3. Provide a distance of more than 200mm between the high-tension equipment or power lines and the PC.



4. Mount the PC as far away as possible from high-tension equipment or power devices for the sake of safety in maintenance and operation.



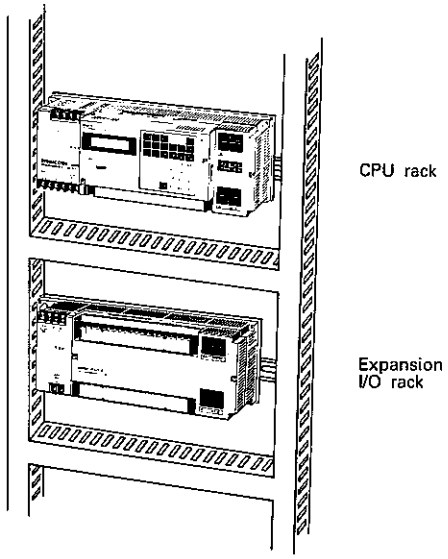
5. Mounting the PC 1,000 to 1,600mm above the installed surface of the control panel will facilitate the operation of the PC.

5.3 HOW TO INSTALL WITHIN CONTROL PANELS

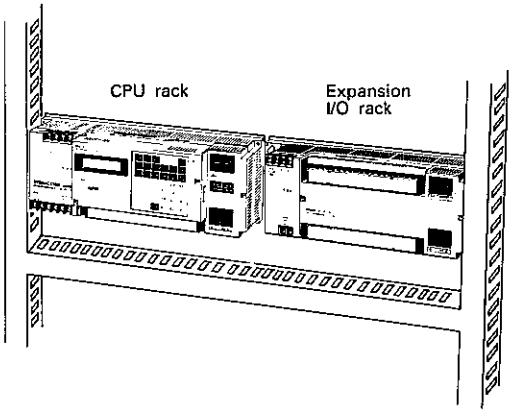
The SYSMAC-C120 can be installed either directly to the mounting panel within a control panel or on a DIN rail. When connecting expansion I/O racks to the CPU rack for system expansion, avoid employment of more than three expansion I/O racks and use an expansion I/O rack connecting cable 2m long maximum.

1. When mounting PC on a DIN rail
   Mount the PC on a DIN rail when installing it within a control panel. Secure the DIN rail attachment to the rear-sides of the PC and expansion I/O racks.
   NOTE: Use Type PFP-100N2 DIN rail and Type 3G2A9-DIN01 DIN rail attachment.

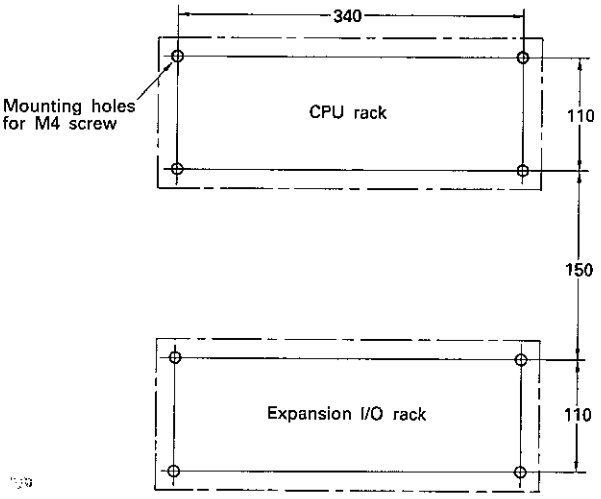
Vertical mounting



Horizontal mounting

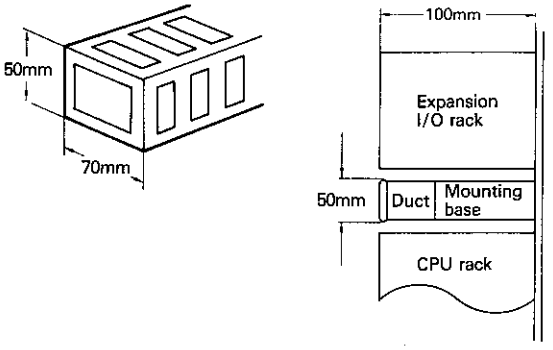


2. Mounting dimensions
   Use M4 mounting screws to secure the CPU rack or expansion rack.
   If an intermediate mounting plate is required, it must be grounded completely and must have been finished with high-conductivity plating to enhance noise immunity.
   Limit the total length of three expansion rack connecting cables to 2m.



3. Wiring ducts
   Use of wiring ducts is recommended for the external wiring of I/O units. Provide each wiring duct with a mounting base to facilitate the wiring from each I/O unit so that the height of the wiring duct becomes nearly the same as that of the expansion I/O rack.

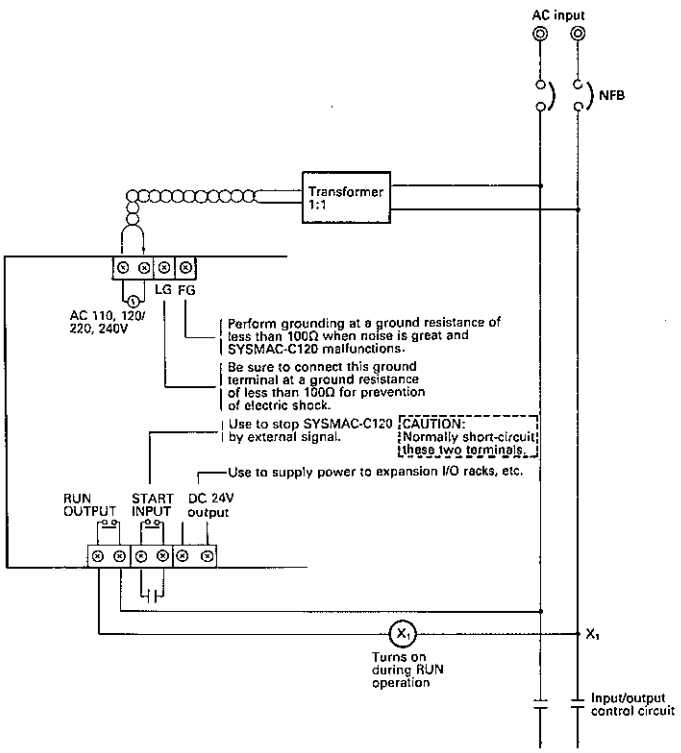
Standard duct dimensions



5.4 PROCESSING OF WIRING WITHIN CONTROL PANELS

1. Pay attention to the following points for wiring within a control panel:
   - Provide a distance of more than 200mm between the high-tension or power lines and the PC.
   - Avoid accommodating the I/O connecting cable in the same duct as other wiring.
   - Complete the wiring so that the I/O lines do not touch the CPU rack.
   - Complete the wiring to facilitate the mounting and removal of I/O units.
   - Complete the I/O wiring so that the I/O operation indicators on each I/O unit are easily visible.

2. About wiring and power supply



Power supply capacity

The power consumption of the PC is less than 60VA. However, upon power application, inrush current of about 5 times the steady-state current will flow through the programmable controller. Take this point into account.

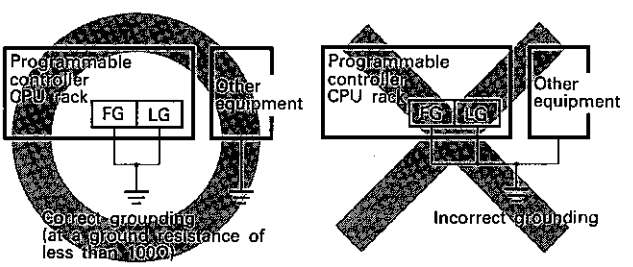
As the power supply line of the PC, employ a wire of 2mm^2 min. to prevent voltage drop. (Use of twisted pair wires is recommended.)

For general noise on the power supply line, the noise suppressing circuit in the PC is sufficient. However, supplying power through a transformer having a transformer voltage ratio of 1:1 will help reduce equipment-to-ground noise to a great extent and installation of such a transformer is recommended.

Terminal FG of the I/O unit is a ground terminal used for prevention of electric shock. Use an exclusive ground wire (having a conductor cross-sectional area of 2mm^2 min.) for grounding at a ground resistance of less than 100Ω. Terminal LG is a noise filter neutral terminal and the grounding is not required. In case of a large noise that may cause an erroneous operation, LG and FG are short-circuited for exclusive grounding (at a ground resistance of less than 100Ω).

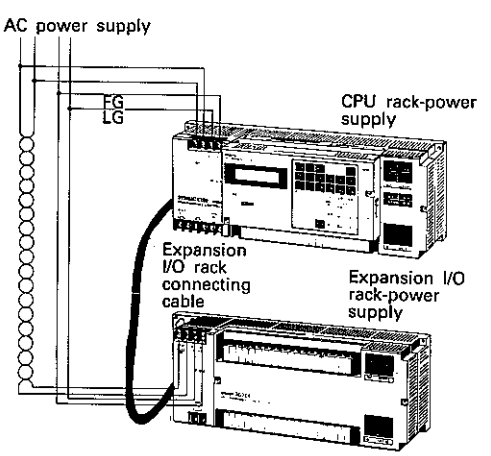
Note that common use of the grounding line with other equipment or connecting to the beam of the building may adversely affect the system. Keep the length of the ground wire within 20m. Care must be taken as to the ground resistance, because it varies depending on the nature of ground, water content, season, and the time elapsed after the underground laying of the ground wire.

GROUNDING WITH OTHER EQUIPMENT



3. Wiring of expansion rack

Use twisted pair wires of 2mm^2 min. as the power supply cable for expansion rack and keep them separate from high-tension or power lines and input/output lines.



Connect the ground wire to the terminals LG and FG on the operating panel of the CPU rack-power supply. Use a wire of more than $2mm^2$ for grounding.

Expansion I/O rack connecting cables are available in three standard lengths:

50cm (3G2A5-CN511)
1m (3G2A5-CN121)

Avoid accommodating the power supply cable for expansion rack and the I/O connecting cable in the same duct as other wiring.

Limit the total length of three expansion I/O rack connecting cables to 2m.

4. Wiring of I/O units

For the wiring of I/O units, use a wire of $1.25mm^2$ or less.

If an input device with a neon lamp operation indicator is used, the operation indicators (LEDs) of an I/O unit may be caused to illuminate at a voltage lower than the rated voltage. To prevent this, insert a bleeder resistor in parallel with the input signal.

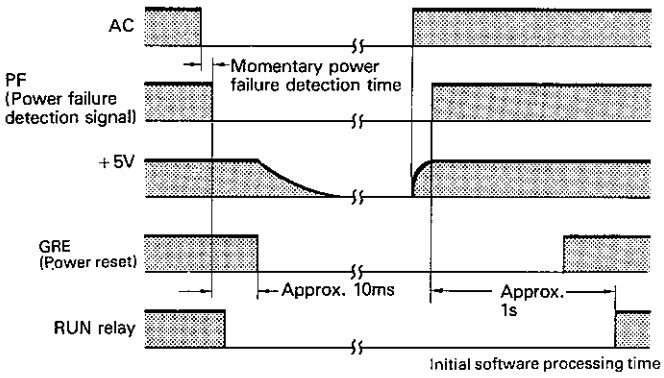
When a triac output type unit is used, the output device connected to the triac output may not be turned off because of a leakage current. If a low-capacitor load is to be connected to the triac output type output unit, insert a bleeder resistor in parallel with the output device.

5.5 OPERATION AT POWER FAILURE

1. Supply the power to the PC within the operating voltage range.

2. The power sequence circuit is incorporated in the power supply unit of the PC to prevent the programmable controller from malfunctioning because of a momentary power failure or a decrease in the supply voltage.
   a. Supply voltage drop
      If the supply voltage drops below its 85%, the operation of the PC stops, causing external output relays to turn off.
   b. Momentary power failure
      The PC ignores a momentary power failure not exceeding 10msec.
      A momentary power failure of 10ms or more and less than 25ms may or may not be detected because it is in an unstable area.
      If a power failure of more than 25ms occurs, the operation of the CPU is stopped and thus its outputs are absent (i.e., the output units are turned OFF).
   c. Automatic reset
      The PC will automatically resume its operation after the supply voltage (more than 85%) is restored.

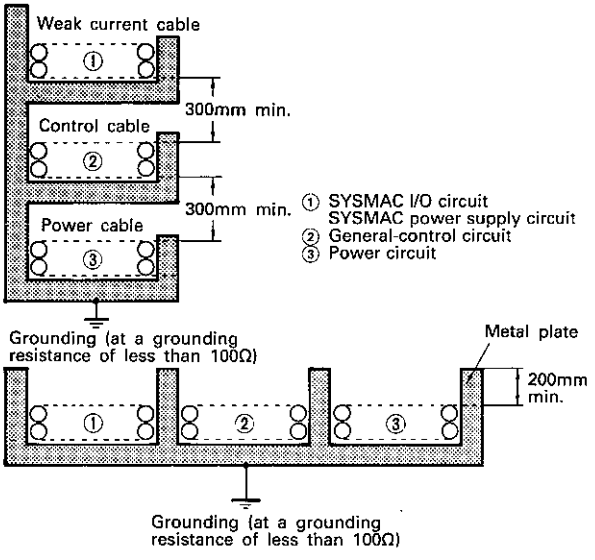
CPU RUN/STOP Timing Chart



5.6 EXTERNAL WIRING

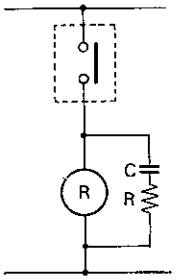
1. Be sure to process the input/output lines of the PC separately from other control lines. (Do not share the conductors of the I/O cable with others.)

2. To process the cables for the PC with power cables rated at 400V 10A max. or 220V 20A max.:
   a. Be sure to provide a minimum distance of 300mm between both cables when their racks are paralleled.
   b. Be sure to screen them with grounded metal plate when both cables are placed in the same duct at the termination process of the cable-laying work.



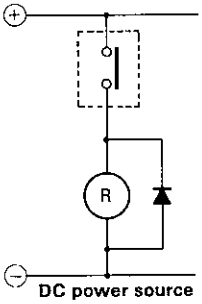
5.7 NOTES ON OUTPUT

If any electrical devices likely to generate electric noise are to be employed as the output loads of the PC, be sure to take measures to absorb this noise. For example, electromagnetic relays and valves generating a noise of 1,200 to 1,300V minimum are subject to noise suppression. For AC-operated noise sources, connect a surge suppressor in parallel with the coil of each device. For DC-operated noise sources, connect a diode in parallel with the coil of each device.



AC power source

C: 0.5μF ±20% min.
Nonpolarity
Withstand voltage: 1,500V min.
R: 50Ω ±30%, 0.5W



DC power source

Select a diode with the breakdown voltage and current ratings according to the load.

Since the output elements of the PC are packaged on a printed circuit board and connected to the terminal board, short-circuiting any of the loads connected to the output elements may result in the burning of, and consequent damage to, the PC board. Therefore the use of fuses is recommended for protection of the output elements.

CHAPTER 6
MAINTENANCE AND INSPECTION

To sustain the proper system operation at all times, it is necessary to inspect the PC daily. If any trouble occurs in the PC, how the system should be protected and how soon it can be recovered from the failure become important. In this chapter, the items to be inspected on the PC and the actions to be taken if the PC fails are described.

6.1 INSPECTION

To make the most of the functions of the PC under the best condition, it is necessary to inspect the PC daily or periodically.

INSPECTION ITEMS

The PC employs semiconductors as its main component elements. However, the semiconductors may deteriorate depending on the environmental conditions and must therefore be inspected periodically. The standard inspection cycle is 6 months to 1 year. If environmental conditions require it, the date of inspection should be moved up. As a result of the daily or periodic inspection, if the PC is found to be outside the criteria in the following table, be sure to correct it so that it falls within the prescribed criteria.

No.	Inspection Item	Particulars of Inspection	Criteria
1	AC power supply (a) Voltage (b) Fluctuation	(1) Is the rated voltage available when measured at the AC input terminal block?	Supply voltage must be operating voltage range.
		(2) Does a momentary power failure occur frequently or is there any sharp rise or drop in the supply voltage?	The supply voltage must be within the permissible fluctuation range described above.
2	Environmental conditions (a) Ambient temperature (b) Humidity (c) Vibration (d) Dust	Are the temperature and humidity within the respective range? (When the PC is installed in a control panel, the temperature within the panel may be regarded as the ambient temperature of the programmable controller.)	(a) 0 to +50°C (b) 30 to 90% RH (c) Must be free from vibration. (d) Must be free from dust.
3	Power supply of expansion I/O rack (a) Voltage (b) Ripple	Are the voltage and ripple within the operating range when measured at the terminal board of each I/O unit?	Must conform with the specifications of each I/O unit.
4	Mounting conditions	(1) Are the CPU rack and expansion I/O rack secured firmly?	The mounting screws must not be loose.
		(2) Is each expansion I/O rack fixed firmly?	Each I/O rack must not be loose.
		(3) Is the expansion I/O rack connecting cable inserted completely?	The connecting cable must not be loose.
		(4) Is there any loose screw in the external wiring?	The screw terminals must not be loose.
		(5) Is there any broken cable in the external wiring?	The external wiring must be free from any abnormalities in appearance.
5	Service life	(1) Output relays in the CPU and expansion I/O units.	Electrically: 300×10^3 operations Mechanically: $50{,}000 \times 10^3$ operations
		(2) Battery	5 years

CAUTION:
Be sure to turn off the power before replacing any unit of the PC.

NOTES ON INSPECTION

1. If a defective unit is discovered and replaced, confirm whether or not the replaced unit is abnormal.
2. In the event of a faulty contact of the cable, wipe the connector pins with a clean all-cotton cloth moistened with industrial alcohol. Be sure to plug in the flat cable after removing the cloth waste.

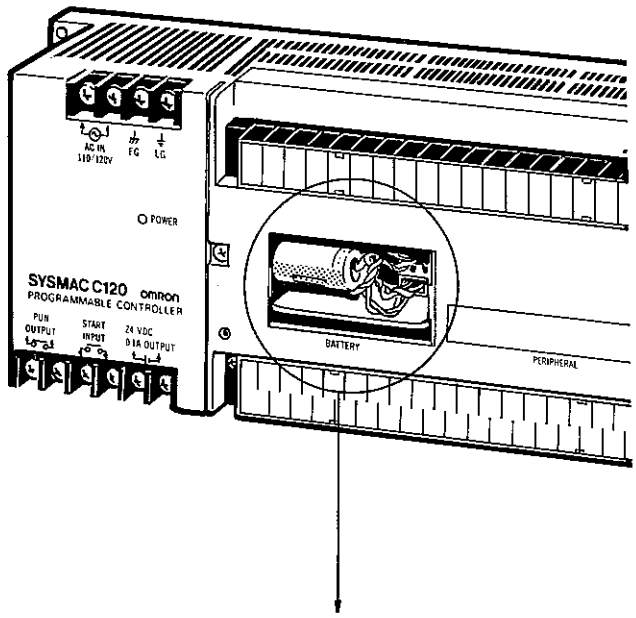
TOOLS AND TESTING EQUIPMENT REQUIRED FOR MAINTENANCE

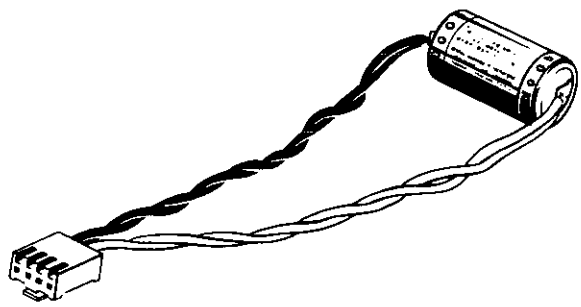
In the maintenance of the PC, the following tools and testing equipment will facilitate the daily or periodic inspection of the programmable controller.

1. Tools and testing equipment recommended as mandatory
   - Screwdrivers (phillips and round-blade)
   - Tester or digital voltmeter
   - Industrial alcohol and all-cotton cloth
2. Measuring instruments recommended only if required
   - Synchroscope
   - Pen-recording oscilloscope

MAINTENANCE PARTS

1. Spare parts
   If the PC fails, its repair is impossible without any spare parts no matter how early the trouble is discovered. So it is recommended to have at least one I/O unit as a spare part.
2. Consumables
   Fuses for overload protection:
   For CPU rack-power supply and expansion I/O rack-power supply . . . 3A.
3. Replacement parts
   - Battery unit (Type 3G2A9-BAT08)
     When the battery has been discharged, "BATTERY FAILURE" indicator illuminates. Be sure to replace the battery with a new one within a week after the "BATTERY FAILURE" indication. The life of the battery is considered to be 5 years.
     Be sure to turn off the power before replacing the battery, and replace it, including the connector, within 5 minutes.
     NOTE: When the AC power is not ON during battery replacement, first apply the AC power for more than 10sec; then turn it off.



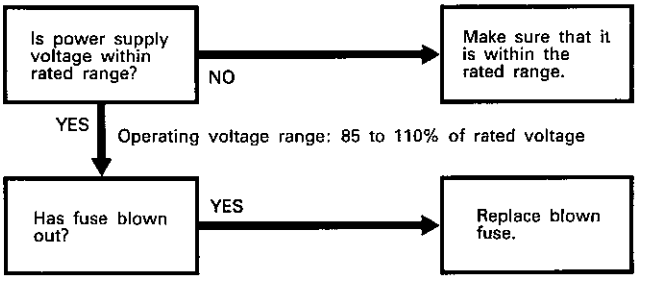


6.2 TROUBLESHOOTING

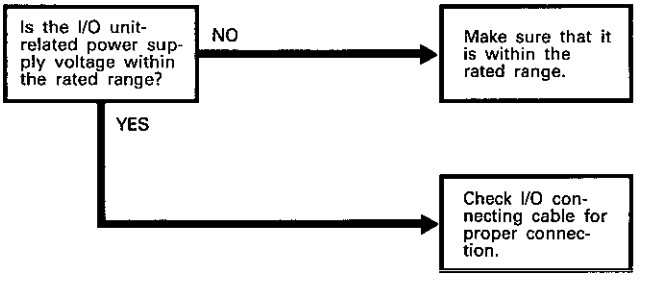
If any abnormality occurs in the PC, thoroughly learn what the trouble is and check whether the symptom is reproducible or caused through relation with other equipment. Then follow the troubleshooting flowcharts shown below.

POWER SUPPLY

1. Main power supply check
   In this check, the AC power being supplied to the PC is confirmed if it is within the rated range.



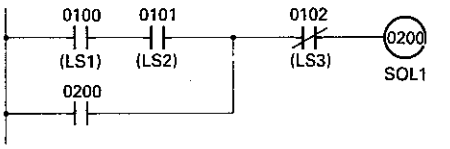
2. I/O unit-related power supply check
   The power supply for loads is connected to the terminals of each I/O unit. Should any abnormality occur in this power supply, the I/O device connected to the I/O unit will not operate.



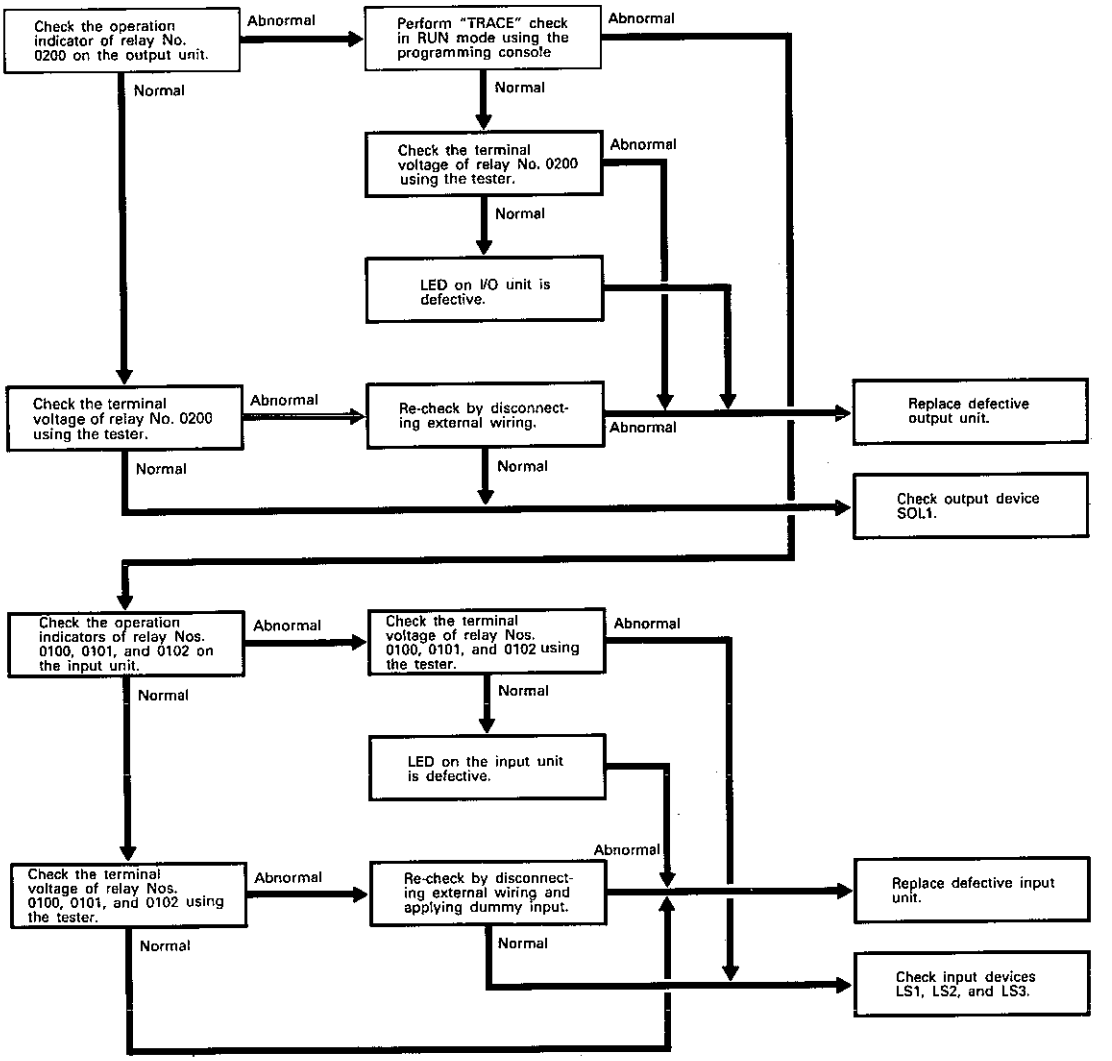
INPUT/OUTPUT UNIT

The following flowchart is indicated on the assumption that the maintenance spare parts are provided. If no spare part is provided, first check I/O devices thoroughly. The flowchart is illustrated based upon the circuit example shown below.

Circuit example



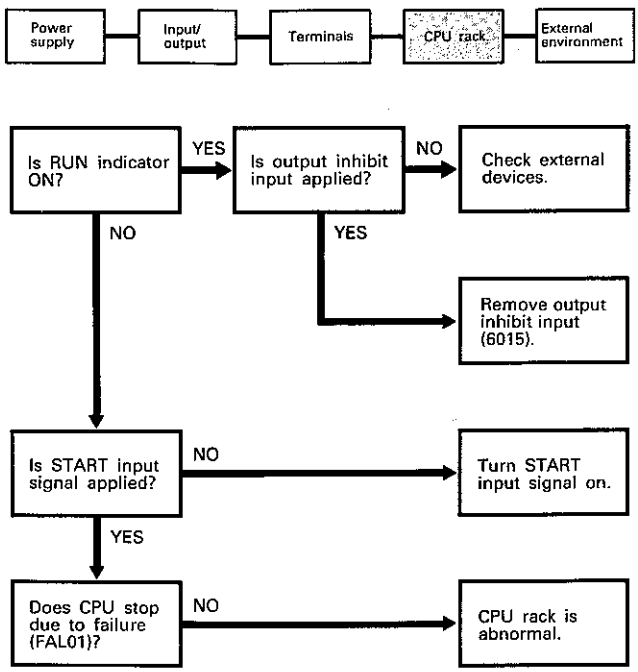
SOL1 malfunctions



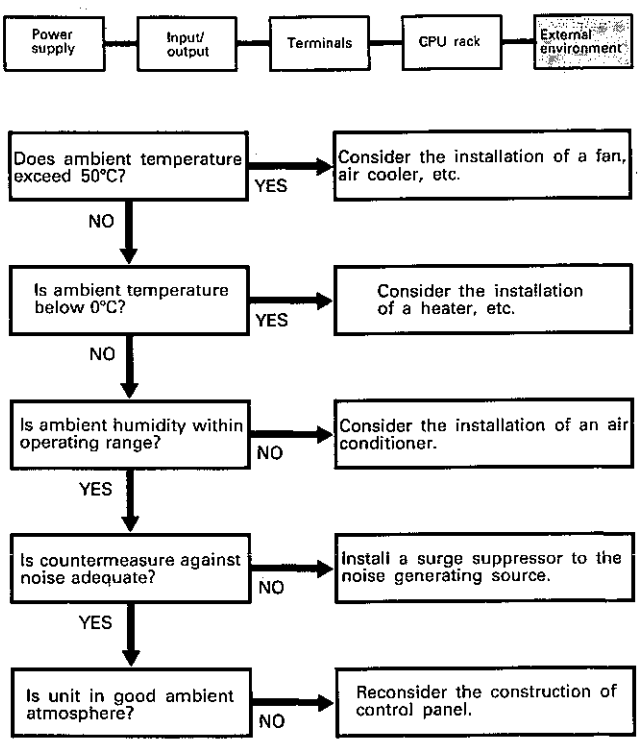
TERMINALS

① Check each I/O unit for loose terminals.
② Check the power supply terminals for loose connection.
③ Check each unit for loose mounting screws.
④ Check the expansion I/O rack-connecting cable for proper mounting.

CPU RACK

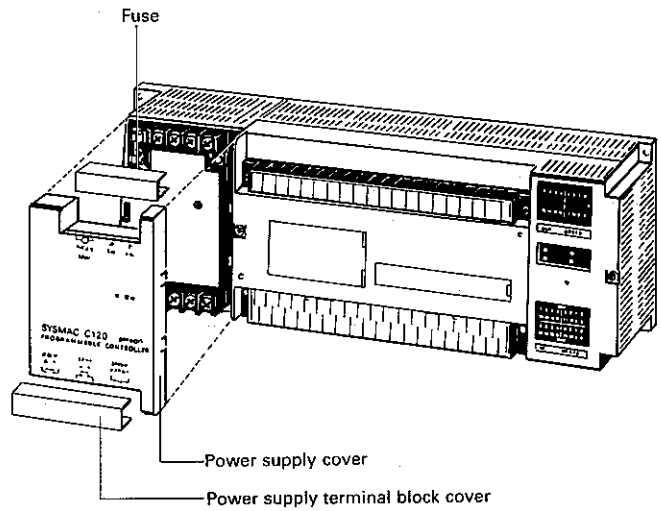


EXTERNAL ENVIRONMENT



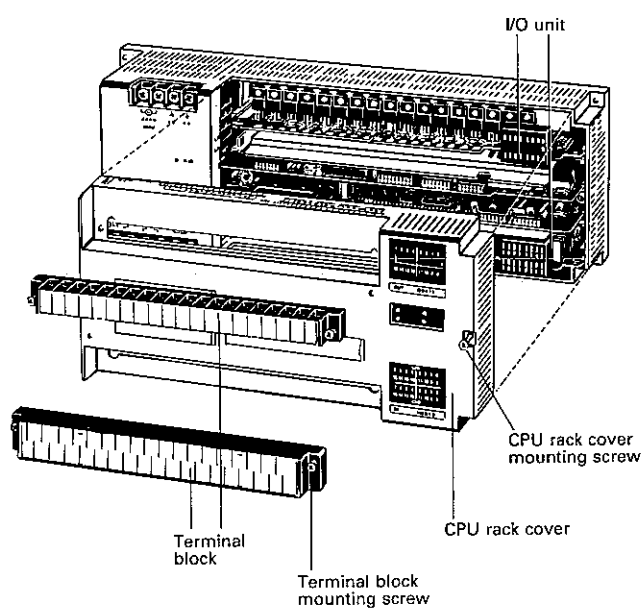
REPLACEMENT OF FUSE

1. Turn off the power.
2. Remove the terminal block cover from the power supply.
3. Remove the cover from the power supply.
4. Replace the fuse with a new one.



REMOVAL OF I/O UNIT

1. Turn off the power.
2. Loosen the terminal block mounting screws and remove the terminal block connector.
3. Remove the CPU rack-cover mounting screws to remove the CPU rack cover.
4. Remove the I/O units. In doing so, do not hold the LED section of the I/O unit by hand.



6.3 ABNORMAL SYMPTOM, POSSIBLE CAUSE, AND CORRECTIVE ACTION

CPU RACK

No.	Abnormal symptom	Possible cause	Corrective action
1	Fuse blows repeatedly.	Pattern is short-circuited or damaged by burning.	Replace CPU rack.
2	DC voltage output failure	Constant voltage circuit is defective.	Replace CPU rack.
3	"RUN output" contact does not turn ON. (RUN indicator ON)	(1) Power circuit is defective.	Replace CPU rack.
4	RUN indicator does not illuminate.	(1) DC voltage is not supplied. (2) Programming error (END instruction is missing.)	Replace CPU rack. Correct program.

EXPANSION I/O RACKS

No.	Abnormal symptom	Possible cause	Corrective action
1	Operation is not executed after specific relay No.	(1) Pattern is broken.	Check each bus line by buzzer.
		(2) Improper soldering	Resolder.
2	Abnormal relay Nos. of expansion I/O rack are in units of 8.	(1) Cable wiring is broken.	Check each bus line by buzzer.
		(2) Improper soldering	Resolder.
3	I/O of a specific relay No. turns on.	(1) Improper soldering of connector	Check each bus line by buzzer.
4	All the relays of a specific I/O unit do not operate.	(1) Same as above	Check each bus line by buzzer.

INPUT UNITS

No.	Abnormal symptom	Possible cause	Corrective action
1	All input units do not turn on.	• Operation indicators (LEDs) are not illuminating. (1) External input voltage is not supplied or is low. • Operation indicators (LEDs) are illuminating. (1) Signal level within unit is faulty.	Supply the power. Raise the supply voltage. Remove all the I/O units being used and insert them one by one to find the defective unit.
2	All of specific input units do not turn on.	(1) Same as above	Same as above. Replace defective input unit.
		(2) Screws of terminal board are loose.	Retighten terminal screws.
3	All of specific input units do not turn off.	(1) Gate circuit is defective.	Replace defective input unit.
		(2) External voltage is not supplied.	Apply the external power supply.
4	Input of a specific relay No. does not turn on.	(1) Gate circuit is defective.	Replace defective input unit.
		(2) Screws of terminal board are loose.	Retighten screw terminals.
		(3) ON time duration of external input is short.	Adjust external device.
		(4) Input circuit (photocoupler, for example) is defective.	Replace defective input unit.
		(5) Input relay No. is incorrectly assigned to the OUT instruction of the program.	Correct the program.
5	Input of a specific relay No. does not turn off.	(1) Contact of jack is defective.	Clean the contact part with alcohol-moistened cloth.
		(2) Input circuit is defective.	Replace defective unit.
		(3) Input relay No. is incorrectly assigned to the OUT instruction of the program.	Correct the program.
6	Relay No. of abnormal operation is in units of 8. (Example) 0000, 0010, 0020	(1) Data bus signal is faulty. (2) IC-RAM of CPU is defective.	Remove all I/O units being used and insert them one by one to find the defective unit.
7	Inputs turn ON and OFF irregularly.	(1) External input voltage is low.	Raise the external voltage.
		(2) Malfunction due to noise.	Countermeasures against noise. • Install a surge suppressor. • Install an insulating transformer. • Wiring with a shielded cable
8	Input operation indicator does not illuminate. (Operation is normal.)	(1) LED indicator is defective.	Since this type of defect does not impede normal operation, repair it in spare time or at the next periodic inspection.

OUTPUT UNITS

No.	Abnormal symptom	Possible cause	Corrective action
1	All output units do not turn on.	(1) Load power supply is not applied.	Apply the load power supply. (Raise the voltage.)
		(2) Signal level within unit is defective.	Remove all the I/O units being used and insert them one by one to find the defective unit.
2	All of specific output units do not turn on.	(1) Same as 1(1).	Same as above.
		(2) Screws of terminal board are loose.	Retighten screw terminals.
		(3) Contact of jack is defective.	Clean the contact with alcohol-moistened cloth.
		(4) Fuse is blown.	Replace defective fuse.
		(5) Internal circuit is defective.	Replace defective unit.
3	All of specific output units do not turn off.	(1) Contact of jack and connector is defective.	Clean with alcohol-moistened cloth.
		(2) Gate circuit is defective.	Replace defective unit.
4	Output of a specific relay No. does not turn on.	• Operation indicator (LED) is not illuminating. (1) ON time duration of output is short. (2) Relay Nos. of the OUT instruction in the program are in duplication. (3) Power circuit is defective.	 Correct the program. Correct the program. Replace defective unit.
		• Operation indicator (LED) is illuminating. (1) Broken connection of external load (2) Screws of terminal board are loose. (3) Pattern is broken.	 Replace defective external load. Retighten screw terminals. Replace defective unit.
5	Output of specific relay No. does not turn off.	• Operation indicator (LED) is not illuminating. (1) Improper reset due to leakage current or saturation voltage.	 Replace defective external load or add a dummy resistor.
		• Operation indicator LED is not illuminating. (1) Contact of jack is defective (bus line) (2) Relay Nos. of OUT instruction in the program are in duplication. (3) Power circuit is defective.	 Clean with alcohol-moistened cloth. Correct the program. Replace defective unit.
6	Relay No. of abnormal operation is in units of 8. (Example) 0020, 0030	(1) Data bus signal is faulty.	Remove all the I/O units being used and insert them one by one to find the defective unit.
		(2) IC-RAM of CPU is defective.	Replace CPU rack.
7	Outputs turn on and off irregularly.	(1) Supply voltage of external load is low.	Raise the external supply voltage.
		(2) Relay Nos. of OUT instruction in the program are in duplication.	Correct the program.
		(3) Malfunction due to noise	Countermeasures against noise • Install a surge suppressor. • Install an insulating transformer. • Wiring with a shielded cable.
8	Output operation indicator does not illuminate. (Operation is normal.)	(1) LED indicator is defective.	Since this type of defect does not impede normal operation, repair it in spare time or at the next periodic inspection.

6.4 DIAGNOSTIC FUNCTIONS

The PC was manufactured with a consistent design philosophy supported by advanced technology for high-density packaging or PC components under stringent quality control. The PC is capable of minimizing the system's downtime should a failure occur in the PC, because it is provided with various diagnostic functions.

Abnormal ... Diagnostic functions for hardware (CPU, I/O unit, remote I/O, for example)

Alarm ..... System diagnosis

These abnormal statuses can be monitored by messages and FAL numbers displayed on the LCD of the programming console.

In addition, the PC has special auxiliary relays, some of which are assigned for abnormal status output. These relays provide the PC flexible countermeasures against failures, because by the user program written to output FAL numbers in these relays, the system (CPU) operation can be stopped or continued as desired in the event of a system failure.

LIST OF ERROR MESSAGES AND ALARM OUTPUTS

	Item	Description	LED indicators on CPU front panel				
			POWER	RUN	ERR	ALARM	OUT INH
–	Remote power ON wait	Remote power is OFF state.	☒	o	–	–	–
	Start input wait	START INPUT terminal is open.	☒	o	–	–	–
A failure that causes the CPU to stop	Power failure	Power failure has occurred longer than 10ms.	o	o	o	o	o
	CPU failure	Watchdog timer (130msec min)	☒	o	☒	–	–
	Memory error	Sum check or incorrect instruction exists.	☒	o	☒	–	–
	End missing error	END instruction is missing at the end of program.	☒	o	☒	–	–
	I/O bus error	Error is detected during data transfer between CPU and I/O unit.	☒	o	☒	–	–
	I/O unit over error	The number of I/O points mounted in excess of 512 is detected as error.	☒	o	☒	–	–
	I/O setting error	Input unit is replaced with output unit or vice versa.	☒	o	☒	–	–
	System failure	FALS instruction is executed by software causing the CPU to stop.	☒	o	☒	–	–
A failure that does not cause the CPU to stop	Remote I/O error	Error is detected during data transmission between remote I/O main and sub units.	☒	–	–	☒	–
	I/O verify error	I/O units are removed.	☒	–	–	☒	–
	System failure	FAL instruction is executed by software that does not cause the CPU to stop.	☒	☒	–	☒	–
	Battery error	Low battery voltage, or no battery is inserted.	☒	–	–	☒	–
–	Output inhibit input ON	Special auxiliary relay (6015) is ON state.	☒	–	–	–	☒
	Scan time over	Watchdog timer (100ms max. and less than 130ms)	☒	☒	–	☒	–

☒: denotes that the indicator illuminates.
o : denotes that the indicator goes off.
These examples of LED indicator are while the PC is in operation.

Message on programming console display	Special auxiliary relay	Failure code	Remedy
CPU WAITG			Turn ON power of remote I/O units.
CPU WAITG			Short-circuit START input terminal.
			Apply power again.
			Set mode selector switch to PROGRAM position and turn off power. Check program.
MEMORY ERR		F1	Confirm mounting or RAM or ROM memory unit. Correct <????> in program. After correction, failure resetting operation must be performed.
NO END INSTR		F0	Write END instruction and then reset failure.
I/O BUS ERR		C0 to C3*	Check bus line between PC and I/O unit. Confirm secure mounting of I/O unit or expansion I/O rack when power is applied.
I/O UNIT OVER		E1	Confirm I/O channels by reading I/O table and then reassign I/O channels. After reassignment, generate I/O table.
I/O SET ERR		E0	Confirm I/O channels by performing I/O verify operation, and then reassign I/O channels. After reassignment, generate I/O table.
SYS FAIL FALS		1 to 99	Check program.
RMTE I/O ERR	6112 ON	B0 to B3**	Check transmission line between PC and remote I/O slave unit. Check remote I/O slave unit for normal operation.
I/O VER ERR	6110 ON	E7	Confirm I/O channels by performing I/O verify operation, and then reassign I/O channels. After reassignment, generate I/O table.
SYS FAIL FAL		1 to 99	Check program.
BATT LOW	6108 ON	F7	Check connector of battery for loose connection. Replace battery with new one.
SCAN TIME OVER	6109 ON	F8	Check program.

NOTES: * 0 to 3 denote rack numbers.
** 0 to 3 denote remote numbers.

CHAPTER 7
SPECIAL I/O UNITS

7.1 AVAILABLE TYPES

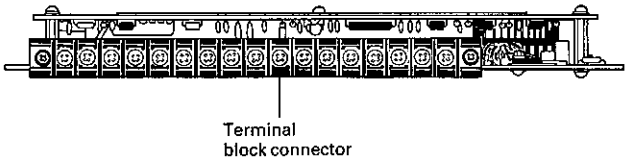
Classification		Specifications	Power supply voltage	Weight	Type
A/D conversion input unit	2-channel	+1 to +5V, +4 to +20mA	—	600g max.	3G2A6-AD001
		0 to +10V	—	600g max.	3G2A6-AD002
		0 to +5V	—	600g max.	3G2A6-AD003
		−10 to +10V	—	600g max.	3G2A6-AD004
		−5 to +5V	—	600g max.	3G2A6-AD005
	4-channel	+1 to +5V, +4 to +20mA	—	650g max.	3G2A6-AD006
		0 to 10V	—	650g max.	3G2A6-AD007
D/A conversion output unit (assigned to two channels of PC)		+1 to +5V, +4 to +20mA	—	600g max.	3G2A6-DA001
		0 to +10V	—	600g max.	3G2A6-DA002
		0 to +5V	—	600g max.	3G2A6-DA003
		−10 to +10V	—	600g max.	3G2A6-DA004
		−5 to +5V	—	600g max.	3G2A6-DA005
High-speed counter unit (assigned to four channels of PC)			—	700g max.	3G2A6-CT001-E
Remote I/O master unit			—	500g max.	3G2A6-RM001-E
Remote I/O slave unit	1:1	With one fiber optics connector for connecting only one slave unit to master unit	—	500g max.	3G2A5-RT001-E
	1:2	With two fiber optics connectors for connecting two slave units to master unit	—	500g max.	3G2A5-RT002-E
Optical transmitting I/O unit	Input unit	Nonvoltage contact, 10mA, 8 points	AC 110/120V	580g max.	3G5A2-ID001-E
			AC 220/240V	580g max.	3G5A2-ID002-E
		AC/DC 12 to 24V, 10mA, 8 points	AC 110/120V	580g max.	3G5A2-IM211-E
			AC 220/240V	580g max.	3G5A2-IM212-E
		AC 110/120V, 10mA, 8 points	AC 110/120V	580g max.	3G5A2-IA121-E
		AC 220/240V, 10mA, 8 points	AC 110/120V	600g max.	3G5A2-IA221-E
			AC 220/240V	600g max.	3G5A2-IA222-E
	Output unit	Relay contact, AC 250/DC 24V, 2A, 8 points	AC 110/120/220/240V	600g max.	3G5A2-OC221-E
		Triac, AC 85 to 250V 1A, 8 points		600g max.	3G5A2-OA222-E
		Transistor, DC 12 to 48V, 0.3A, 8 points		600g max.	3G5A2-OD411-E
Fiber optics cable		0.1m-long with connector (used commonly for optical transmitting I/O unit)	—	20g max.	3G5A2-OF011
		1m-long with connector (used commonly for optical transmitting I/O unit)	—	40g max.	3G5A2-OF101
		2m-long with connector (used commonly for optical transmitting I/O unit)	—	60g max.	3G5A2-OF201
		3m-long with connector (used commonly for optical transmitting I/O unit)	—	80g max.	3G5A2-OF301
		5m-long with connector (used commonly for optical transmitting I/O unit)	—	120g max.	3G5A2-OF501
		10m-long with connector (used commonly for optical transmitting I/O unit)	—	220g max.	3G5A2-OF111
		20m-long with connector (used commonly for optical transmitting I/O unit)	—	420g max.	3G5A2-OF211
		30m-long with connector (used commonly for optical transmitting I/O unit)	—	620g max.	3G5A2-OF311
		50m-long with connector (used commonly for optical transmitting I/O unit)	—	1kg max.	3G5A2-OF511

MOUNTING POSITIONS OF I/O UNIT ON CPU RACK/EXPANSION I/O RACK

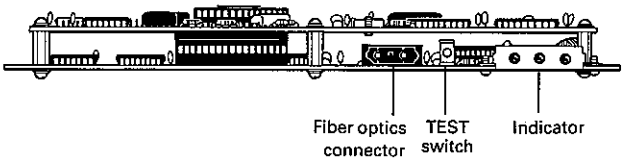
Rack	Mounting position	UNIT 0 position (lower position)	UNIT 1 position (upper position)
CPU rack	3G2C4-SC023-E 3G2C4-SC024-E 3G2C4-SC021-E 3G2C4-SC022-E	Basic input unit	Basic input unit Basic output unit
Expansion I/O rack	3G2C4-SI021 3G2C4-SI022	Basic input unit Basic output unit	Basic input unit Basic output unit
	3G2C4-SI023 3G2C4-SI024	Basic input unit Basic output unit	I/O link unit
	3G2C4-SI025 3G2C4-SI026	Basic input unit Basic output unit	A/D conversion input unit D/A conversion output unit High-speed counter unit
	3G2C4-SI027 3G2C4-SI028	Basic input unit Basic output unit	Remote I/O master unit

7.2 NAMES OF PARTS

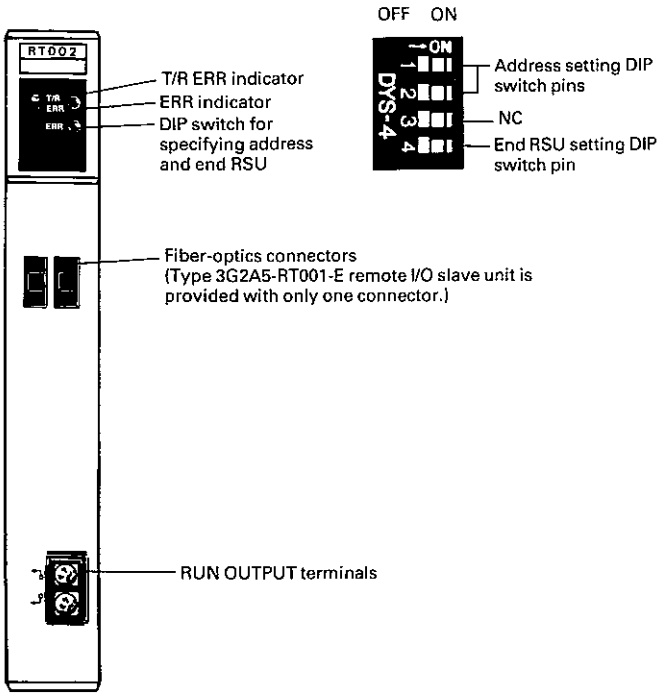
7.2.1 A/D conversion input unit (Type 3G2A6-AD00□)/D/A conversion output unit (Type 3G2A6-DA00□)/High-speed counter input unit (Type 3G2A6-CT001-E)



7.2.2 Remote I/O master unit (Type 3G2A6-RM001-E)



7.2.3 Remote I/O slave unit (Type 3G2A5-RT002-E/-RT001-E)



INDICATORS

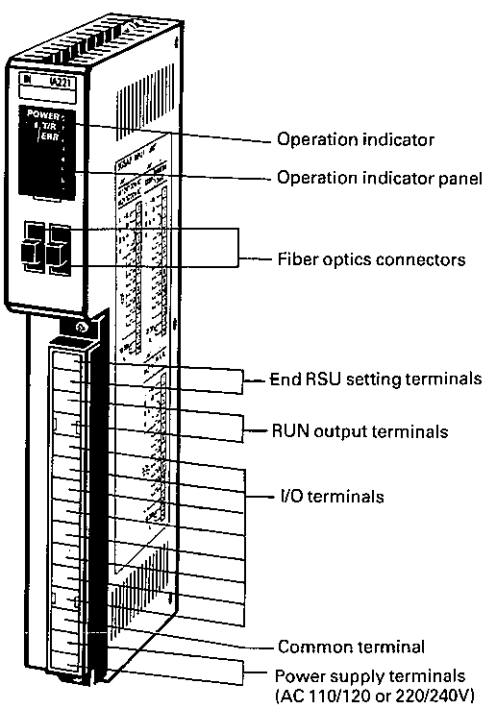
	Name of indicator	Function
Master/ slave unit	☼ T/R ● ERR	Blinks (☼) during normal data transmission and lights up (●) when a transmission error occurs.
Master unit	● TEST ○ OK	Lights up (●) if the transmission line is normal and does not (○) if it is abnormal when the transmission line is tested by using the TEST switch. This test can be repeatedly conducted while the TEST switch is being held down, but the TEST OK indicator goes out if a failure in the transmission line is detected.
	● END ○ RS CHK	Lights up (●) if no end RSU is found and does not (○) if the end RSU is found.
Slave unit	● I/O ERR	Lights up (●) when a failure occurs in the I/O bus of the slave unit or when the input or output to/from the slave unit is incorrectly recognized by the programmable controller.

CONTROLS

	Name of parts	Function
Master unit	TEST switch	Tests the transmission for normal operation repeatedly while this switch is being held down when the programmable controller is in the PROGRAM mode.
Slave unit	Address/ END station setting DIP switch	Nos. 1 and 2 pins of this DIP switch specifies the address of the remote I/O slave unit. No. 4 pin specifies the end RSU. No. 3 pin is independent.
	RUN OUTPUT	Turns ON when no transmission error occurs with the programmable controller in the RUN or MONITOR mode and turns OFF under other conditions (e.g., when the programmable controller is in the PROGRAM mode or when a transmission error occurs with the controller in the RUN or MONITOR mode).

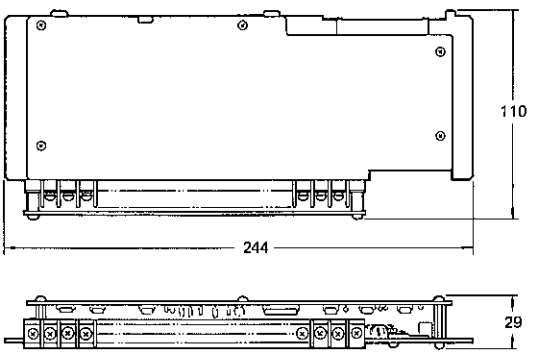
7.2.4 Optical transmitting I/O unit

3G5A2-ID00□-E/-IM21□-E/-IA□□□-E/-OC221-E/ -OA221-E/-OD411-E



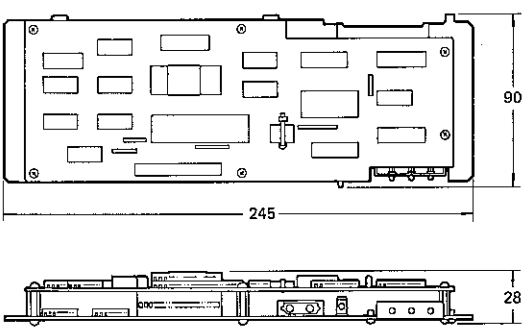
7.3 DIMENSIONS

7.3.1 A/D conversion input unit (3G2A6-AD00□)/ D/A conversion output unit (3G2A6-DA00□)/ High-speed counter unit (3G2A6-CT001-E)

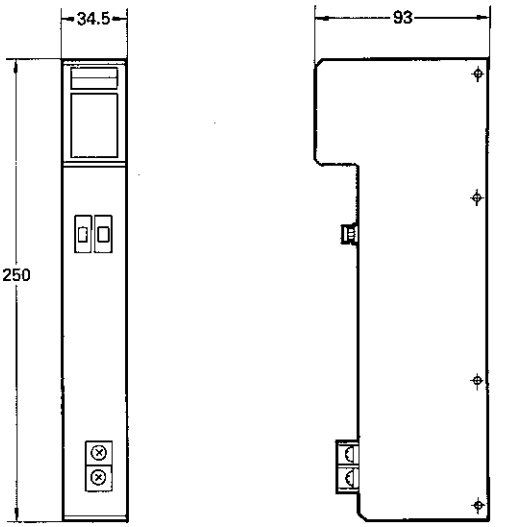


7.3.2 Remote I/O units

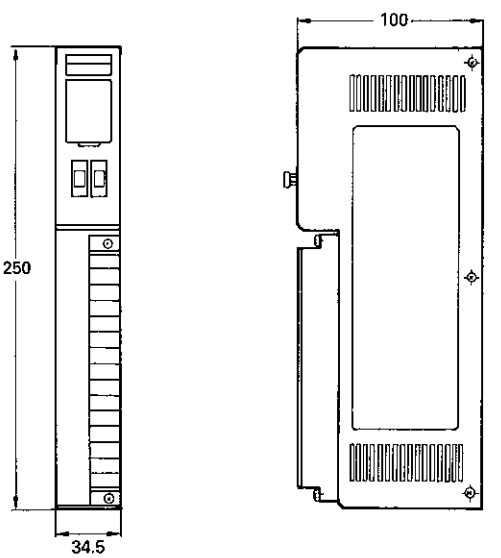
Remote I/O master unit (3G2A6-RM001-E)



Remote I/O slave unit (3G2A5-RT00□-E)



7.3.3 Optical transmitting I/O unit (3G5A2-ID00□-E/-IM21□-E/-IA□□□-E/ -OC221-E/-OA221-E/-OD411-E)



7.4 A/D CONVERSION INPUT UNIT

The A/D conversion input units available are broadly divided into two types by the number of channels: 2-channel type and 4-channel type.

The 2-channel type A/D conversion input unit is capable of converting an analog input signal into a 12-bit binary data.

Various input signal ranges are available. For voltage input, the signal range can be 0 to +10V, 0 to +5V, +1 to +5V, −5 to +5V, or −10 to +10V. For current input, a signal range of +4 to +20mA is available.

This type of A/D conversion input unit has identical circuitry for each of the two channels (Line 1 and Line 2).

The 4-channel type A/D conversion input unit converts an analog input signal into 10-bit binary data. For voltage input, the signal range can be 0 to +10V or 1 to +5V. For current input, the signal range is +4 to +20mA.

This type of A/D conversion input unit has identical circuitry for each of the four channels (Lines 1 to 4).

7.4.1 Specifications

CHARACTERISTICS

Input channel	2 channels	4 channels
External input range *1	Voltage input: 0 to +10V 0 to +5V +1 to +5V −5 to +5V −10 to +10V	Voltage input: 0 to +10V +1 to +5V
	Current input: +4 to +20mA	
External input impedance	Voltage input: 1MΩ min.	
	Current: 250Ω	
Resolution	1/4,095 of full scale	1/1,023
Output signal to SYSMAC-C Series *2	Binary 12 bits	Binary 10 bits
Linearity	±0.1% max.	±0.2% max.
Accuracy	±0.2% max. of full scale (at 25°C)	
Temp. coefficient	±100PPM/°C of full scale	±150PPM/°C of full scale
Conversion time	2.5ms/point max.	
Conversion cycle	5ms max.	10ms max.
Conversion mode	Sequential comparison	
Max. permissible external input	Voltage input: ±15V max.	
	Current input: ±60mA max.	
Terminal for external connection	Terminal block (cannot be dismounted)	
Internal power supply	+5V, 300mA max.	+5V, 750mA max.
Weight	600g max.	650g max.

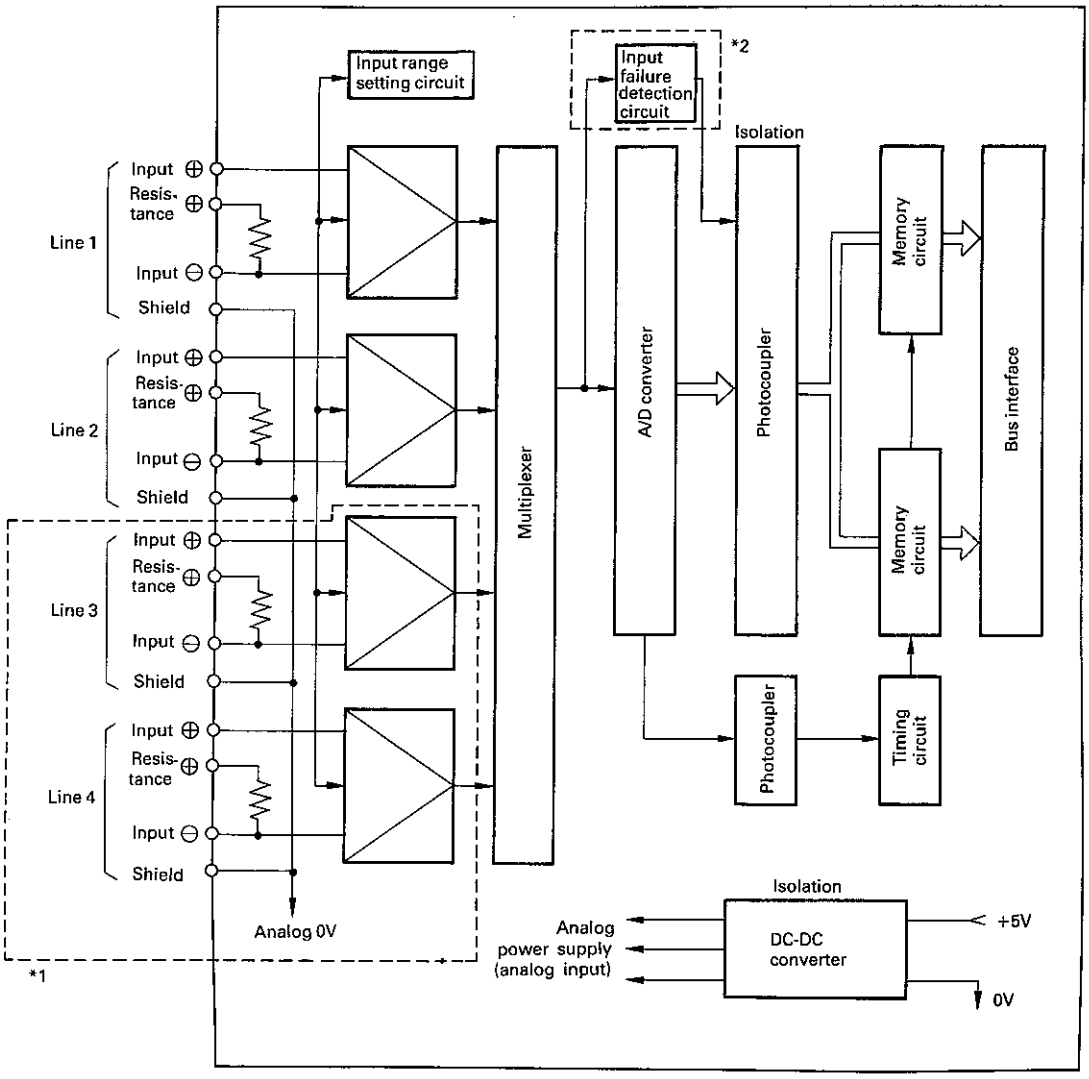
*1: Select and use the type with a desired input signal range by referring to 7.1, Available types.
The current input function is provided to only Types 3G2A6-AD001 and 3G2A6-AD006, whose voltage input ranges are both +1 to +5V.

*2: An input analog signal is converted into a 12-bit binary data consisting of a sign bit and 11-bit data when the A/D conversion input unit (2-channel type only) with input signal range of −5 to +5V or −10 to +10V is used.

NOTES:

1. Connect the A/D conversion input unit to the SYSMAC-C250 via an expansion I/O rack of either the SYSMAC-C120 or SYSMAC-C500.
2. Insert the A/D conversion input unit to the upper slot of an expansion I/O rack when mounting the unit to the SYSMAC-C120.
3. To mount the unit to the SYSMAC-C120, use Type 3G2C4-SI025 or 3G2C4-SI026.

7.4.2 Block diagram



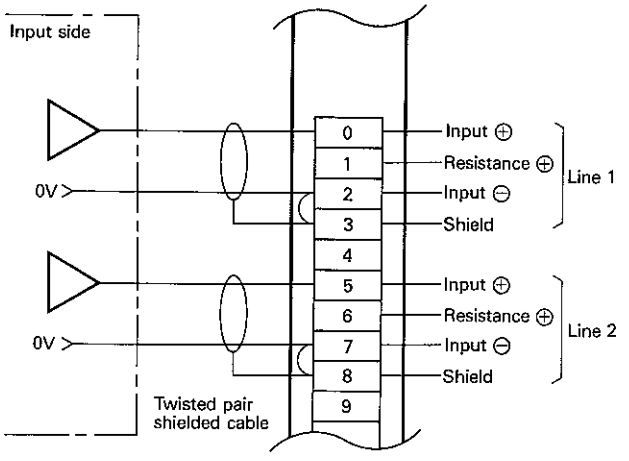
*1 The circuitry for these two lines are not provided to the 2-channel type A/D conversion input unit.
*2 The input failure detection circuit is not provided to the 4-channel type A/D conversion input unit.
NOTE: An input failure is detected by only Type 3G2A6-AD001 (+1 to +5 for voltage input or +4 to +20mA for current input.)

7.4.3 External connection diagram

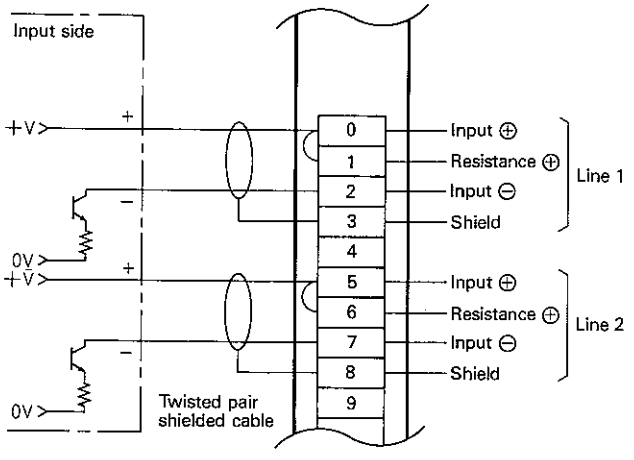
2-CHANNEL TYPE

- Connection for voltage input

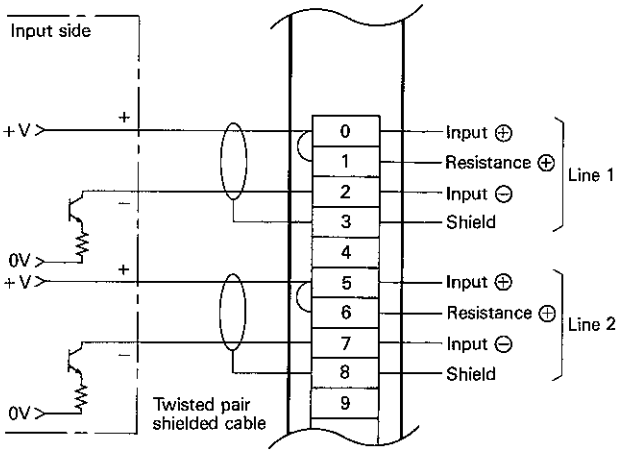
1. When the signal is a common mode input



2. When the signal is a differential output



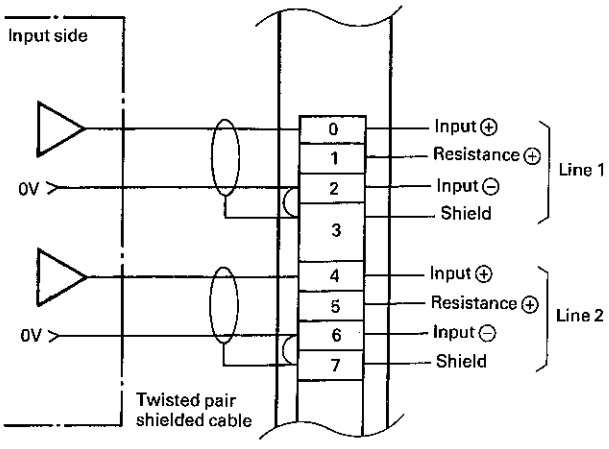
- Connection for current input



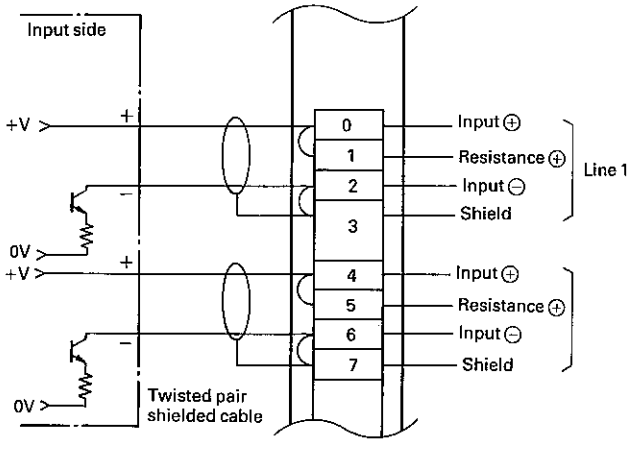
NOTES: 1. Be sure to use a twisted pair shielded cable for input.
2. Short-circuit the Shield, Input ⊕, and Input ⊖ terminals of the circuit that is not used.

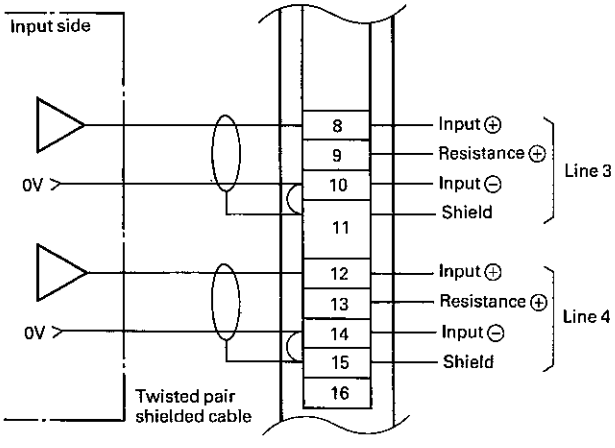
4-CHANNEL TYPE

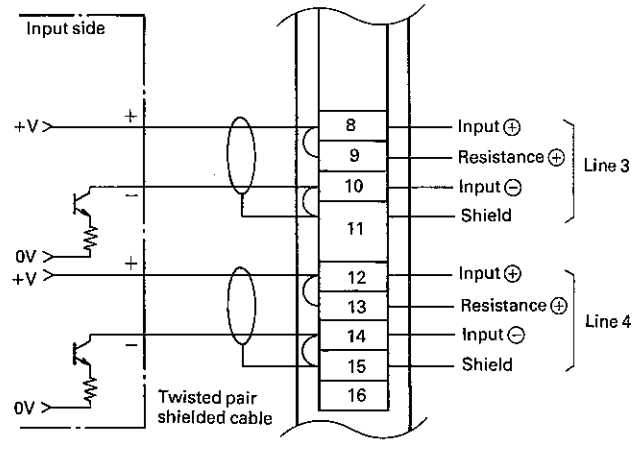
- Connection for voltage input



- Connection for current input







NOTES: 1. Be sure to use a twisted pair shielded cable for input.
2. Short-circuit the Shield, Input ⊕, and Input ⊖ terminals of the circuit that is not used.

7.4.4 Assignment of relay number (Output from A/D conversion input unit)

2-CHANNEL TYPE

Channel No. / Bit No.	nCH	n+1 CH	
0	A/D converted data 2^0	A/D converted data 2^0	
1	A/D converted data 2^1	A/D converted data 2^1	
2	A/D converted data 2^2	A/D converted data 2^2	
3	A/D converted data 2^3	A/D converted data 2^3	
4	A/D converted data 2^4	A/D converted data 2^4	
5	A/D converted data 2^5	A/D converted data 2^5	
6	A/D converted data 2^6	A/D converted data 2^6	
7	A/D converted data 2^7	A/D converted data 2^7	
8	A/D converted data 2^8	A/D converted data 2^8	
9	A/D converted data 2^9	A/D converted data 2^9	
10	A/D converted data 2^{10}	A/D converted data 2^{10}	
11	A/D converted data 2^{11}	A/D converted data 2^{11}	*
12	0	0	
13	0	0	
14	0	0	
15	0	0	**
	Line 1 input	Line 2 input	

NOTES:
* Bit No. 11 is used as either an A/D converted data or the sign bit. When used as the sign bit, the level of this bit becomes "1" when the level of the input signal is high and becomes "0" when the level of the input signal is low.
** Bit No. 15 of Type 3G2A6-AD001 A/D conversion I/O input unit (+1 to +5V for voltage input or +4 to +20mA for current input) detects an input failure. The level of this bit becomes "1" when an input failure occurs and remains "0" during normal operation of the unit.
The signal level of bit No.15 of other A/D conversion input units remains "0".

4-CHANNEL TYPE

Channel No. / Bit No.	n CH	n+1 CH	n+2 CH	n+3 CH
0	A/D converted data 2^0	A/D converted data 2^0	A/D converted data 2^0	A/D converted data 2^0
1	A/D converted data 2^1	A/D converted data 2^1	A/D converted data 2^1	A/D converted data 2^1
2	A/D converted data 2^2	A/D converted data 2^2	A/D converted data 2^2	A/D converted data 2^2
3	A/D converted data 2^3	A/D converted data 2^3	A/D converted data 2^3	A/D converted data 2^3
4	A/D converted data 2^4	A/D converted data 2^4	A/D converted data 2^4	A/D converted data 2^4
5	A/D converted data 2^5	A/D converted data 2^5	A/D converted data 2^5	A/D converted data 2^5
6	A/D converted data 2^6	A/D converted data 2^6	A/D converted data 2^6	A/D converted data 2^6
7	A/D converted data 2^7	A/D converted data 2^7	A/D converted data 2^7	A/D converted data 2^7
8	A/D converted data 2^8	A/D converted data 2^8	A/D converted data 2^8	A/D converted data 2^8
9	A/D converted data 2^9	A/D converted data 2^9	A/D converted data 2^9	A/D converted data 2^9
10	0	0	0	0
11	0	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	0	0	0	0
	Line 1	Line 2	Line 3	Line 4

7.4.5 Input signal and converted data

The A/D conversion input unit is capable of converting an analog input signal into a digital data.

Note that five types of units are available and that their input signal ranges are different from each other.

In terms of input signal, two types of analog input signals are available; one is a unipolar signal input only to the + terminal of the unit, and the other is a bipolar signal input to both the + and − terminals. The resolution differs depending on which input signal range is employed.

UNIPOLAR INPUT SIGNAL

- Input range
  2-channel type: 0 to +10V, 0 to +5V, +1 to +5V, or +4 to 20mA
  4-channel type: 0 to +10V, +1 to +5V, or +4 to 20mA
- Converted output
  2-channel type: A/D converted, 12-bit binary data
  4-channel type: A/D converted, 10-bit binary data

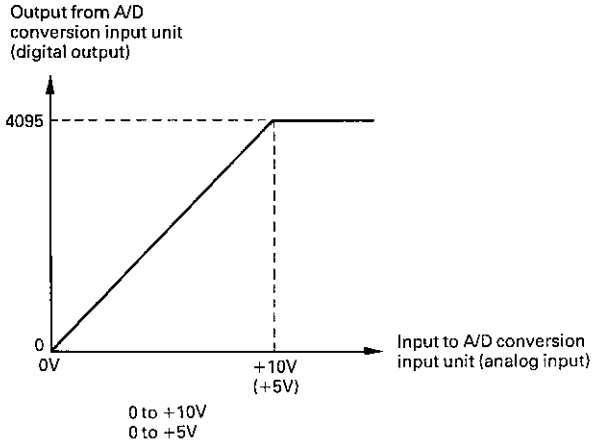
NOTE:

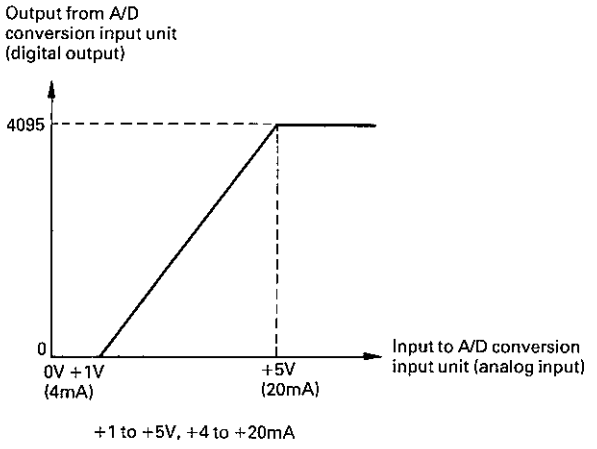
Bit No. 15 of Type 3G2A6-AD001 (+1 to +5V for voltage output or +4 to +20mA for current output) is an input failure detection bit.

The level of this bit becomes "1" when an input failure occurs and becomes "0" during normal operation.

If the voltage input signal decreases below +0.5V, or if the current input signal decreases below +2mA, an input failure is detected and therefore, the level of bit No. 15 becomes "1".

- Relation between analog input signal and A/D converted data





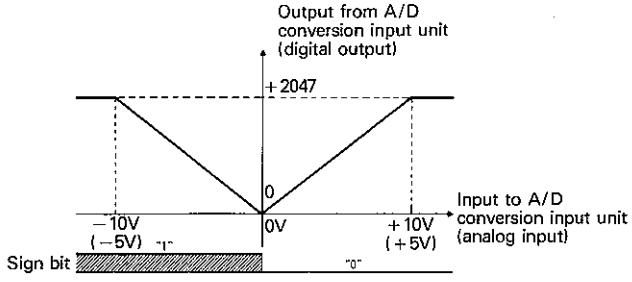
BIPOLAR INPUT SIGNAL (only for 2-channel type)

- Input range: −5 to +5V or −10 to +10V
- Converted output: Sign bit (1 bit) and A/D converted, 11-bit binary data

NOTES:

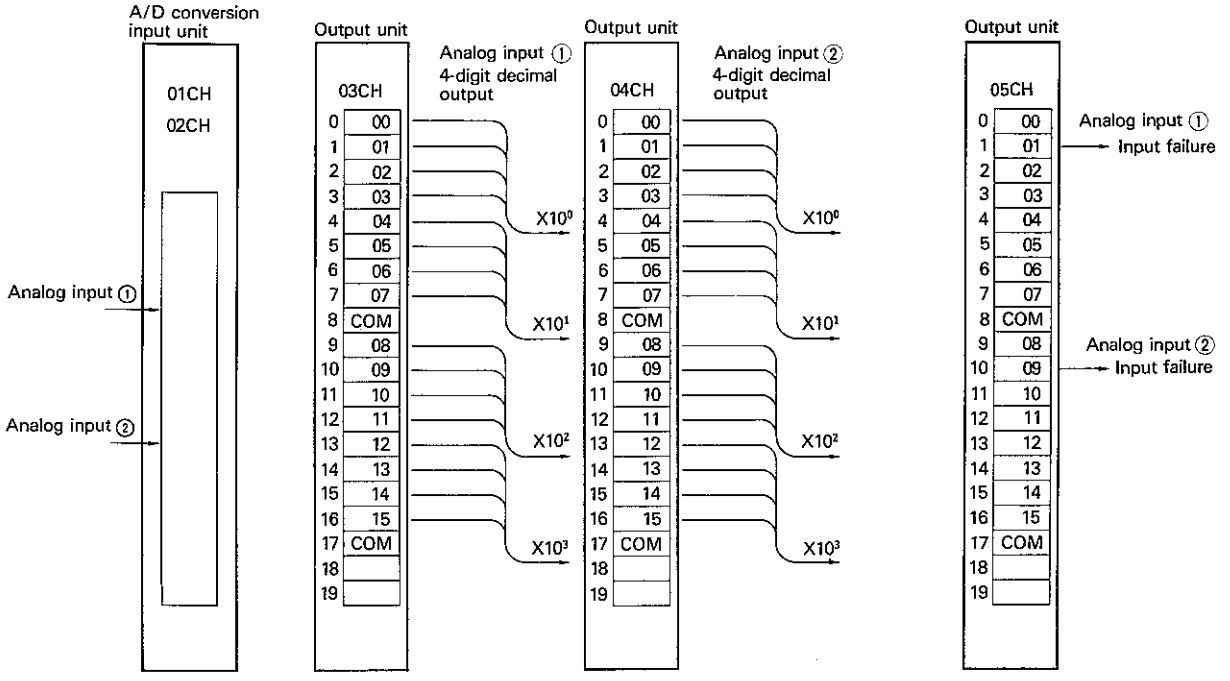
1. Bit No. 11 is the sign bit. The level of this bit becomes "0" when the analog signal input to the A/D conversion input unit is positive and becomes "1" when a negative analog signal is input.
2. Conversion code: Sign magnitude method.

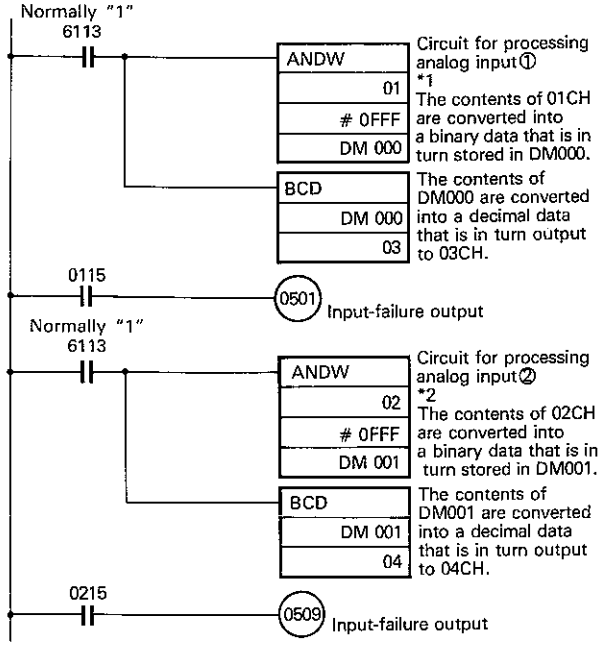
- Relation between analog input signal and A/D converted data



7.4.6 Programming example

In this example, two types of analog signals are input to the A/D conversion input unit from external devices and are converted by the unit into decimal 4 digits (less than 4095).





NOTE: Data are output from the A/D conversion input unit in increments of 16 bits. Because a Sign bit is output from the unit in addition to the A/D converted data, only the converted data are fetched into the CPU by program steps *1 and *2 above.

7.5 D/A CONVERSION OUTPUT UNIT

The D/A conversion output unit is capable of converting a 12-bit binary data from a SYSMAC-C Series programmable controller into an analog output signal. A wide variation of output signal ranges are available:
0 to +10V, 0 to +5V, +1 to +5V, −10 to +10V, −5 to +5V for voltage output and +4 to +20mA for current output.
The D/A conversion output unit has an identical circuitry for each of the two channels (Line 1 and Line 2).

7.5.1 Specifications

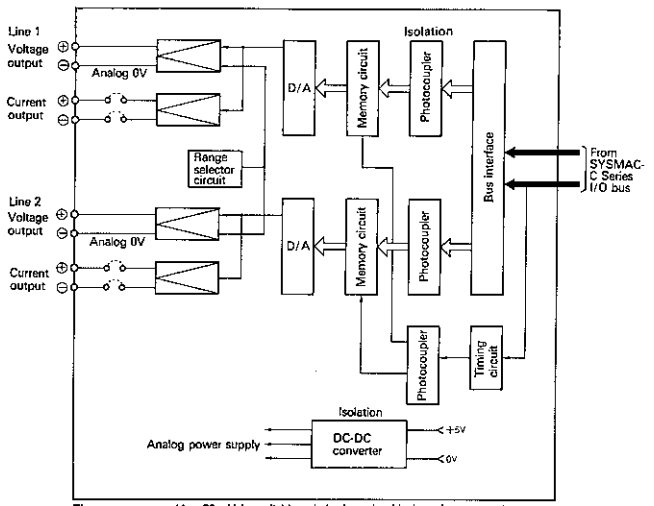
CHARACTERISTICS

No. of output points	2	
External output range *1	Voltage output:	0 to +10V 0 to +5V +1 to +5V −10 to +10V −5 to +5V
	Current output:	+4 to +20mA
External output impedance	Voltage output: 0.5Ω max.	
Max. current for external output	Voltage output: 15mA	
Permissible load resistance for external output	Current output: 550Ω max.	
Resolution	1/4,095 of full scale	
Input signal from SYSMAC-C Series *2	Binary 12 bits	
Linearity	±1/2 LSB max. at 25°C	
Accuracy	±0.2% max. of full scale at 25°C	
Temp. coefficient	±50PPM/°C	
Conversion time	5ms max.	
Conversion cycle	Program execution cycle of SYSMAC-C Series	
Terminal for external connection	Terminal block (cannot be dismounted)	
Internal power supply	+5V, 550mA max.	
Weight	600g max.	

*1: Specify the external output range when placing your order (refer to 7.1, Available types). Current output is available only in Type 3G2A6-DA001 whose voltage output range is +1 to +5V.
*2: The binary code output from the types with the voltage output ranges consists of 1 sign bit and 11 bits.

NOTES:
1. Connect the D/A conversion output unit to the SYSMAC-C250 via an expansion I/O rack of either the SYSMAC-C120 or SYSMAC-C500.
2. Insert the D/A conversion output unit to the upper slot of an expansion I/O rack when mounting the unit to the SYSMAC-C120.
3. To mount the unit to the SYSMAC-C120, use Type 3G2C4-SI025 or 3G2C4-SI026.

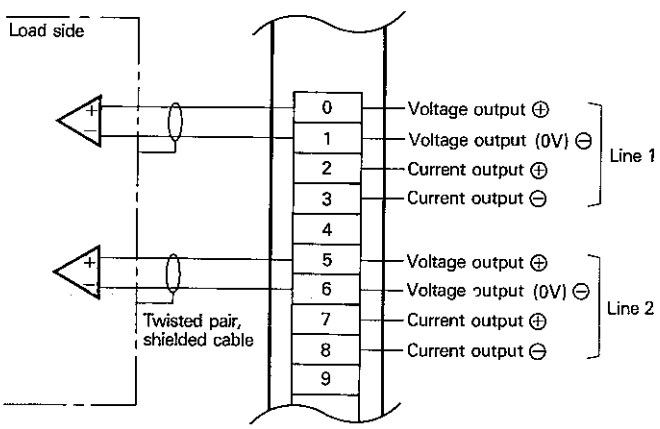
7.5.2 Block diagram



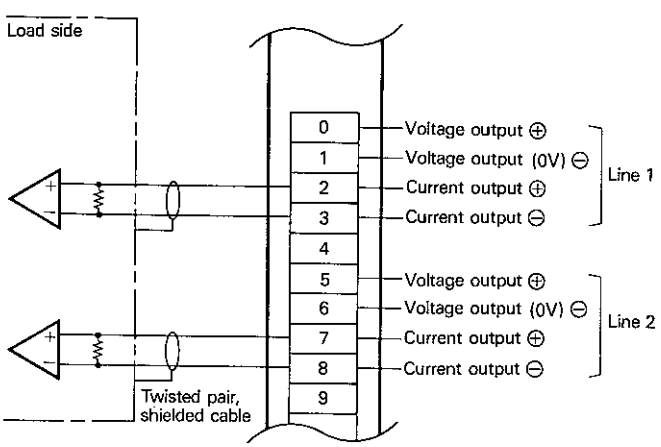
The current output (4 to 20mA) is available only in the unit with the voltage output range +1 to +5V. The terminal for the current output of the unit with the other voltage range is therefore opened.

7.5.3 External connection diagram

CONNECTION FOR VOLTAGE OUTPUT



CONNECTION FOR CURRENT OUTPUT



NOTES: 1. Be sure to use a twisted pair shielded cable for external output connection.
2. Use the shielded cable at the load side for both current and voltage outputs.

7.5.4 Assignment of relay number (inputs to D/A conversion output unit)

Channel No. / Bit No.	nCH	n+1 CH
0	D/A converted data 2^0	D/A converted data 2^0
1	D/A converted data 2^1	D/A converted data 2^1
2	D/A converted data 2^2	D/A converted data 2^2
3	D/A converted data 2^3	D/A converted data 2^3
4	D/A converted data 2^4	D/A converted data 2^4
5	D/A converted data 2^5	D/A converted data 2^5
6	D/A converted data 2^6	D/A converted data 2^6
7	D/A converted data 2^7	D/A converted data 2^7
8	D/A converted data 2^8	D/A converted data 2^8
9	D/A converted data 2^9	D/A converted data 2^9
10	D/A converted data 2^{10}	D/A converted data 2^{10}
11	D/A converted data 2^{11}	D/A converted data 2^{11}
12		
13		
14		
15		

* Line 1 input / Line 2 input

NOTES:
1. * During the D/A conversion, the contents of bits 12 to 15 are ignored. These bits can thus be used as internal auxiliary relays.
2. The function bit 11 performs changes depending on whether the unit in use is designed for unipolar output or bipolar output. That is, bit 11 of a unipolar output type unit is a D/A converted data, and bit 11 of a bipolar output type serves as a sign bit. The level of the sign bit becomes 0 when the unit outputs a negative analog signal and becomes 1 when the unit outputs a positive analog signal.

7.5.5 Operation

CONVERTED DATA AND OUTPUT SIGNAL

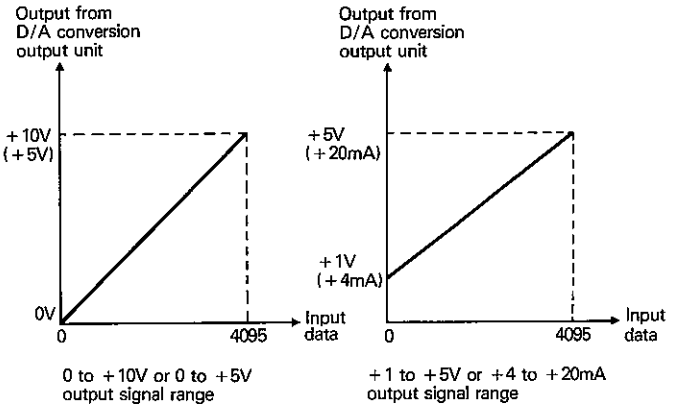
The D/A conversion output unit converts an input digital data into an analog data. It converts a 12-bit binary data output from a SYSMAC-C Series programmable controller into a voltage or a current. Five types of units with different output signal ranges are available. Make a correct choice from these five types. The converted analog signal may be output from only a positive pole of the terminals or from both the positive and negative poles, depending on the signal range of the used unit. Note that the resolution of the signal also differs depending on the signal range.

Unipolar output signal

Output range: 0 to +10V, 0 to +5V, +1 to +5V, +4 to +20mA

D/A converted data: A 12-bit binary data is input to the unit.

Relation between input digital signal and output analog signal



Note that an input binary data exceeding 12 bits (decimal 4095) cannot be converted into an analog signal.

Bipolar output signal

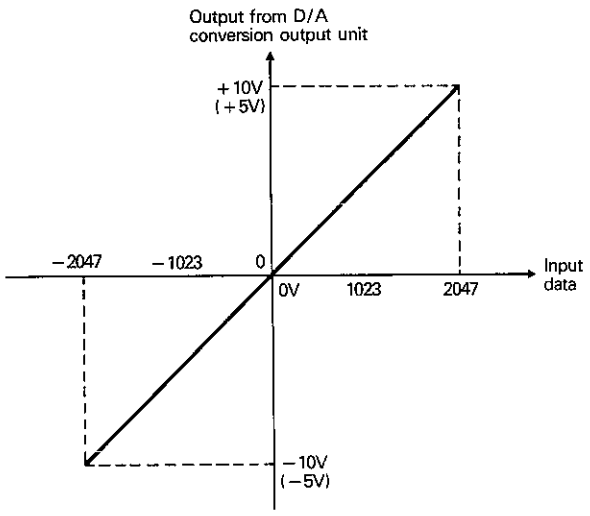
Output range: −10 to +10V, −5 to +5V

D/A converted data: A binary 11-bit data with one sign bit is input to the unit.

NOTE: Bit 11 is a sign bit. The level of this bit becomes "0" when the digital data input to the D/A conversion output unit is positive, and it becomes "1" when the input digital signal is negative.

- Relation between input digital and output analog signal

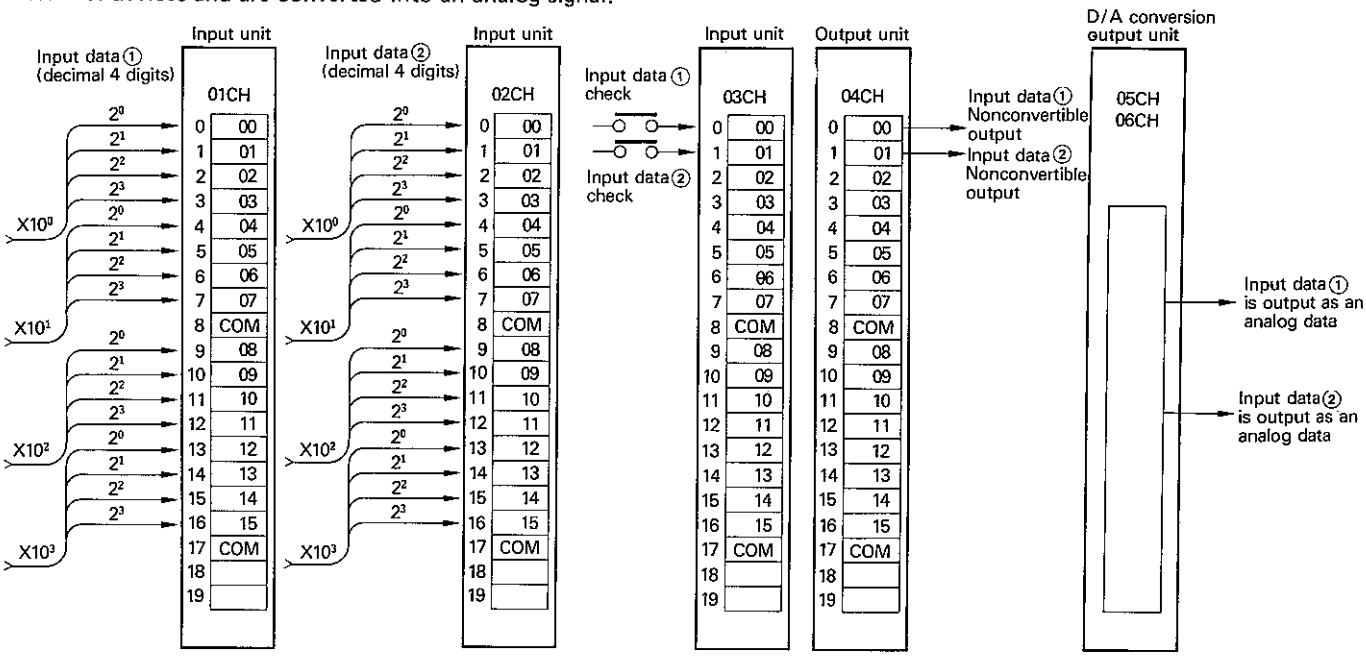
The digital data input to the D/A conversion output unit, which exceeds decimal +2048 or is less than −2048, cannot be converted into an analog signal.

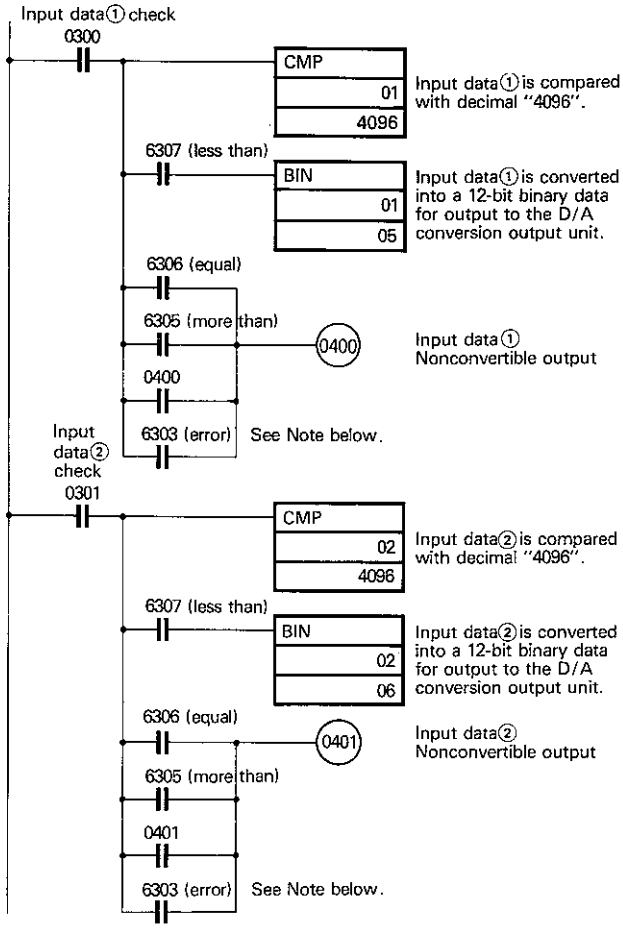


The digital data input to the D/A conversion output unit, which is in a range of decimal +2048 to +4095 (i.e., when the sign bit is 1), is treated as being in the range of decimal −1 to −2047. Therefore, the voltage output range in this case is 0 to −5V or 0 to −10V.

7.5.6 Programming examples

In this example, two types of 4-digit decimal data (less than 4095) are input to the D/A conversion output unit from external devices and are converted into an analog signal.





NOTE: Special auxiliary relay No. 6303 of a SYSMAC-C Series programmable controller serves as an error flag. The level of this flag becomes "1" if an input data is not a BCD code.

7.6 HIGH-SPEED COUNTER UNIT

The high-speed counter unit is a 6-digit-BCD high-speed reversible counter that is connected to a SYSMAC-C Series programmable controller and sensor, such as a rotary encoder, and is capable of counting clock pulses at a rate of 50K counts per second. This unit is ideal for positioning control or high-speed measurement operations and can be connected with various sensors.

7.6.1 Characteristics

Count input	Input signal *	Count input 1 Count input 2
	Voltage level of input signal	H: 6 to 12V L: 0 to 4V
	Input modes	• Command input 1/command input 2: UP/DOWN count command is to be executed by a program or count input 2 • Phase differential inputs: Specifies whether UP/DOWN count command is to be executed by the phase difference between count inputs 1 and 2 as follows: UP: When count input 1 leads count input 2 by 90°. DOWN: When count input 1 lags count input 2 by 90°. (The above three modes are selectable by using the DIP switch in the unit.)
	Counting speed	Solid-state input: 50K cps max. (20K cps max. for phase differential input) Contact input: 30 cps max. (The above two counting speeds are selectable by using the DIP switch in the unit.)
Reset input	Voltage level of input signal	H: 6 to 12V L: 0 to 4V
	ON-delay time	1.5ms max.
	OFF-delay time	2ms max.
Output signals		• Output by hardware Coincidence signal: Relay contact output and transistor (open collector) output Present count value > set count value output signal: transistor (open collector) output
Internal power supply		+5V 300mA max.
Terminal for external connection		Terminal block (cannot be dismounted)
Power supply for sensor		DC 12V ±10% 100mA (per point)
Power supply to outside circuit		DC 24V ±10% 500mA
Weight		700g max.

NOTE: * Count input 1 can be connected to both the solid-state and contact inputs. Count input 2 can be connected to the solid-state input only.

RELAY OUTPUT SPECIFICATIONS

Output switching capacity	Relay contact output (G6B) AC 250V/2A (p.f.=1) DC 24V/2A
On-delay time	10ms max.
OFF-delay time	15ms max.
Service life	Electrically: 300 x 10^3 operations Mechanically: 20 x 10^6 operations

OPEN COLLECTOR TYPE TRANSISTOR OUTPUT SPECIFICATIONS

Max. switching ability	DC 24V 200mA
Leakage current	500μA max.
Saturation voltage	1.3V max.
ON-delay time	50μs max.
OFF-delay time	50μs max.

NOTES:
1. Connect the high-speed counter unit to the SYSMAC-C250 via an expansion I/O rack of either the SYSMAC-C120 or SYSMAC-C500.
2. Insert the high-speed counter unit to the upper slot of an expansion I/O rack when mounting the unit to the SYSMAC-C120.
3. To mount the unit to the SYSMAC-C120, use Type 3G2C4-SI025 or 3G2C4-SI026.

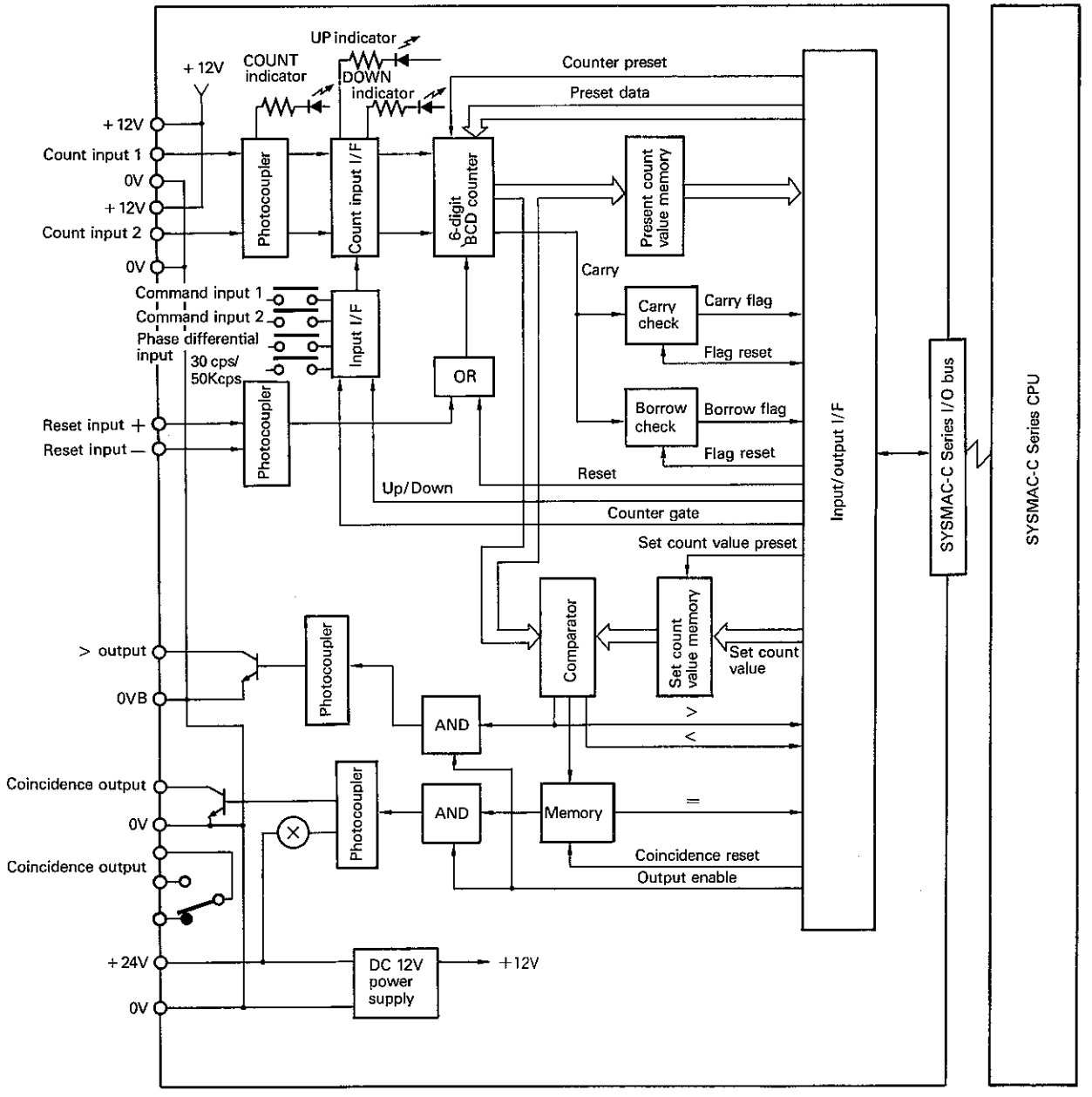
INDICATORS

Indicator		Function
☀ / ○	COUNT	Lights up when count input 1 is L and goes out when count input 1 is H.
☀	UP	Lights up while the counter is performing an up-count operation.
☀	DOWN	Lights up while the counter is performing a down-count operation.
☀	PV > SV	Lights up when a present count value is greater than a set count value (present count value > set count value).
☀	PV = SV	Lights up when a present count value is equal to a set count value (present count value = set count value). This indicator, however, unconditionally goes out when the "Output enable" relay is turned OFF (relay to Chapter 3, Assignment of Relay Numbers).
☀	PV < SV	Lights up when a present count value is less than a set count value (present count value < set count value).
☀	+12V	Lights up when the power supply for sensor is +12V.

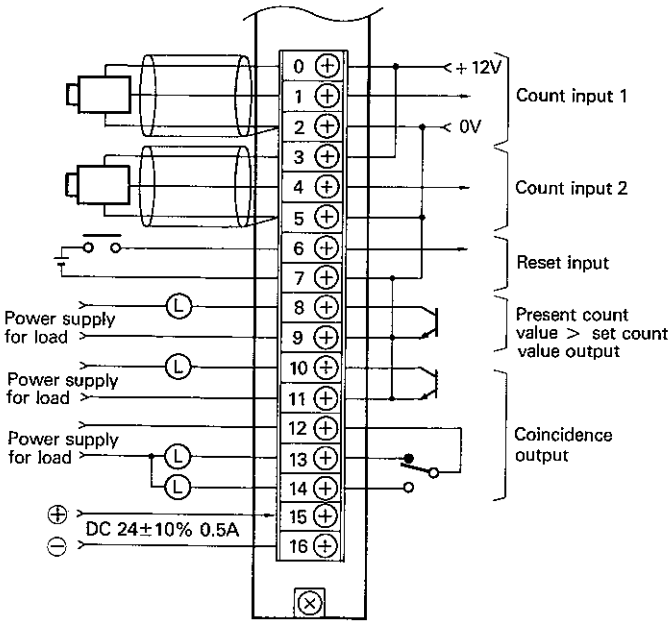
DIP SWITCH FOR COUNT INPUT MODE SETTING

Specifies the count input mode of the counter.

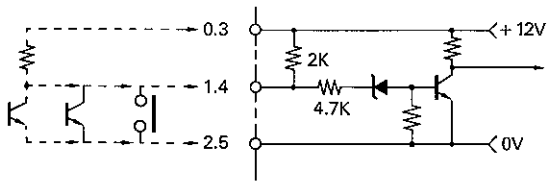
7.6.2 Block diagram



7.6.3 External connections



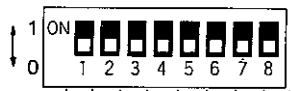
COUNT INPUT SIGNAL



NOTE: Because the high-speed counter unit performs its operation at a counting speed of 50K counts per second, avoid connecting loads and wirings that may generate much noise to the coincidence output terminals.

7.6.4 Setting DIP switch for count input mode

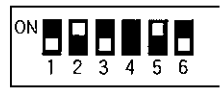
DIP SW SETTING POSITION



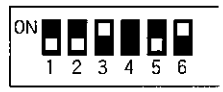
INPUT MODE	COMMAND INPUT	1	1	0	0					
		2	0	1	1					
	PHASE DIFFERENTIAL INPUT		0	0	1					
	NO VOLTAGE CONTACT INPUT					1				
	WHEN PHASE DIFFERENTIAL INPUT						1	0		
	WHEN NOT PHASE DIFFERENTIAL INPUT						0	1		
IN 1	WHEN NOT EMITTER FOLLOWER SENSOR CONNECTION								1	
IN 2	WHEN NOT EMITTER FOLLOWER SENSOR CONNECTION									1

SETTING OF COUNT INPUT MODE

Command input 1 mode: This mode is used to specify UP/DOWN count command signal by a program.



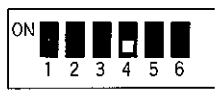
Command input 2 mode: This mode is used to specify UP/DOWN count command signal by count input 2.



Phase differential input mode: This mode is used to identify whether up-count or down-count operation is to be performed by the phase difference between count input 1 and 2.

SETTING OF FREQUENCY RESPONSE

30 cps (contact input): With this pin set in the "ON" position, the counter unit can be operated in command input 1 mode only, and the response frequency of count input 1 is set to 30 cps.



50K cps (Solid-state input): With this pin set in the "OFF" position, the counter unit can be operated in all input modes, and the response frequency of both count inputs, 1 and 2, is set to 50K cps.

SETTING OF SENSOR OUTPUT

Set this pin in the "OFF" position when the output from the sensor that is connected to count input 1 is of the emitter follower type. Otherwise set the pin in the "ON" position.

Set this pin in the "OFF" position when the output from the sensor that is connected to count input 2 is of the emitter follower type. Otherwise set the pin in the "ON" position.

7.6.5 Assignment of relay numbers

I/O of SYSMAC-C	OUT				IN			
Channel / Bit	nth CH		nth+1 CH		nth+2 CH		nth+3 CH	
0	Counter preset		Preset data 1	$\times10^{2}$	Carry		Present count data 1	$\times10^{2}$
1	Set count value preset		Preset data 2		Borrow		Present count data 2	
2	Count gate		Preset data 4		Present count value > set count value		Present count data 4	
3	UP/DOWN count command		Preset data 8		Present count value = set count value		Present count data 8	
4	Carry reset		Preset data 1	$\times10^{3}$	Present count value < set count value		Present count data 1	$\times10^{3}$
5	Borrow reset		Preset data 2		Normally ON		Present count data 2	
6	Coincidence reset		Preset data 4		Normally ON		Present count data 4	
7	Output enable		Preset data 8		Normally ON		Present count data 8	
8	Preset data 1	$\times10^{0}$	Preset data 1	$\times10^{4}$	Present count data 1	$\times10^{0}$	Present count data 1	$\times10^{4}$
9	Preset data 2		Preset data 2		Present count data 2		Present count data 2	
10	Preset data 4		Preset data 4		Present count data 4		Present count data 4	
11	Preset data 8		Preset data 8		Present count data 8		Presnet count data 8	
12	Preset data 1	$\times10^{1}$	Preset data 1	$\times10^{5}$	Present count data 1	$\times10^{1}$	Present count data 1	$\times10^{5}$
13	Preset data 2		Preset data 2		Present count data 2		Present count data 2	
14	Preset data 4		Preset data 4		Present count data 4		Present count data 4	
15	Preset data 8		Preset data 8		Present count data 8		Present count data 8	

NOTE: The term "set count value" is synonymous with "preset data"

FUNCTION OF RELAYS

The following signals are input to the high-speed counter unit from the programmable controller.

Name of relay	Function
Counter preset	Presets the data set as a preset data to the counter; in other words, modifies a currently set value.
Set count value preset	Presets data set as a preset data to the set count value memory.
Count gate	Controls starting and stopping the counter. When this relay is turned ON, the counting operation starts, and when it is turned OFF, the counting operation stops. On power application, the count gate relay specifies that the counting operation is stopped.
UP/DOWN count command	Specifies the up-count or down-count operation by the user program when the high-speed counter unit is in the command input 1 mode. When this relay is turned ON, the down-count operation is specified. When it is OFF, the up-count operation is specified. On power application, the up-count command is given.
Carry reset	Resets the Carry signal of the counter. Once the Carry signal has been reset, it will not be set again until the count gate relay is turned ON and a counting operation is performed.
Borrow reset	Resets the Borrow signal of the counter. Once the Borrow signal is reset, it will not be set again until the counter gate relay is turned ON and a counting operation is performed.
Coincidence reset	Resets the present count value = set count value signal of the counter. Once the present count value = set count value signal has been reset, it will not be set again until the counter gate relay is turned ON and a counting operation is performed. If this relay is turned ON while the present count value coincides with the set count value, the present count value = set count value relay (i.e., bit No. 3 of n+2CH) will not be turned ON.
Output enable	Enables the external output signals (coincidence output and present count value > set count value output) to be output. On power application, the output is disabled, and therefore, both the contact and transistor outputs are turned OFF.
Preset data (10^5 through 10^0)	Represent the preset data of the counter or the set count value memory. If these relays represent the data of the counter, those data are the present count value. The value of the data can be 000000 to 999999. On power application, the data are 000000.

The following signals are input to the programmable controller from the high-speed counter unit.

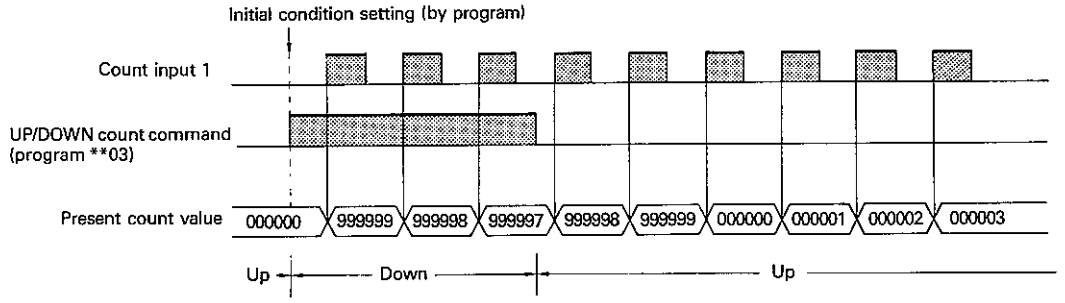
Carry	Turns ON when the present count value changes from 999999 to 000000 during the Add operation. This relay is turned OFF by the carry reset relay or an external reset signal.
Borrow	Turns ON when the present count value changes from 000000 to 999999. This relay is turned OFF by the borrow reset relay of an external reset signal.
Present count value > set count value	Turns ON when the present count value is greater than the set count value.
Present count value = set count value	Turns ON when the present count value coincides with the set count value. This relay is turned OFF by the coincidence reset relay or an external reset signal.
Present count value < set count value	Turns ON when the present count value is less than the set count value.
Present count value data	Present count value (000000 to 999999)

NOTE: On power application, all the relays are turned OFF.

7.6.6 Operation

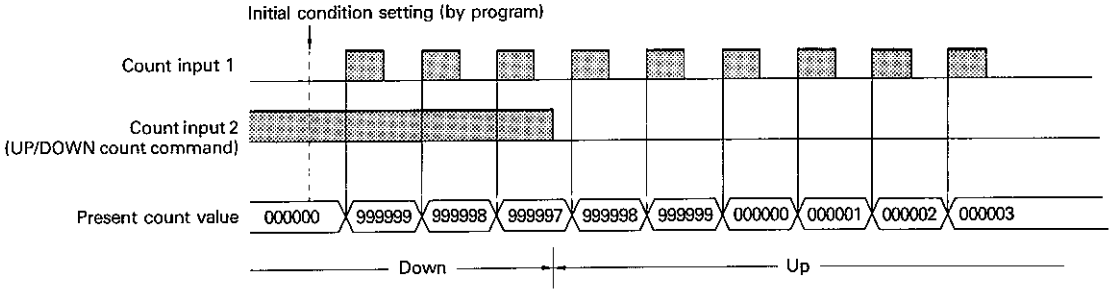
TIMING CHARTS OF COUNT MODE

Command input mode 1



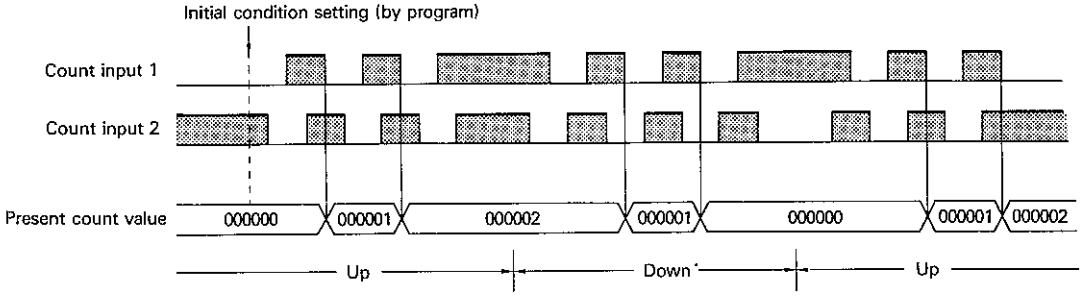
In this mode, the counter counts each leading edge of count input 1. The user program specifies either the UP or DOWN operation. The signal of count input 2 is ignored.

Command input mode 2



In this mode, the counter counts each leading edge of count input 1. Count input 2 specifies either the UP or DOWN operation. That is, the UP operation is performed when the input level of count input 2 is high, and if it is low, the DOWN operation is specified.

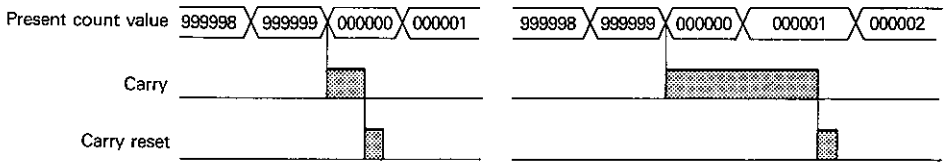
Phase differential input mode



In this mode, whether the UP or DOWN operation is performed is specified by the phase difference between count inputs 1 and 2.
When count input 1 leads count input 2 by 90° at the leading edge of count input 1, the UP operation is specified at the trailing edge of count input 1. The DOWN operation, on the other hand, is specified when count input 1 lags count input 2 by 90° at the leading edge of count input 1.
Permissible phase differential error range is 90°±45°.

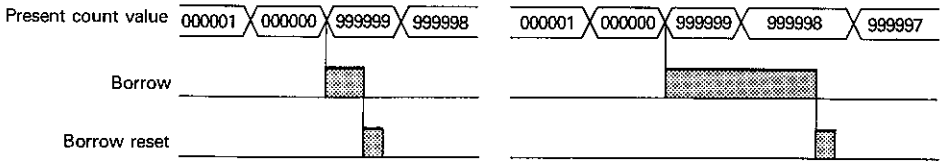
TIMING CHARTS OF CARRY, BORROW, AND COINCIDENCE SIGNALS

Carry signal



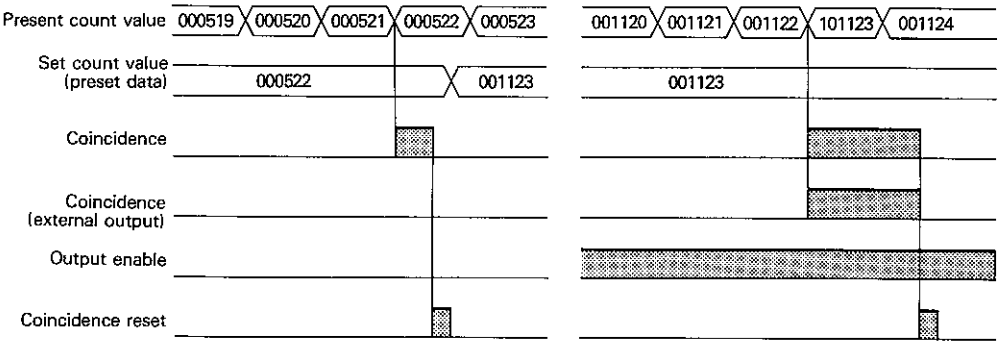
The level of the carry signal becomes high when the present count value of the counter changes from 999999 to 000000. This high level will be retained until the level of the carry reset or external reset signal becomes high.

Borrow signal



The level of the borrow signal becomes high when the present count value of the counter changes from 000000 to 999999. This high level will be retained until the level of the borrow reset or external reset signal becomes high.

Coincidence signal



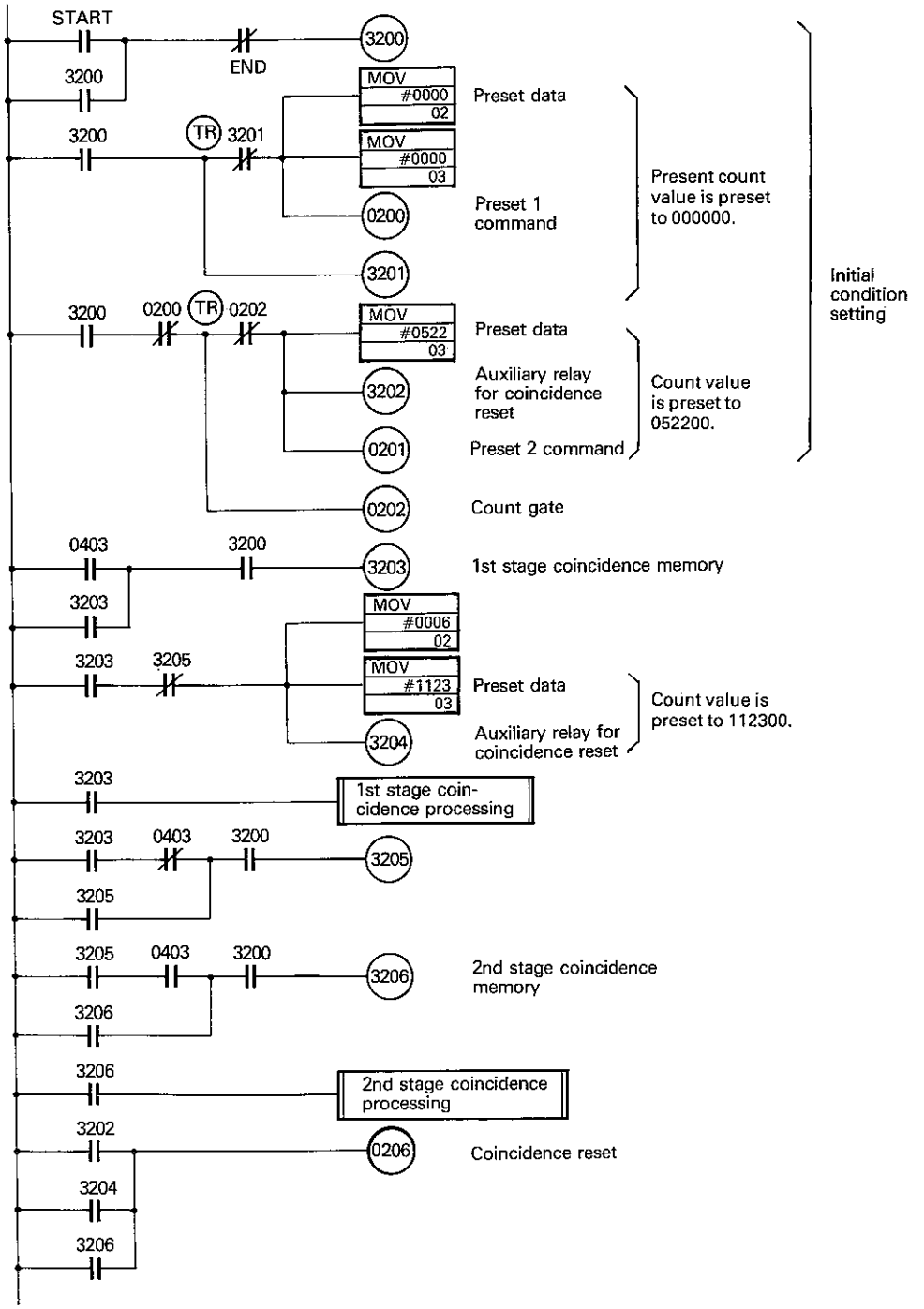
The level of the coincidence signal becomes high when the present count value of the counter coincides with the set count value. This high level will be retained until the level of the coincidence reset or external reset signal becomes high. The coincidence signal is not output until the level of the output enable signal becomes high.

7.6.7 Programming examples

DOUBLE PRESET COUNTER

In this example, two count values "052200" and "112300" are processed with a double preset counter. (The high-speed counter unit is assigned to Channel Nos. 2 to 5 in the CPU rack.)

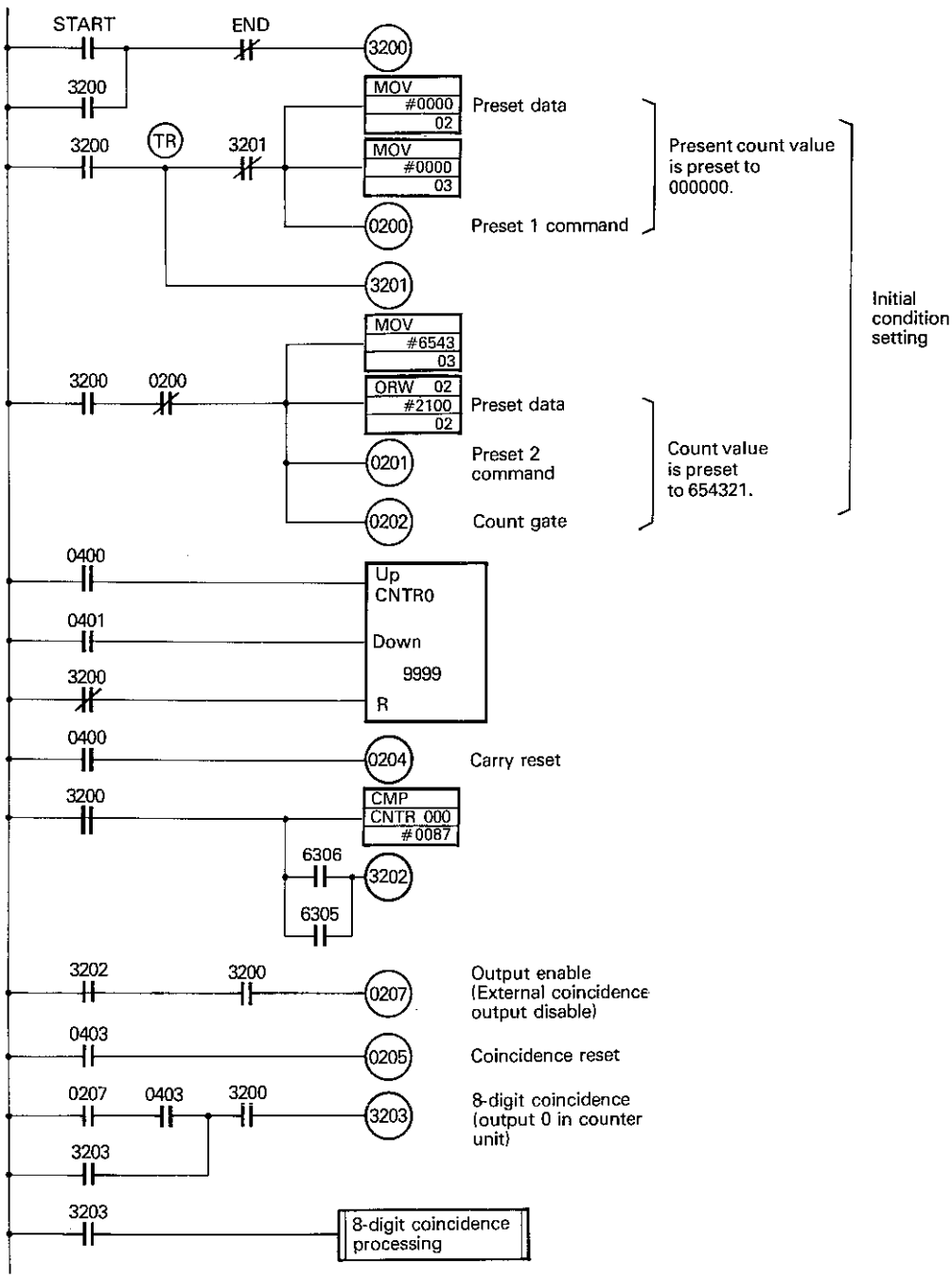
Nos. 3200 to 3206 denote the internal auxiliary relays of the programmable controller.



NOTE: Preset 1 command, preset 2 command, and coincidence reset command cannot be executed properly if their coil numbers are used in duplication.

MULTIDIGIT PRESET UP COUNTER (MORE THAN 6 DIGITS)

In this example, count value "87654321" is processed with a multidigit preset UP counter. (The high-speed counter unit is assigned to Channel Nos. 2 to 5 in the CPU rack.)



7.7 REMOTE IO/ UNIT

Two remote I/O units are used to control I/O units remotely situated from a SYSMAC-C Series programmable controller; one serving as a master station (Type 3G2A5-RM001-E or 3G2A6-RM001-E) is called the remote master unit (RMU), and the other serving as a slave station (Type 3G2A5-RT002-E or 3G2A5-RT001-E) is the remote slave unit (RSU). The two stations are connected with SYSBUS (a pair of fiber optics cables) and can optically transmit data to each other at a high speed.

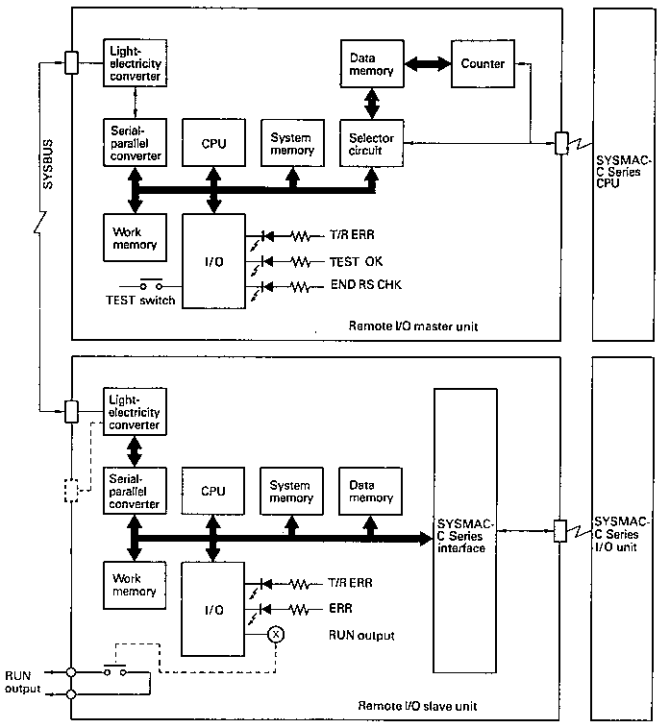
Because the remote I/O master unit can be used as a primary station of the remote I/O slave unit and an optical transmitting I/O unit (Type 3G5A2-XXX-E) as well, various system configuration is possible by using the master unit, such as connecting the master unit to the optical transmitting I/O unit(s) only or to a combination of the remote I/O slave unit and optical transmitting I/O unit(s).

The remote I/O master and slave units are capable of transmitting a maximum of 512 I/O points at a transmission speed of 128 points per 16ms.

7.7.1 Characteristics

Item	Master unit	Slave unit
Transmission system	Time-division multiplexing cyclic system	
Communication method	4-wire, half duplex system	
Transmission speed	187.5k bps	
Transmission delay	128 points per 16ms	
Transmission line	Polymer-clad quartz core fiber optics	
Line distance	800m max.	
No. of I/Os that can be transmitted	512 I/O points max. including special I/O unit	
External RUN output	—	G6B SPST-NO relay contact (closed during RUN mode) Contact capacity: AC 250V 2A (p.f.=1) DC 24V 2A
Internal power supply	+5V, 750mA max.	+5V, 550mA max.
Weight	500g max.	500g max.

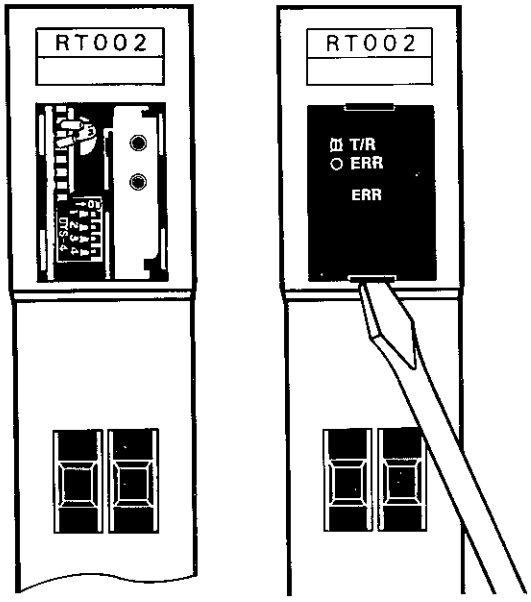
7.7.2 Configuration

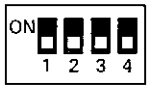


7.7.3 Setting address and end RSU

SETTING ADDRESS AND END RSU OF REMOTE I/O SLAVE UNIT

Remove the indication panel from the remote I/O slave unit with a flat-blade screwdriver, and a 4-pin DIP switch will be found on a PC board. Set the DIP switch in reference to the following figure and table.



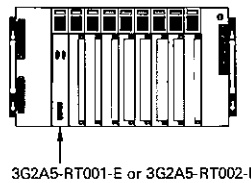
DIP switch	Function
Address/End RSU setting DIP switch 	 To specify No. 0 sub unit as the end RSU
	 To specify sub unit other than No. 0 as the end RSU
	 To specify No. 1 sub unit as the end RSU
	 To specify sub unit other than No. 1 as the end RSU

NOTES: 1. A protective cap is attached as an accessory. Put it on the unused fiber optics connector of the remote I/O slave unit specified as the end RSU to prevent a malfunction of the unit from external interference light.
2. Although Type 3G2A5-RT001-E is exclusively used as the end RSU, perform the setting for the end RSU in the same manner as the other remote I/O slave units.

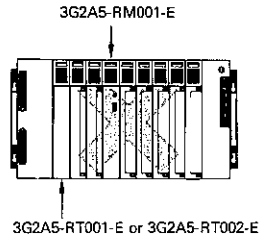
CAUTION
1. **Be sure to perform the setting with the power turned OFF.**
2. **If the same address is specified to plural remote I/O slave units in duplication (e.g., two slave units are assigned address 0), data will compete for the SYSBUS, causing a transmission error to occur. Therefore, never specify the address in duplication.**

7.7.5 Hints on correct use

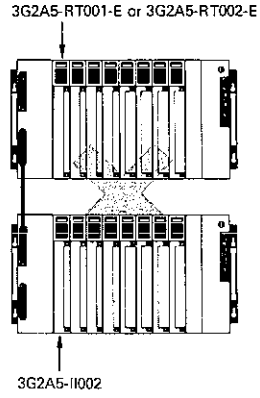
A maximum of four remote I/O master units can be connected to the CPU or the expansion I/O rack of the SYSMAC-C500 and three to the expansion I/O rack of the SYSMAC-C120. The remote I/O slave unit must be inserted to the leftmost slot of the expansion I/O rack of the SYSMAC-C500.



The remote I/O master unit must not be mounted to the SYSMAC-C500 to which a remote I/O slave unit is already mounted.



The expansion I/O rack of the SYSMAC-C500 must not be connected for the purpose of system expansion to the SYSMAC-C500 to which a remote I/O slave unit is already mounted.



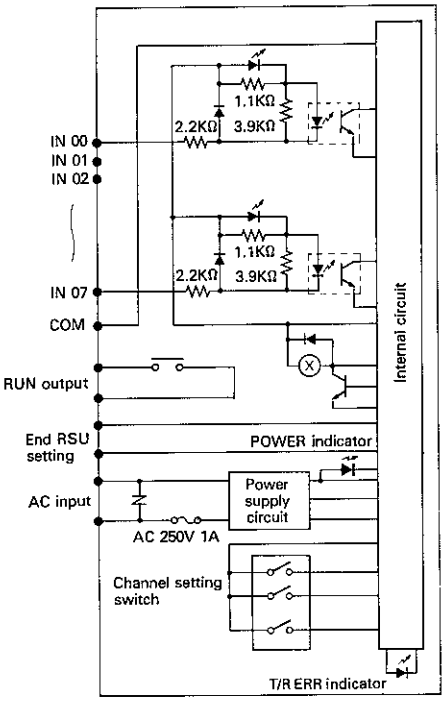
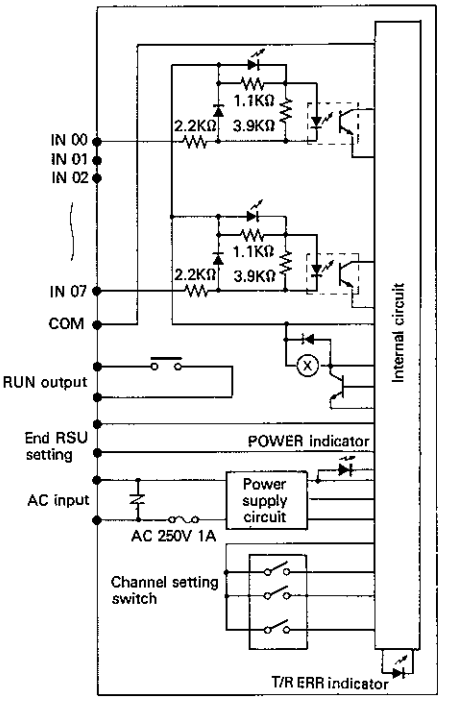
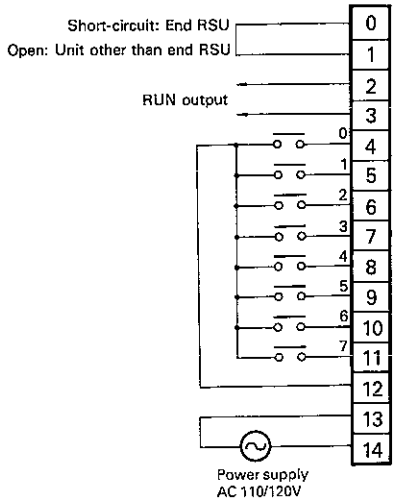
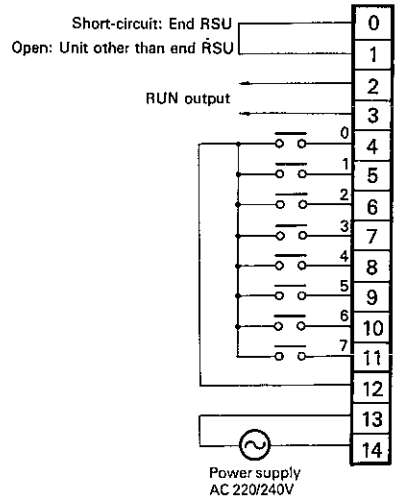
7.8 OPTICAL TRANSMITTING I/O UNIT

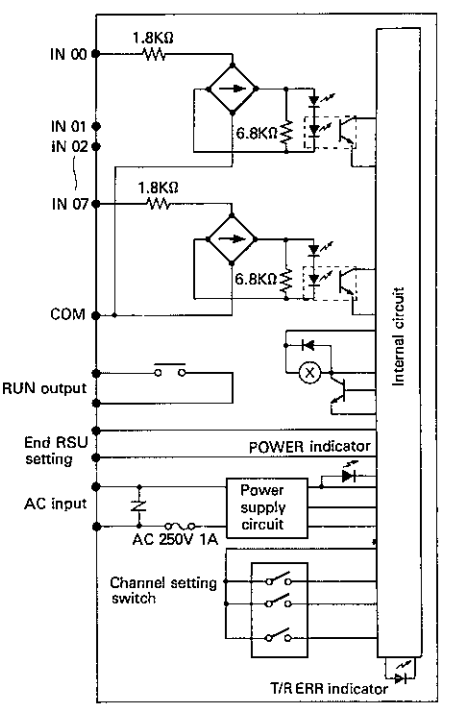
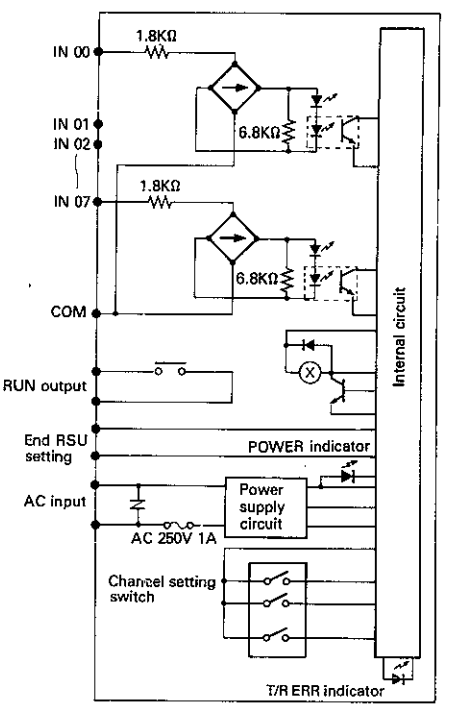
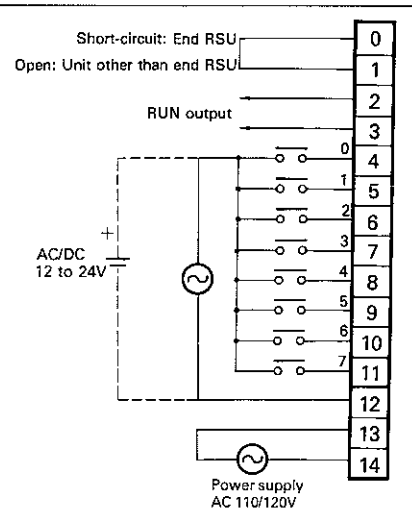
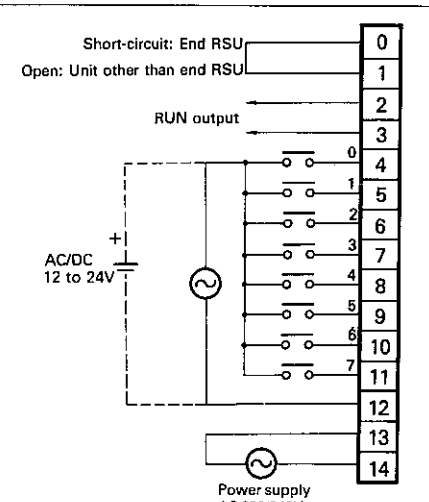
By connecting the optical I/O transmitting unit to the remote I/O master unit with a fiber optics cable, high-speed optical data transmission can be performed. The remote I/O master unit, which serves as the primary station of a data transmission system configured thereby, can be connected to plural optical I/O transmitting units only, or to a combination of the remote I/O slave unit and optical I/O transmitting units.

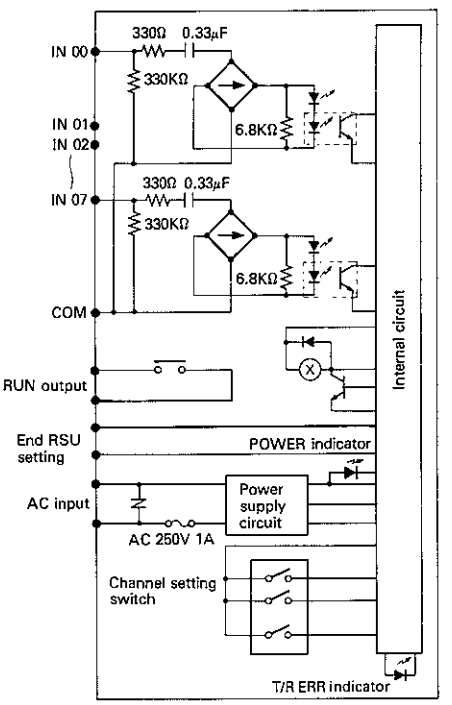
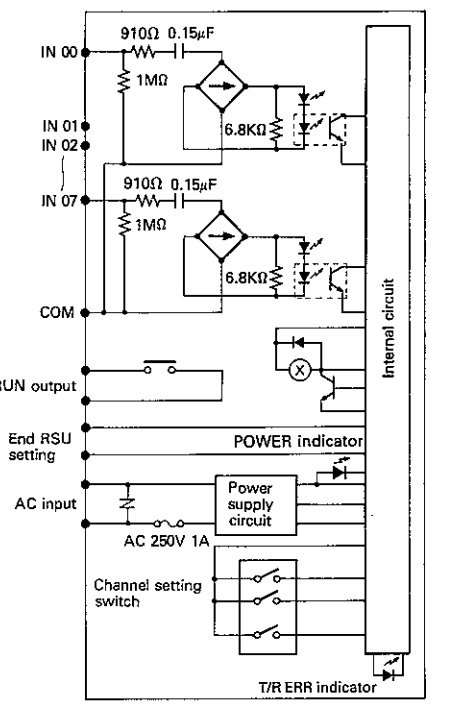
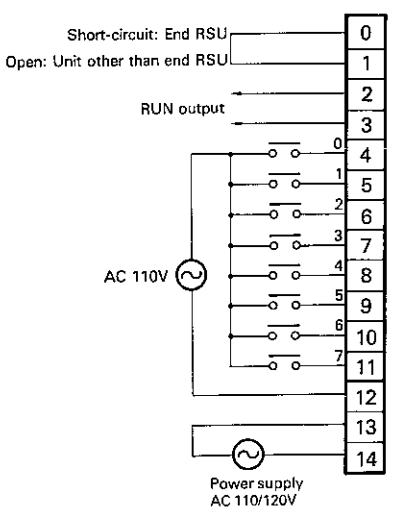
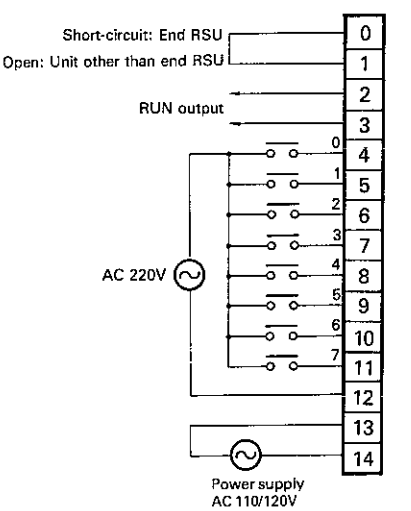
Since the number of I/O points per optical I/O transmitting unit is 8, a maximum of 64 optical I/O transmitting unit can be connected per remote I/O master unit when the SYSMAC-C500, which possesses 512 points of input/output relays, is used. However, the maximum number of units connectable to the SYSMAC-C120 or SYSMAC-C250 is 32 because these programmable controllers have 256 I/O points each.

7.8.2 Specifications

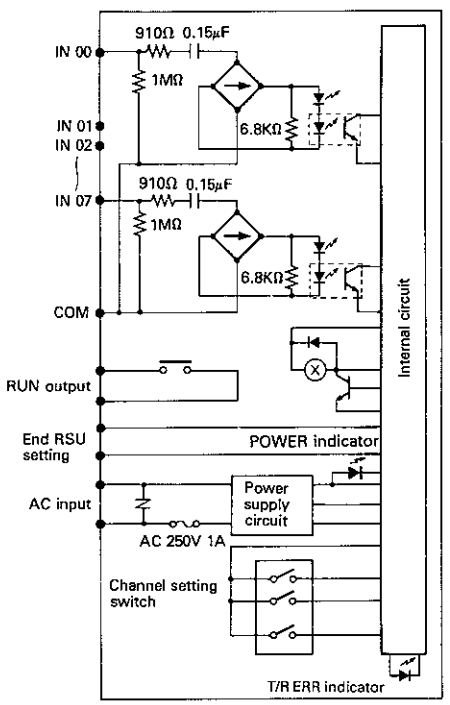
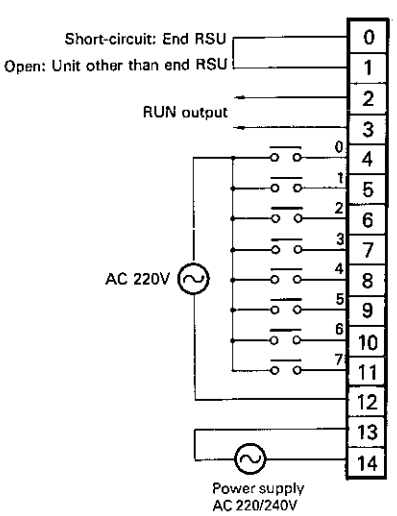
INPUT UNIT

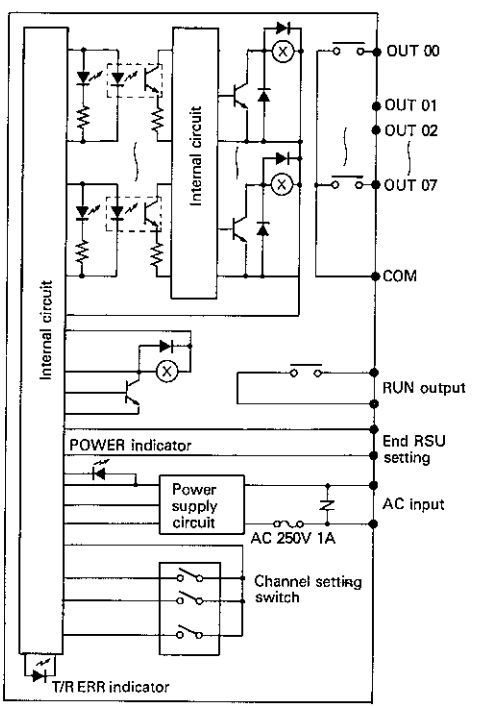
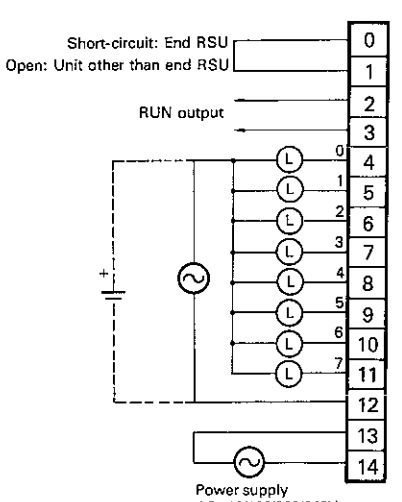
Item \ Type	No-voltage contact input unit	
	3G5A2-ID001-E	3G5A2-ID002-E
Input voltage	No-voltage contact	No-voltage contact
Input impedance	–	–
Input current	10mA typ.	10mA typ.
ON-delay time	10ms max.	10ms max.
OFF-delay time	15ms max.	15ms max.
Number of circuits	8 (8 points/common)	8 (8 points/common)
ON voltage	–	–
OFF voltage	–	–
Supply voltage	AC 110/120V, 50/60Hz	AC 220/240V, 50/60Hz
Power consumption	20VA max.	20VA max.
Weight	580g max.	580g max.
Circuit configuration		
Terminal connection		

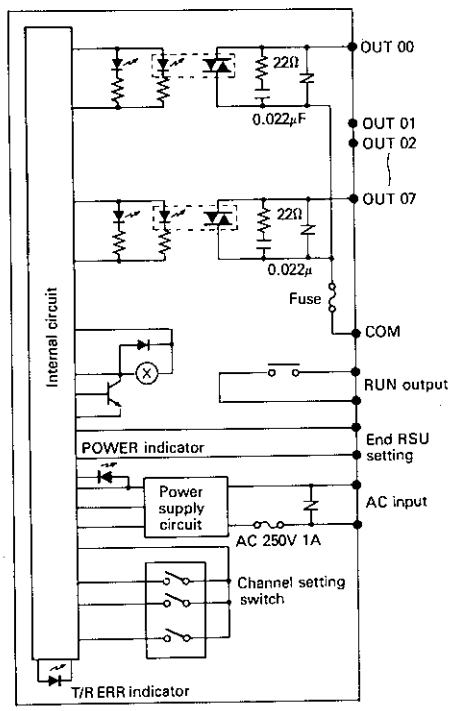
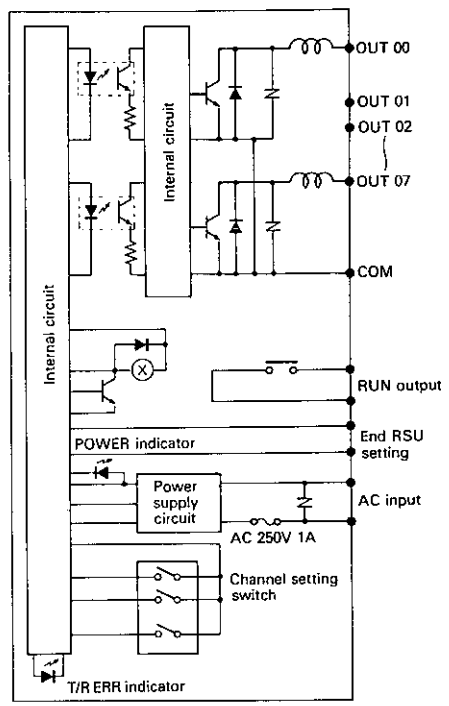
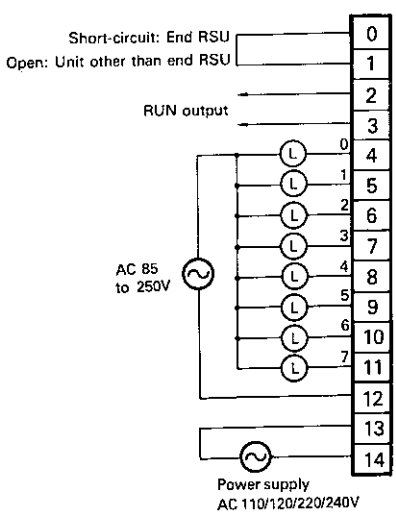
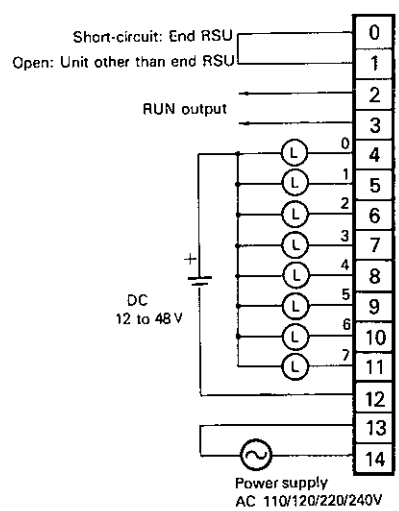
Item \ Type	AC/DC input unit 3G5A2-IM211-E	AC/DC input unit 3G5A2-IM212-E
Input voltage	AC/DC 12 to 24V +10% −15%	AC/DC 12 to 24V +10% −15%
Input impedance	1.8kΩ	1.8kΩ
Input current	10mA typ. (DC 24V)	10mA typ. (DC 24V)
ON-delay time	10ms max.	10ms max.
OFF-delay time	15ms max.	15ms max.
Number of circuits	8 (8 points/common)	8 (8 points/common)
ON voltage	10.2V max.	10.2V max.
OFF voltage	3.0V min.	3.0V min.
Supply voltage	AC 110/120V, 50/60Hz	AC 220/240V, 50/60Hz
Power consumption	20VA max.	20VA max.
Weight	580g max.	580g max.
Circuit configuration		
Terminal connection		

Item \ Type	AC input unit	
	3G5A2-IA121-E	3G5A2-IA221-E
Input voltage	AC 110V +10% 50/60Hz −15%	AC 220V +10% 50/60Hz −15%
Input impedance	9.7kΩ (50Hz), 8kΩ (60Hz)	22kΩ (50Hz), 18kΩ (60Hz)
Input current	10mA typ. (AC 100V)	10mA typ. (AC 200V)
ON-delay time	10ms max.	10ms max.
OFF-delay time	15ms max.	15ms max.
Number of circuits	8 (8 points/common)	8 (8 points/common)
ON voltage	AC 60V max.	AC 120V max.
OFF voltage	AC 20V min.	AC 40V min.
Power supply	AC 110/120V, 50/60Hz	AC 110/120V, 50/60Hz
Power consumption	20VA max.	20VA max.
Weight	580g max.	600g max.
Circuit configuration		
Terminal connection		

OUTPUT UNIT

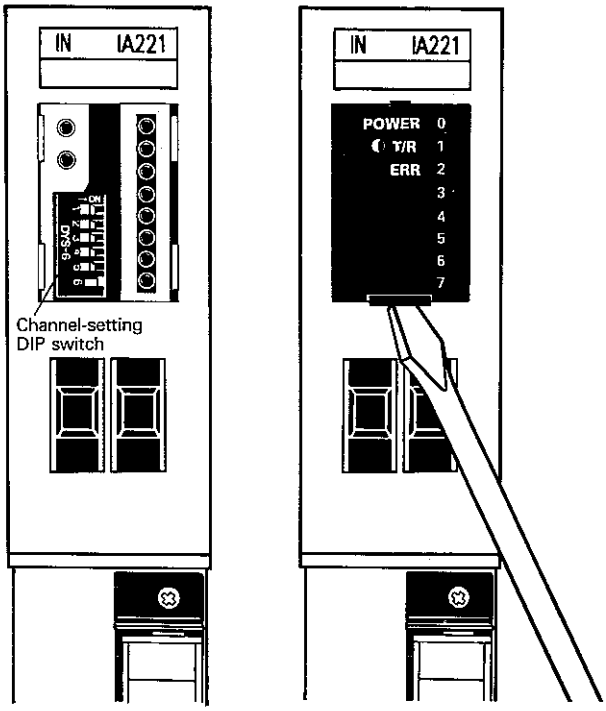
Item \ Type	AC input unit
	3G5A2-IA222-E
Input voltage	AC 220V +10% −15% 50/60Hz
Input impedance	22kΩ (50Hz), 18kΩ (60Hz)
Input current	10mA typ. (AC 200V)
ON-delay time	10ms max.
OFF-delay time	15ms max.
Number of circuits	8 (8 points/common)
ON voltage	AC 120V max.
OFF voltage	AC 40V min.
Power supply	AC 220/240V, 50/60Hz
Power consumption	20VA max.
Weight	600g max.
Circuit configuration	
Terminal connection	

Item \ Type	Contact output unit
	3G5A2-OC221-E
Max. switching capacity	AC 250V/2A (p.f.=1), DC 24V/2A (8A/common)
Min. switching capacity	DC 5V 100mA
ON-delay time	15ms max.
OFF-delay time	15ms max.
Number of circuits	8 (8 points/common)
Service life	Electrically: 300,000 operations Mechanically: 50,000,000 operations
Power supply	AC 110/120/220/240V, 50/60Hz
Power consumption	20VA max.
Weight	600g max.
Circuit configuration	
Terminal connection	

Item \ Type	Triac output unit 3G5A2-OA222-E	Transistor output unit 3G5A2-OD411-E
Max. switching capacity	AC 85 to 250V +10% 1A, 50/60Hz −15%	DC 12 to 48V +10% 0.3A −15%
Min. switching capacity	10mA/AC 100V	–
Leakage current	3mA max./AC 100V 6mA max./AC 200V	100μA max.
Saturation voltage	1.2V max.	1.5V max.
ON-delay time	1ms max.	0.2ms max.
OFF-delay time	1/2 load frequency max.	0.3ms max.
Number of circuits	8 (8 points/common)	8 (8 points/common)
Fuse capacity	5A/8 points	No fuse is provided.
Supply voltage	AC 110/120/220/240V, 50/60Hz	AC 110/120/220/240V, 50/60Hz
Power consumption	20VA max.	20VA max.
Weight	600g max.	600g max.
Circuit configuration		
Terminal connection		

7.8.3 Channel and end RSU settings

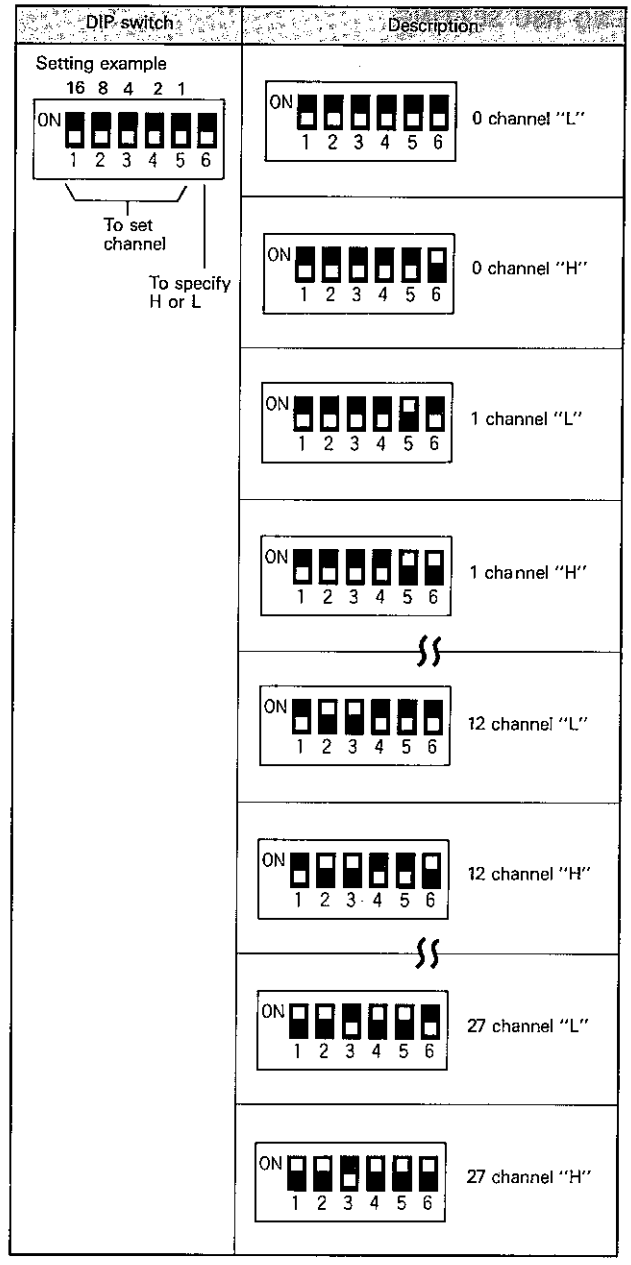
CHANNEL SETTING



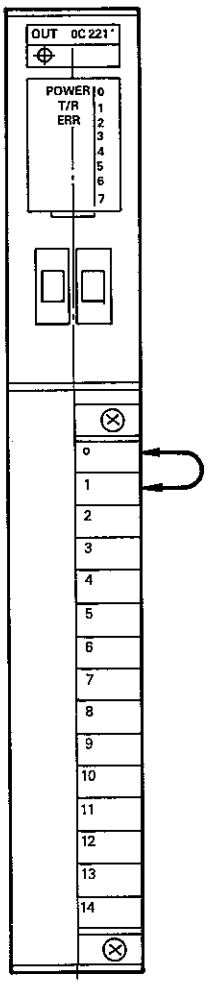
Remove the operation indicator panel of the optical transmitting I/O unit with a flat-blade screwdriver. Set the channel by using the 6-pin DIP switch mounted on the PC board. The channel number is set as a binary number. Set the channel in reference to the examples shown on the right.

CAUTION

1. **Be sure to perform the setting with the power turned OFF.**
2. **When the same channels are specified in duplication for the input or output of an optical transmitting unit, the data will compete for the SYSBUS, causing a transmission error to occur. Therefore, never set the same channel in duplication.**



END RSU SETTING



To specify an optical transmitting I/O unit as the end RSU, short-circuit terminal Nos. 0 and 1 as shown in the above figure.

Put the protective cap attached as an accessory on one of the fiber optics connectors to prevent a malfunction caused by an external interference light.

7.9 OPERATION, DIAGNOSTIC FUNCTIONS, AND FAILURE DETECTION OF REMOTE I/O UNIT AND OPTICAL TRANSMITTING I/O UNIT

7.9.1 Address and channel setting and assignment of I/O channels

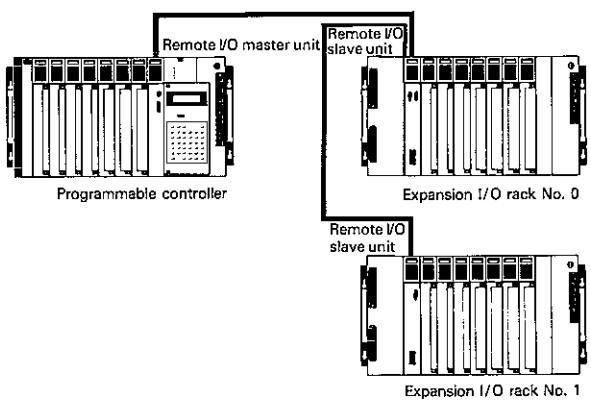
SIGNIFICANCE OF ADDRESS SETTING

Up to two remote I/O slave units, each of which functions as a slave station, or 64 optical transmitting I/O units can be connected to a remote I/O master unit that serves as a master station.

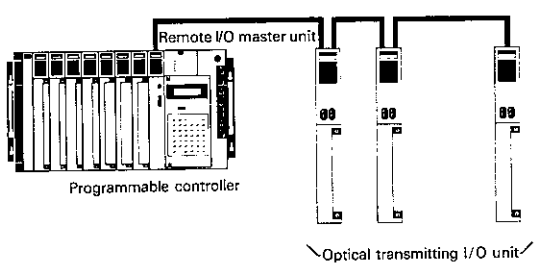
The maximum number of I/O points of the optical transmitting I/O units that can be connected to a SYSMAC-C Series programmable controller is the same as the total number of the I/O relays provided to that programmable controller. For example, because the SYSMAC-C500 has 512 I/O relays, up to 512 points of the optical transmitting I/O units can be connected to this programmable controller. Because the remote I/O master unit must recognize the addresses and channels of each I/O unit connected to the master unit, setting the addresses and channels of these I/O units is important to facilitate the managing of the connected I/O units by the master unit.

ADDRESS OF REMOTE I/O SLAVE UNITS

Two remote I/O slave units can be connected to a remote I/O master unit. Set the address of each connected remote I/O slave unit so that the remote I/O master unit identifies the address of each expansion I/O rack to which each I/O sub unit is mounted. For details on DIP switch setting of the remote I/O slave unit, refer to 7.7.4, Setting address and end RSU (remote I/O slave unit).



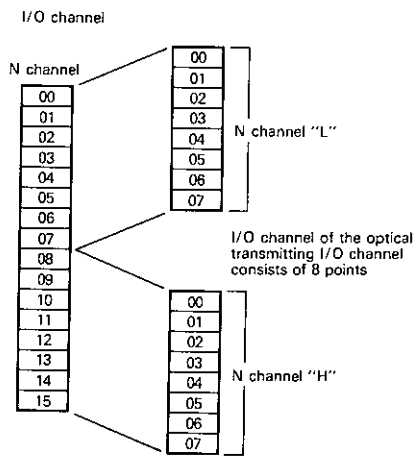
CHANNEL SETTING FOR OPTICAL TRANSMITTING I/O UNIT



An I/O channel of the SYSMAC-C Series programmable controller consists of 16 points, and that of an optical transmitting I/O unit, 8 points. When setting the I/O channel of an optical transmitting I/O unit, pay attention to these two items.

First, the I/O channel of the programmable controller to which the optical transmitting I/O unit is assigned must be determined. *Unlike the remote I/O slave unit that is automatically assigned with an I/O channel when it is mounted to the expansion I/O rack, the channel of each optical transmitting I/O unit must be set by using the DIP switch incorporated in the unit.*

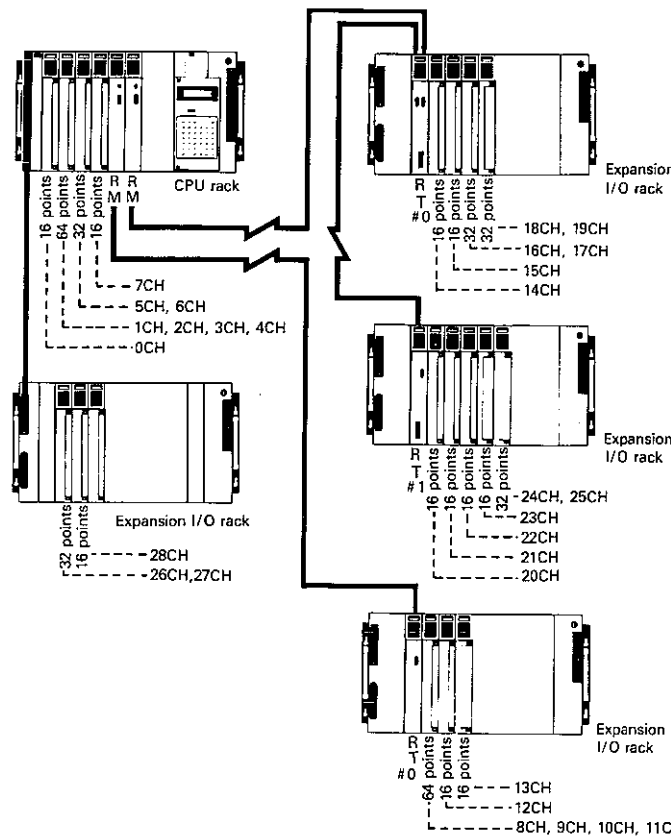
Second, as stated, an I/O channel of the SYSMAC-C Series programmable controller consists of 16 points, whereas that of an optical transmitting unit consists of 8 points. *Therefore, relay numbers 00 to 07 of a specific I/O channel are regarded as lower-order (L) addresses, and relay numbers 08 to 15 are treated as higher-order (H) addresses, and an optical transmitting I/O unit is connected to each of the L and H address.*



Note, however, that *an optical transmitting input and output unit must not be assigned to the L and H addresses of the same channel.* To set the DIP switch of the optical transmitting I/O unit, refer to 7.8.3, Channel and end RSU settings of optical transmitting I/O unit.

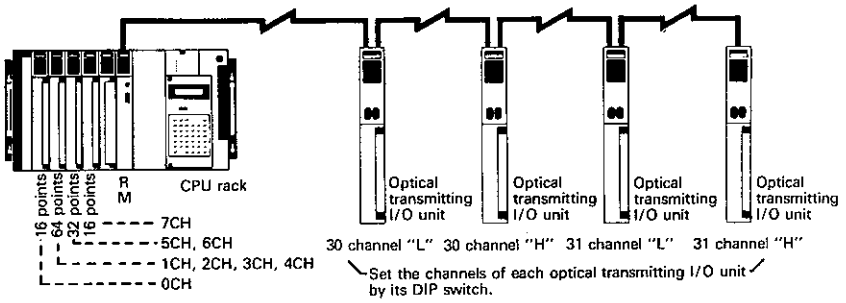
ASSIGNMENT OF I/O CHANNELS

Example 1: Connection between SYSMAC-C500 and remote I/O units

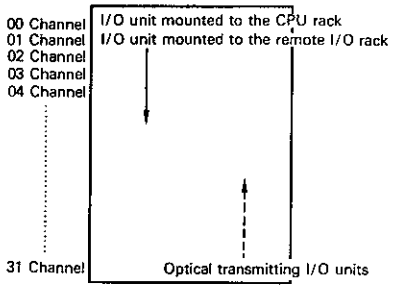


When an I/O unit is mounted to an expansion I/O rack mounting a remote I/O unit, the programmable controller automatically assigns a channel to the I/O unit. Refer to 3.2 Free location concept and I/O channels in Part 1 as necessary.

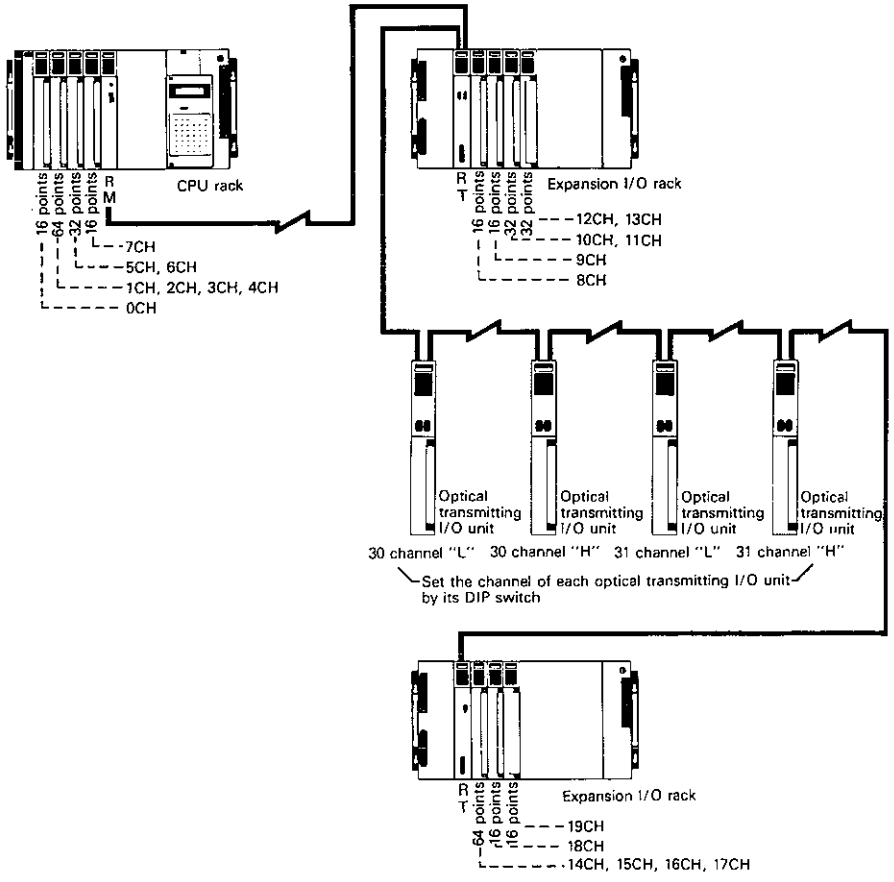
Example 2: Connection between SYSMAC-C500 and optical transmitting I/O unit



Because the channel is automatically assigned to the I/O unit(s) mounted to the CPU rack of the programmable controller or to the expansion I/O rack in sequence starting from channel 00, the channel to optical transmitting I/O unit(s) must be assigned in reverse sequence starting from channel 31. In so doing, pay special attention so that the I/O channels of the programmable controller and those of the optical transmitting I/O units do not overlap.



Example 3: Connection between SYSMAC-C500, remote I/O units and optical transmitting I/O units

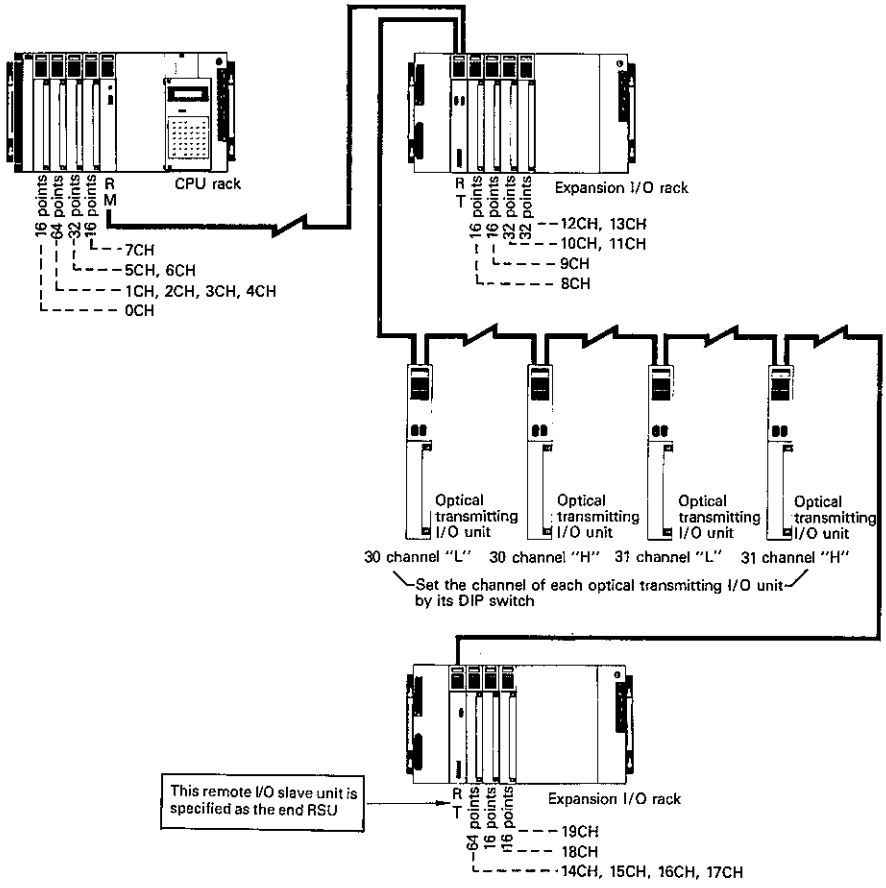


Connect the remote I/O units or optical transmitting I/O units to the SYSMAC-C120 or SYSMAC-C250 in the same manner as described in examples 1 to 3 above. For details, refer to 7.9.3, System configuration examples.

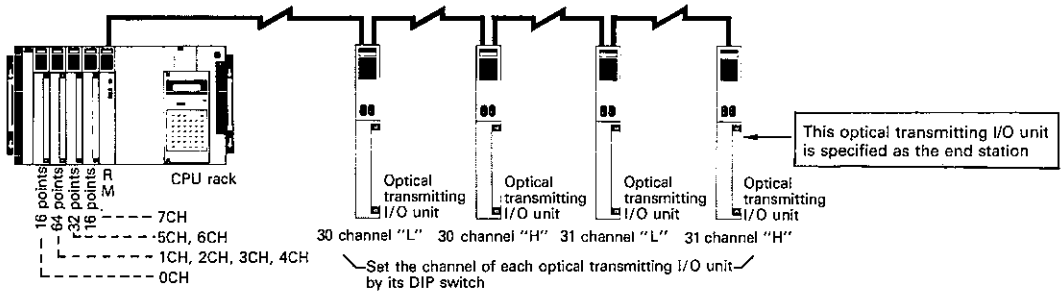
MEANING OF END STATION

On power application, the remote I/O master unit checks whether a remote I/O slave unit or an optical transmitting I/O unit that is specified as the end RSU is connected to it. If an I/O unit specified as the END station exists, the remote I/O master unit recognizes the I/O units currently connected to the SYSBUS. The remote I/O slave unit transmits data to and from the I/O units connected to the SYSBUS. The I/O units not connected to the SYSBUS or the optical transmitting I/O units connected after the end RSU are consequently ignored by the remote I/O master unit. To prevent this, specify the I/O unit with the greatest I/O channel number as the end RSU.

Example 1



Example 2



7.9.2 Mounting procedures of remote I/O units and optical transmitting I/O units

MOUNTING REMOTE I/O UNITS AND OPTICAL TRANSMITTING UNITS

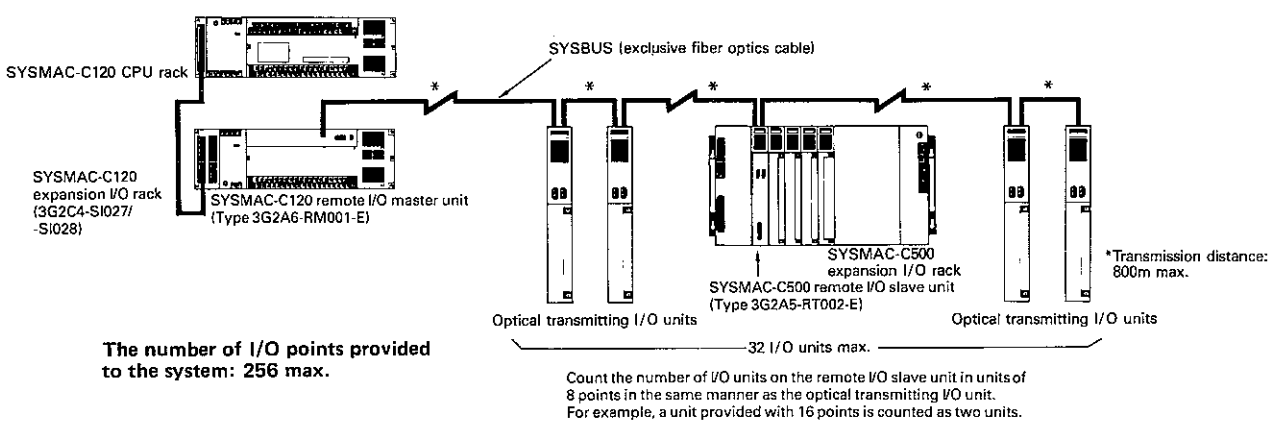
Observe the following procedures when newly mounting remote I/O unit(s) or optical transmitting I/O unit(s) to the CPU rack.

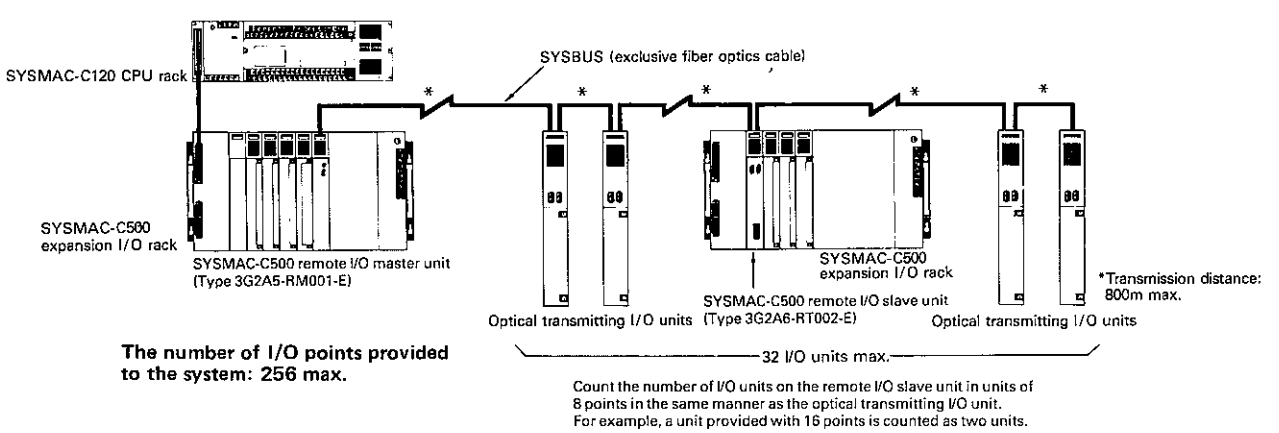
1. Check the I/O units currently mounted to the CPU rack for the last I/O channel number.
2. Set the address of the newly mounted remote I/O slave unit. Also set the channel of the newly mounted optical transmitting I/O unit. In so doing, pay particular attention so that the set channel number does not overlap with the last channel number of the I/O unit mounted to the CPU rack. Note that the number of I/O points of the set channel must not exceed the maximum number of I/O relays provided to the PC. In case the number of the I/O points of the set channel exceeds the maximum number of the programmable controller's I/O relays, an I/O unit over error occurs.
3. Sequentially connect the fiber optics cables (SYSBUS) to the connector of each unit starting from the remote I/O master unit. Type 3G2A5-RT002-E remote I/O slave unit and the optical transmitting I/O unit have two fiber optics connectors. The fiber optics cable from the remote I/O master unit can be connected to either of them.
4. Specify the I/O unit that has been connected last to the SYSBUS as the END station. When doing so, confirm that any other I/O unit connected to the SYSBUS is not specified as the END station.
5. Turn on the power of each unit in the system. This may be done in any order.
6. After the END STA CHECK indicator of the remote I/O master unit goes out, generate an I/O table by using the programming console of the PC.
7. With the programming console, check whether the newly mounted remote I/O slave unit and optical transmitting I/O unit have been correctly registered to the CPU of the PC.

NOTES:
1. Once the above procedures have been performed, the system is ready for operation on power application.
2. Should the system not operate normally after the above procedures have been correctly observed, refer to List of error messages and alarm output in 7.9.4.
3. Generate or check the I/O table by using the programming console.

7.9.3 System configuration examples

When connecting remote I/O slave unit and optical transmitting I/O units to SYSMAC-C120 via remote I/O master unit:





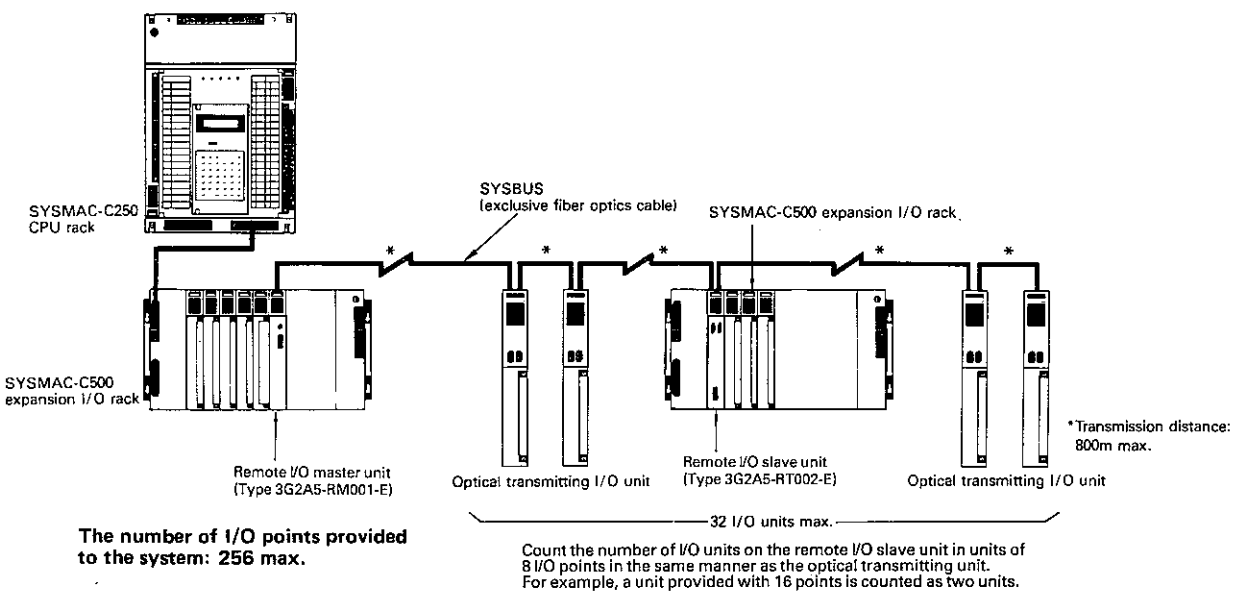
The remote I/O master unit can be inserted in the upper slot of the SYSMAC-C120 expansion I/O rack or in any I/O connector of the SYSMAC-C500 expansion I/O rack. It cannot, however, be directly connected to the SYSMAC-C120 CPU rack.

Up to two remote I/O slave units or 64 optical transmitting I/O units can be connected to a remote I/O main unit. Note, however, that I/O units cannot be connected to the SYSMAC-C120 exceeding 256 I/O points because the maximum number of I/O relays provided to the PC is 256.

In terms of the optical transmitting unit, the maximum number of units taht can be connected to the SYSMAC-C120 is 32 because eight I/O points are provided per optical transmitting I/O unit.

When mounting Type 3G2A6-RM001-E remote I/O master unit to the SYSMAC-C120 expansion I/O rack, use Type 3G2C4-SI027/-SI028.

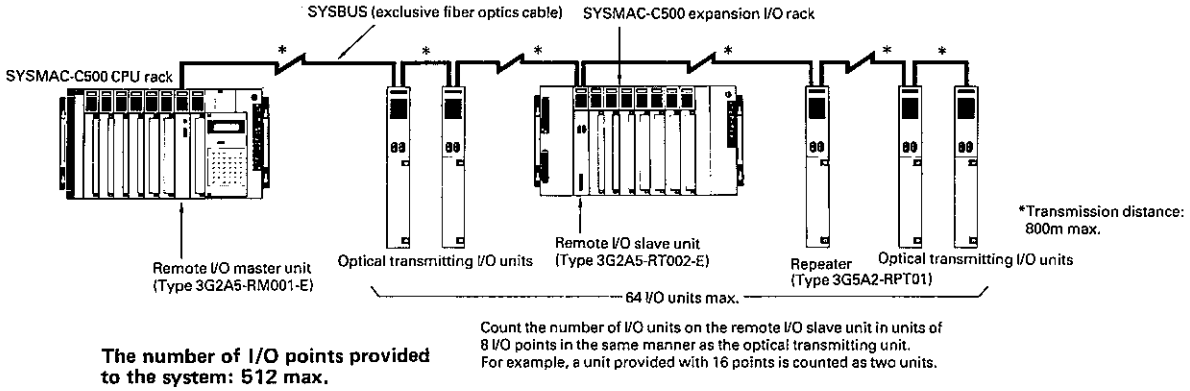
When connecting remote I/O slave unit and optical transmitting I/O units to SYSMAC-C250 via remote I/O master unit:



The remote I/O master unit can be connected to any I/O connector of the SYSMAC-C500 expansion I/O rack.

Up to two remote I/O slave units or 64 optical transmitting I/O units can be connected to a remote I/O master unit. Note, however, that I/O units cannot be connected to the SYSMAC-C250 exceeding 256 I/O points because the maximum number of I/O relays provided to the PC is 256. In terms of optical transmitting I/O unit, the maximum number of units that can be connected to the SYSMAC-C250 is 32 because eight I/O points are provided per optical transmitting I/O unit.

When connecting the remote I/O units and/or optical transmitting I/O units to the SYSMAC-C500:



The number of I/O points provided to the system: 512 max.

The remote I/O master unit can be connected to any I/O connector on the SYSMAC-C500 CPU rack or to the SYSMAC-C500 expansion I/O rack.

Up to two remote I/O slave units or 64 optical transmitting I/O units can be connected to a remote I/O master unit. Note, however, that I/O units cannot be connected to the SYSMAC-C500 exceeding 512 I/O points because the maximum number of I/O relays provided to the PC is 256. In terms of optical transmitting I/O unit, the maximum number of units that can be connected to the SYSMAC-C500 is 64 because eight I/O points are provided per optical transmitting I/O unit.

If more than 32 units of the optical transmitting and remote I/O slave units are to be connected to the programmable controller, a repeater (Type 3G5A2-RPT01) must be connected as the 33rd unit. (In this case, disregarding the number of I/O points the remote I/O slave unit possesses, count it as one unit.)

7.9.4 Diagnostic functions

The SYSMAC-C series programmable controller is manufactured with a consistent design philosophy supported by high technology for integration of components under the most advanced quality control system. As a result of these excellent manfuacturing conditions, the PC is capable of minimizing time required for troubleshooting should a failure occur. This is because the PC is provided with various diagnostic functions.

- Diagnostic functions for hardware
  (Checks CPU, I/O unit bus, and SYSBUS)
- System diagnosis
  (Checks the remote I/O unit system for correct use)

These abnormal statuses can be monitored by messages and FAL numbers displayed on the LCD of the programming console.
In addition, the PC has the special auxiliary relays, each of which is assigned to output an abnormal status. These relays associated with the user program allow the PC to provide flexible countermeasures against failure because the decision can be made whether to continue or stop the operation of the system.

LIST OF FAILURES AND ALARM OUTPUTS

	Item	Description	LED indicators on CPU rack					Message on programming console	LED indicators on remote I/O master unit		
			POWER	RUN	ERR	ALARM	OUT INH		T/R ERR	TEST OK	END RS CHK
A failure that occurs before the CPU operates	Remote power ON wait	• Power of expansion I/O rack is turned OFF. • Transmission line (SYSBUS) is disconnected.	✱	○	–	–	–	CPU WAITG	✱	–	✱
		No END station is specified.							✱	–	–
		Transmission error occurs on SYSBUS. ****							✱		–
		Failure has occurred in I/O bus of expansion I/O rack.							✱	–	–
		Failure has occurred in remote I/O slave unit or optical transmitting I/O unit.							○	○	○
		Failure has occurred in remote I/O master unit.							✱	–	–
		Wrong address has been set for remote I/O slave unit.									
A failure that does not cause the CPU to stop	Remote I/O error	• Transmission error occurs in SYSBUS. **** • SYSBUS is disconnected.	✱	–	–	✱	–	RMTE I/O ERR	✱	–	–
		• Power of remote I/O unit or optical transmitting I/O unit is turned OFF. • Failure has occurred in CPU.							✱	–	–
		Failure has occurred in I/O bus of expansion I/O rack.							✱	–	–
		Failure has occurred in remote I/O master unit.							○	○	○
	I/O verify error	• I/O unit or optical transmitting I/O unit is removed from or mounted to expansion I/O rack. • Channel number assigned to I/O unit of programmable controller and that assigned to optical transmitting I/O unit are overlapped.	✱	–	–	✱	–	I/O VER ERR	–	–	–
A failure that causes the CPU to stop	I/O setting error	Mounting positions of input and output units mounted to expansion I/O rack are exchanged.	✱	○	✱	–	–	I/O SET ERR	–	–	–
		Both optical transmitting input and output units are assigned to same channel.							–	–	–

NOTES:

* ● : illumination ○ : extinguish ○ : flashing

** Failure codes B0 to B3 are assigned to remote I/O master units in sequence starting from the unit assigned with the lowest-order channel number.

*** These numbers indicate the special auxiliary relay numbers of the PC.

**** If the same address is assigned to two remote I/O slave units or the same channel is assigned to plural optical transmitting I/O units in duplication, the data will compete for the SYSBUS. Consequently, a transmission error will frequently occur. The transmission error also occurs because of influence of external interference light when no protective cap is put on the unused of the two fiber optics connectors on the end RSU.

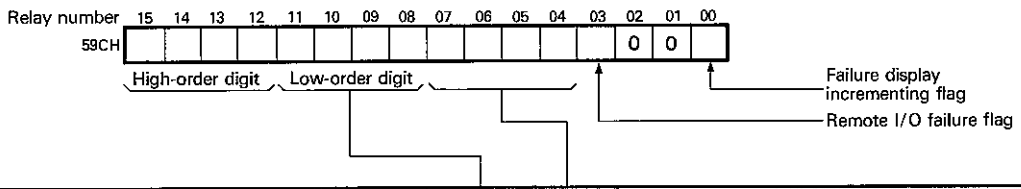
LED indicators on remote I/O slave unit		LED indicators on optical transmitting I/O unit		Special auxiliary relay	Failure code	Remedy
T/R ERR	ERR	POWER	T/R ERR			
–	–	–	–	–		Turn on power of expansion I/O rack and optical transmitting I/O unit one after another.
–	–	–	–	6112 ON ***		• Specify remote I/O slave unit or optical transmitting I/O unit assigned with the greatest channel number as end RSU. • For details on specifying end RSU, refer to 7.9.5, identifying abnormal I/O unit when transmission error occurs in SYSBUS.
–	✱	–	–	–		Check remote I/O slave unit, I/O unit, and base unit mounted to expansion I/O rack.
○	○	✱	○			Replace faulty remote I/O slave unit or optical transmitting I/O unit with new one.
–	–	–	–			Replace faulty remote I/O master unit with new one.
–	–	✱	–			• Assign address either 0 or 1 to remote I/O slave unit. • If 2 or 3 is specified as address of remote I/O slave unit, this address will be ignored.
✱	–	✱	✱	6112 ON ***	80 to B3**	When cause of failure is removed, unit will recover from abnormal state automatically. If not, replace power supply of each unit or unit itself with new one. For details on this, refer to 7.9.5, Identifying abnormal I/O unit when transmission error occurs in SYSBUS.
○	○	–	○			
–	✱	–	–			Check remote I/O slave unit, I/O unit, and expansion I/O rack.
–	–	–	–			Replace remote I/O master unit with new one.
–	–	–	–	6110 ON ***	E7	After verifying I/O table by using programming console, assign channel number to each I/O unit correctly.
–	✱	–	–		E0	After verifying I/O table by using programming console: • Return input and output units to their original mounting positions. • Generate I/O table again.
–	–	–	–			

INTERNAL AUXILIARY RELAYS AND FAILURE CODE

In case a failure of those listed in List of failures and alarm outputs in 7.9.4 occurs in any of the remote or optical transmitting I/O units connected to a SYSMAC-C series programmable controller, the abnormal unit can be identified by monitoring the internal auxiliary relays of channel number 59 of the PC.

The following figure and table show the relation between how each relay of channel number 59 is used to identify the abnormal unit and what each failure code displayed on the programming console of the controller means.

Configuration of 59CH

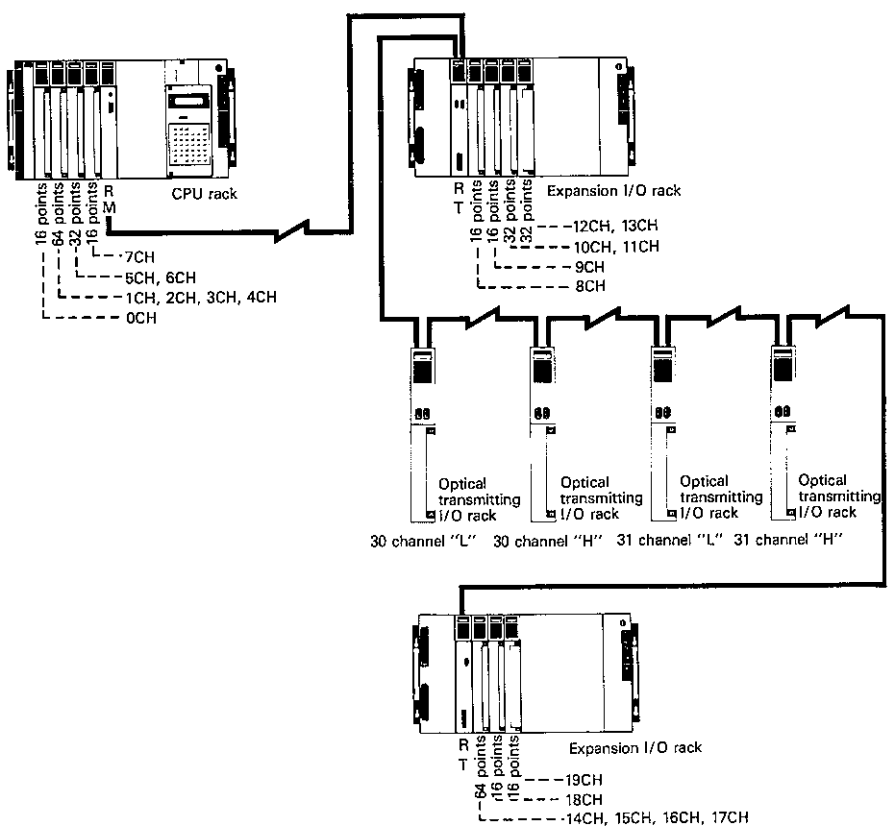


Location of failure	Meaning of failure code	Data of 59CH		Meaning of failure code
Remote I/O unit	The failure codes B0 to B3 are sequentially assigned to the remote I/O master units mounted to the CPU rack of the PC or an expansion I/O rack starting from the unit assigned with the lowest-order channel number.	B0 to B3	8	Number 8 indicates that a failure has occurred in a remote I/O master unit.
			0	Number 0 indicates that a failure has occurred in the remote I/O slave unit mounted to the expansion I/O rack number 0.
			1	Number 1 indicates that a failure has occurred in the remote I/O slave unit mounted to the expansion I/O rack number 1.
Optical transmitting I/O unit	Numbers 00 to 31 indicate the channel numbers assigned to the optical transmitting I/O unit in use.	00 to 31	0	Number 0 indicates the optical transmitting I/O unit specified as an L channel.
			1	Number 1 indicates the optical transmitting I/O unit specified as an H channel.

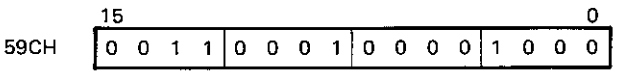
Failure display incrementing flag : When a failure has occurred in plural units, the displayed failure code can be incremented by turning this flag ON and OFF.

Remote I/O failure flag : This flag indicates that a failure has occurred in a remote I/O unit or an optical transmitting I/O unit.

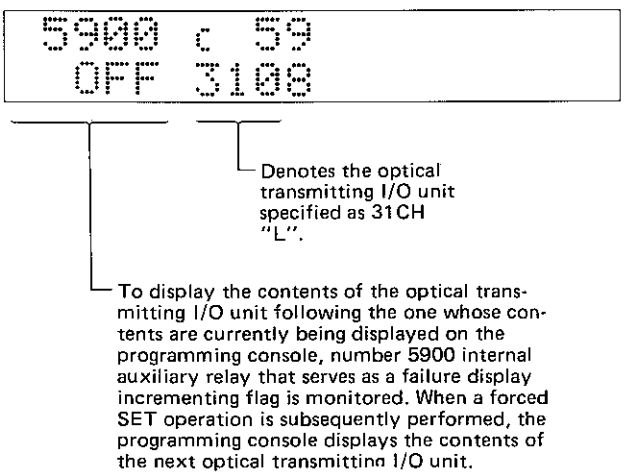
EXAMPLES OF IDENTIFYING ABNORMAL UNIT



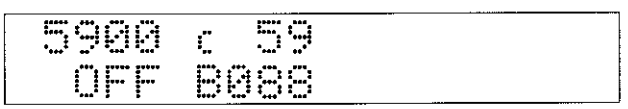
1. In the above system, if a failure occurs in the optical transmitting I/O unit specified as channel number 31 with lower-order addresses (31CH "L"), the contents of number 59 channel will be as follows.



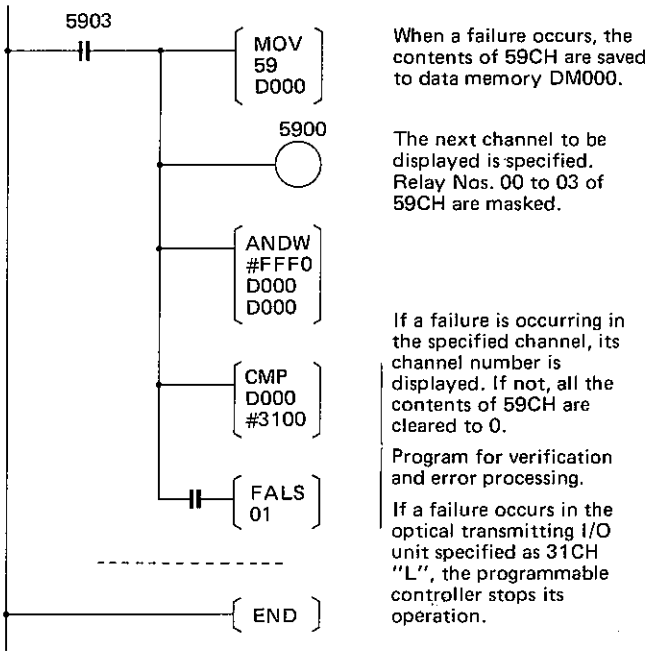
At this point, when number 59 channel is monitored by using the multipoint monitoring function of the programming console, the following message will be displayed on the console.



If a failure occurs in the remote I/O master station mounted on the CPU rack, the display becomes as follows.



2. Example of user program for failure display
The following is the user program for failure display (59CH).



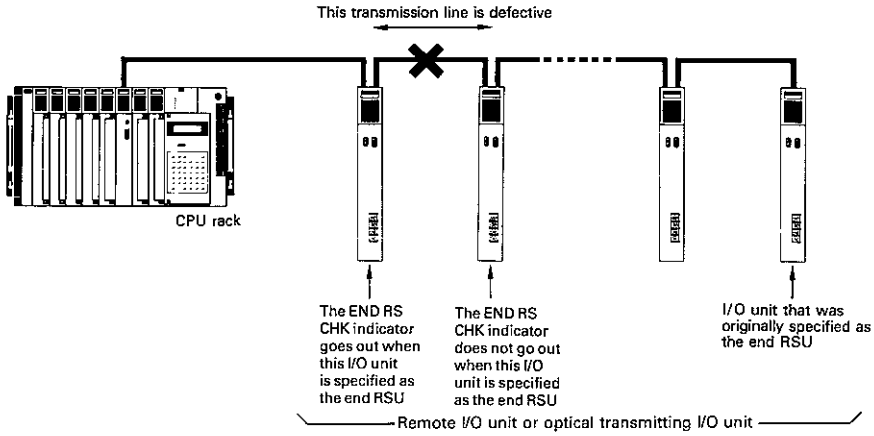
7.9.5 Identifying abnormal I/O unit when transmission error occurs in SYSBUS

FAILURE BEFORE REMOTE I/O MAIN UNIT RECOGNIZES END RSU

On some occasions, the T/R ERR indicator on the remote I/O master unit blinks while the END RS CHK indicator remains illuminated, even though the end RSU is specified. In such case, chances are that the transmission line (SYSBUS) may be disconnected, or the power of the expansion I/O rack or optical transmitting I/O unit may be turned OFF.

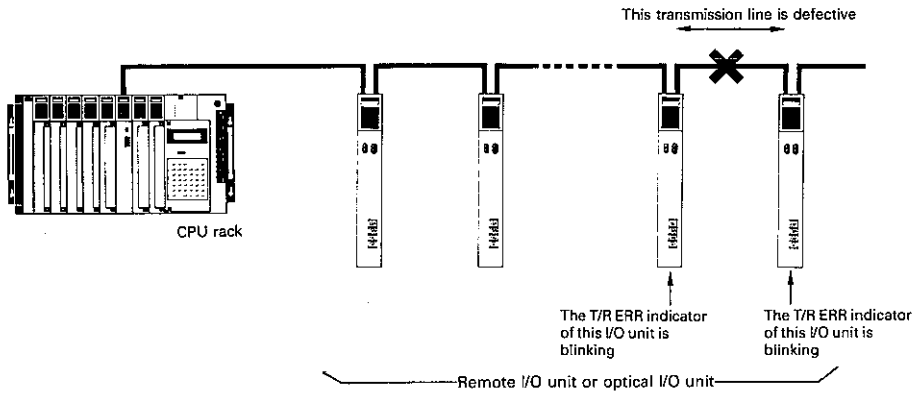
To spot the location of the failure, observe the following procedures.

1. Specify I/O unit immediately before the one specified as the end RSU.
2. Check that the END RS CHK indicator on the remote I/O master unit extinguishes.
   Repeat this procedure until the END STA CHECK indicator goes out. When the END STA CHECK indicator extinguishes, it means that the failure occurred in the transmission line between the I/O unit being specified as the end RSU when the indicator goes out and the I/O unit that was specified as the end RSU immediately before.



AFTER REMOTE I/O MAIN UNIT RECOGNIZES END RSU

Check the I/O units one after another. The failure has occurred between the I/O unit whose T/R ERR indicator is illuminating and the one whose T/R ERR indicator is blinking.



7.10 HANDLING OF FIBER OPTICS CABLE

Although the fiber optics cable possesses adequate mechanical durability, be careful not to drop any heavy object on it.

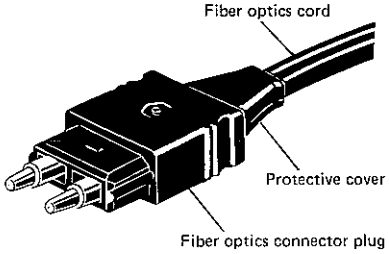
Connect or disconnect the fiber optics connector by holding its plug, and never by the fiber optics cable.

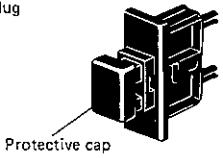
The fiber optics connector cannot be connected in the reverse direction, so confirm its direction when connecting it and be sure to insert the connector until it locks.

Be careful not to soil the connecting portion of the fiber optics connector. Place the protective cap; attached as an accessory, on the connector when not in use. Should the connector be soiled, wipe the dirt off gently with absorbent cotton soaked with ethyl alcohol or a clean tissue paper.

Do not use an organic solvent other than ethyl alcohol.

The fiber optics cable is very flexible and has a minimum bending radius of 15mm, but avoid using it with small bending radius.





CHAPTER 8
GUIDE FOR SYSTEM

8.1 HOST COMPUTER LINKAGE SYSTEM CONFIGURATION

The SYSMAC-C Series realizes an efficient as well as effective decentralized control of factory automation by linking a host computer to the PC.

CONNECTING PLURAL PROGRAMMABLE CONTROLLERS (1 TO 32) WITH ONE HOST COMPUTER SUCH AS MINICOMPUTER OR PERSONAL COMPUTER (SYSWAY)

All internally controlled data of the programmable controller such as the SYSMAC-V8, SYSMAC-C500, or SYSMAC-C250 can be transmitted to/from the host computer.

The data transmission rate is selectable from 300, 600, 1.2k, 2.4k, 4.8k, 9.6k, and 19.2k bps.

The RS-232C or RS-422 interface can be used to connect the host computer with the programmable controller.

For data transmission between the host computer and programmable controller, an exclusive synchronization is employed. Therefore, the data transmission rate of the host computer must be synchronized with that of the programmable controller.

Type 3G2A5-LK007-E/3G2A5-LK008-E host link unit must be mounted to the programmable controller (SYSMAC-C500 and SYSMAC-C250).

The number of Type 3G2A9-AL001 link adapters that serve as the distributor for the data transmission cables is determined by the number of pieces of equipment linked with the programmable controller. That is, where the number of those pieces of equipment is represented as n, n-1 link adapters are required.

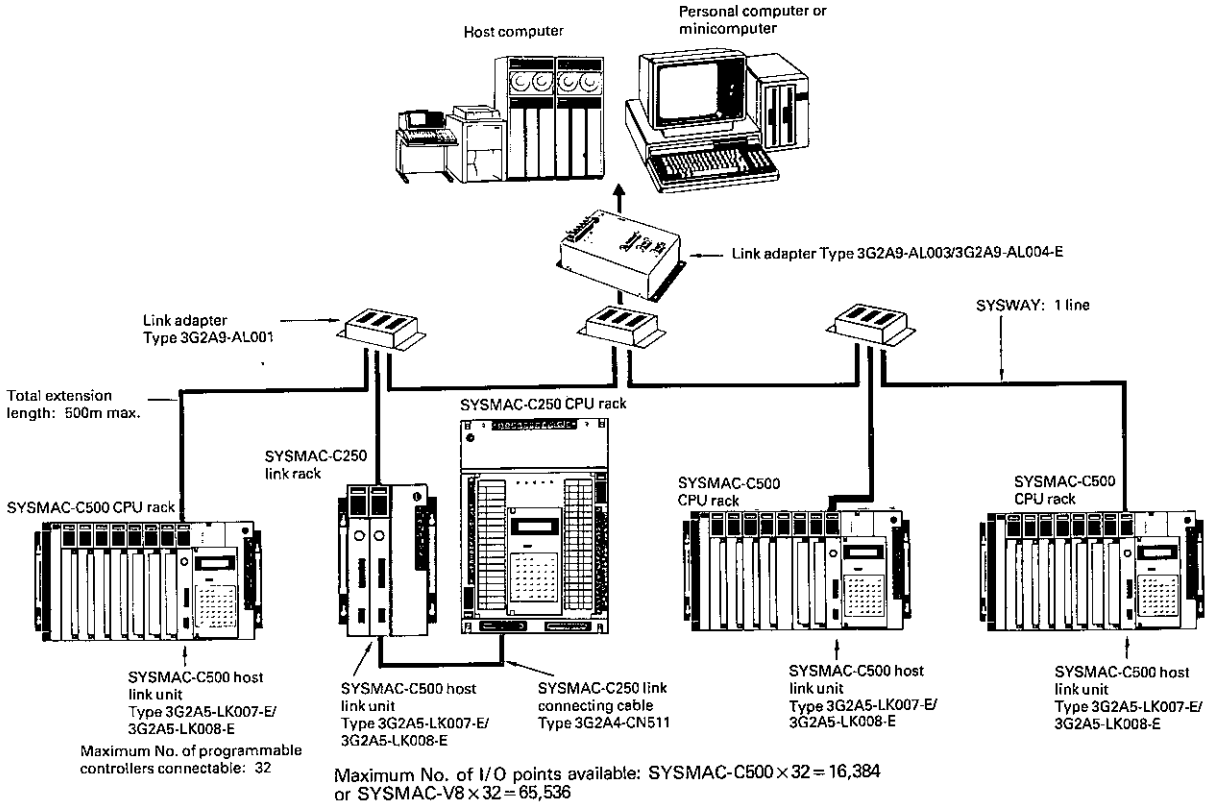
The twisted pair, shielded cable of the RS-422 interface provides an extension of 500m.

Systems configured of remote I/O, I/O, or PC link unit can be used in parallel with the system of the host computer linkage.

Be sure to use an exclusive power supply unit (Type 3G2A4-PS221-E) for the linkage rack of the SYSMAC-C250.

SYSWAY SYSTEM

Communication method: 4-wire, half duplex system
Transmission format: 1:N (RS-422) or 1:1 (RS-232C)
Transmission rate: 300, 600, 1.2k, 2.4k, 4.8k, 9.6k, or 19.2k bps selectable
Synchronization system: Start-stop synchronization system, independent synchronization system
Transmission control procedure: Exclusive control procedure (1:N) or OMRON original protocol (1:1)
Maximum No. of programmable controllers connectable: 32 (when the 1:N transmission control procedure is used)
Transmission line: Twisted pair, shielded cable



Maximum No. of I/O points available: SYSMAC-C500 × 32 = 16,384
or SYSMAC-V8 × 32 = 65,536

8.2 PROGRAMMABLE CONTROLLER LINKAGE SYSTEM CONFIGURATION

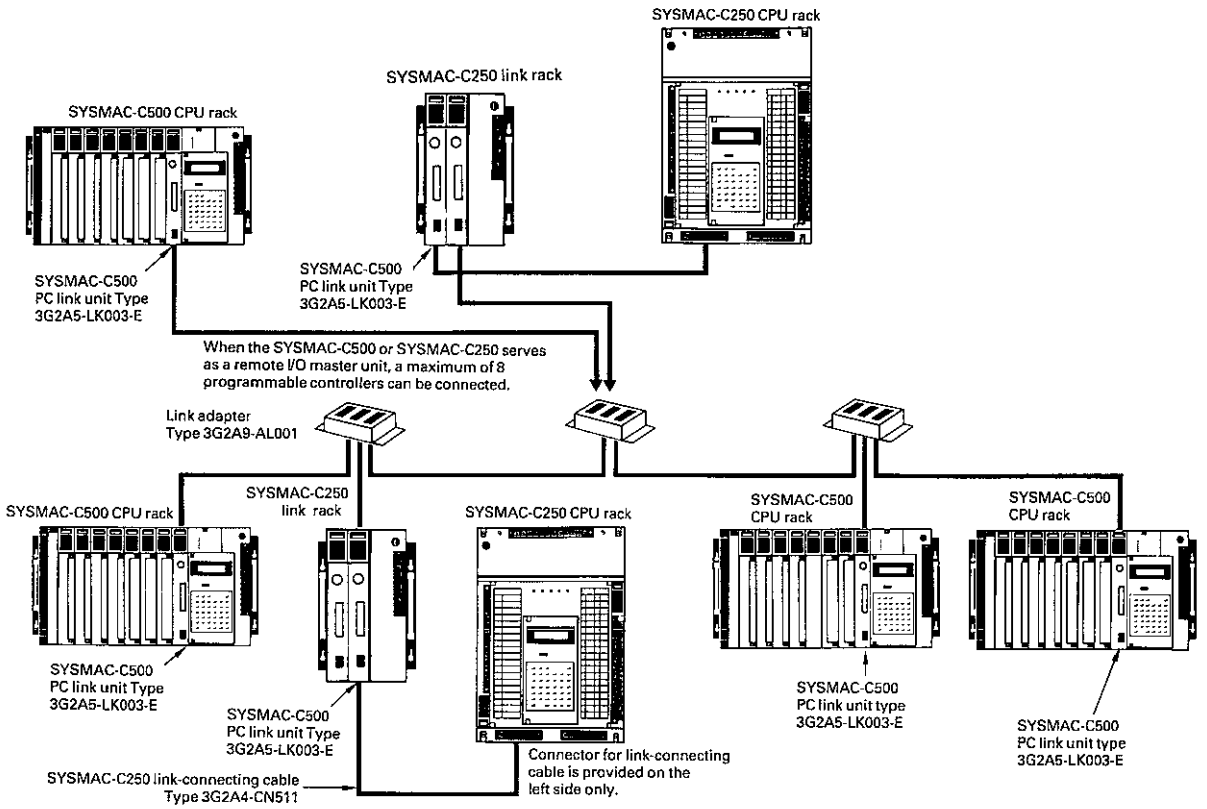
This system is designed for the purpose of decentralized control and allows data transmission between programmable controllers to be easily performed by using an exclusive relay area.

The wiring procedure has been simplified, thereby significantly reducing the installation cost.

Be sure to use an exclusive power supply unit (Type 3G2A4-PS221-E) for the link rack of the SYSMAC-C250.

Transmission rate	128k bps
Maximum no. of programmable controllers connectable	8 (when SYSMAC-C250 or SYSMAC-C500 serves as a master station)
Cable used	Twisted pair, shielded cable
Data transmission time	Approx. 25ms (64 points x 8 programmable controllers)
Transmission distance (Total cable length)	500m max. (branch cable: 10m max.)
Diagnostic functions	CPU watchdog timer, transmission error check
Maximum no. of I/O points to be transmitted (when SYSMAC-C250 or SYSMAC-C500 serves as a master station)	When 8 programmable controllers linked: 64 points/controller When 4 programmable controllers linked: 128 points/controller When 2 programmable controllers linked: 256 points/controller

NOTE: When the system is configured of SYSMAC-C series programmable controllers only, the number of controllers to be linked can be specified by using a selector switch.



8.3 I/O LINKAGE SYSTEM CONFIGURATION

The employment of fiber optics cables has improved noise-resistance of the PC resulting in higher reliability of the system.

The wiring procedure has been simplified, thereby significantly reducing the installation cost.

The maximum transmission distance between the PCs is 800m.

By using the user program of the PC to which the remote I/O master unit is mounted and the user program of the controller to which an I/O link unit is connected, the data of the I/O base can be transmitted/received among a maximum of 16 PCs.

The PC to which the remote I/O master unit is connected functions as the primary station that controls the flow of data.

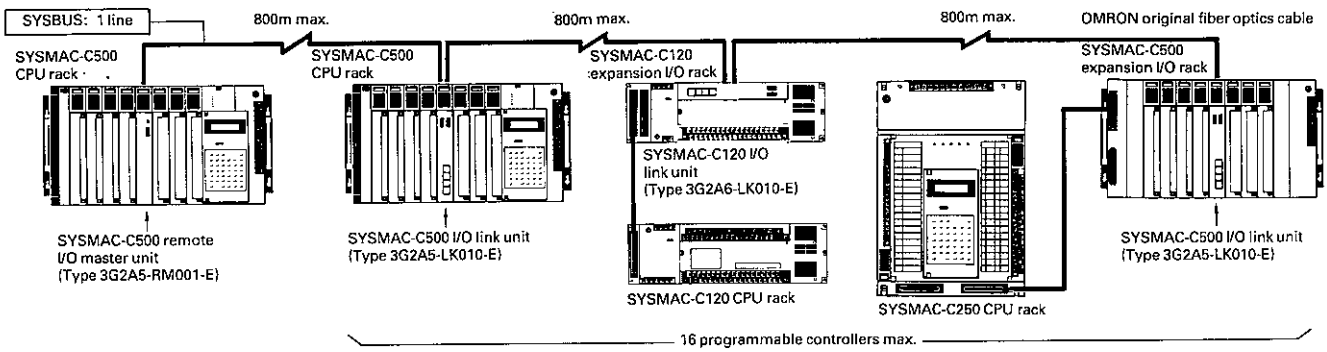
The PCs to which an I/O unit is connected functions as a secondary station that actually transmits and receives data.

The maximum number of I/O link units that can be controlled by the remote I/O master unit differs depending on the maximum number of I/O points provided to the PC to which the remote I/O master unit is connected and the number of I/O points of each I/O link unit connected.

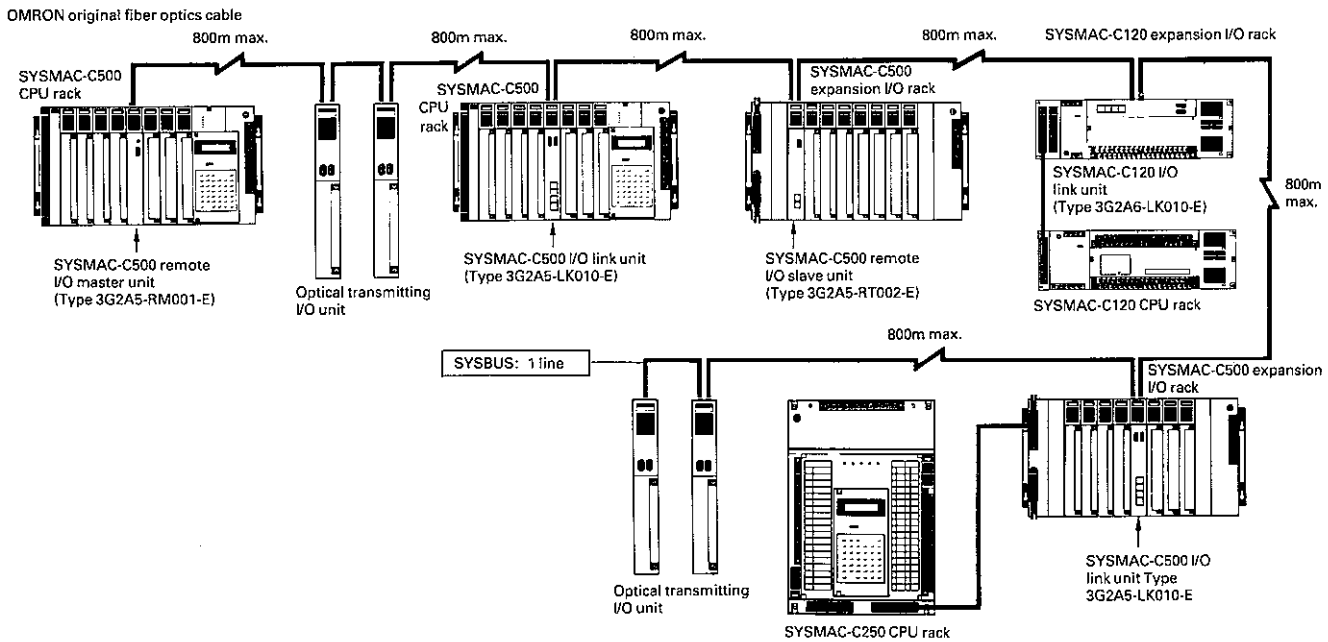
The number of the I/O link units is determined as follows:

The maximum number of I/O points of the programmable controller to which the remote I/O master unit is mounted $\geqq$ the total number of I/O points of each I/O link unit connected.

CONNECTING I/O LINK UNITS ONLY TO REMOTE I/O MASTER UNIT (SYSBUS):



CONNECTING I/O LINK UNIT, OPTICAL TRANSMITTING I/O UNIT, AND REMOTE I/O SLAVE UNIT TO REMOTE I/O MASTER UNIT (SYSBUS):



SYSBUS SYSTEM

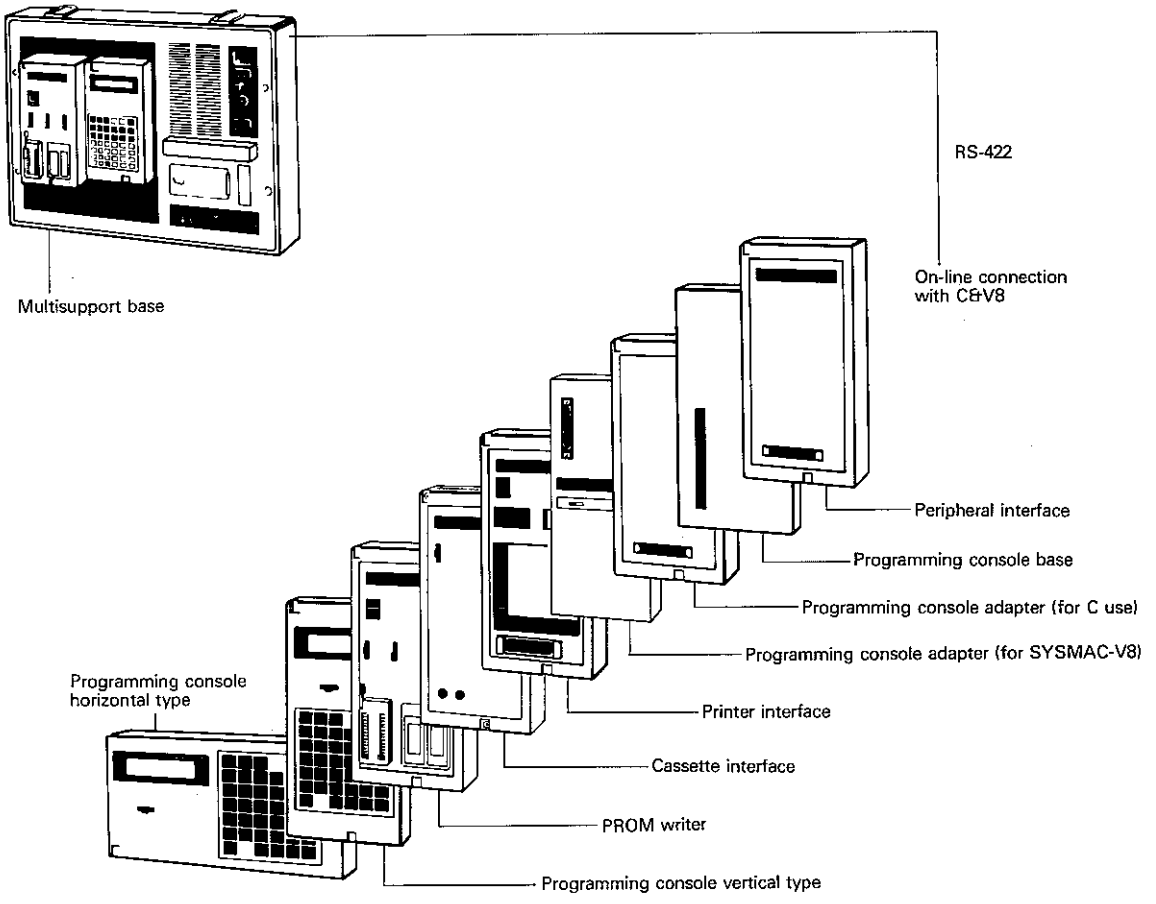
Communication method: Bidirectional, half-duplex
Transmission format: 1:N
Transmission rate: 187.5k bps
Transmission system: TDM (Time Division Multiplex system)
Synchronization: Start-stop synchronization
Transmission control procedure: Exclusive transmission (cyclic control system)
Maximum number of programmable controllers connectable: 64 (transmission capacity: 8 points/unit)
Transmission cable: 2-core fiber optics cable (quartz-polymer, 250μm dia. core)

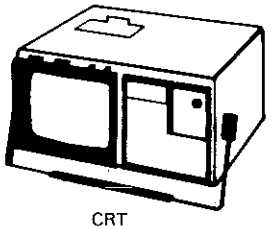
CHAPTER 9
PERIPHERAL EQUIPMENT

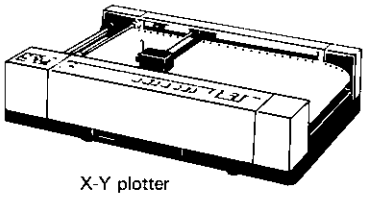
9.1 AVAILABLE TYPES

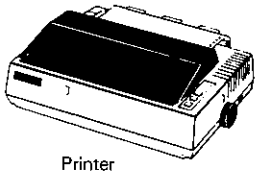
Product name	Specifications		Type	Weight
Multisupport base	• Supply voltage: AC 110/120V • No. of pieces of peripheral equipment that can be mounted: 2 max. • Programmable controller connectable • Memory cassette (option)		3G2A5-MSB01-E	8kg max.
	• Supply voltage: AC 220/240V • No. of pieces of peripheral equipment that can be mounted: 2 max. • Programmable controller connectable • Memory cassette (option)		3G2A5-MSB02-E	8kg max.
Programming console	Vertical type (for SYSMAC-C500 and SYSMAC-C250) • Current consumption: 260mA max.		3G2A5-PRO13-E	400g max.
	Horizontal type (for SYSMAC-C120) • Current consumption: 260mA max.		3G2A6-PRO15-E	400g max.
Programming console adapter	Connect this adapter to the PC when the programming console is connected to the controller via a connecting cable.		3G2A5-AP001-E	400g max.
Programming console base	Mount this base to the programming console when the programming console is connected to the controller via a connecting cable.		3G2A5-BP001	400g max.
PROM writer	For PROM, ROM-GA (2732A), ROM-H (2764), ROM-I (27128) • Current consumption: 850mA max.		3G2A5-PRW04-E	540g max.
Printer interface	Interface for X-Y plotter or printer • Memory cassette (option) • Current consumption: 400mA max.		3G2A5-PRT01-E	540g max.
Peripheral interface	Interface between programmable controller and graphic programming console (CRT) or multisupport base (MSB)		3G2A5-IP001-E	400g max.
Cassette interface	For SYSMAC-V8, SYSMAC-M1R, SYSMAC-M5R, SYSMAC-P0R, and SYSMAC-S6 • Current consumption: 160mA max.		3G2A5-CMT01-E	400g max.
Programming console adapter	For SYSMAC-V8 programming console or MSB interface		3G2A5-AP002	400g max.
Memory cassette for multisupport base	For SYSMAC-C Series (ladder diagram)		3G2A5-MP001-E	100g max.
Memory cassette for printer interface	For SYSMAC-C Series (ladder diagram)		3G2A5-MP002-E	200g max.
	For SYSMAC-M1R or SYSMAC-M5R		3G2A5-MP003-E	200g max.
	For SYSMAC-P0R		3G2A5-MP004-E	200g max.
	For SYSMAC-S6		3G2A5-MP005-E	200g max.
	For SYSMAC-V8		3G2A5-MP006-E	200g max.
Graphic programming console	For SYSMAC-C Series (ladder diagram) • Keyboard unit • Memory cassette mounted	AC 100/110/120V	3G2A5-CRT19	20kg max.
		AC 220/240V	3G2A5-CRT20	20kg max.
Spare parts required to modify CRT 10 into 3G2A5-CRT19/20	Keyboard unit for CRT of C series (incl. 3G2A5-CMP01)		3G2A5-CKB19	1kg max.
	Memory cassette		3G2A5-CMP01	500g max.
	Character generator ROM		3G2A5-CCG01	
	PC board of RAM mounting		3G2A2-CMB01	
	Connecting interface board		3G2A2-CIB12	
Programming console connecting cable	2m (for programming console, CRT, multisupport base, and SYSMAC-V8)		3G2A2-CN221	350g max.
Printer connecting cable	2m (also for X-Y plotter)		SCY-CN201	220g max.
Cassette deck connecting cord	1.5m		SCYP0R-PLG01	50g max.

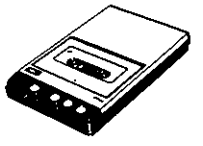
9.2 APPEARANCE



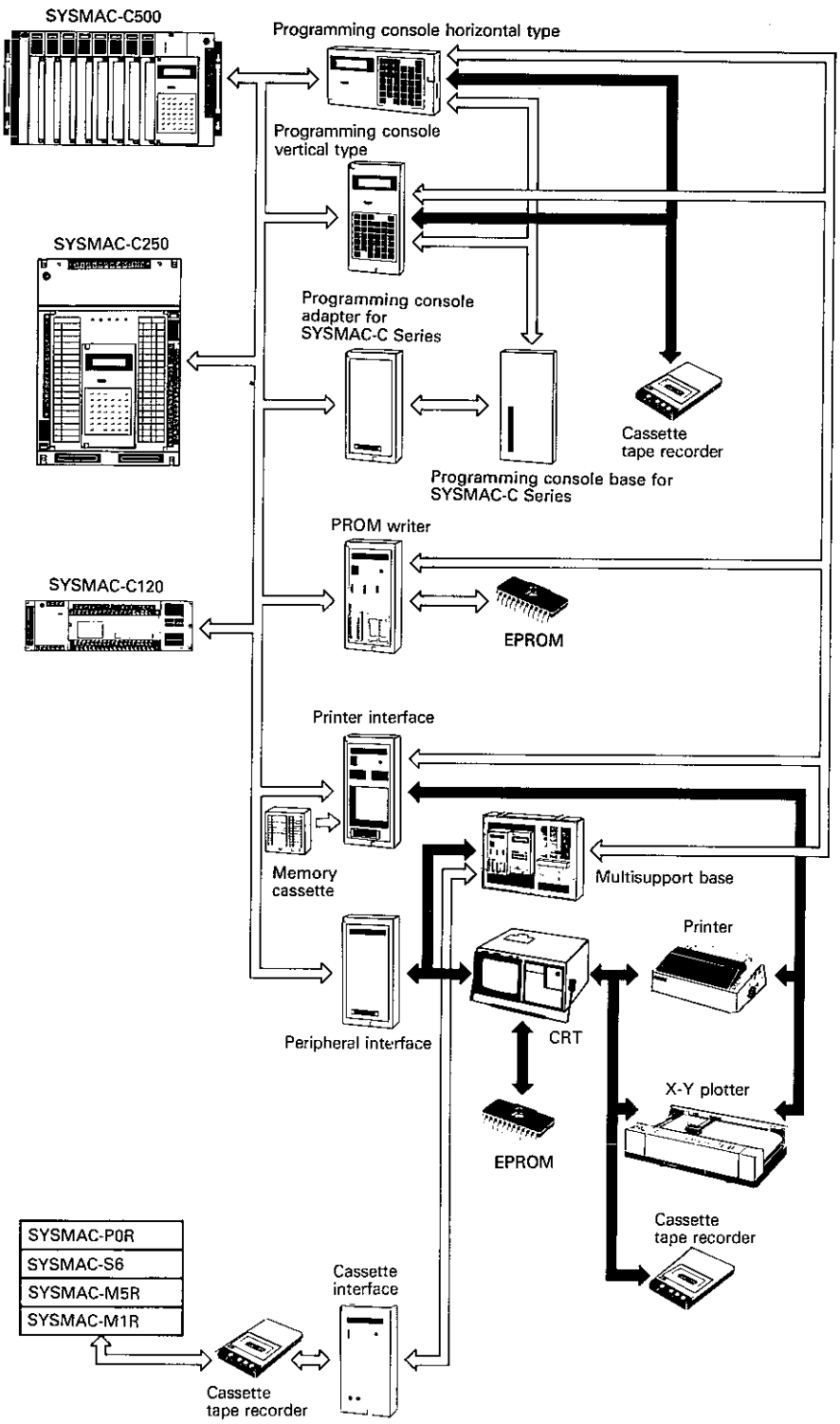

CRT


X-Y plotter


Printer


Cassette tape recorder

9.3 CONNECTIONS



9.4 AVAILABLE FUNCTIONS

Item	Program read/write	Program monitoring or debugging in RUN mode	When detaching console from PC	Storing program in EPROM chip	Hardcopy printout by using X-Y plotter or printer		Saving data to cassette tape
					SYSMAC-C Series	SYSMAC-M1R, M5R, -F0R, -S6, and -V8	
Programming console	0	0	0				0
Graphic programming console (CRT)	0	0					0
Programming console adapter			0				
Programming console base			0				
PROM writer				0			
Printer interface					0	0	
Peripheral interface	0	0					
Cassette interface						0	
Multisupport base	0	0				0	

------ A peripheral interface is needed to connect the graphic programming console and multisupport base to the PC connected on-line.

- Printer
  EPSON terminal printer (Model MX-80 TYPE II/III or Model RX-80)
- X-Y plotter (manufactured by GRAPHTEC CORP.)
  Models WX4638R, WX4731, MP1000, WX4675, or WX4631R
- Cassette tape recorder (commercially available)

APPENDIX A
LIST OF RELAY NUMBERS

Name	No. of points	Relay number															
		0000 to 3115															
		00CH	01CH	02CH	03CH	04CH	05CH	06CH	07CH	08CH	09CH	10CH	11CH	12CH	13CH	14CH	15CH
Input/output relay	256	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
		01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
		02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
		03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
		04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04
		05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05
		06	06	06	06	06	06	06	06	06	06	06	06	06	06	06	06
		07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
		08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
		09	09	09	09	09	09	09	09	09	09	09	09	09	09	09	09
		10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
		11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
		12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
		13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13
		14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
		15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15

NOTE: Relays 1600 to 3115 (i.e., 256 points), in other words, relays of channels 16 to 31 can be used as internal auxiliary relays.

Name	No. of points	Relay number															
		3200 to 6010															
		32CH	33CH	34CH	35CH	36CH	37CH	38CH	39CH	40CH	41CH	42CH	43CH	44CH	45CH	46CH	47CH
		00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
		01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
		02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
		03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
		04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04
		05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05
		06	06	06	06	06	06	06	06	06	06	06	06	06	06	06	06
		07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
		08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
		09	09	09	09	09	09	09	09	09	09	09	09	09	09	09	09
		10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
		11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
		12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
		13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13
		14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
Internal auxiliary relay	459	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15
		48CH	49CH	50CH	51CH	52CH	53CH	54CH	55CH	56CH	57CH	58CH	59CH	60CH	61CH	62CH	63CH
		00	00	00	00	00	00	00	00	00	00	00	00	00			
		01	01	01	01	01	01	01	01	01	01	01	01	01			
		02	02	02	02	02	02	02	02	02	02	02	02	02			
		03	03	03	03	03	03	03	03	03	03	03	03	03			
		04	04	04	04	04	04	04	04	04	04	04	04	04			
		05	05	05	05	05	05	05	05	05	05	05	05	05			
		06	06	06	06	06	06	06	06	06	06	06	06	06			
		07	07	07	07	07	07	07	07	07	07	07	07	07			
		08	08	08	08	08	08	08	08	08	08	08	08	08			
		09	09	09	09	09	09	09	09	09	09	09	09	09			
		10	10	10	10	10	10	10	10	10	10	10	10	10			
		11	11	11	11	11	11	11	11	11	11	11	11				
		12	12	12	12	12	12	12	12	12	12	12	12				
		13	13	13	13	13	13	13	13	13	13	13	13				
		14	14	14	14	14	14	14	14	14	14	14	14				
		15	15	15	15	15	15	15	15	15	15	15	15				

* 59CH is used for diagnostic operations related to the remote I/O units only when the 59CH is in use. Refer to 7.7, Remote I/O unit in Part 2 for details.

Name	No. of points	Relay No.		Description	
Special auxiliary relay	45	60 CH	6011	This relay turns ON when the FUN99 (STOP) instruction is executed and indicates that a power failure has occurred in the input power supply.	These relays can be turned ON or OFF by an OUT or OUT-NOT instruction.
			6012	This relay serves as a data retention flag. When it is turned ON, the data of I/O relays, internal auxiliary relays, and link relays are retained and when it is turned OFF, those data are all cleared on starting the RUN operation. This relay functions only when the operation mode of the PC is changed from PROGRAM to MONITOR or RUN.	
			6013	*3	
			6014	*2	
			6015	This relay serves as a LOAD OFF flag. If it is turned ON, all outputs will be turned OFF, and if this flag is turned OFF, all outputs will continue.	
		61 CH	6100 6101 6102 6103	1 2 4 8 × 10^0	When the FAL or FALS (diagnostic) instruction is executed, the FAL No. (01 to 99) is output in each of these relay numbers.	Input only
			6104 6105 6106 6107	1 2 4 8 × 10^1		
			6108	This relay turns ON when the battery in the CPU is abnormal.	
			6109	This relay turns ON when the scan time of user program exceeds 100msec.	
			6110	This relay turns ON when the number of I/O units mounted disagrees with that registered.	
			6111	*3	
			6112	*1	
			6113	This relay is normally ON.	
			6114	This relay is normally OFF.	
			6115	This relay operates only one scan time at the beginning of the operation.	
		62 CH	6200 6201 6202 6203 6204 6205 6206 6207 6208 6209 6210 6211 6212 6213 6214 6215	*2	
		63 CH	6300	This relay is used to generate 0.1-sec clock pulse.	
			6301	This relay is used to generate 0.2-sec clock pulse.	
			6302	This relay is used to generate 1.0-sec clock pulse.	
			6303	This relay turns ON when the result of an arithmetic operation is not output in BCD or when an error is detected in indirectly addressed data (error flag).	
			6304	This relay turns ON if a carry exists in the result of an arithmetic operation (carry flag).	
			6305	This relay turns ON if the result when the Compare (CMP) instruction is executed is more than (> flag).	
			6306	This relay turns ON if the result when the Compare (CMP) instruction is executed is equal or 0 (= flag).	
			6307	This relay turns ON if the result when the Compare (CMP) instruction is executed is less than (< flag).	
Temporary memory relay	8	TR	0	Temporary memory relay 0	These relays are used with an LD or OUT instruction.
			1	Temporary memory relay 1	
			2	Temporary memory relay 2	
			3	Temporary memory relay 3	
			4	Temporary memory relay 4	
			5	Temporary memory relay 5	
			6	Temporary memory relay 6	
			7	Temporary memory relay 7	

NOTE: For function details and use of relays
*1 to *3, refer to the following.
*1 — 7.7, Remote I/O unit in Part 2.
*2 — User's manual for PC link unit
*3 — User's manual for Host link unit

Name	No. of points	Relay number															
		LR0000 to 3115															
		00CH	01CH	02CH	03CH	04CH	05CH	06CH	07CH	08CH	09CH	10CH	11CH	12CH	13CH	14CH	15CH
		00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
		01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
		02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
		03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
		04	04	04	04	04	04	04	04	04	04	04	-04	04	04	04	04
		05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05
		06	06	06	06	06	06	06	06	06	06	06	06	06	06	06	06
		07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
		08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
		09	09	09	09	09	09	09	09	09	09	09	09	09	09	09	09
		10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
		11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
		12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
		13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13
		14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
		15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15
Link relay	512	16CH	17CH	18CH	19CH	20CH	21CH	22CH	23CH	24CH	25CH	26CH	27CH	28CH	29CH	30CH	31CH
		00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
		01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
		02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
		03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
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		05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05
		06	06	06	06	06	06	06	06	06	06	06	06	06	06	06	06
		07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
		08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
		09	09	09	09	09	09	09	09	09	09	09	09	09	09	09	09
		10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
		11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
		12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
		13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13
		14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
		15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15

NOTE: If no PC link unit is used, the link relays can be used as internal auxiliary relays.
For details on how to use these relays, refer to the user's manual for the PC link unit.

Name	No. of points	Relay number															
		HR0000 to 3115															
		00CH	01CH	02CH	03CH	04CH	05CH	06CH	07CH	08CH	09CH	10CH	11CH	12CH	13CH	14CH	15CH
		00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
		01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
		02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
		03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
		04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04
		05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05
		06	06	06	06	06	06	06	06	06	06	06	06	06	06	06	06
		07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
		08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
		09	09	09	09	09	09	09	09	09	09	09	09	09	09	09	09
		10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
		11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
		12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
		13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13
Holding relay (This relay retains the data during a power failure)	512	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
		15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15
		16CH	17CH	18CH	19CH	20CH	21CH	22CH	23CH	24CH	25CH	26CH	27CH	28CH	29CH	30CH	31CH
		00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
		01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
		02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
		03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
		04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04
		05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05
		06	06	06	06	06	06	06	06	06	06	06	06	06	06	06	06
		07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
		08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
		09	09	09	09	09	09	09	09	09	09	09	09	09	09	09	09
		10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
		11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
		12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
		13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13
		14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
		15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15

Name	No. of points	Timer/counter numbers												
		TIM.CNT000 to 127												
		000	010	020	030	040	050	060	070	080	090	100	110	120
		001	011	021	031	041	051	061	071	081	091	101	111	121
		002	012	022	032	042	052	062	072	082	092	102	112	122
		003	013	023	033	043	053	063	073	083	093	103	113	123
Timer/counter	128	004	014	024	034	044	054	064	074	084	094	104	114	124
		005	015	025	035	045	055	065	075	085	095	105	115	125
		006	016	026	036	046	056	066	076	086	096	106	116	126
		007	017	027	037	047	057	067	077	087	097	107	117	127
		008	018	028	038	048	058	068	078	088	098	108	118	
		009	019	029	039	049	059	069	079	089	099	109	119	

NOTES: 1. Because the same timer or counter number is shared by the TIM, TIMH, CNT, and CNTR instructions, no timer or counter number can be assigned to those instructions in duplication. Therefore do not program a circuit in which timers or counters having the same number may be simultaneously turned on.
2. When a power failure occurs, the data in the area used by a counter instruction (CNT or CNTR) is retained.

Name	No. of Points	Data memory number															
		DM000 to 511															
Data memory	512 x 16 bit	000	010	020	030	040	050	060	070	080	090	100	110	120	130	140	150
		001	011	021	031	041	051	061	071	081	091	101	111	121	131	141	151
		002	012	022	032	042	052	062	072	082	092	102	112	122	132	142	152
		003	013	023	033	043	053	063	073	083	093	103	113	123	133	143	153
		004	014	024	034	044	054	064	074	084	094	104	114	124	134	144	154
		005	015	025	035	045	055	065	075	085	095	105	115	125	135	145	155
		006	016	026	036	046	056	066	076	086	096	106	116	126	136	146	156
		007	017	027	037	047	057	067	077	087	097	107	117	127	137	147	157
		008	018	028	038	048	058	068	078	088	098	108	118	128	138	148	158
		009	019	029	039	049	059	069	079	089	099	109	119	129	139	149	159
		160	170	180	190	200	210	220	230	240	250	260	270	280	290	300	310
		161	171	181	191	201	211	221	231	241	251	261	271	281	291	301	311
		162	172	182	192	202	212	222	232	242	252	262	272	282	292	302	312
		163	173	183	193	203	213	223	233	243	253	263	273	283	293	303	313
		164	174	184	194	204	214	224	234	244	254	264	274	284	294	304	314
		165	175	185	195	205	215	225	235	245	255	265	275	285	295	305	315
		166	176	186	196	206	216	226	236	246	256	266	276	286	296	306	316
		167	177	187	197	207	217	227	237	247	257	267	277	287	297	307	317
		168	178	188	198	208	218	228	238	248	258	268	278	288	298	308	318
		169	179	189	199	209	219	229	239	249	259	269	279	289	299	309	319
		320	330	340	350	360	370	380	390	400	410	420	430	440	450	460	470
		321	331	341	351	361	371	381	391	401	411	421	431	441	451	461	471
		322	332	342	352	362	372	382	392	402	412	422	432	442	452	462	472
		323	333	343	353	363	373	383	393	403	413	423	433	443	453	463	473
		324	334	344	354	364	374	384	394	404	414	424	434	444	454	464	474
		325	335	345	355	365	375	385	395	405	415	425	435	445	455	465	475
		326	336	346	356	366	376	386	396	406	416	426	436	446	456	466	476
		327	337	347	357	367	377	387	397	407	417	427	437	447	457	467	477
		328	338	348	358	368	378	388	398	408	418	428	438	448	458	468	478
		329	339	349	359	369	379	389	399	409	419	429	439	449	459	469	479
		480	490	500	510												
		481	491	501	511												
		482	492	502													
		483	493	503													
		484	494	504													
		485	495	505													
		486	496	506													
		487	497	507													
		488	498	508													
		489	499	509													

NOTE: The contents of the data memories are retained during a power failure.

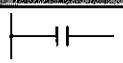
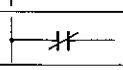
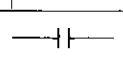
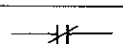
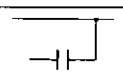
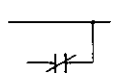
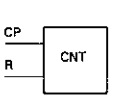
A data memory consists of 16 bits.

000	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
001	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
002	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
003	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
510	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
511	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NOTES:
1. *The data memories cannot be used with bit designation instruction (for example, LD, AND, OR, OUT) or SFT instruction.*
2. *The data memories can be specified indirectly.*

APPENDIX B
LIST OF INSTRUCTIONS

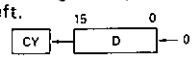
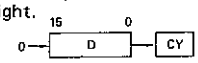
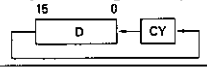
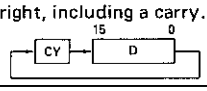
BASIC INSTRUCTION

Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
LOAD		4	LD	Relay No.	Logical start operation	Relay No. Input/output relays Internal auxiliary relays 0000 to 6307 Link relays LR0000 to 3115 Holding relays HR0000 to 3115 Timers TIM000 to 127 Counters CNT000 to 127 Temporary memory relays TR0 to 7 (Temporary memory relays can only be used with the LD instruction.)	4-1
LOAD NOT		4	LD NOT	Relay No.	Logical NOT start operation		4-1
AND		3	AND	Relay No.	Logical AND operation		4-1
AND NOT		3	AND NOT	Relay No.	Logical AND NOT operation		4-1
OR		3	OR	Relay No.	Logical OR operation		4-1
OR NOT		3	OR NOT	Relay No.	Logical OR NOT operation		4-1
AND LOAD		5	AND LD		Logical AND operation with the previous condition	—	4-2
OR LOAD		5	OR LD		Logical OR operation with the previous condition		4-3
OUT		6	OUT	Relay No.	Outputs the result of a logical operation to the specified output relay, internal auxiliary relay, latching relay, or shift register.	Relay No. 0000 to 6015 LR0000 to 3115 HR0000 to 3115 TR0 to 7 (Temporary memory relays can be used with the OUT instruction only.)	4-1
OUT NOT		8	OUT NOT	Relay No.	Inverts the result of a logical operation and then outputs it to a specified output relay, internal auxiliary relay, holding relay, or shift register.		4-1
TIMER		8	TIM	Timer No. Set value	ON-delay timer operation Set time: 0 to 999.9 sec	Timers/counters 000 to 127 Set value Constant 0000 to 9999 External setting 00 to 63 LR00 to 31 HR00 to 31	4-3
COUNTER		8	CNT	Counter No. Set value	Down counter operation Set value: 0 to 9999		4-5

APPLIED INSTRUCTIONS

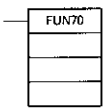
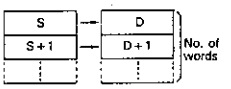
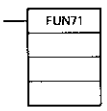
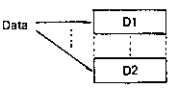
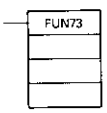
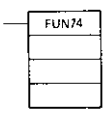
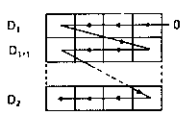
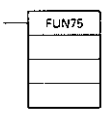
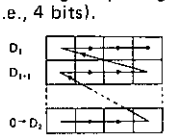
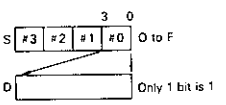
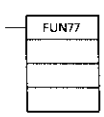
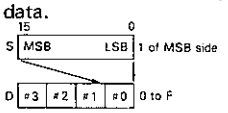
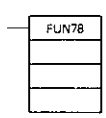
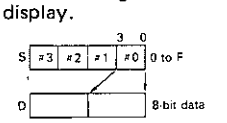
FUN No.	Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
00	NO FUNCTION		3	NOP (FUN00)		–	–	–
01	END	END	3	END (FUN01)		End of a program		4-7
02	INTERLOCK	IL	4	IL (FUN02)		Causes all the relay coils between this instruction and the ILC instruction to be reset or not reset according to the result immediately before this instruction.	–	4-7
03	INTERLOCK CLEAR	ILC	4	ILC (FUN03)		Clears the IL instruction.		4-7
04	JUMP	JMP	4	JMP (FUN04)		Causes all the contents of a program between this instruction and the JME instruction to be ignored or executed according to the result immediately before this instruction.	–	4-8
05	JMP END	JME	4	JME (FUN05)		Clears the JMP instruction.		4-8
06	FAIL RESET	FAL 00	6	FAL (FUN06)	00	Clears FAL or FALS instructions or alarm indications.	Content of an alarm is cleared at one scanning.	4-9
06	DIAGNOSTIC (FAL)	FAL	6	FAL (FUN06)	No.	Indicates the type of failure or abnormal mode.	No. 01 to 99	4-9
07	DIAGNOSTIC (FALS)	FALS	6	FALS (FUN07)	No.	Indicates the type of failure or abnormal mode that causes the PC to stop its operation.		
10	SHIFT REGISTER	IN, CP, R, SFT	8	SFT (FUN10)	Start CH-No. CH-No. End	Shift register operation 15 0 15 0 End CH ... Start CH ← IN	Channel Numbers 00 to 60 LR00 to 31 HR00 to 31 * Start CH ≤ End CH * Start and end channels can be used at same area.	4-10
11	LATCHING RELAY	S, KEEP, R	6	KEEP (FUN11)	Relay No.	Latching relay operation	Relay No. 0000 to 6015 LR0000 to 3115 HR0000 to 3115	4-11
12	UP-DOWN COUNTER	ACP, SCP, R, CNTR	8	CNTR (FUN12)	Counter No. Set value	Up-down counter operation Set value: 0000 to 9999	Timer/counters 000 to 127 Set value Constant 0000 to 9999 External setting 00 to 63 LR00 to 31 HR00 to 31	4-12

FUN No.	Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
13	DIFFERENTIATION UP	DIFU	6	DIFU (FUN13)	Relay No.	Causes a specified relay to operate for one scan time at the leading edge of the result of a logical arithmetic operation.	Relay No. 0000 to 6015 LR0000 to 3115 HR0000 to 3115	4-13
14	DIFFERENTIATION DOWN	DIFD	6	DIFD (FUN14)	Relay No.	Causes a specified relay to operate for one scan time at the trailing edge of the result of logical arithmetic operation.		
15	HIGH-SPEED TIMER	TIMH	8	TIMH (FUN15)	Timer No. Set value	Performs a high-speed on-delay (down type) timer operation. Set time: 00.00 to 99.99 sec	Timers/counters 000 to 127 Set value Constant 0000 to 9999 External setting 00 to 63 LR00 to 31 HR00 to 31	4-14
16	WORD SHIFT	WSFT	8	WSFT (FUN16)	D1 D2	Shifts words by I/O channel data unit (i.e., 16 bits). Data "0" → D1 … D2	D1 , D2 Same as MOVE instruction * Start CH ≤ End CH * Start and end channels can be used at same area.	4-14
20	COMPARE	CMP	8	CMP (FUN20)	S1 S2	Compares a channel data or a 4-digit constant against another channel data. $S_1 \lessgtr S_2$	S , S1 , S2 Input/output relays Internal auxiliay relays 00 to 63 Link relays LR00 to 31 Holding relays HR00 to 31 Timers TIM00 to 127 Counters CNT000 to 127 Data memory DM000 to 511 Indirectly addressed *DM000 to 511 Constant 0000 to FFFF	4-15
21	MOVE	MOV	8	MOV (FUN21)	S D	Transfers a channel data or a 4-digit constant (16 bits) to a specified channel. S → D		4-16
22	MOVE NOT	MVN	8	MVN (FUN22)	S D	Inverts a channel data or a 4-digit constant and transfers it to a specified channel. $\overline{S} \rightarrow D$	D 00 to 60 LR00 to 31 HR00 to 31 DM000 to 511 *DM000 to 511	4-16
23	BCD-TO-BIN CONVERSION (BIN)	BIN	8	BIN (FUN23)	S D	Converts BCD data into binary data. S → D (BCD) (BIN)	S 00 to 63 LR00 to 31 HR00 to 31 TIM/CNT000 to 127 DM000 to 511 *DM000 to 511 * TIM/CNT can be used with BCD-TO-BIN conversion instruction only. D Same as MOV instruction.	4-17
24	BIN-TO-BCD CONVERSION (BCD)	BCD	8	BCD (FUN24)	S D	Converts binary data into BCD data. S → D (BIN) (BCD)		4-18

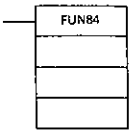
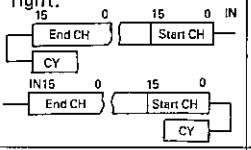
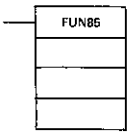
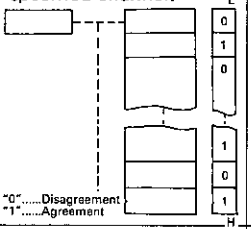
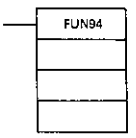
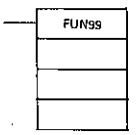
FUN No.	Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
25	ARITH-METIC SHIFT LEFT	ASL	7	ASL (FUN25)	D	Shifts a channel data including a carry to the left. 	D 00 to 60 LR00 to 31 HR00 to 31 DM000 to 511 *DM000 to 511	4-19
26	ARITH-METIC SHIFT RIGHT	ASR	7	ASR (FUN26)	D	Shifts a channel data including a carry to the right. 		4-20
27	ROTATE LEFT	ROL	7	ROL (FUN27)	D	Rotates a channel data left, including a carry. 		4-20
28	ROTATE RIGHT	ROR	7	ROR (FUN28)	D	Rotates a channel data right, including a carry. 		4-21
29	COMPLE-MENT	COM	7	COM (FUN29)	D	Inverts a channel data (16-bit) $\overline{D} \rightarrow D$		4-22
30	ADD	ADD	10	ADD (FUN30)	S1 S2 D	Performs BCD addition of a channel data or a 4-digit constant to a specified channel data. $S_1 + S_2 + CY$ $= D, CY$	S1 S2 00 to 63 LR00 to 31 HR00 to 31 TIM/CNT000 to 127 DM000 to 511 *DM000 to 511 Constant 0000 to 9999 D Same as MOVE instruction.	4-22
31	SUBTRACT	SUB	10	SUB (FUN31)	S1 S2 D	Performs BCD subtraction of a channel data or a 4-digit constant from a specified channel data. $S_1 - S_2 - CY$ $= D, CY$		4-23
32	MULTIPLY	MUL	10	MUL (FUN32)	S1 S2 D	Performs BCD multiplication of a channel data by a channel data or a 4-digit constant. $S_1 \times S_2 = D, D+1$ (LSB) (MSB)	S1 S2 Same as ADD instruction. D 00 to 59 LR00 to 30 HR00 to 30 DM000 to 510 *DM000 to 511	4-24
33	DIVIDE	DIV	10	DIV (FUN33)	S1 S2 D	Performs BCD division of a channel data by a specified channel data or a 4-digit constant. $S_1 \div S_2$ = D Remainder D+1		4-25
34	AND WORD	ANDW	10	ANDW (FUN34)	S1 S2 D	Performs a logical AND operation between two 16-bit data. $S_1 \wedge S_2 \rightarrow D$	S1 , S2 Same as MOVE instruction. D Same as MOVE instruction.	4-26
35	OR WORD	ORW	10	ORW (FUN35)	S1 S2 D	Performs a logical OR operation between two 16-bit data. $S_1 \vee S_2 \rightarrow D$		4-27

FUN No.	Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
36	EXCLUSIVE OR WORD	XORW	10	XORW (FUN36)	S1 S2 D	Performs an exclusive logical OR operation between two 16-bit data. $S_1 \veebar S_2 \rightarrow D$	–	4-27
37	EXCLUSIVE OR NOT WORD	XNRW	10	XNRW (FUN37)	S1 S2 D	Performs an exclusive logical OR NOT operation between two 16-bit data. $\overline{S_1 \veebar S_2} \rightarrow D$		4-28
38	INCREMENT (INC)	INC	7	INC (FUN38)	D	Increments a 4-digit BCD data by 1. D + 1 → D		4-29
39	DECREMENT (DEC)	DEC	7	DEC (FUN39)	D	Decrements a 4-digit BCD data by 1. D − 1 → D		4-30
40	SET CARRY (STC)	STC	4	STC (FUN40)		Sets the carry (CY) to "1". 1 → CY	–	4-31
41	CLEAR CARRY (CLC)	CLC	4	CLC (FUN41)		Clears the carry (CY) to "0". 0 → CY		4-31

SPECIAL INSTRUCTIONS

FUN No.	Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
70	BLOCK MOVE		10	FUN70	No. of words S D	Transfers consecutive channel data at one time. 	Number of words #0000 to #0511 S Same as BCD-TO-BIN CONVERSION instruction. Data Same as S of MOVE instruction. D , D_1 , D_2 00 to 60 LR00 to 31 TIM/CNT000 to 127 DM000 to 511 *DM000 to 511	4-31
71	BLOCK SET		10	FUN71	Data D1 D2	Sets the same data to all consecutive channels. 		4-32
72	SQUARE ROOT		10	FUN72	S D —	Computes the square root of an 8-digit BCD data. $\sqrt{\text{S , S+1}} \rightarrow$ D (LSB) (MSB)	S 00 to 62 LR00 to 30 HR00 to 30 TIM/CNT000 to 126 DM000 to 510 *DM000 to 511 D Same as MOVE instruction.	4-32
73	DATA EXCHANGE		10	FUN73	D1 D2 —	Exchanges data between channels. D1 ↔ D2	D_1 , D_2 Same as BLOCK MOVE instruction.	4-33
74	ONE DIGIT SHIFT LEFT		10	FUN74	D1 D2 —	Shifts data between the start and end channels to the left by 1 digit (i.e., 4 bits). 	S Same as BCD-TO-BIN CONVERSION instruction. D , D_1 , D_2 Same as MOVE instruction.	4-34
75	ONE DIGIT SHIFT RIGHT		10	FUN75	D1 D2 —	Shifts data between the start and end channels to the right by 1 digit (i.e., 4 bits). 	Digit designation #0000 to #0003	4-35
76	4-TO-16 DECODER		10	FUN76	S Digit designation D	Decodes a 4-bit binary data of 16 bits to a 16-bit channel data. 		4-36
77	16-TO-4 ENCODER		10	FUN77	S D Digit designation	Encodes a 16-bit decimal data into 4 bits of another 16-bit binary data. 		4-37
78	7-SEGMENT DECODER		10	FUN78	S Digit designation D	Converts 4 bits of 16-bit data into an 8-bit data for 7-segment display. 		4-39

FUN No.	Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
79	FLOATING POINT DIVIDE	FUN79	10	FUN79	S1 S2 D	Performs a floating-point arithmetic operation between two 7-digit BCD data. (LSB) (MSB) (S1, S1+1)÷(S2, S2+1) →(D, D+1)	S1 S2 Same as S of SQUARE instruction D Same as MULTIPLY instruction	4-40
80	DATA DISTRIBUTION	FUN80	10	FUN80	S D1 D2	Distributes 16-bit data to a channel that is a base address with an offset added. S Base address (D1)+ Offset (D2) (S)→(D1+D2)	S Same as S of MOVE instruction D1 , D2 Same as D of BLOCK MOVE instruction	4-42
81	DATA EXTRACTION	FUN81	10	FUN81	S1 S2 D	Extracts 16-bit data from a channel that is a base address with an offset added and transfers the data to a specific channel. Base address (S1) Offset (S2) D	S1 00 to 63 LR00 to 31 HR00 to 31 TIM/CNT000 to 127 DM000 to 511 *DM000 to 511 S2 D Same as D of BLOCK MOVE instruction	4-43
82	BIT TRANSFER	FUN82	10	FUN82	S Control data D	Transfers a specific bit to another specified bit. Control data To specify bit from which data is transferred To specify bit to which data is transferred	S 00 to 63 LR00 to 31 HR00 to 31 DM000 to 511 *DM000 to 511 Constant 000 to FFFF Control data 00 to 60 LR00 to 31 HR00 to 31 TIM/CNT000 to 127 DM000 to 511 *DM000 to 511 Constant D Same as D of MOVE instruction	4-44
83	DIGIT TRANSFER	FUN83	10	FUN83	S Control data D	Tranfers channel data in units of digits (4 bits) to a specified channel. M L S D Control data Digit from which data is transferred No. of digits to be transferred Digit to which data is transferred Ignored	S Same as S of ADD instruction Control data 00 to 60 LR00 to 31 HR00 to 31 TIM/CNT000 to 127 DM000 to 511 *DM000 to 511 Constant D Same as D of BLOCK SET instruction	4-45

FUN No.	Instruction	Symbol	Instruction word length (byte)	Mnemonic	Operand	Function	Data	Page
84	LEFT/RIGHT SHIFT REGISTER		10	FUN84	Control data Start CH No. End CH No.	Shifts specified 16-bit data 1 bit to the left or to the right. 	00 to 60 LR00 to 31 HR00 to 31	4-46
85	TABLE COMPARE		10	FUN85	S T D	Compares 16-bit data against data in 16 channels (table) and outputs the results to a specified channel. 	Control data CH No. 00 to 60 LR00 to 31 HR00 to 31 DM000 to 511 *DM000 to 511 • Start CH ≦ End CH • The start CH must be in the same relay area as the end CH.	4-48
94	WATCHDOG TIMER SETTING		10	FUN94	No. of times — —	Refreshes the set time of the watchdog timer.	No. of times 0 to 63	4-49
99	RUN STOP		10	FUN99	— — —	Stops the RUN operation when the specified relay is turned OFF and starts the operation when it is turned ON.		4-49

RELATIONSHIP BETWEEN SPECIAL AUXILIARY RELAYS AND INSTRUCTION WORDS

Relay No.		Special auxiliary relays				
		6307 (<)	6306 (=)	6305 (>)	6304 (CY)	6303 (ER)
Operation of relay / Instruction executed	FUN No.	Turns ON if result when Compare instruction is executed is less than.	Turns ON if the result when Compare instruction is executed is equal or 0000.	Turns ON if result when Compare instruction is executed is more than.	Turns ON if a result carry exists in result of an arithmetic operation.	Turns ON if data subject to BCD operation are binary or indirectly addressed data error.
TIM						↕
TIMH	15					↕
CNT						↕
CNTR	12					↕
CMP	20	↕	↕	↕		↕
MOV	21		↕			↕
MVN	22		↕			↕
BIN	23		↕			↕
BCD	24		↕			↕
ASL	25		↕		↕	↕
ASR	26		↕		↕	↕
ROL	27		↕		↕	↕
ROR	28		↕		↕	↕
COM	29		↕			↕
WSFT	16					↕
ADD	30		↕		↕	↕
SUB	31		↕		↕	↕
MUL	32		↕			↕
DIV	33		↕			↕
ANDW	34		↕			↕
ORW	35		↕			↕
XORW	36		↕			↕
XNRW	37		↕			↕
INC	38		↕			↕
DEC	39		↕			↕
STC	40				"1"	
CLC	41				"0"	
FUN	70					↕
FUN	71					↕
FUN	72		↕			↕
FUN	73					↕
FUN	74					↕
FUN	75					↕
FUN	76					↕
FUN	77					↕
FUN	78					↕
FUN	79		↕			↕
FUN	80		↕			↕
FUN	81		↕			↕
FUN	82					↕
FUN	83					↕
FUN	84				↕	↕
FUN	85		↕			↕
END	01	"0"	"0"	"0"	"0"	"0"

NOTES:
1. The BCD-check operation of a set value is performed at reset of a TIM, TIMH, or CNT instruction or at count up of a CNTR instruction.
2. When special auxiliary relay 6303(ER) turns ON, no instruction is executed except the TIM, TIMH, CNT, and CNTR instructions.
3. When the 6303 is ON, the status of other special auxiliary relays (6304 to 6307) is not changed.
4. The status of these special auxiliary relays is not changed by executing instructions other than those listed in the above table.

Legend: ↕ — Change
Vacant — No change