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DIAX03

Plug-in modules for digital intelligent drive controllers

Project Planning Manual

DOK-DIAX03-PLUG*IN*MOD-PR03-EN-P

Rexroth Indramat

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The purpose of the documentation? This documentation supports the development of the electronic construction of the machine manufacturer.

In support of these efforts, this documentation summarizes and includes technical documentation, terminal diagrams and detailed signal paths of the individual plugin modules.

Published by

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Changes with respect to previos Version DOK-DIAX03-PLUG*IN*MOD-PR03-EN-P

Where	What
Complete document	Cable + connector idents brought up to date
Complete document	Cable numbers now four positions
DEA-Chards	Sub D connector dimensions (including some right angle connectots) corrected.

Changes

Note: This List is not exhaustive, the author may make further small changes not listed here.

Notes

Contents

Notes

1 About this documentation

1.1 Plugin module applications

The plugin modules documented here are intended for use in digital drive controllers belonging to the DIAX03 drive family.

Depending upon the selected configured drive controller, different plugin modules can be inserted into the slots on the drive controller.

Which plugin module and which software can be combined in the drive controller is specified in the documentation "Drive configuration".

Notes

2 Storing and transporting plugin modules

2.1 Storing and transporting plugin modules

Protection against electrostatic loads

Electrostatic loads endanger electronic components. Bodies coming into contact with components and printed circuit boards must be discharged by grounding:

- The human body must contact a conductive, grounded object.
- A soldering iron during soldering.
- Parts and tools must be placed on a conductive service.

Note: Endangered parts such as plugin modules must be stored and transported in conductive packaging only.

Temperature and humidity

Ambient temperature during operations	+5...+45°C
Ambient temperature during storage and transport	-30...+85°C
Permissible relative humidity	max. 95%
Permissible absolute humidity	max. 25g water/m³

Fig. 2-1: Permissible temperature and humidity

Notes

3 Plugin module design

3.1 Plugin modules with plastic and metallic front panels

The plugin modules of the drive controllers belonging to the DIAX03 and 04 drive families are outfitted with a metal front panel having two knurled screws at top and bottom (see Fig. 3-1).

The plugin modules for the drive controllers of the DIAX02 drive family (see Fig. 3-1) can, therefore, not be used in the drive controllers of the DIAX03 type as it is not possible to mount the plugin modules into the drive controllers.

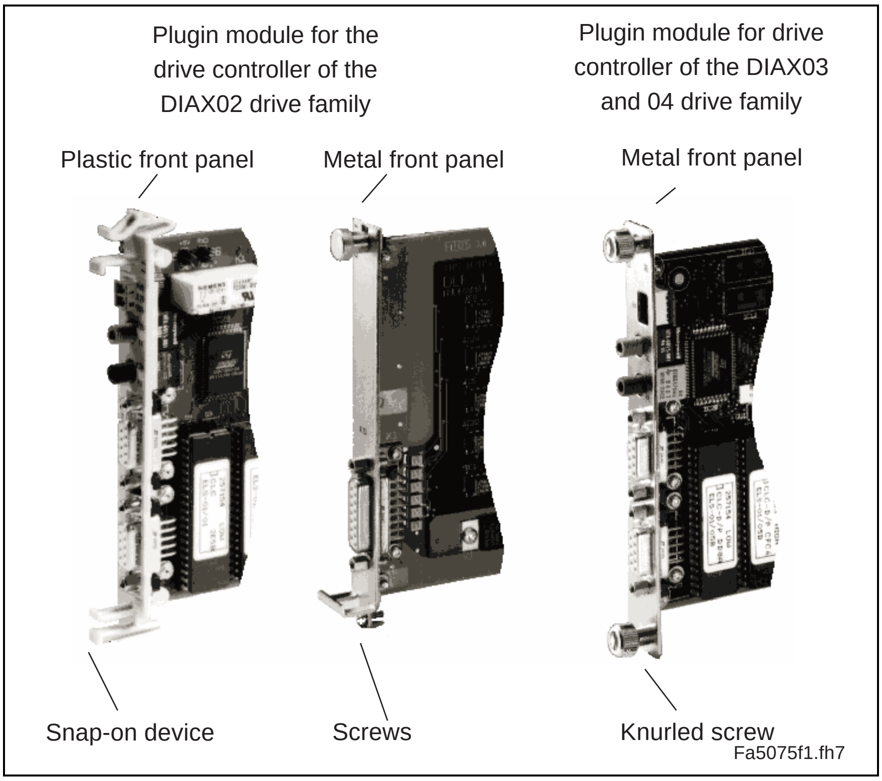


Fig. 3-1: Plugin modules with plastic and metallic front panels

3.2 Type codes

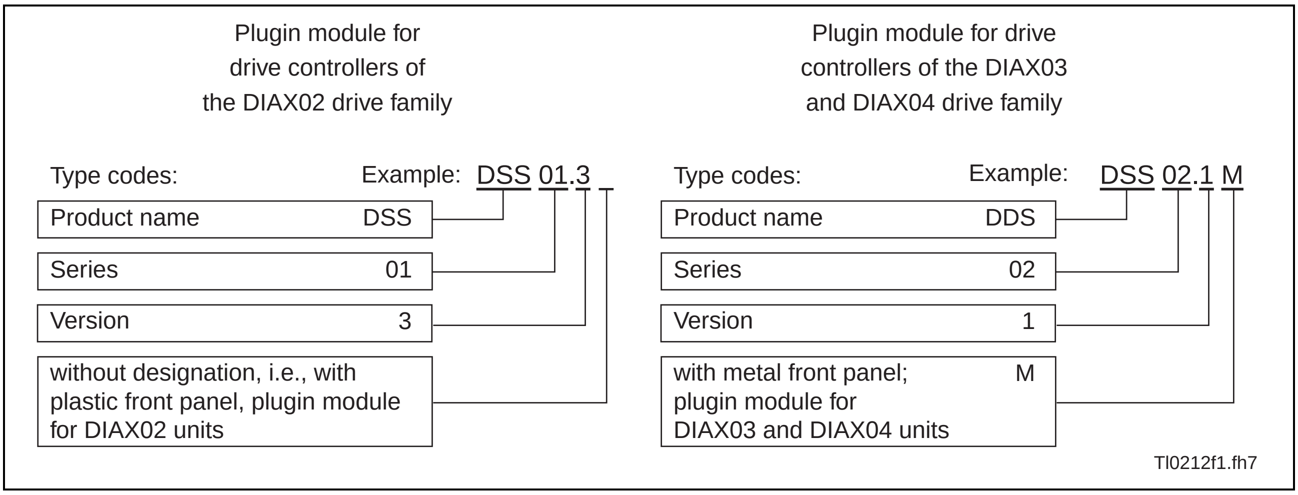


Fig. 3-2: Type codes

Notes

4 Ground reference of the plugin module connections

4.1 Extra-low voltage circuits DC 5...24 V and galvanically coupled signal inputs and outputs

All connections and terminals with voltages of 5 to 50 volts in INDRAMAT products are protective extra-low voltages (PELV = Protective Extra Low Voltage).

They are contact-proof in accordance with the following standards:

- international:IEC 364-4-411.1.5
- European countries of the EU: EN 50178/1994, section 5.2.8.1.

These connections are grounded electric circuits. Their reference potential is identified with the designations 0VM, GND or 0VL on the supply unit connected with the housing and therefore grounded. The signal connections and terminals of the drive controllers are a part of these electric circuits.

Opening these ground connections up -- even for metrological purposes -- is not possible for safety reasons. If these electrical circuits were separated from the housing (ground potential), then a proper functioning of the electronic components could not be guaranteed.

The terminal diagram specifies the connections to which this applies.

4.2 Optocoupler interface

The extra-low voltage circuits (e.g., DC 24 V) needed to operate the plugin modules must be grounded. In other words, the 0V potential must be connected to the central grounding point within the control cabinet. Even if the DC 24 V electric circuits of the plugin modules are generally galvanically isolated, they should nonetheless be grounded in this manner (see Fig. 4-1).

Experience has shown that non-grounded voltage circuit interference signals can, under some circumstances, be conducted via the coupling capacitors of the optocouplers and generate error messages in the drive.

The galvanic separation using an optocoupler in the plugin modules prevents three-phase transient currents coming over the evaluation electronics.

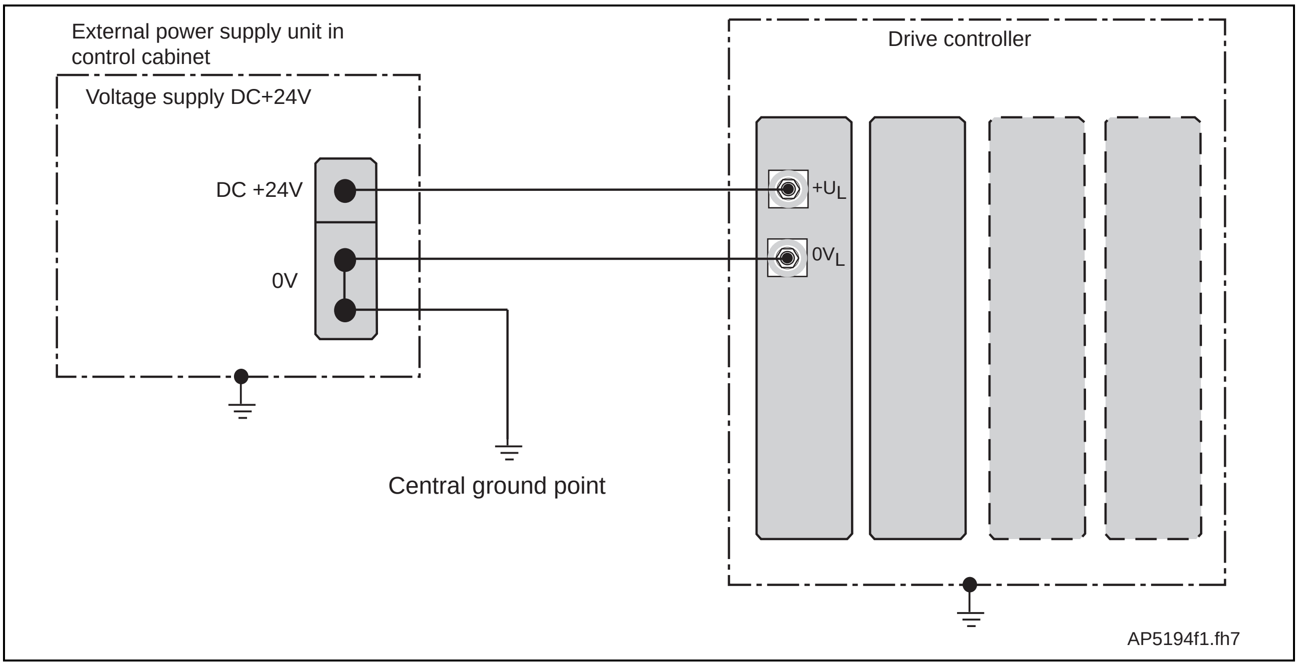


Fig. 4-1: Connecting the DC 24 V voltage source for the optocoupler interface

4.3 Notes on short to ground monitoring

Due to the ground connections of the above reference electric circuits it is basically not possible in INDRAMAT drives and control systems to monitor shorts to ground. It is necessary to ground the electric circuits to secure sufficient operating safety and reliability.

A short to ground monitoring only makes sense with relay circuits. This detects the shorts to ground frequently occurring there. Electronic apparatus does not require short to ground monitoring, a monitoring which frequently does not serve its purpose, namely, achieving greater operating reliability.

5 Control cards CLC-D02.1M-FW and CLC-D02.3M-FW

5.1 Terminal diagrams CLC-D02.1M-FW and CLC-D02.3M-FW

The terminal diagrams for the control cards CLC-D02.1M-FW and CLC-D02.3M-FW is the same.

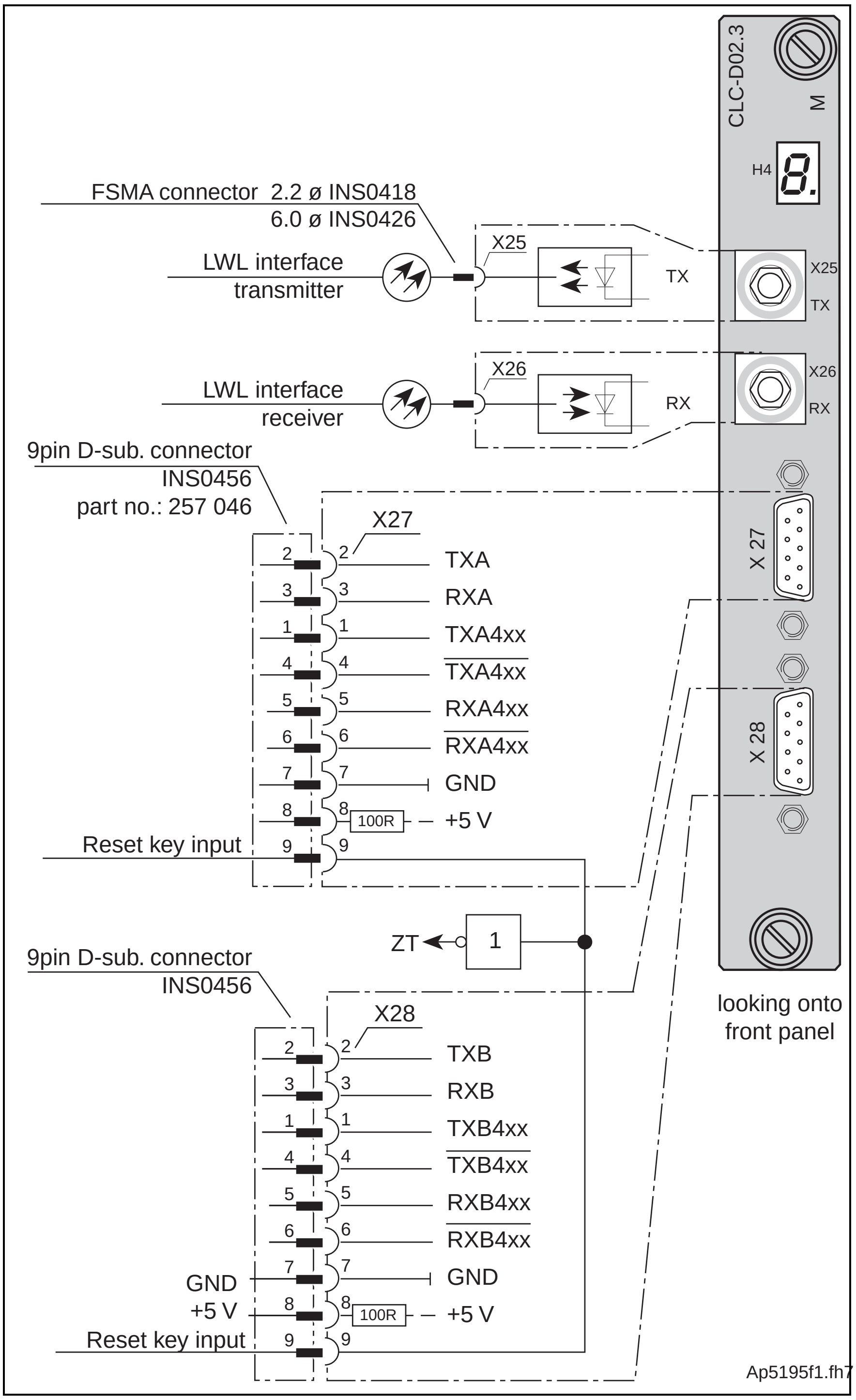


Fig. 5-1: Terminal diagram CLC-D02.1M-FW and CLC-D02.3M-FW

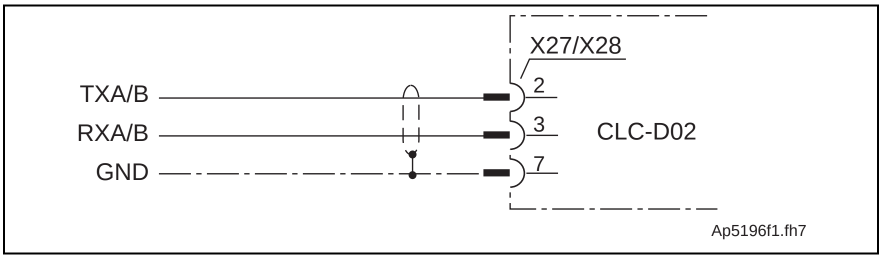


Fig. 5-2: Terminal diagram RS 232

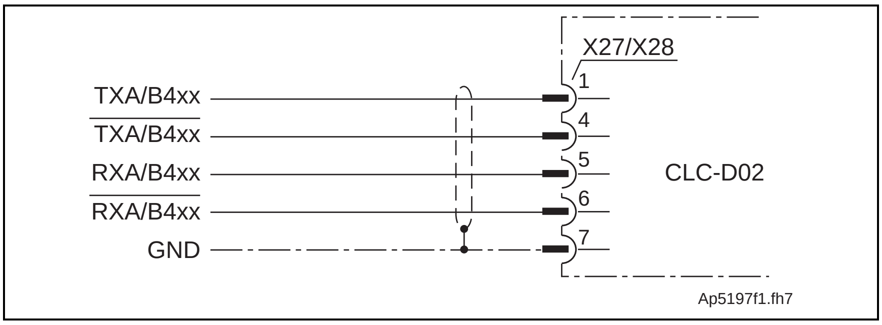


Fig. 5-3: Terminal diagram RS 422

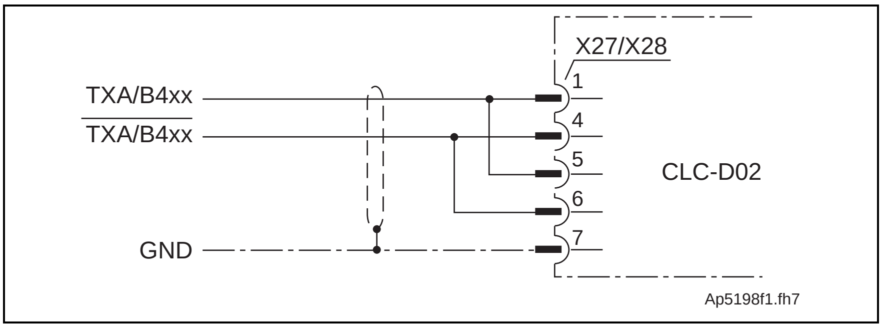


Fig. 5-4: Terminal diagram RS 485

Parameter	RS 232	RS 422	RS 485
Type	non-symmetric	symmetric	symmetric
max. line length	15m	1200m	1200m
max. transmission rate	38400 baud	9600 baud	9600 baud
max. transmission output voltage	±15 V	±5 V*	±5 V*
max. receiver input voltage	±25 V	±14 V*	-14 V*
input sensitivity	±3 V	±200 mV	±200 mV
input resistance	3...7 kΩ	4 kΩ	12 kΩ
*) diferential signals			

Fig. 5-5: Technical data RS 232, RS 422, RS 485

Technical data of the LWL interface

	Name	Abbreviation	Unit	Value
Transmitter data Tx	max. transmission output with opt. low level	P_{SmaxL}	dBm/µW	-28.2/1.5
	min. transmission output with opt. high level	P_{SminH}	dBm/µW	-7.5/180
	max. transmission output with opt. high level	P_{SmaxH}	dBm/µW	-3.5/450
	wavelength of the transmitter diode: peak wavelength spectral bandwidth	λp λp	nm nm	640…675 nm (0° C..55° C) - 30 nm (25° C)
Receiver data Rx	max. input power for opt. low level	P_{EmaxL}	dBm/µW	-31.2/0.75
	min. input power for opt. high level	P_{EminH}	dBm/µW	-20/10
	max. input power for opt. high level	P_{EmaxH}	dBm/µW	-5/320
	max. damping of transmission distance	$P_{SminH}…P_{EminH}$	dB	12.5
Transmission output can be set via the parameters in the software.				

Fig. 5-6: Technical data of the LWL interface

Battery

There is a three voltage battery on the CLC-D02 for RAM backup.

Note: Once the battery is empty, the C and A parameters are lost. Therefore, backup the parameters**!**

INDRAMAT part number: 254 284

Battery lifespan

At the time of delivery, the battery has a minimum capacity of 75% of total capacity.

Once it reaches the 10% level of total capacity, the battery is empty.

The lifespan of the battery depends on how the CLC is operated. The table gives some general guidelines:

Ambient temperature	3-shift operations	2-shift operations	1-shift operations	Storage
25° C	4 yrs.	4 yrs.	4 yrs.	3 yrs.
35° C	4 yrs.	3 yrs.	2 yrs.	1.5 yrs.
45° C	3 yrs.	2 yrs.	1.2 yrs.	0.8 yrs.

Fig. 5-7: Battery lifespan

Note: The battery is generally empty after this period of time and must be replaced**.**

Replacing the battery

After the battery is removed, the parameters are backed up for only **one minute**.

Procedure:

⇒ keep new batteries handy

⇒ switch installation off

⇒ CLC card must be pulled out

⇒ pull old battery out

⇒ new battery must be inserted in at least one minute

Notes:

6 ANALOG interface with actual position value output DAE02.1M

6.1 General information

The plugin module DAE02.1M enables the operation of the digital intelligent AC servo drive with conventional controls via an analog interface. It also contains control inputs and signal outputs for communications with a connected control as well as generating either incremental encoder signals or absolute encoder signals (SSI) which can be used as actual position values.

6.2 Terminal diagram DAE02.1M

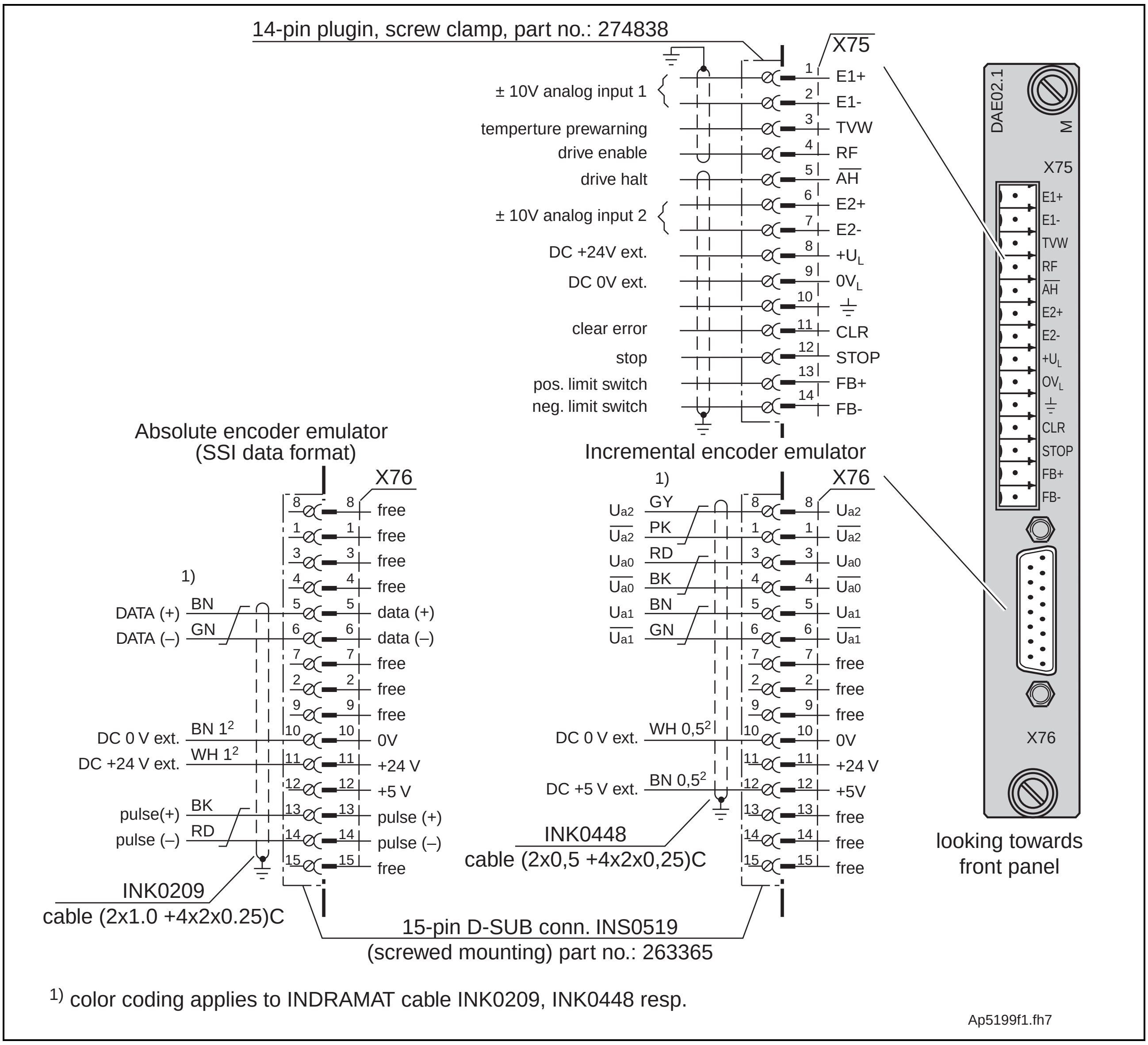


Fig. 6-1: Terminal diagram of the DAE02.1M

6.3 Technical data

Analog interface

Designation		Unit	min.	max.
Input voltage 1)	E1+, E2+	V	-10	+10
	E1-, E2-	V	-10	+10
	|(E1+)-(E1-)| |(E2+)-(E2-)|	V		10
Input current	E1+, E2+	mA	-0.25	+0.25
	E1-, E2-	mA	-0.5	+0.5
1) The input voltage resolution equals: $20V/2^{16}$=0.3 mV				

Fig. 6-2: Analog interface data

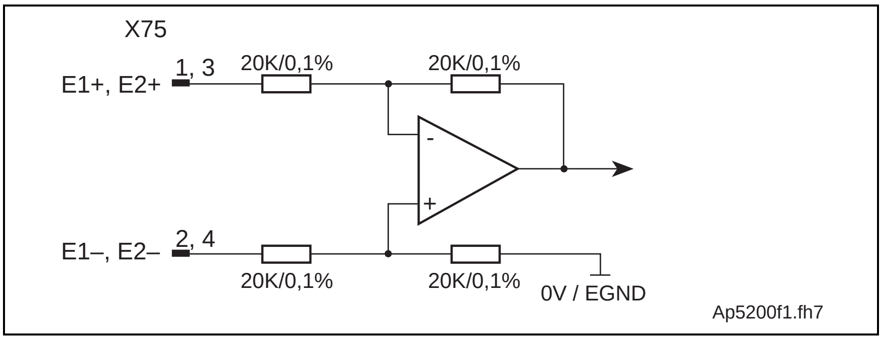


Fig. 6-3: Analog interface input circuits

Voltage source / digital inputs and outputs

The inputs and outputs are isolated, receiving their power via connector X75 with 24 V. The external voltage source is reverse protected.

Designation		Unit	min.	Type	max.
ext. voltage source $+U_L$		V	18	24	32
current consumption of the $+U_L$		mA			100
inputs RF, AH, CLR,	U_{High}	V	14	24	32
STOP, FB+, FB-	U_{Low}	V	0	<1	10
output TVW	I_{Out}	mA			100

Fig. 6-4: Voltage source and digital input and output data

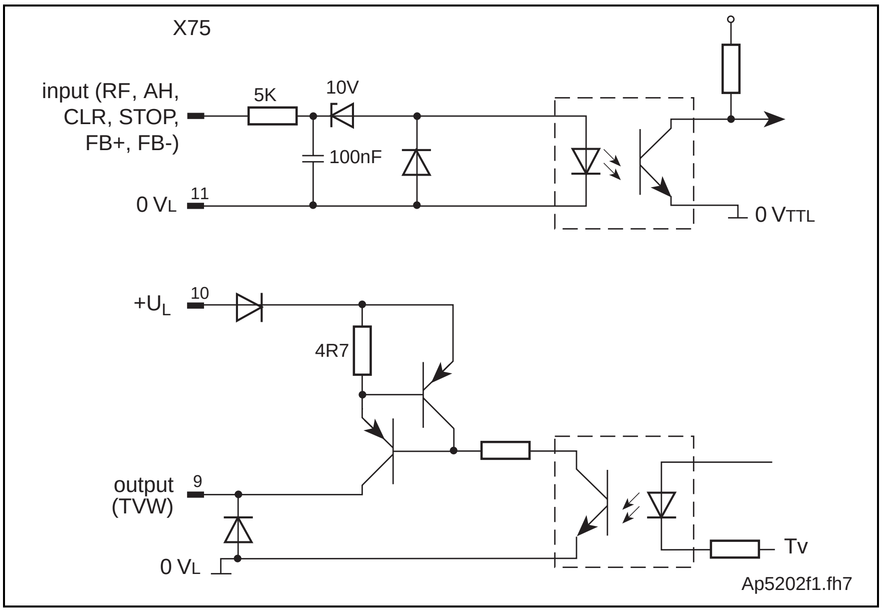


Fig. 6-5: Input and output circuits

Actual position value output

To transmit the actual position value to the NC control, the actual position value can be either incrementally or absolutely output.

Incremental encoder emulation

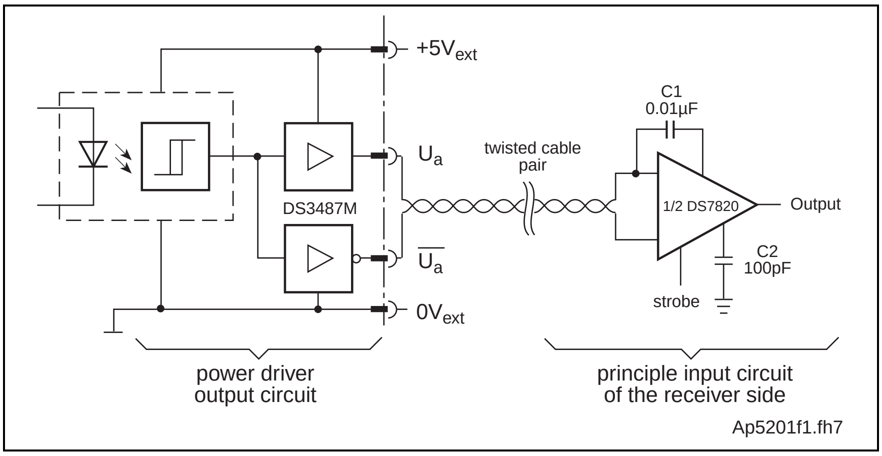


Fig. 6-6: Incremental encoder output circuit

System Limits

In contrast to conventional incremental encoders in which the pulse output frequency can be infinitely set in very fine increments (i.e., pulse flanks always allocated to fixed positions), an emulated incremental encoder signal is subject to some limitations. This is the direct result of the drive controller and the way the encoder emulation card DAE02.1M must work in a digital fashion.

Number of Lines

The number of encoder lines usually ranges between 16 and 262144, taking maximum output frequency into account, and can be freely selected.

Note: When emulating the actual positon value 1 gained from a non-absolute resolver, the number of lines must be divisible by the number of resolver pole pairs.

Maximum output frequency

The pulse output register on the DAE02.1M has a width of 10 bits per control cycle. At 250µs this means it can process a maximum of 2^{10}-1 = 1023 increments. The maximum pulse frequency that can be output thus equals: 1023/4 = 256 pro 250µs = 1.023 MHz.

If this frequency is exceeded, then pulses can go missing. This results in a position offset of the emulated in contrast to the real position.

Run Time between Real and Emulated Positions

If real position detection takes place at time t_n then an internal computation process is started. At time t_{n+1} the number of computer increments is output. The output is completed no later than t_{n+2}.

A runtime compensation is presently not available.

Depending on sampling time of the control, minimum run time thus equals 250µs, maximum equals 500µs (mean runtime 375µs).

Note:	If the master axis position is emulated, then the missing runtime compensation of the emulation does not cause a constant error as master axis position processsing is also delayed in the drives.

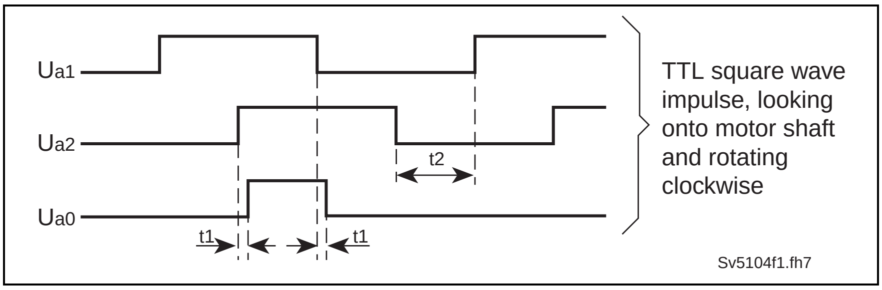


Fig. 6-7: Incremental encoder output signals

Designation		Unit	min.	Type	max.
supply voltage +5V external		V	4.75	5	5.25
current consumption of the +5V external		mA			175
Signal level	U_{high} ($I_{OUT} \le 20$ mA)	V	2.5	3.4	
U_{a0}, U_{a1}, U_{a2}	U_{low} ($I_{OUT} \le 40$ mA)	V		0.3	0.5
output current		mA			40
output frequency		MHz			1
rise and drop time		ns			100
reference point delay t1		ns	0		100
edge distance t2		ns	200		

Fig. 6-8: Voltage supply and signal level of incremental encoder emulation

Absolute encoder emulation

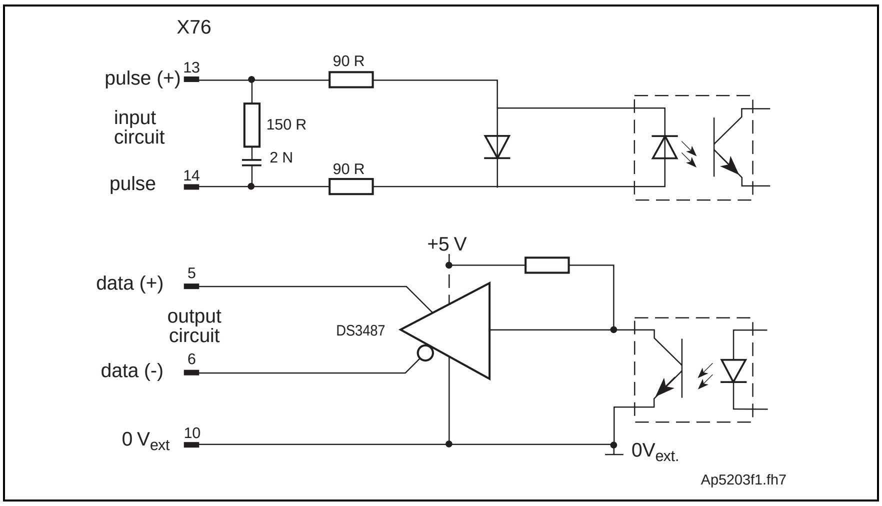


Fig. 6-9: Absolute encoder output circuit

Voltage supply for absolute encoder emulation

Designation	Unit	min.	Type	max.
supply voltage +24V external	V	10	24	32
current consumption +24V external	mA		100	200

Fig. 6-10: Voltage supply and signal level of incremental encoder emulator

Recommended pulse frequency for data transmission

Data transmission depends on line length.

Line length in m	Pulse frequency in kHz
< 10	< 2000
< 20	< 1000
< 50	< 500
< 75	< 250
< 100	< 125

Fig. 6-11: Line length and pulse frequency

Actual position output in absolute format

probe code:	Gray Code
data scope:	4096 rotations
resolution:	4096 increments/rotations
data format:	24 Bit + PFB
count direction:	switchable
data transmission:	synchronous, serial
input/output circuit:	driver per EIA RS 422 A
least significant bit:	G0
most significant bit:	G23
pulse frequency:	f_T= 100 kHz ... 2 MHz
pulse signal period:	T = 10 µs ... 0.5 µs
monoflop time:	tm= 16 µs
clock pulse:	Tp = tm + T/2
delay time:	tv = 200 ns ... 250 ns
power failure bit (PFB):	not used, logically always "0"

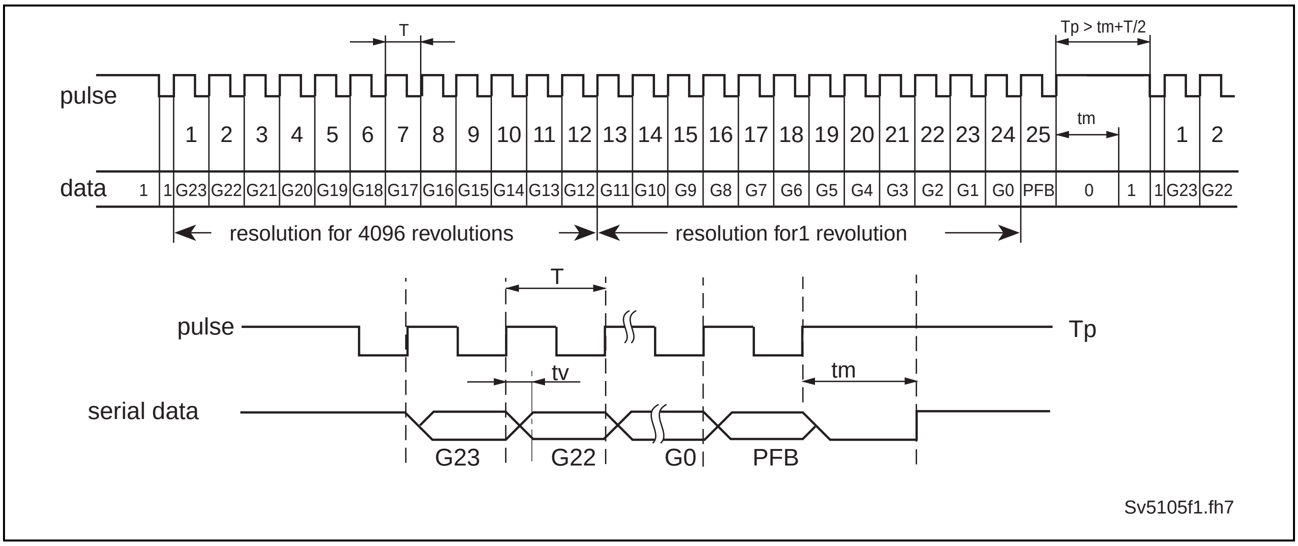


Fig. 6-12: Principle of signal paths illustrated

DANGER

Error in control of motor and moving parts
Bodily harm and property damage due to accidental axis movements.
If breaks in the power supply occur $+U_{ext}$ by dropping below 10 V over periods of time longer than 100 µs, then the encoder information could be faulty.
⇒ Activate the lag distance monitor in the control.

Actual position output in modulo format

probe code:	Gray Code
data scope:	1 table rotation
resolution:	262 144 increments per table rotation
data format:	18 Bit
count direction:	switchable
data transmission:	synchronous, serial
input/output circuit:	driver per EIA RS 422 A
least significant bit:	G0
most significant bit:	G17
pulse frequency:	f_T= 100 kHz ... 2 MHz
pulse signal period:	T = 10 µs ... 0,5 µs
monoflop time:	tm= 16 µs
pulse break:	Tp = tm + T/2
delay time:	tv = 200 ... 250 ns
power failure bit (PFB):	is not used and logically always "0"
stored parallel information:	m

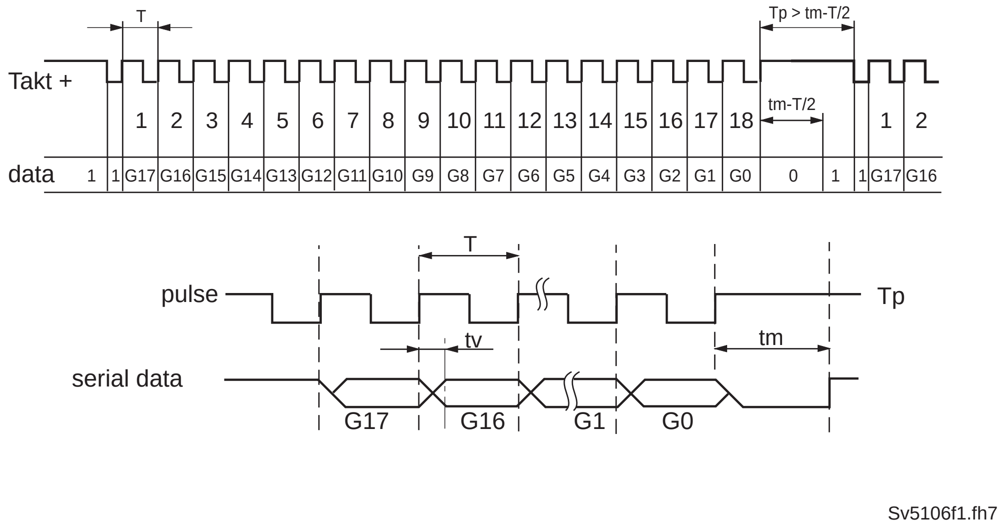


Fig. 6-13: Principle of signal paths illustrated

DANGER

Error in control of motor and moving parts
Bodily harm and property damage due to accidental axis movements.
If breaks in the power supply occur $+U_{ext}$ by dropping below 10 V over periods of time longer than 100 µs, then the encoder information could be faulty.
⇒ Activate the lag distance monitor in the control.

7 Encoder interface DAG01.2 M

7.1 General information

Encoder interface DAG 01.2 M evaluates:

- linear and angle measuring systems using the bidirectional interface EnDat
- angle scales as per SSI standards

Setting interfaces

If the measuring system is equipped with an EnDat interface, then set the S2/4 switch on the printed circuit board to OFF.

If it works according to SSI standards, then set this switch to ON.

Select pulse frequency

Pulse frequency depends on line length.

Select pulse frequency as per the following table.

max. line length in m	pulse frequency in kHz
10	to 2 MHz
20	to 1 MHz
50	to 500 kHz
75	to 250 kHz
100	to 125 kHz

Fig. 7-1: Select pulse frequency

Setting pulse frequency

Set pulse frequency with S2/1, 2, 3, on PCB as per table below:

Pulse frequency	Switch position S2/1	Switch position S2/2	Switch position S2/3
2 MHz	ON	ON	ON
1 MHz	OFF	ON	ON
500 kHz	ON	OFF	ON
250 kHz	OFF	OFF	ON
125 kHz	ON	ON	OFF

Fig. 7-2: Setting pulse frequency

condition at delivery

The following is programmed at the time of delivery:

Cycle frequency	Switch setting S2/1	Switch setting S2/2	Switch setting S2/3
125KHz	ON	ON	OFF

Interface	Switch setting S4
Endat	OFF

7.2 Encoder interface DAG01.2 M with EnDat interface

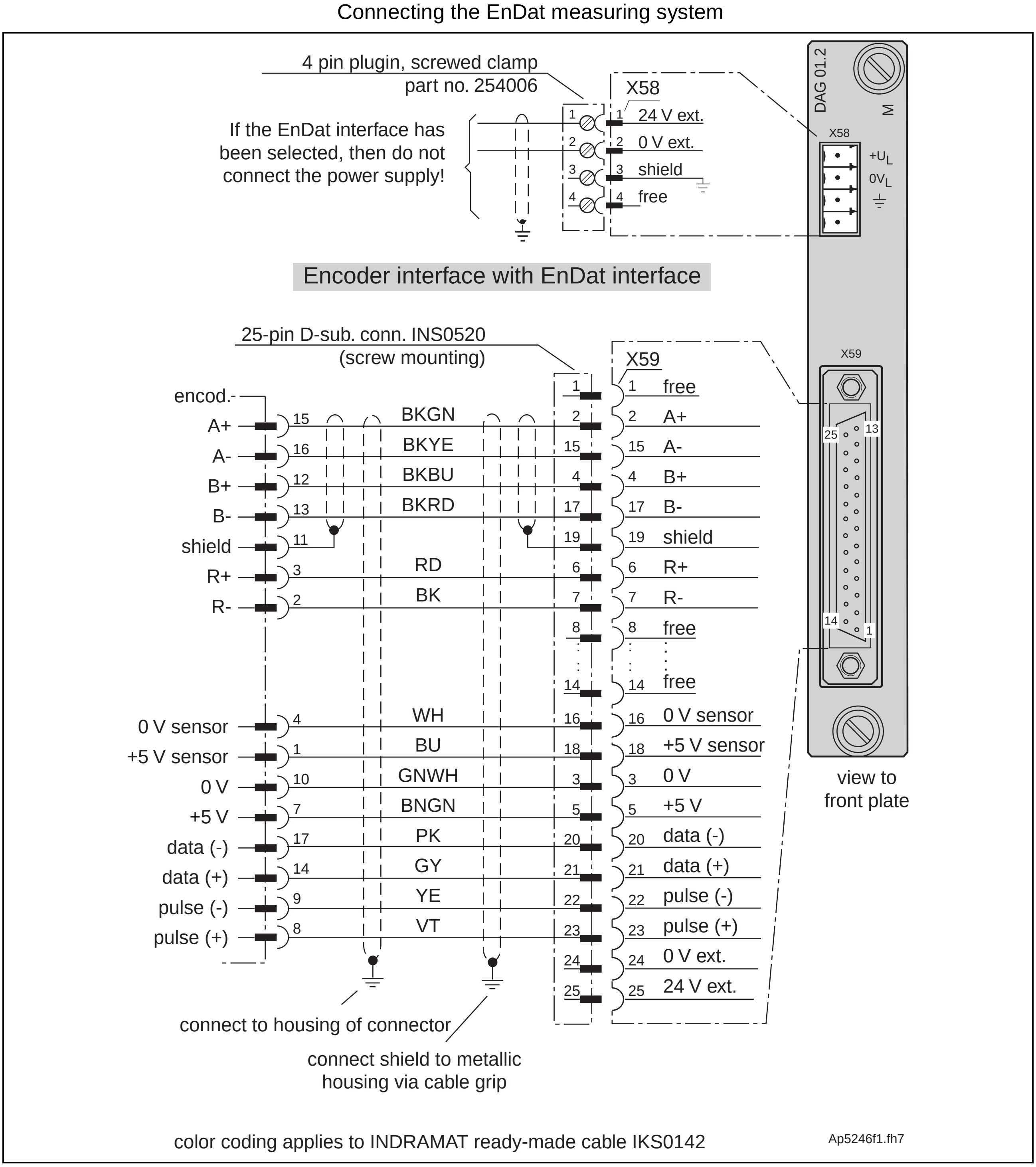


Fig. 7-3: Terminal diagram EnDat measuring system

Ready-made cable for X59

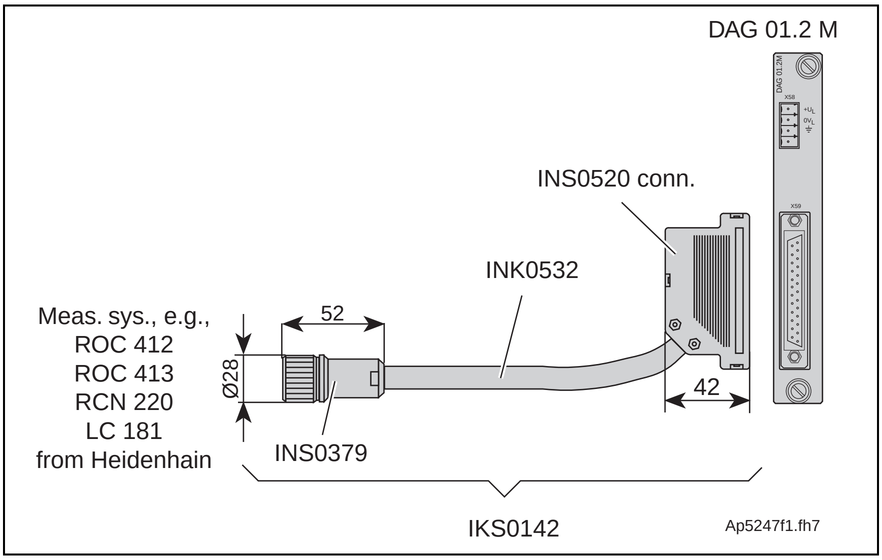


Fig. 7-4: Ready-made cable for X59

EnDat Interface - technical data

interface EnDat interface (bidirectional serial interface)

Power supply for external measuring system

output voltage X59/5:	DC +5V (±2.5%)
maximum output load X59/5:	350 mA

Signals from measuring system

Signals A and B are two approximate sinusoidal signals.

R is the reference marker signal.

Resolution The signal periods coming from the measuring system has a resolution of 8192-fold.

Power signals

Signal voltage for A, B, R:	1 V_{SS} (+10/-20%)
Max. signal voltage offset:	0.2 V
Max. frequency of meas. system signals A, B:	500 kHz
Max. frequency for ref. marker signal R:	15 kHz

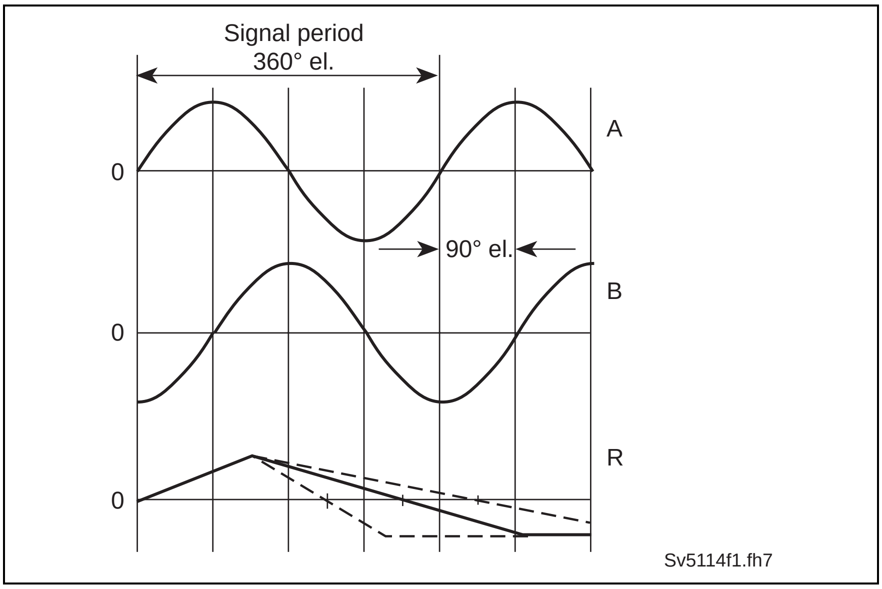


Fig. 7-5: Principle of signal paths illustrated

Code signal

Data output Signal pulse(+) and pulse(-) from differential line driver per EIA standard RS-485.

Data input Signal data(+) and data(-) for differential line receiver per EIA standard RS-485 with cable end Z_0=120 Ohm.

Data transmission

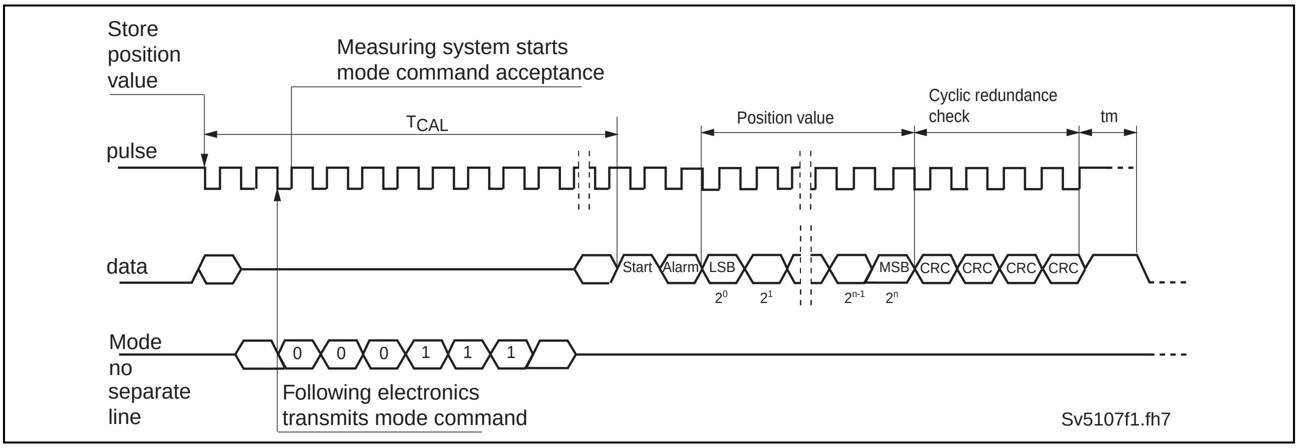


Fig. 7-6: Overview of data transmission

Circuit principle

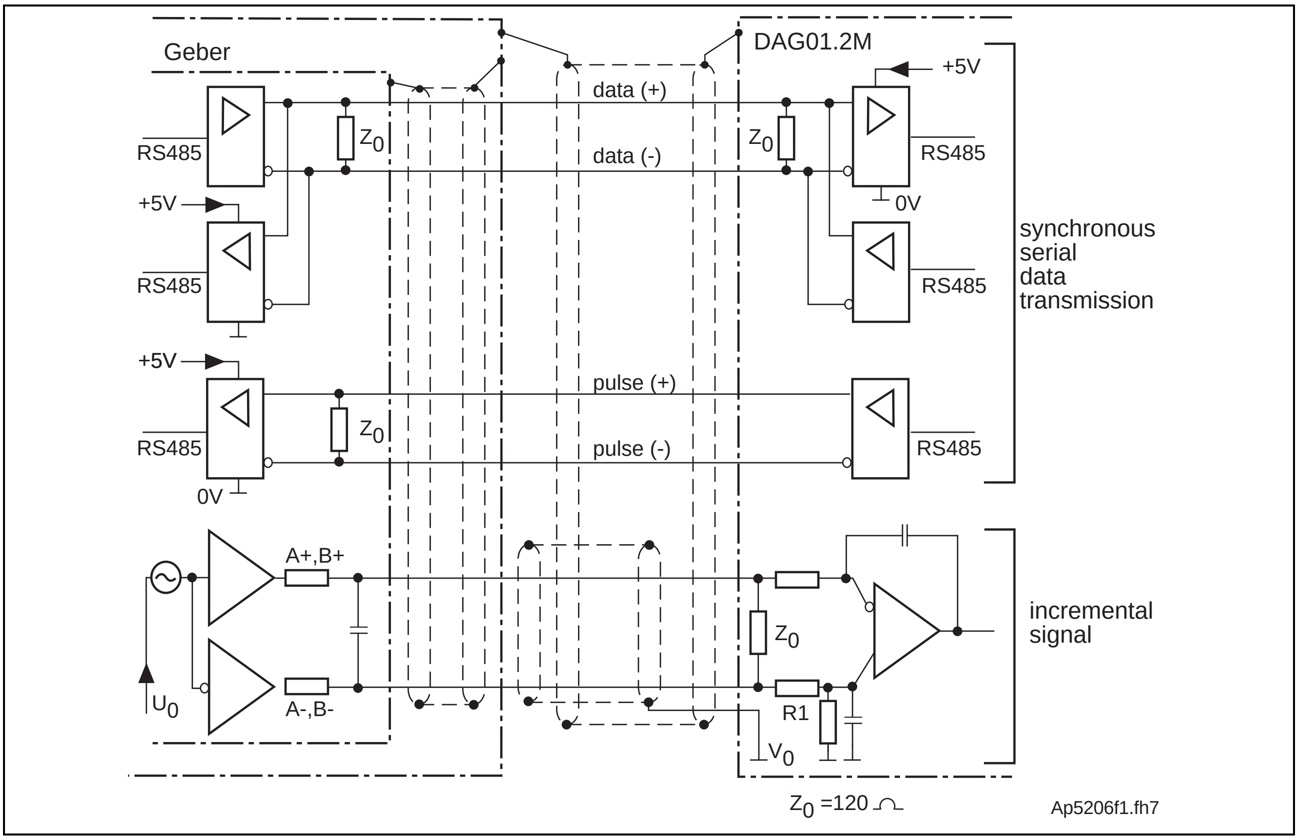


Fig. 7-7: Circuit principle illustrated

7.3 Encoder interface DAG01.2 M with Synchronous Serial Interface (SSI)

Connecting an SSI measuring system

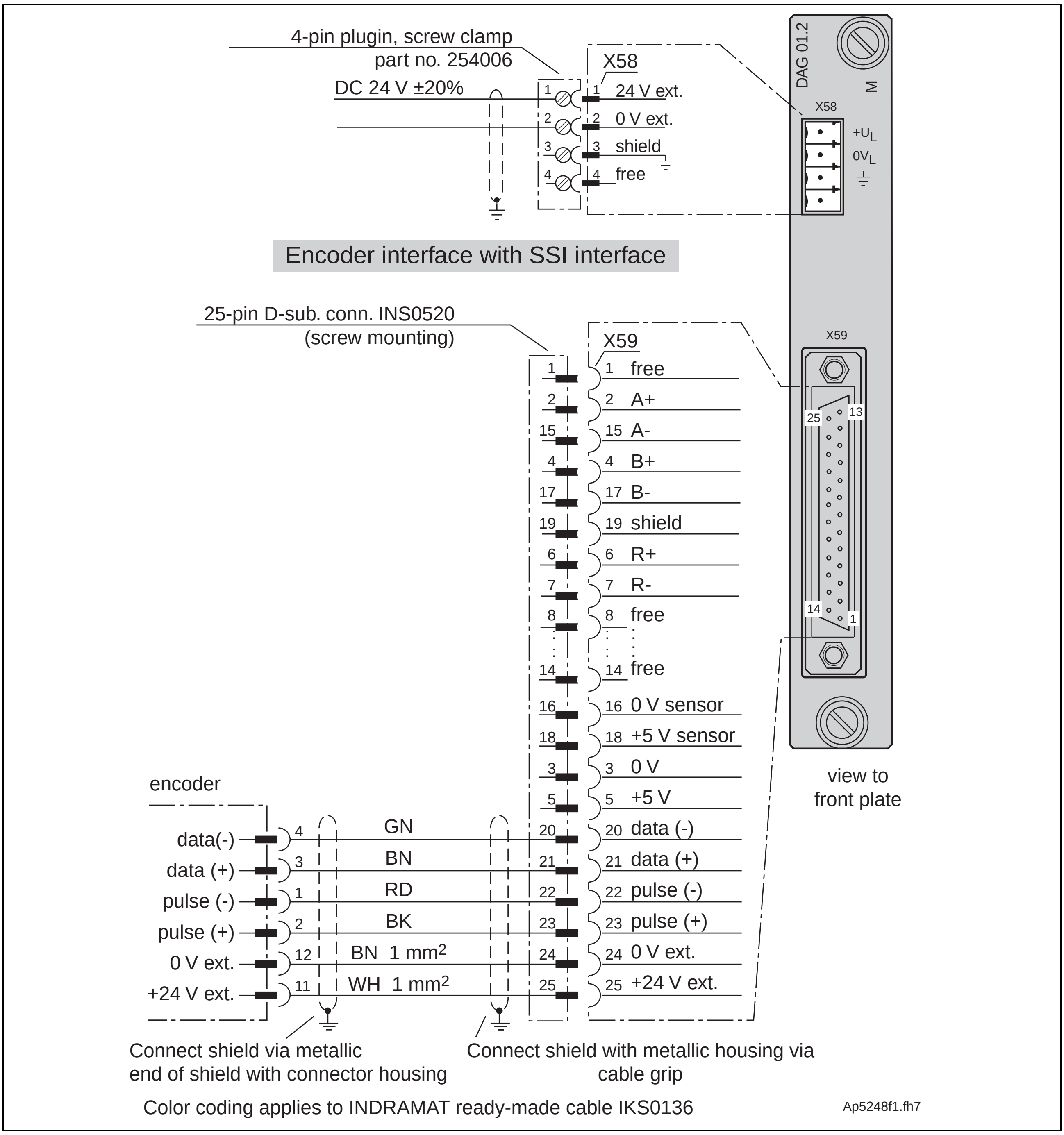


Fig. 7-8: Terminal diagram - SSI measuring system

Ready-made cable for X59

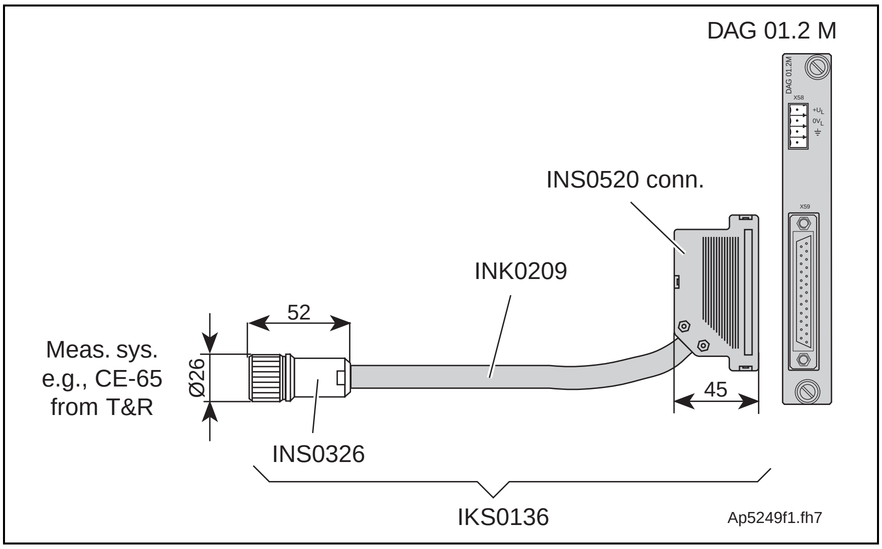


Fig. 7-9: Ready-made cable for X59

SSI data format

probe code:	Gray Code
data scope:	4096 rotations
resolution:	4096 increments/rotation
data format:	24 bit + power failure bit
data transmission:	synchronous, serial
least significant bit:	G0
most significant bit:	G23
pulse frequency:	f_T = 125 kHz…2MHz
pulse signal period:	T = 8…0.5 µs
monoflop time:	tm = 30 µs
pulse break:	Tp = 250 µs - 26 * T - 30 µs
power failure bit (PFB):	0: no error 1: error

Serial data is accepted with the following positive pulses:

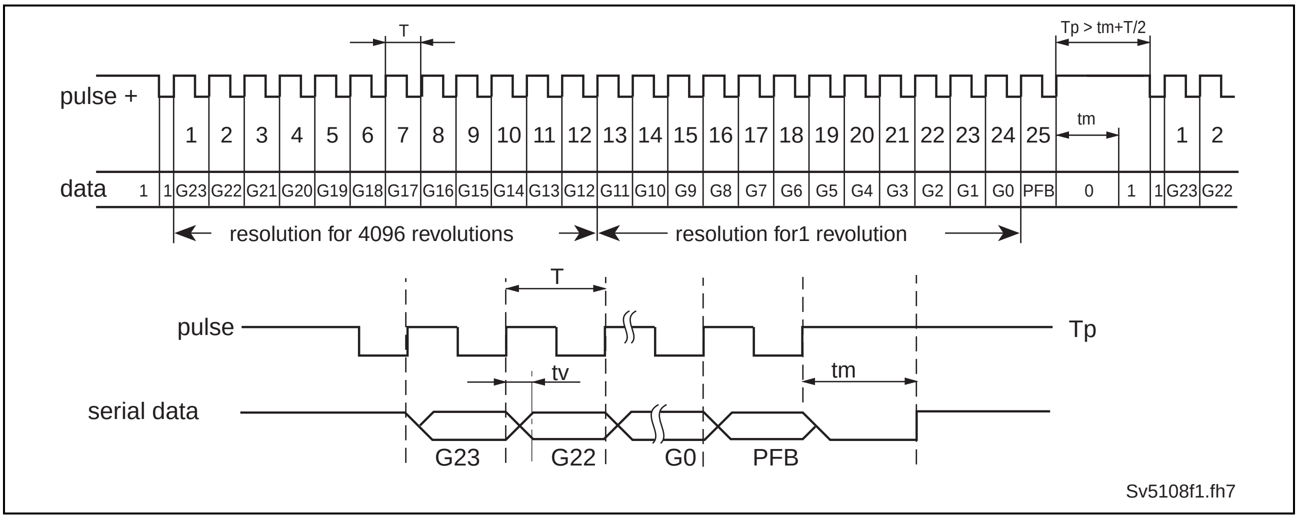


Fig. 7-10: Principle of signal paths illustrated

SSI-Interface - technical data

Power supply for plugin module DAG01.2M

input voltage X58/1:	DC 24V (±20%)
max. current consumption X58/1:	1.5 A

Power supply for external SSI measuring system

output voltage X59/25:	DC 24V (± 20%)
max. load for output X59/25:	1.5 A

Code signal

Data output Signal pulse(+) and pulse(-) from differential line driver per EIA standard RS-485.

Data input Synchronous, serial signals data(+) and data(-) for differential line receiver per EIA standard RS-485 with cable end Z_0=121 Ohm.

Notes

8 ARCNET coupler card DAK01.1M

8.1 Connecting the ARCNET coupler card DAK01.1M

The plugin module "ARCNET coupler card" is a plugin card for the CLC-D 2 control cards and creats the interface to an ARCNET bus system.

The node number can be selected via a switch on the front panel.

The green LED on the front panel displays that the ARCNET interface has been initialized and connected into the ARCNET bus.

Front panel DAK01.1 M

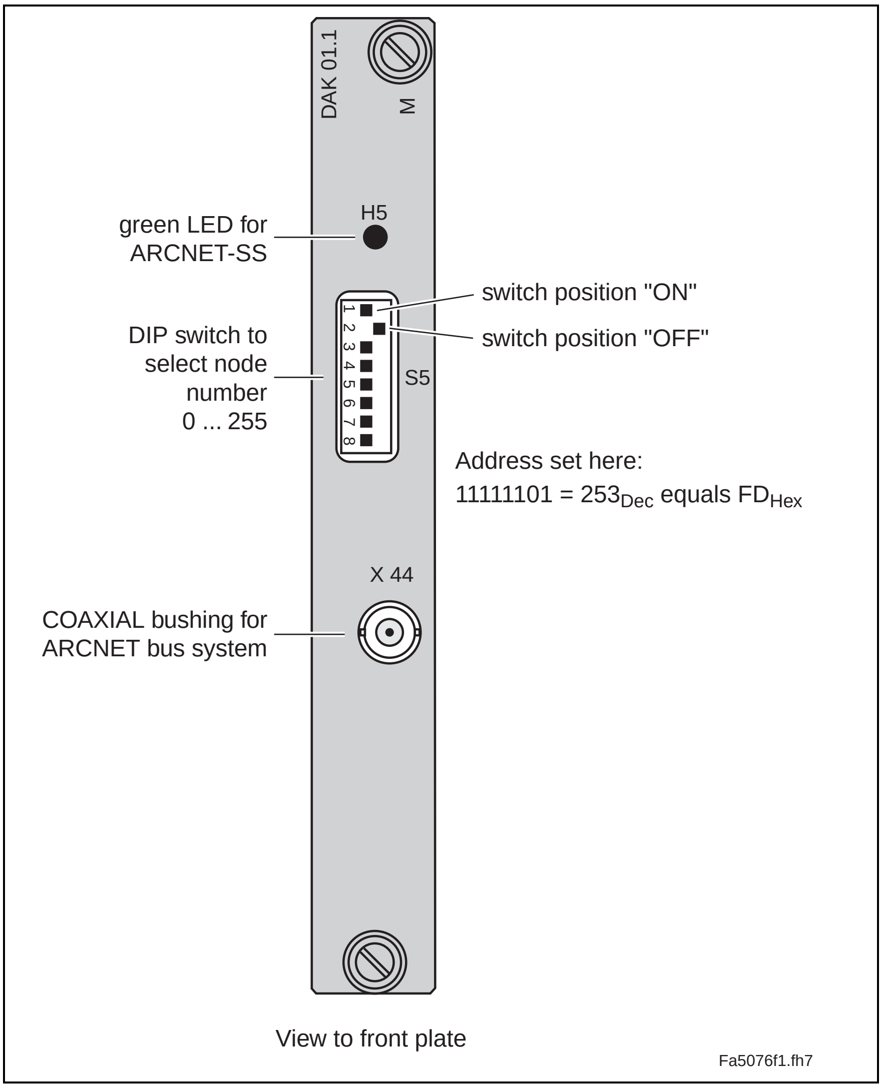


Fig. 8-1: Front panel DAK01.1M

Block diagram of an ARCNET bus system

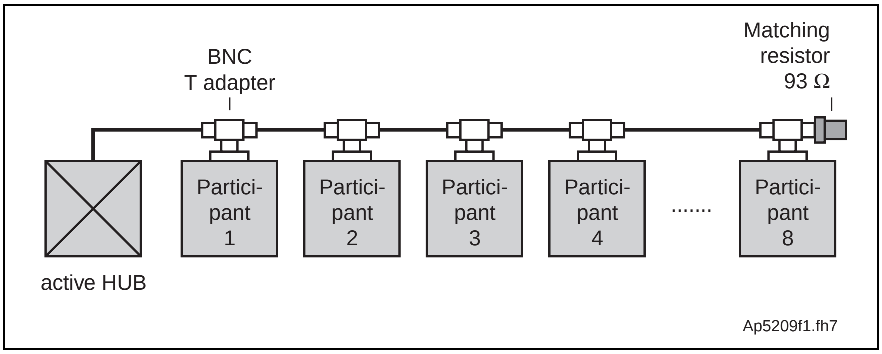


Fig. 8-2: Block diagram of an ARCNET bus system

Transmission medium, bus connection and termination

The network must be constructed using a coaxial cable of the RG-62 type or RG-71 with an impedance of 93 Ω .

The final ARCNET bus participant must be connected with a 93 Ω-terminator.

Each network participant must be connected into the bus segment via a T-BNC adapter.

Node number (participant number)

The node number is needed to clearly identify a bus participant. This node number must lie within a range of 0 ... 255 and set at the time the network is started up. Any node number change does not become effective until the CLC-D is switched off and on again once.

DAK bus connection

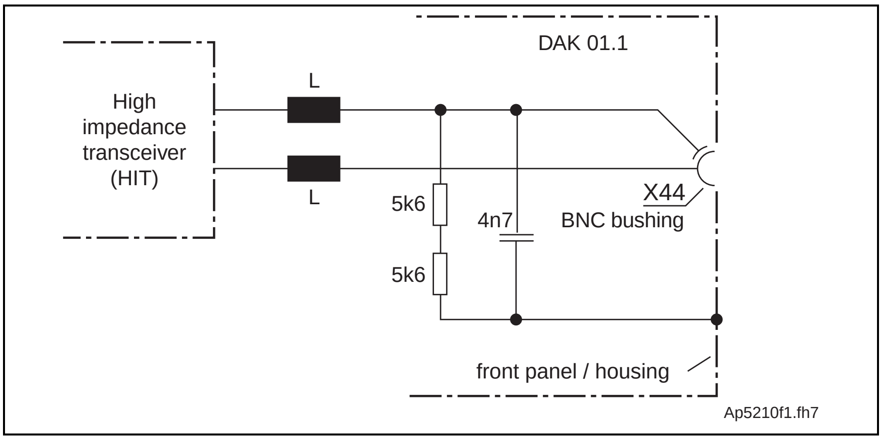


Fig. 8-3: DAK bus connection

9 CLC link interface with ARCNET DAQ02.1M

9.1 General information

Plugin module DAQ02.1M is a plugin card for the CLC-D control cards. It makes it possible to link several CLCs in one application with several master axes.

This link can be either a simple system (primary ring only) or a redundant system (primary and secondary rings).

It is also the interface to an ARCNET bus system.

9.2 DAQ02.1M - terminal diagram

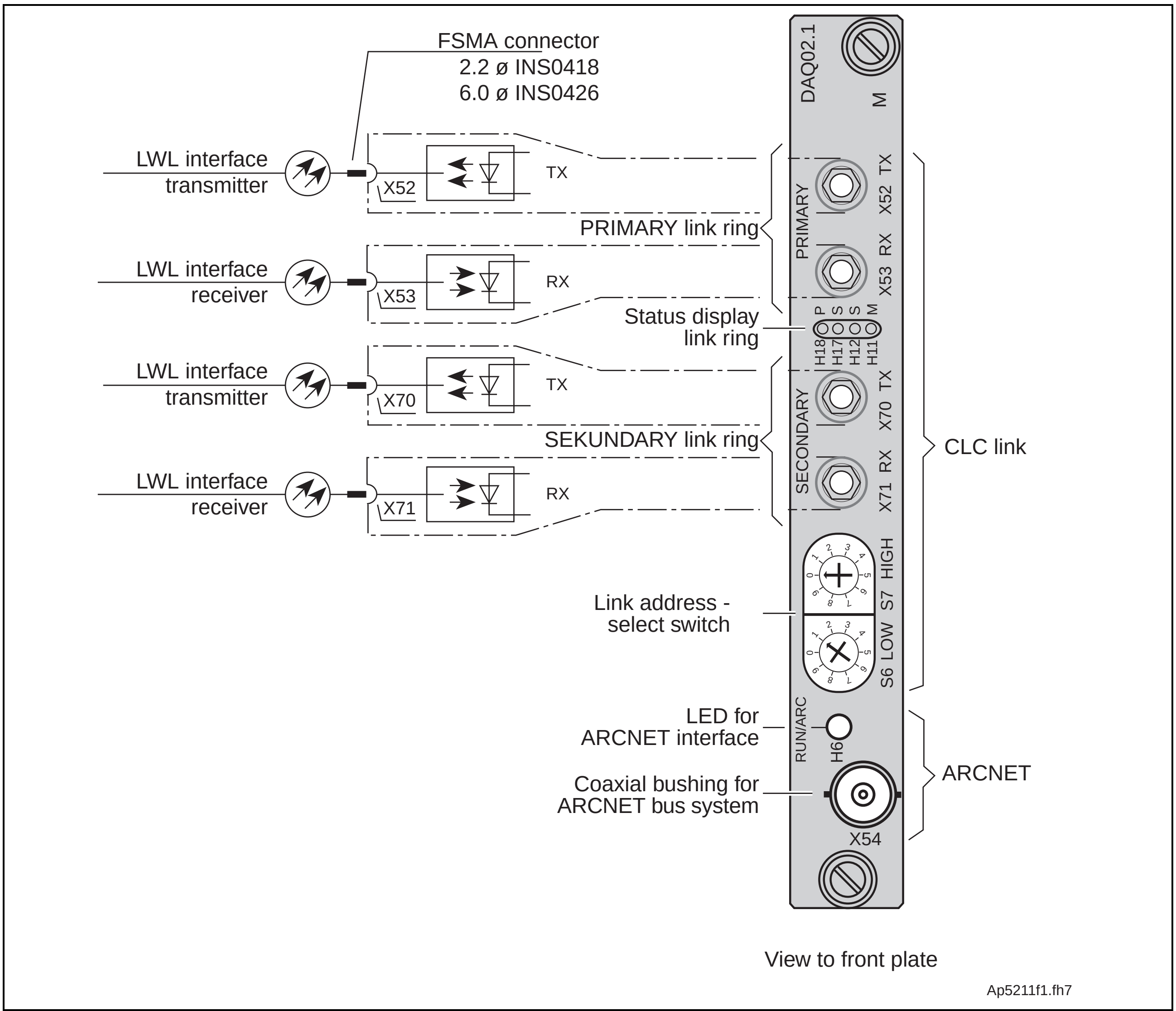


Fig. 9-1: DAQ02.1M - terminal diagram

9.3 CLC link with primary ring (simple ring)

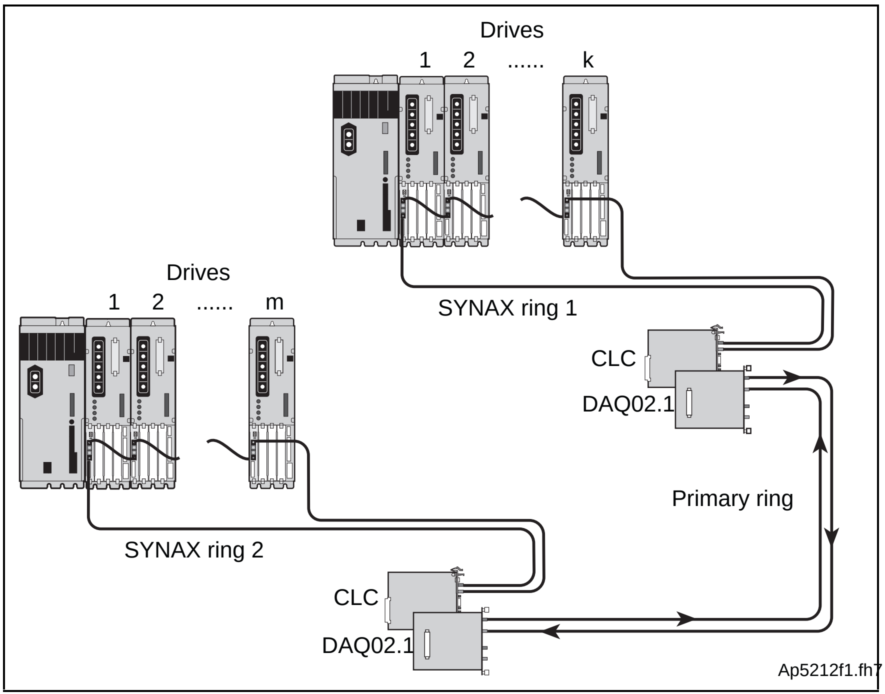


Fig. 9-2: CLC link with primary ring (simple ring)

9.4 CLC link with primary and secondary rings (double ring)

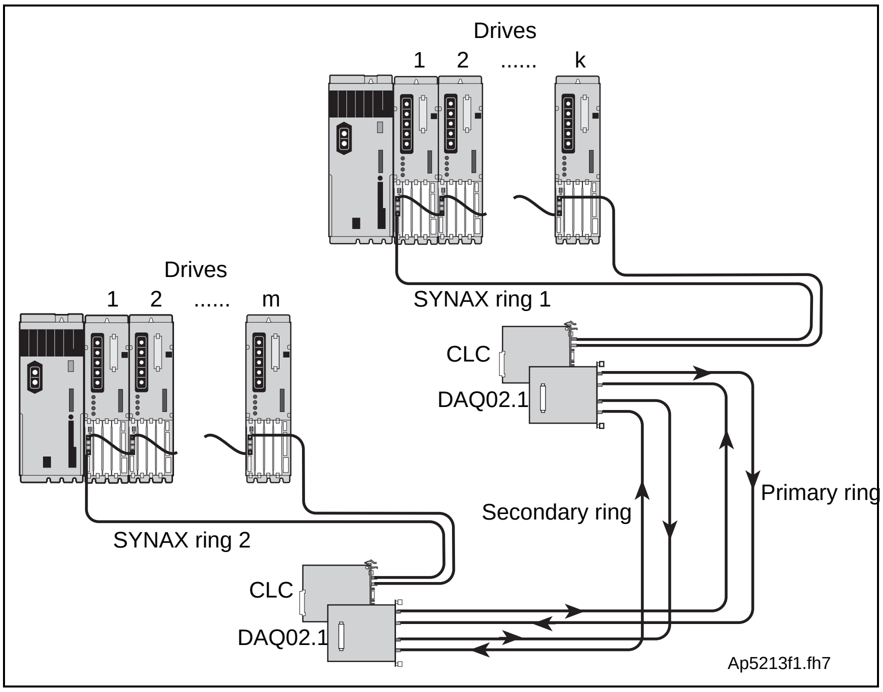


Fig. 9-3: CLC link with primary and secondary ring (double ring)

9.5 Technical data of the LWL interface primary and secondary rings

	Name	Abbreviation	Unit	Value
Transmitter data Tx	max. transmission output with opt. low level	P_{SmaxL}	dBm/µW	-28.2/1.5
	min. transmission output with opt.high level	P_{SminH}	dBm/µW	-7.5/180
	max. transmission output with opt. high level	P_{SmaxH}	dBm/µW	-3.5/450
	wavelength of the transmitter diode: peak wavelength spectral bandwidth	λp λp	nm nm	640…675 nm (0° C..55° C) - 30 nm (25° C)
Receiver data Rx	max. input power for opt. low level	P_{EmaxL}	dBm/µW	-31.2/0.75
	min. input power for opt. high level	P_{EminH}	dBm/µW	-20/10
	max. input power for opt. high level	P_{EmaxH}	dBm/µW	-5/320
	max. transmission distance damping	P_{SminH}…P_{EminH}	dB	12.5
Transmission output can be set via software parameters.				

Fig. 9-4: Technical data of the LWL interface

9.6 ARCNET bus system

Block diagram of an ARCNET bus system

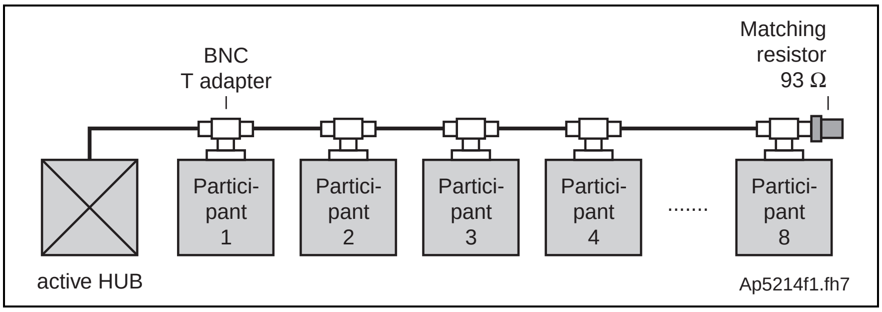


Fig. 9-5: Block diagram of an ARCNET bus system

Transmission media, bus connection and termination

The network must be constructed using a coaxial cable of the RG-62 type or RG-71 with an impedance of 93 Ω .

The final ARCNET bus participant must be connected with a 93 Ω-terminator.

Each network participant must be connected into the bus segment via a T-BNC adapter.

Node number (participant number)

The node number is needed to clearly identify a bus participant. This node number must lie within a range of 0 ... 255 and set at the time the network is started up. Any node number change does not become effective until the CLC-D is switched off and on again once.

The node number is set via S1 and S2 circuits which are on the printed circuit board (They are labelled.)

Bus connection DAQ02.1M

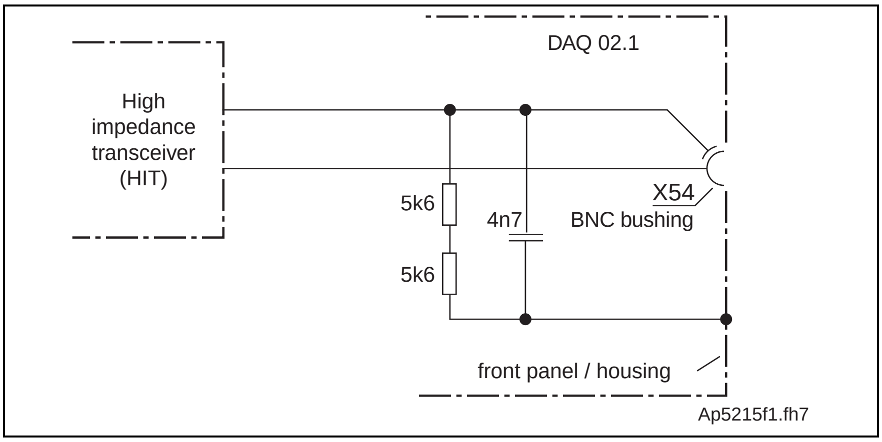


Fig. 9-6: Bus connection DAQ02.1M

10 INTERBUS-S slave assembly DBS03.1M

10.1 General information

The INTERBUS - S slave assembly DBS03.1M makes it possible to connect the control assembly CLC-D into an INTERBUS - S system.

The INTERBUS - S interface of the DBS03.1M assembly has been constructed as a long-distance bus interface and meets the standards specified by the INTERBUS - S certificate.

The DBS03.1M assembly is a plugin assembly, conceived for direct insertion onto the control assembly. Once screwed into place (with three control bolts) it becomes one unit with the CLC-D.

Note: Additional assemblies can be added to the DBS03.1M. This must be noted when dismantling or removing from card carrier!

10.2 Terminal diagram

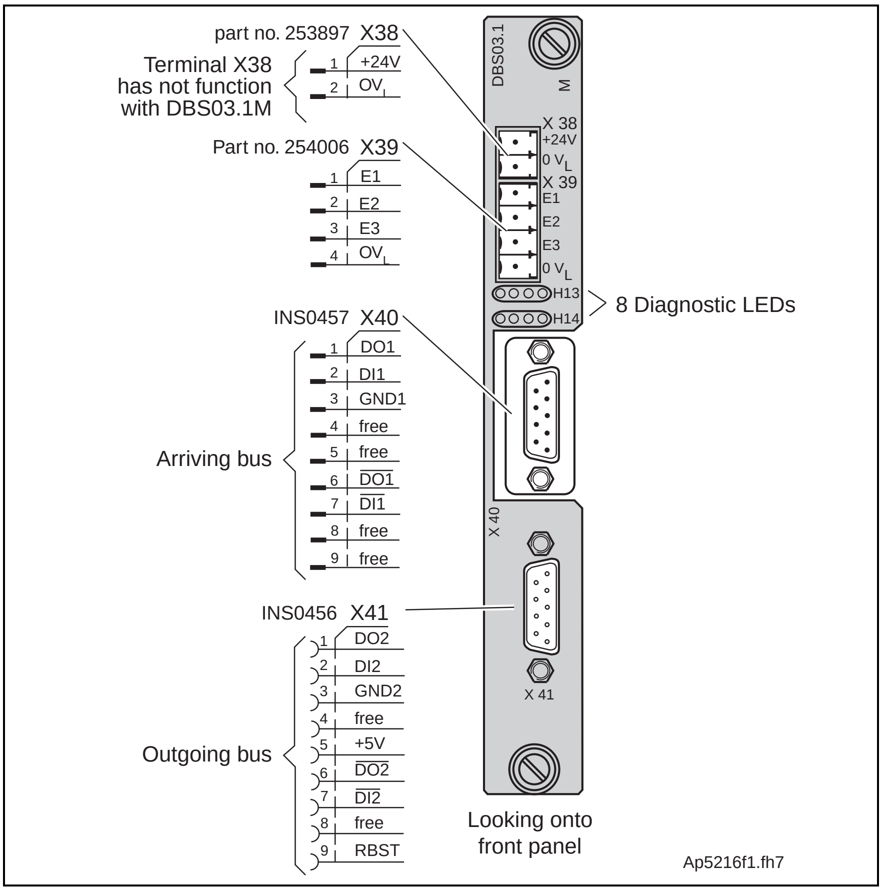


Fig. 10-1: Terminal diagram

10.3 Technical data

INTERBUS-S

Arriving interface

INTERBUS - S standard interface per DIN E 19258 for long-distance bus participants via a 9-pin D-SUB connector. The interface is completely galvanically isolated. It is outfitted with a duplex circuit based on RS 485 to couple in the previous INTERBUS - S ring participant.

Departing interface

INTERBUS - S standard interface per DIN E 19258 for long-distance bus participants via a 9-pin D-SUB connector. The interface is is also completely galvanically isolated. It is outfitted with a duplex circuit based on RS 485 to couple in the next participant. There is also a strobe signal to detect any continuing INTERBUS-S.

External inputs

The DBS03.1M assembly makes three hardware inputs (+24V) available. These can only be used in conjunction with a CLC-D if it is supported by pertinent firmware. The signal states at the inputs are transmitted, independent of INTERBUS-S status (On/Off), to the CLC-D. The INTERBUS -S master can also query these via the PD or PCP channel.

X3	Designation	Input voltage for high	Input voltage for low
1	E1	+16 V... +32 V	-0.5 V ... +8 V
2	E2	+16 V... +32 V	-0.5 V ... +8 V
3	E3	+16 V... +32 V	-0.5 V ... +8 V
4	$0V_L$	reference potential 0V	reference potential 0V

Fig. 10-2: Signal allocation X3 - external inputs

Note: The DBS03.1M assembly does not have an INTERBUS - S repeater function maintained by an external power source if the DBS03.1M is isolated from an internal source. This means that the X38 connected should not be wired.

11 Input/output interface DEA04.2M, DEA05.2M, DEA06.2M

11.1 General information

These plugin modules have 15 inputs and 16 outputs each via which the drive can exchange binary signals with the PLC.

The three types described are differentiated in terms of the address which has been set.

To prevent any confusing during installation, the D-subminiature plugin connectors are labelled.

11.2 Terminal diagram

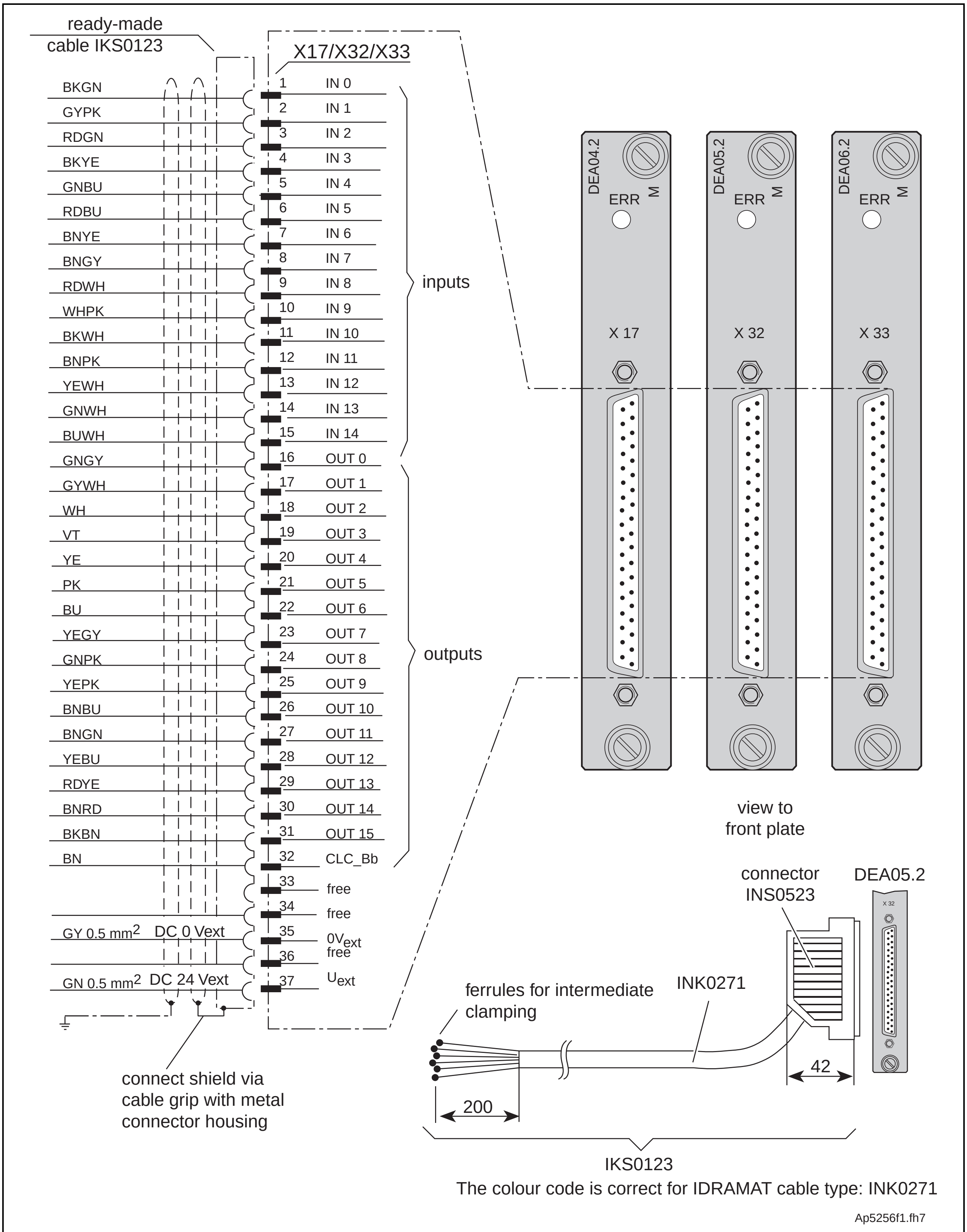


Fig. 11-1: Terminal diagram DEA 04.2M, DEA 05.2M, DEA 06.2M

11.3 Technical data DEA04.2M, DEA05.2M, DEA06.2M

Designation		Unit	min.	Type	max.
power source	$+U_{ext}$	V	18	24	32
current consumption	I_{ext}	A	0.15	0.2 1)	2.2 2)
inputs X17/1…15	$+U_{High}$ $+U_{Low}$	V V	14 0	24 <1	32 3
outputs X17/16…31	$+U_{high}$ $+U_{low}$ I_L	V V mA	U_{ext}-2 0 0	U_{ext}-1 1,6 -	U_{ext} 2 80 3)

1) current consumption of 0.2 A with no 24 V load at outputs

2) current consumption of 2.2 A with 80 mA load at each outputs

3) for the control of lamps, an inrush current must be restricted with a resistor (e.g., 100 R) to 250 mA as otherwise the overcurrent monitor is actuated and the output locked

Fig. 11-2: Technical data DEA04.2M, DEA05.2M, DEA06.2M

Block diagram of digital input and output circuits

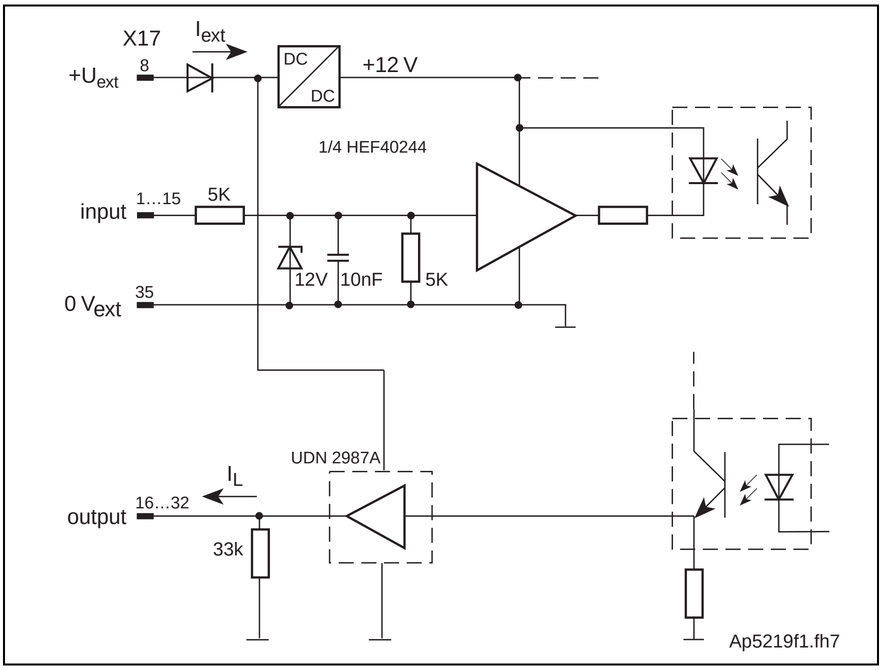
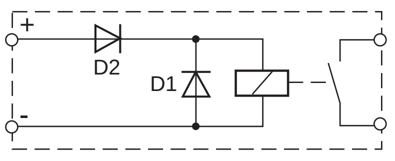


Fig. 11-3: Block diagram of digital input and output circuits

Recommended load inductance protective circuit

All relays must have free-wheeling diodes. These are protected by another diode used as protection against polarity reversal.



D1: free-wheeling diode
D2: protection against polarity reversal

Ap5218f1.fh7

Fig. 11-4: Recommended load inductance protective circuit

Error LED ERR

Note: Driver UND 2987 A limits short-circuit currents to 350mA.

If the short-circuit limit remains active for more than 1µs, then the affected output is locked (I_L=0). The other outputs are functional. The affected output remains locked until power has been switched on and off once.

Note: If driver UND 2987 A has switched one or more outputs off due to overload, then a pertinent error message is displayed in the LED.

Output CLC_ Bb

Output CLC_Bb is set to high with every edge change of output OUT15. Output CLC_Bb remains at high for 100 ms. If the state of output OUT15 does not change during this time, then output CLC_Bb goes back to low.

If there is a change within these 100 ms, then output CLC_Bb is triggered again and remains in a "high" state.

Retrigger time: 100 ms

Note: If output CLC_Bb is used, then output OUT15 can no longer be used because output OUT15 is used to retrigger output CLC_Bb.

Application:

Output CLC_Bb can be used as a kind of "Watchdog".

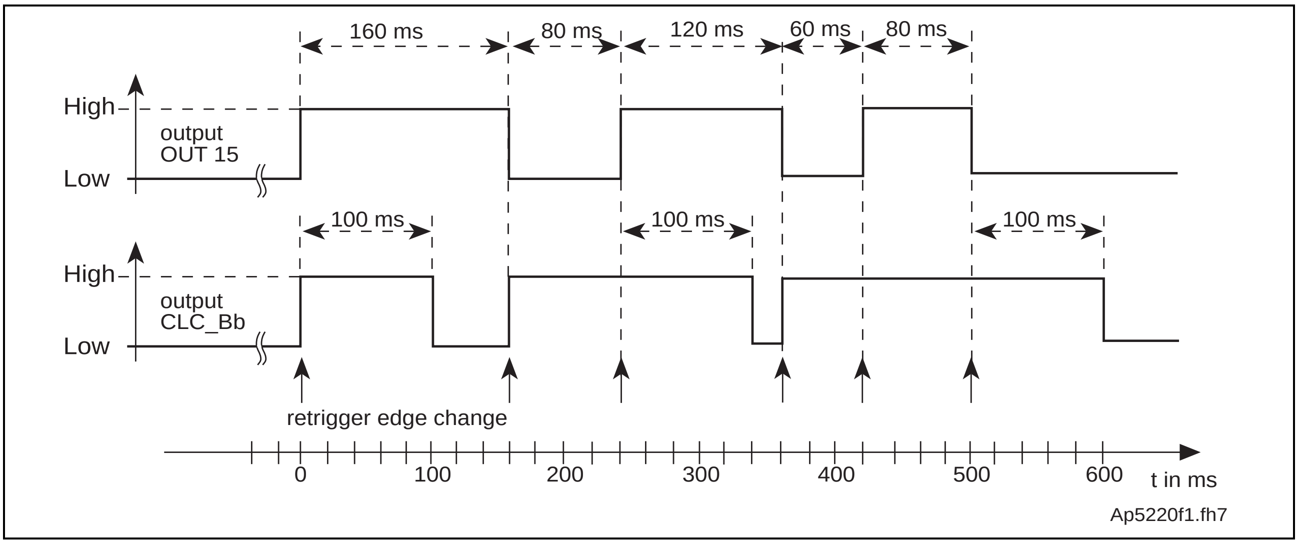


Fig. 11-5: How output CLC_Bb works

12 Input/output interface DEA08.1M, DEA09.1M, DEA10.1M

12.1 General information

These plugin modules have 32 inputs and 24 outputs each and a CLCBb output.

Up to 3 DEAs can be inserted into one drive controller.

The three aforementioned types are differentiated in terms of the address scopes set and the plugin connection designations.

To avoid confusing during installation, the plugin connectors have been labelled accordingly.

The inputs/outputs are isolated. An external power supply of DC +24V must be connected. The power supply input is protected against reversal.

12.2 Terminal diagram DEA08.1M, DEA09.1M, DEA10.1M

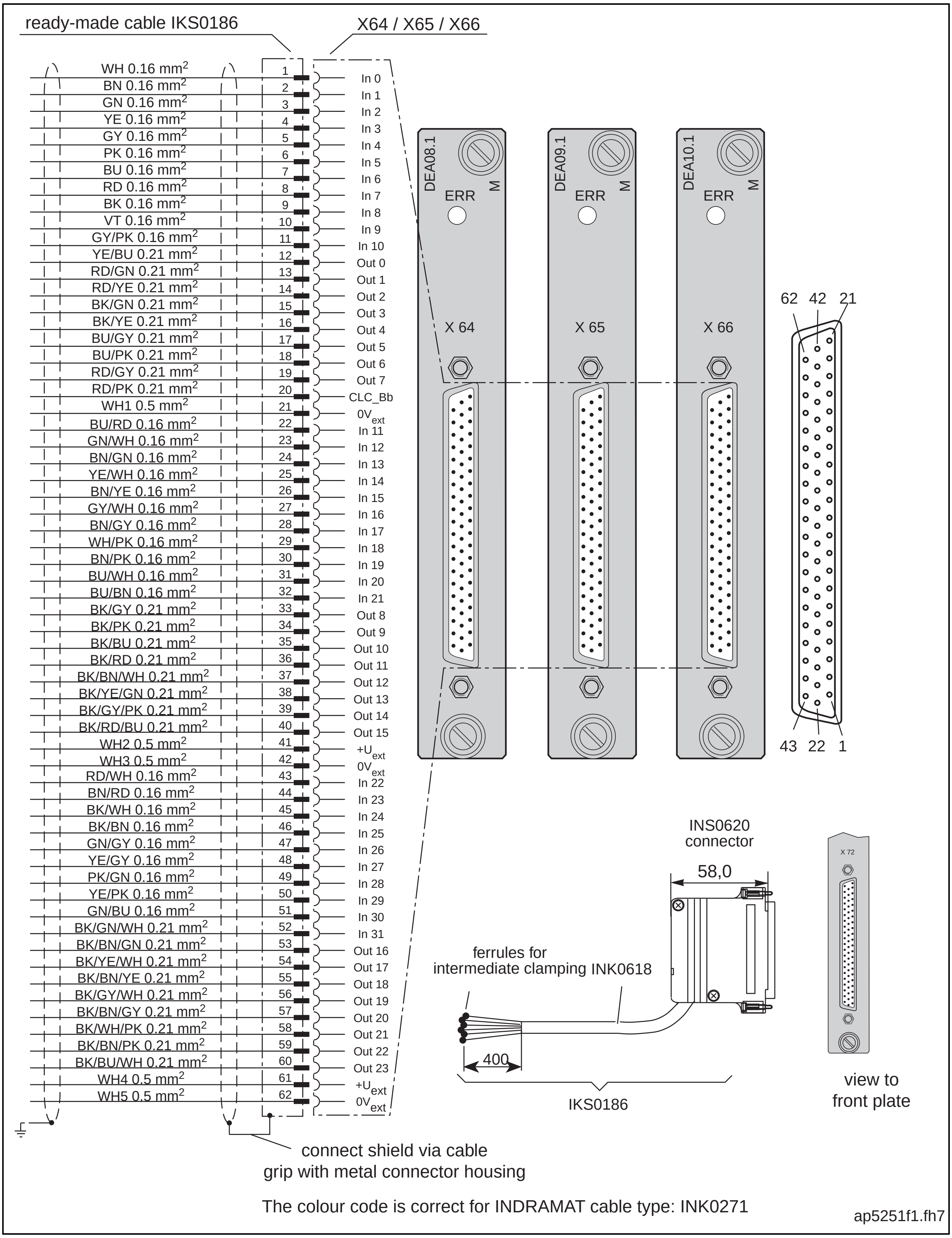


Fig. 12-1: Terminal diagram DEA08.1M, DEA09.1M, DEA10.1M

12.3 Technical data DEA08.1M, DEA09.1M, DEA10.1M

Designation		Unit	min.	Type	max.
power source	$+U_{ext}$	V	18	24	32
current consumption	I_{ext}	A	0.15	0.2[1)]	2.2[2)]
inputs IN 0…IN 31	$+U_{High}$ $+U_{Low}$	V V	14 0	24 <1	32 3
outputs OUT 0...OUT 23 CLCBb	$+U_{high}$ $+U_{low}$ I_L	V V mA	U_{ext}-2 0 0	U_{ext}-1 1,6 -	U_{ext} 2 80[3)]
1) current consumption of 0.2 A with no 24 V load at outputs					
2) current consumption of 2.2 A with 80 mA load at each outputs					
3) for the control of lamps, an inrush current must be restricted with a resistor (e.g., 100 R) to 250 mA as otherwise the overcurrent monitor is actuated and the output locked.					

Fig. 12-2: Technical data DEA08.1M, DEA09.1M, DEA10.1M

Block diagram of the digital input and output circuits

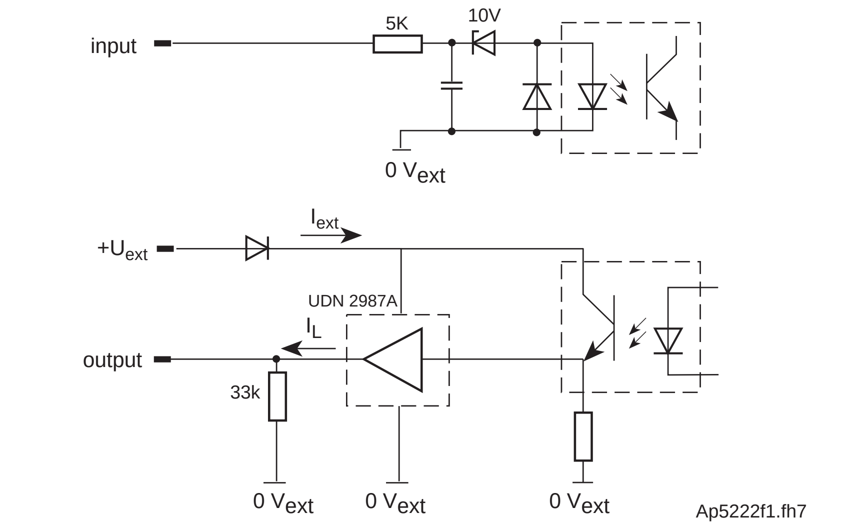
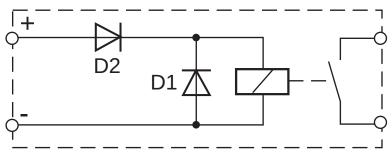


Fig. 12-3: Block diagram of the digital input and output circuits

Recommended load inductance protective circuit

All relays must have free-wheeling diodes. These are protected by another diode used as protection against polarity reversal.



D1: free-wheeling diode
D2: protection against polarity reversal

Ap5221f1.fh7

Fig. 12-4: Recommended load inductance protective circuit

Error LED ERR

Note: Driver UND 2987 A limits short-circuit currents to 350mA.

If the short-circuit limit remains active for more than 1µs, then the affected output is locked (I_L=0). The other outputs are functional. The affected output remains locked until power has been switched on and off once.

Note: If the driver UND 2987 A has locked one or more outputs due to overload, then this error is displayed.

Output CLC_ Bb

Output CLC_Bb is set to high with every edge change in a parameter. Output CLC_Bb remains at high for 100 ms. If the state of the bit does not change in this time, then output CLC_Bb goes back to low.

If there is a change in the relevant bit within these 100 ms, then output CLC_Bb is triggered again and remains in "high" state.

Retrigger time: 100 ms

Application:

Output CLC_Bb can be used as a kind of "Watchdog"

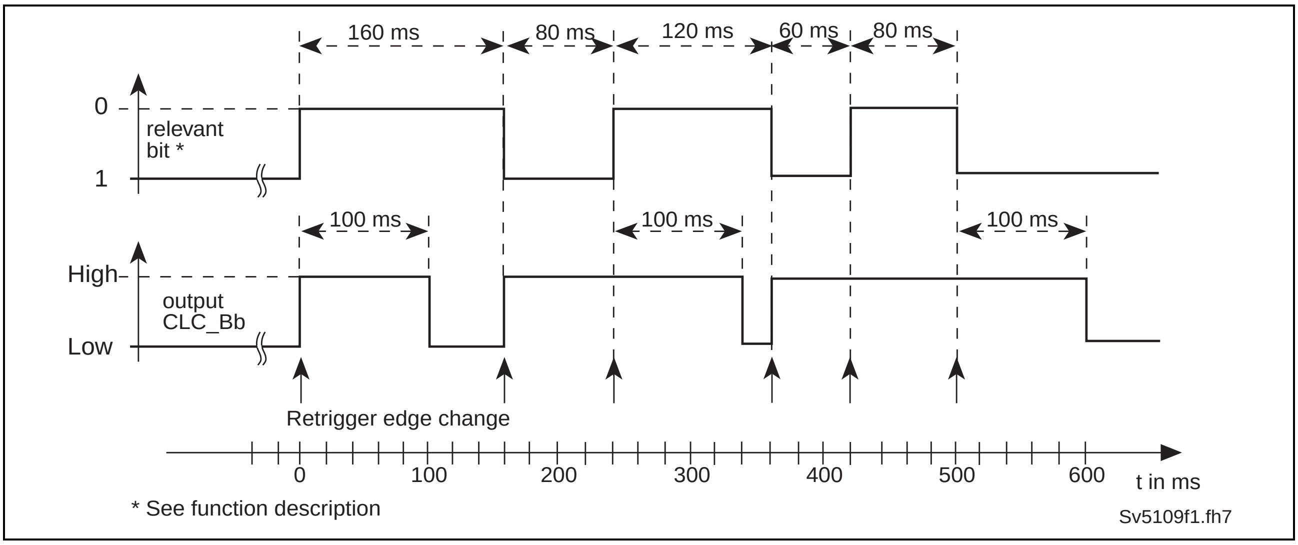


Fig. 12-5: How output CLC_Bb works

13 Input/output interface DEA28.1M, DEA29.1M, DEA30.1M

13.1 General information

These plugin modules have 32 inputs, 24 outputs and a CLC Bb output each. The plugin modules are inserted into control cards CLC-D... (see illustration below).

Up to three DEAs can be inserted into one CLC-D... control card.

The three aforementioned plugin modules are differentiated in terms of the address scope set and the designations of the plugin connections. To avoid confusion during installation, these have been labelled.

Arranging the DEAs on the CLC-D ...

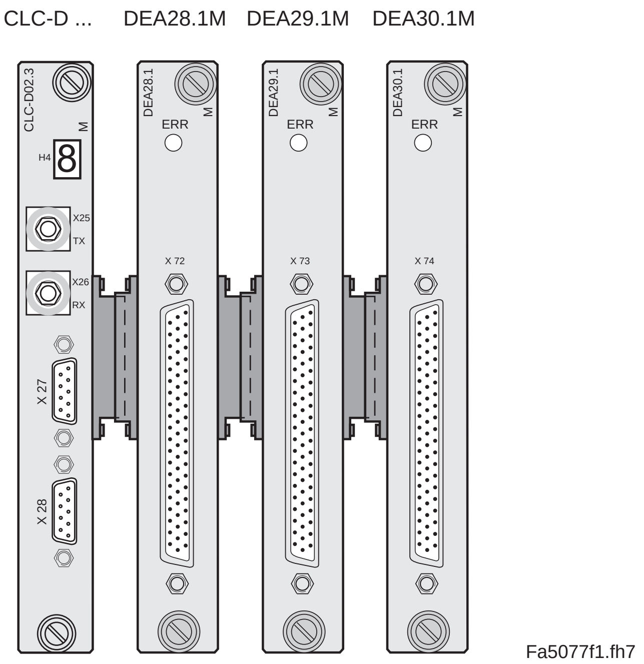


Fig. 13-1: Arranging the DEAs on the CLC-D ...

The inputs and outputs are isolated. An external power supply of DC +24 V has to be connected. The input for the power supply is protected against reversal.

13.2 Terminal diagram

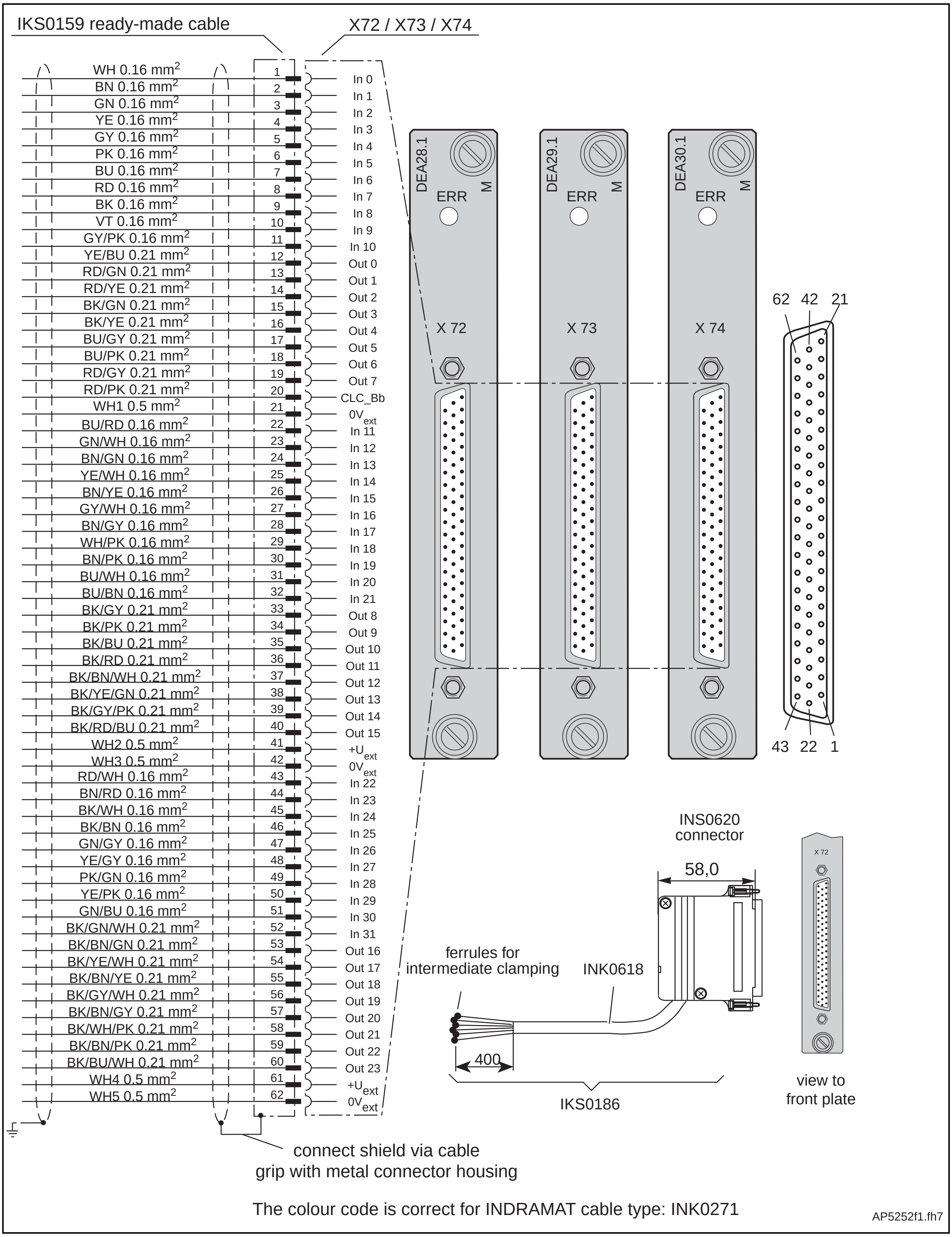


Fig. 13-2: Terminal diagram DEA28.1M, DEA29.1M, DEA30.1M

13.3 Technical data DEA28.1M, DEA29.1M, DEA30.1M

Technical data

Designation		Unit	min.	Type	max.
Power source	$+U_{ext}$	V	18	24	32
current consumption	I_{ext}	A	0,15	0,2[1)]	2,2[2)]
inputs IN 0…IN 31	$+U_{High}$ $+U_{Low}$	V V	14 0	24 <1	32 3
outputs OUT 0...OUT 23 CLCBb	$+U_{high}$ $+U_{low}$ I_L	V V mA	U_{ext}-2 0 0	U_{ext}-1 1,6 -	U_{ext} 2 80[3)]
1) current consumption of 0.2 A with no 24 V load at outputs 2) current consumption of 2.2 A with 80 mA load at each outputs 3) for the control of lamps, an inrush current must be restricted with a resistor (e.g., 100 R) to 250 mA as otherwise the overcurrent monitor is actuated and the output locked.					

Fig. 13-3: Technical data DEA28.1M, DEA29.1M, DEA30.1M

Block diagram of the digital input and output circuits

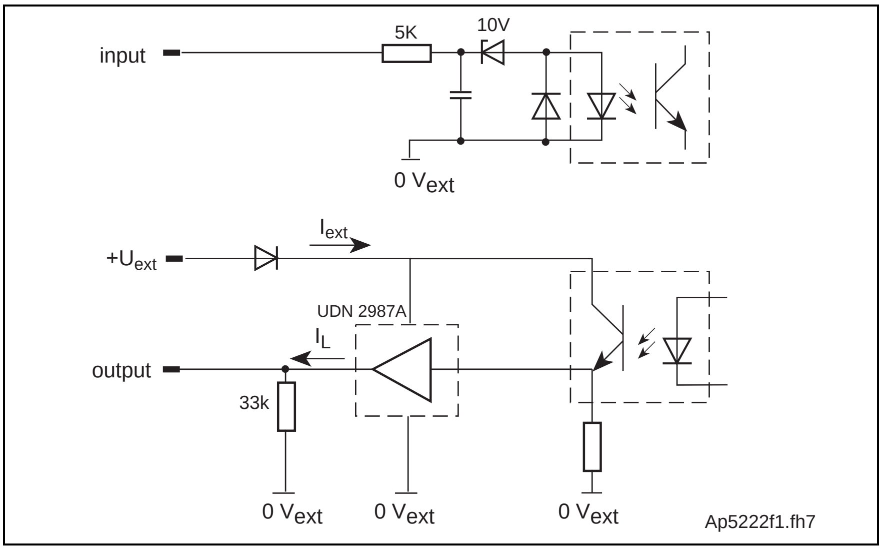
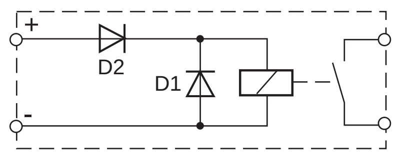


Fig. 13-4: Block diagram of the digital input and output circuits

Recommendded load inductance protective circuit

All relays must have free-wheeling diodes. These are protected by another diode used as protection against polarity reversal.



D1: free-wheeling diode
D2: protection against polarity reversal

Ap5221f1.fh7

Fig. 13-5: Recommended load inductance protective circuit

Error LED ERR

Note: Driver UND 2987 A limits short-circuit currents to 350mA.

If the short-circuit limit remains active for more than 1µs, then the affected output is locked (I_L=0). The other outputs are functional. The affected output remains locked until power has been switched on and off once.

Note: If the driver UND 2987 A has locked one or more outputs due to overload, then this error is displayed.

Output CLC_ Bb

Output CLC_Bb is set to high with every edge change in a parameter. Output CLC_Bb remains at high for 100 ms. If the state of the bit does not change in this time, then output CLC_Bb goes back to low.

If there is a change in the relevant bit within these 100 ms, then output CLC_Bb is triggered again and remains in "high" state.

Retrigger time: 100 ms

Application:

Output CLC_Bb can also be used as a kind of "Watchdog".

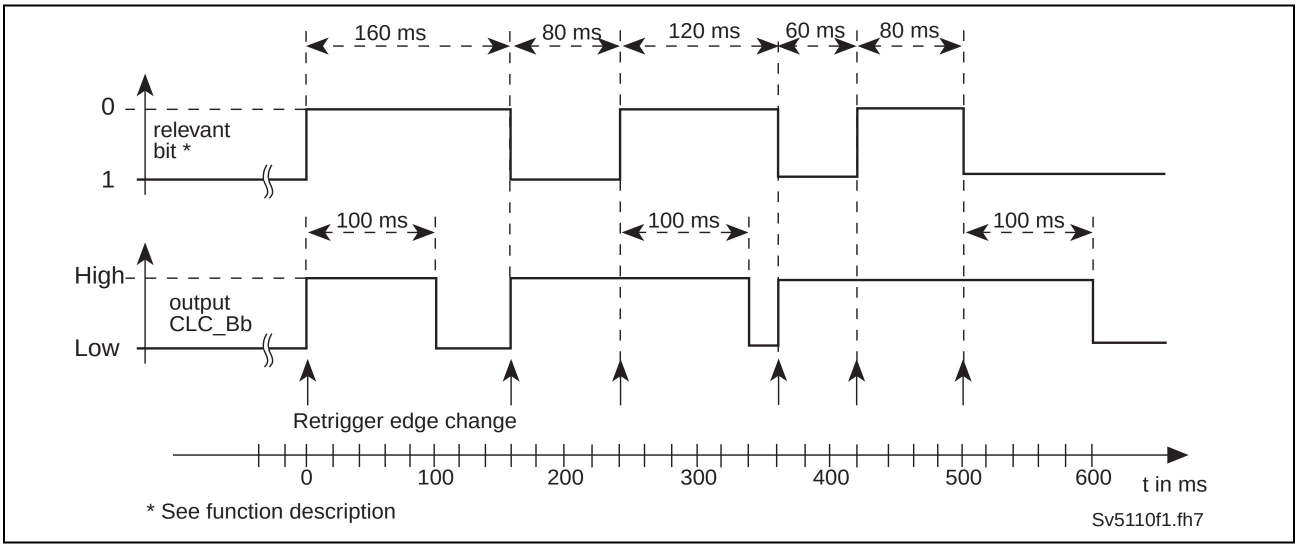


Fig. 13-6: How output CLC_Bb works

14 Position interface for square-wave signals DEF01.1M and DEF02.1M

14.1 General information

The plugin modules "Incremental position interface" support square-wave signal acceptance in the drive controller for detecting measuring systems mounted externally, directly on moving machine parts.

The incremental positioning interfaces for squarewave signals DEF01.1M and DEF02.1M differentiate in the way they respond to different address ranges. These are automatically divided up during the initialization phase to whatever positioning interfaces have been inserted.

The D-subminiature plug-in connections have been variously labelled to avoid any confusion during installation.

14.2 Connector assignment - DEF01.1M and DEF02.1M

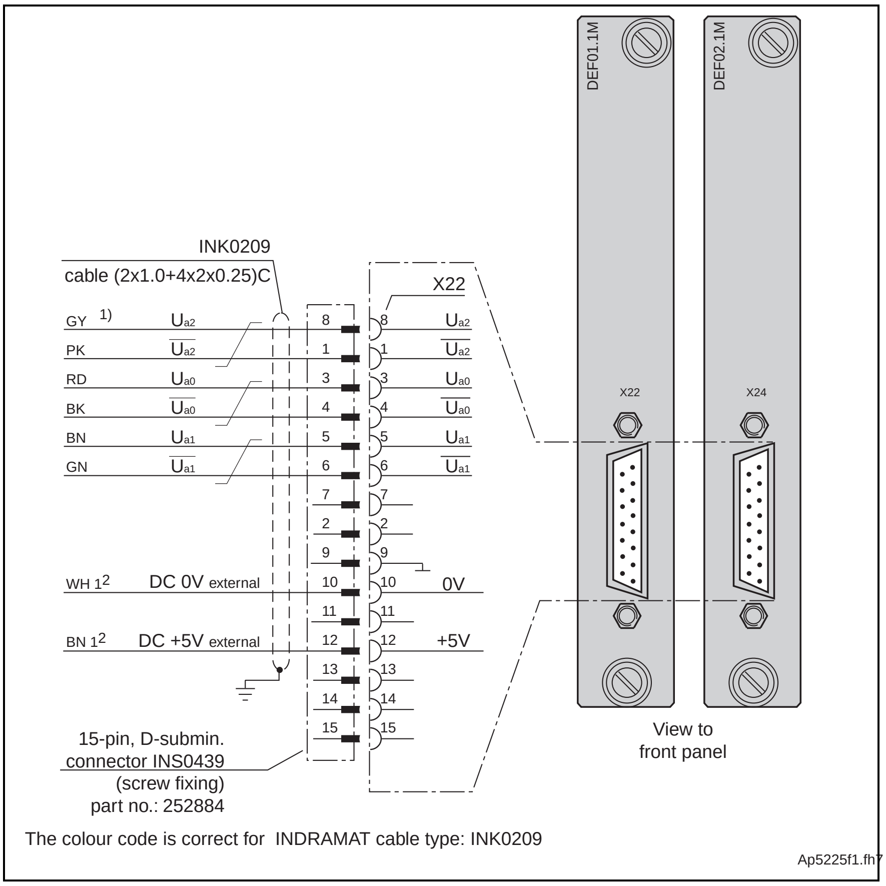


Fig. 14-1: Connector assignment - position interface for square-wave signals DEF01.1M and DEF02.1M

14.3 Technical data DEF01.1M and DEF02.1M

Power source of the external measuring system

Designation	Unit	min.	type / value	max.
output voltage +5 V	V	4.75	5	5.25
output current +5 V	mA			250

Fig. 14-2: Power source of the external measuring system

Voltage level and phase position of input signals

Designation		Unit	min.	type / value	max.
signal voltage	U_{High}	V	2,5		
signal voltage	U_{Low}	V			0.5
phase position	U_{a1}	°el.		0	
phase position	U_{a2}	°el.		90	
max. input frequency		kHz			1000
signal period interpolation				4 -fold	
reference point delay t1		ns			50
edge distance t2		ns	250		

Fig. 14-3: Voltage level and phase position of the input signals

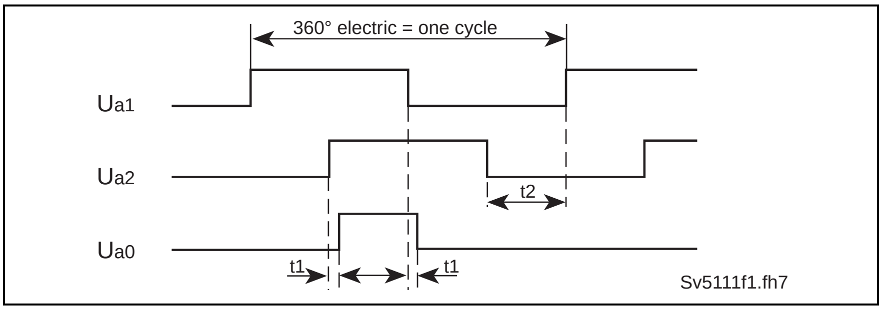


Fig. 14-4: Principle of signal paths illustrated

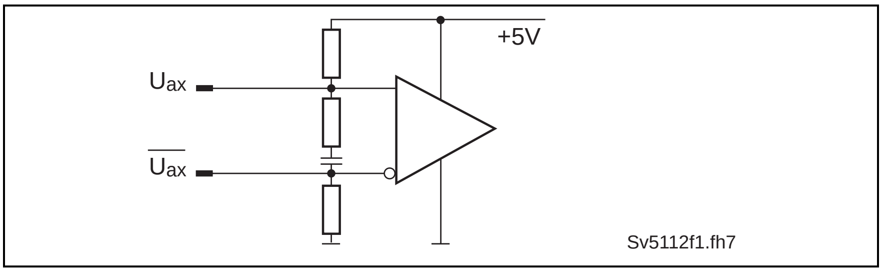


Fig. 14-5: Principle of the input circuit illustrated

15 Encoder interface DFF01.1M

15.1 General information

The plugin module "Encoder interface DFF01.1M" supports position determination of a measuring system GDS01.1 / GDM01.1 directly mounted to moving machine components.

Application example:

The single turn encoder interface DFF01.1M can support the connection of a main shaft encoder GDS01.1 to a digital drive controller and the transmission of encoder signals to other drive controllers.

Application:

- electronic shaft
- synchronization of the drive to the main shaft encoder

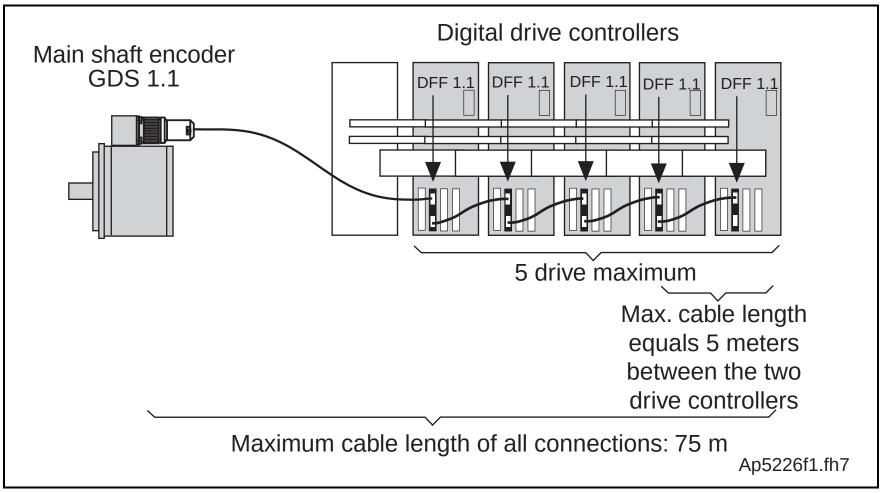


Fig. 15-1: Arrangement of the DFF01.1M

15.2 Terminal diagram

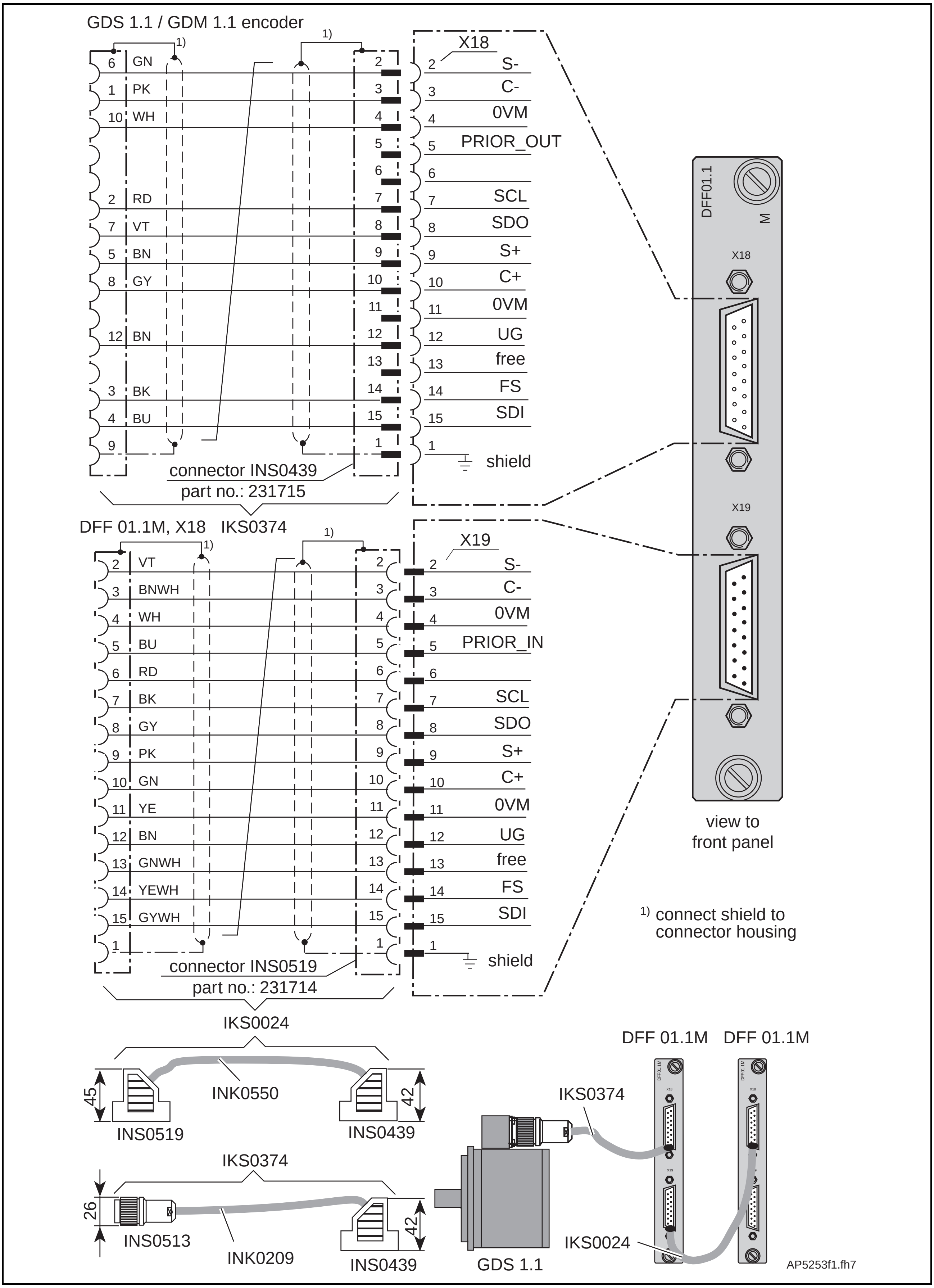


Fig. 15-2: Terminal diagram DFF01.1M

16 High-resolution position interface for sinusoidal signals DLF01.1M

16.1 General information

Measuring systems

The plugin module "High-resolution position interface DLF01.1M" supports the acceptance of sinusoidal signals for position detection of external measuring systems mounted directly to moving machine parts.

The high-resolution position interface DLF01.1M evaluates measuring systems with

- sinusoidal **current** signals (7 ... 11 µA$_{SS}$) or with
- sinusoidal **voltage** signals (1 V$_{SS}$).

Changing current to voltage signals

By bridging X23/1 and X23/12 in the connector of the DLF01.1M plugin modules, the DLF01.1M can be switched to evaluate voltage signals.

If this connection is missing, then the DLF01.1M evaluates current signals.

16.2 Terminal diagrams

Terminal diagram for measuring systems with voltage signals

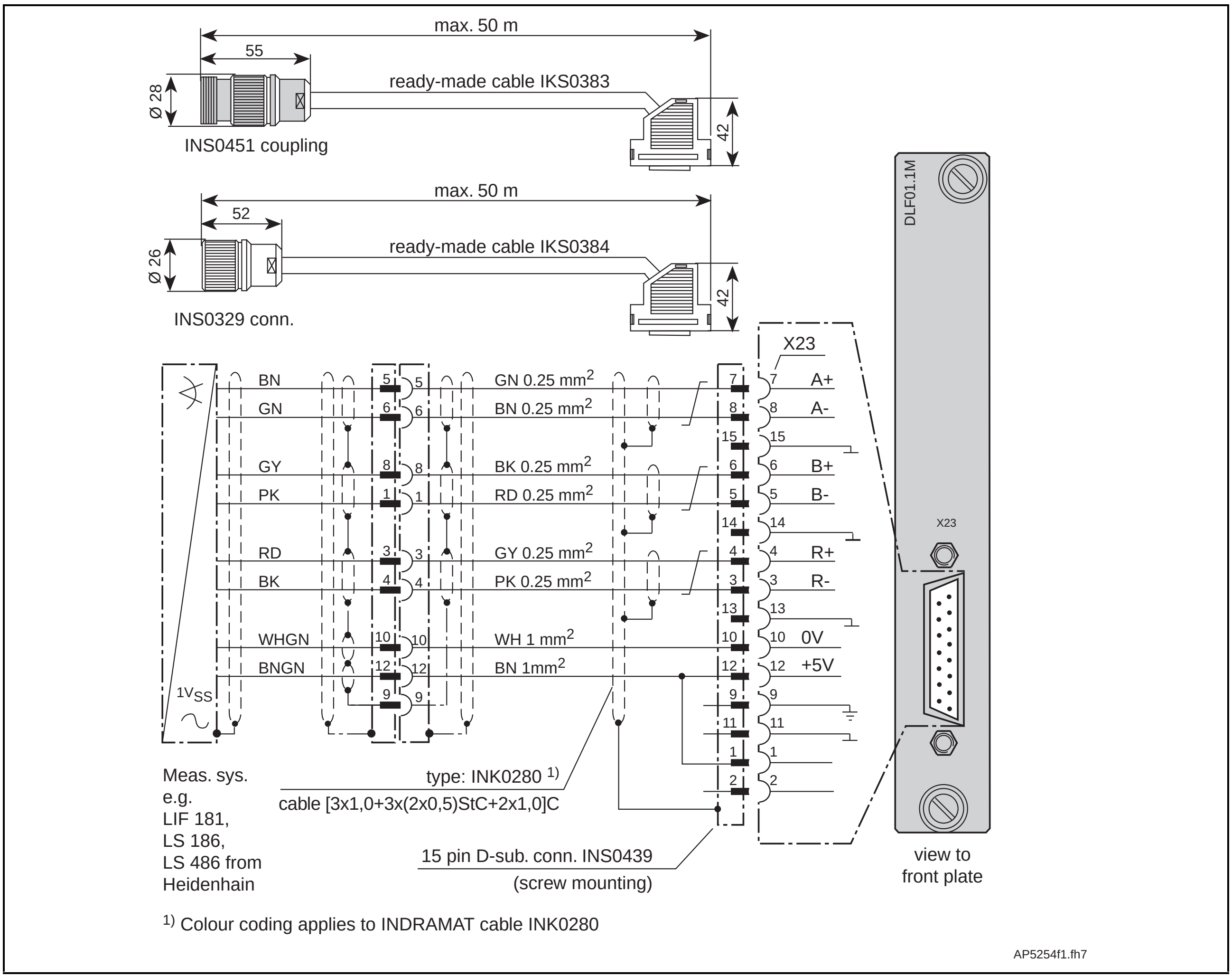


Fig. 16-1: Terminal diagram for measuring systems with voltage signals

Signal breakdown of measuring systems with voltage signals

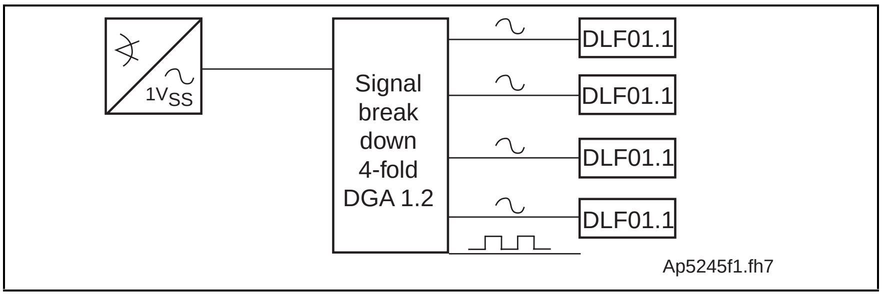


Fig. 16-2: Signal breakdown of measuring systemsn with voltage signals

For further information see encoder branching DGA01.2 (S.23-1).

Terminal diagram for measuring systems with current signals

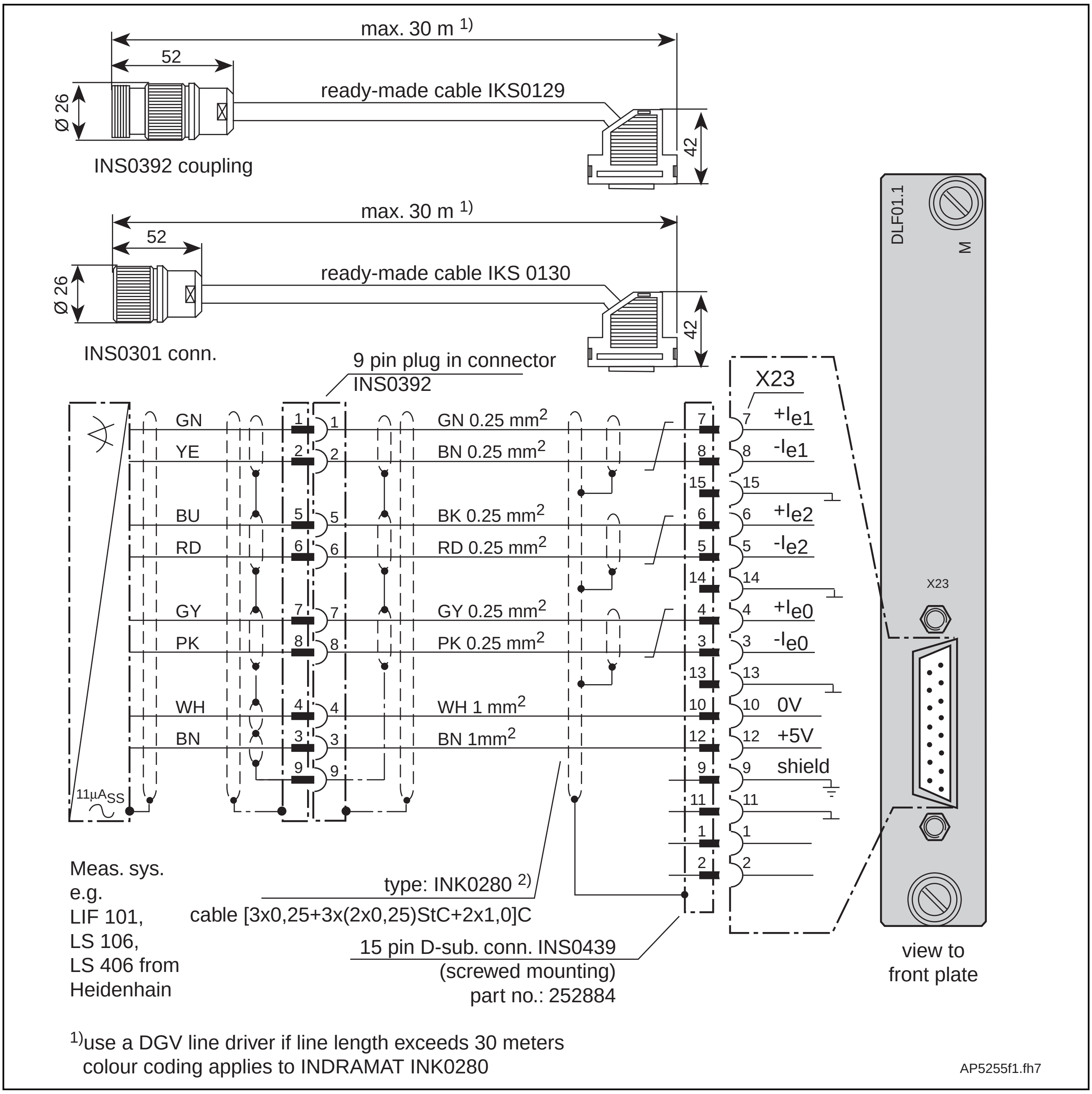


Fig. 16-3: Terminal diagram for measuring systems with current signals

With line lengths >30m, use line driver DGV01.1 (see S. 23-6).

16.3 Technical data DLF01.1M

Power source for external measuring system	output voltage X23/12:	DC +5	V (±5%)		
	maximum output load X23/12:	150	mA		
Signal form	approximate sinusoidal signals				
Resolution	The signal periods supplied by the measuring system have a 2048-fold resolution.				
Voltage signals	signal voltage:	A, B, R	1	V_{SS}	
	max. frequency for measuring system signals:	A, B	500	kHz	
	max. frequency for referencing signals:	R	15	kHz	
Current signals	Signal current:	I_{e1}, I_{e2}	7…16	μA_{SS}	
		I_{e0}	2…8	μA_{SS}	
	max. frequency for measuring system signals:	I_{e1}, I_{e2}	150	kHz	
	max. frequency for referencing signals:	I_{e0}	15	kHz	

Signal input circuit

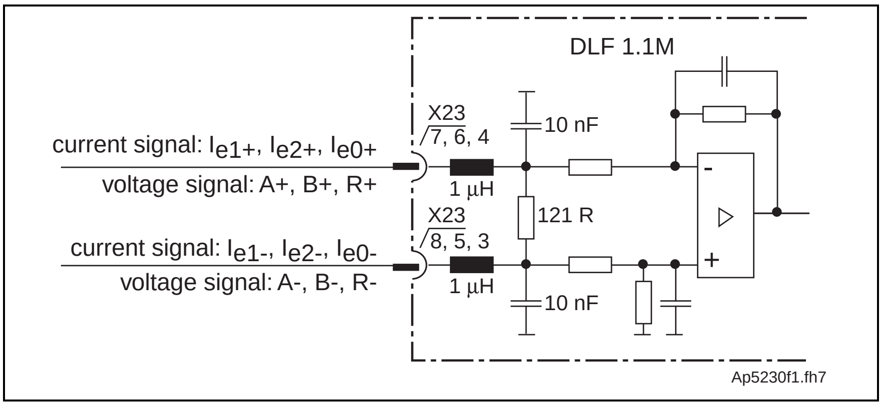


Fig. 16-4: Signal input circuit

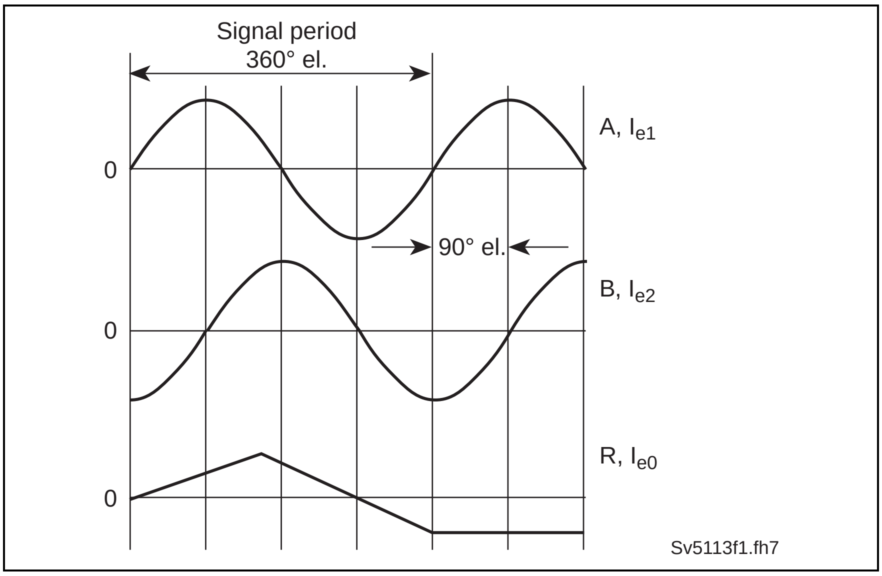


Fig. 16-5: Principle of signal paths illustrated

Notes

17 Profibus Interface DPF05.1M-FW

17.1 General information

The Profibus interface DPF05.1M-FW makes it possible to connect the control board CLC-D into a Profibus system. By designing the board in the form of a Profibus-DP-Combi-slave, it is possible to connect it into Profibus networks of the Profibus-DP or Profibus-FMS types or a mixture as per DIN19245-3.

The DPF05.1M-FW has been designed as a plugin assembly which can be directly inserted into the control board. After it is screwed into place with the guide bolts, it creates one unit with the CLC-D.

Note: Additional boards can be inserted into the DPF05.1M-FW. This must be noted when dismantling or removing the card carrier!

17.2 Terminal diagram

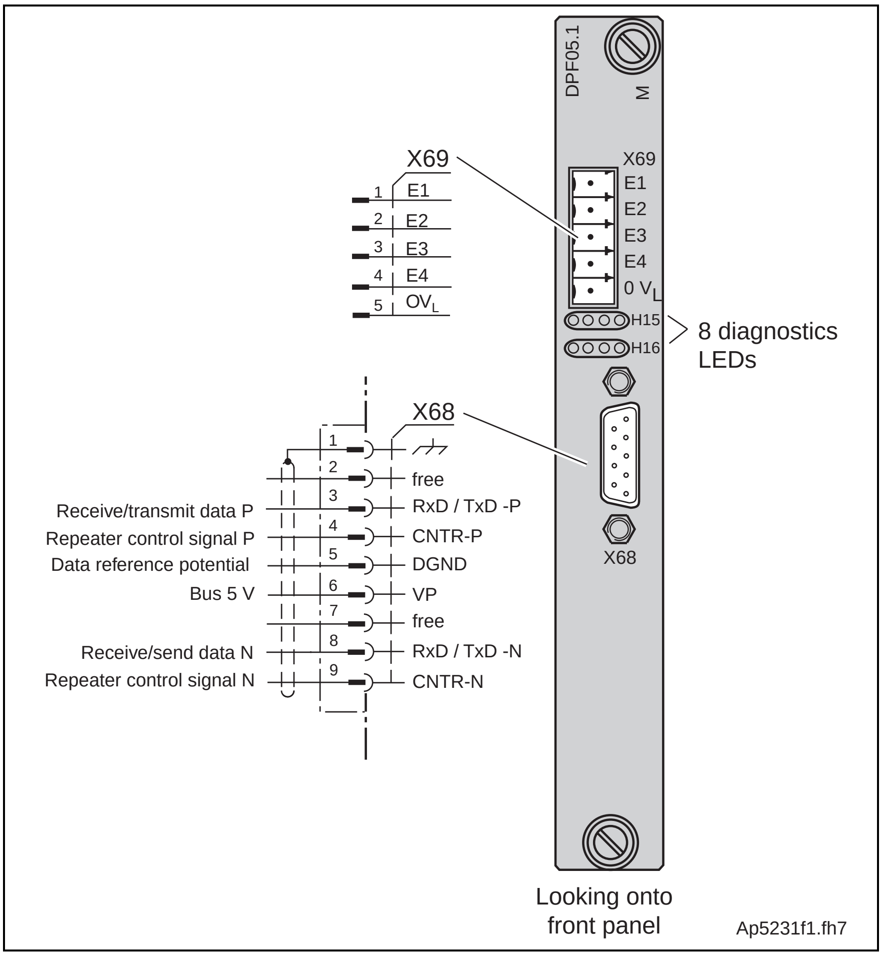


Fig. 17-1: Terminal diagram DPF05.1M-FW

17.3 Technical data

External inputs

The DPF05.1M makes four hardware inputs (+24V) available. These can only be used in conjunction with the CLC-D, if it is supported by the pertinent firmware. The signal states at these inputs are transmitted, independent of Profibus status (On/Off), to the CLC-D. The Profibus master can, however, also query them via the DP or FMS channel.

X69	Designation	Input voltage for high	Input voltage for low
1	E1	+16 V... +32 V	-0.5 V ... +8 V
2	E2	+16 V... +32 V	-0.5 V ... +8 V
3	E3	+16 V... +32 V	-0,. V ... +8 V
4	$0V_L$	reference potential 0V	reference potential 0V

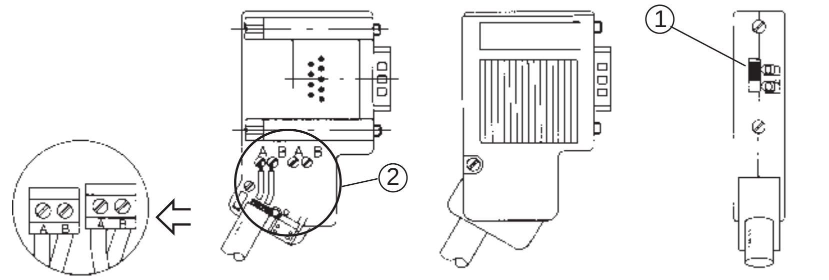
Fig. 17-2: Signal allocation - X69 - external inputs

Profibus interface

Profibus interface per DIN 19245, sec. 1 with line termination for lines of categories A or B as per DIN 19245, section 3.

The Profibus line is connected at X68. The connector is not supplied with DPF05.1M, but can be ordered separately.

The PROFIBUS connector is outfitted with one switchable terminating resistor. It must be switched on at the first and final bus participant. Do not confuse cores A and B. Connect as per the following illustration.

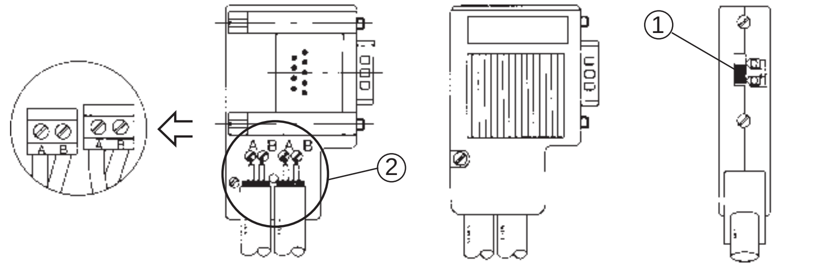


① Switch position for the first and final slave in the Profibus-DP

② The cable shield must be applied bare to the metal guide.

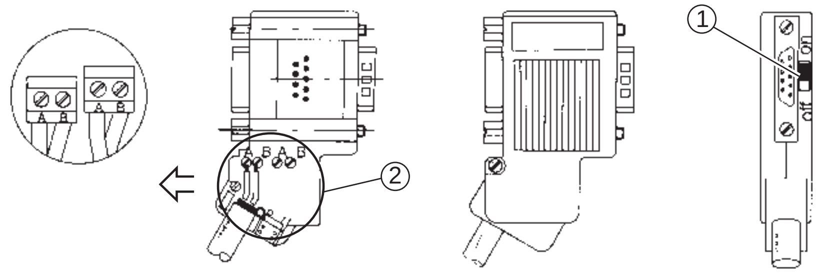
Fa5079f1.fh7

Fig. 17-3: Bus connection for the first and final slave, bus connector INS0450 without 9-pin D-subminiature bushing



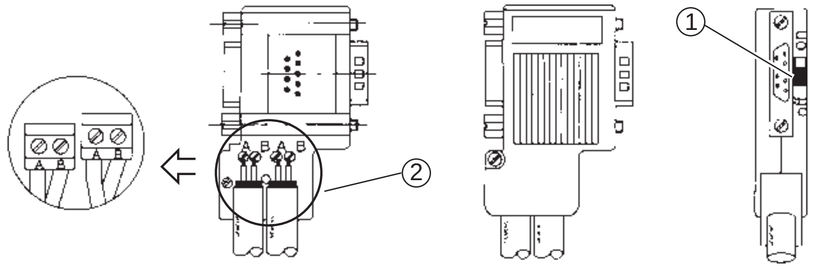
① Matching resistor is switched off.
② The cable shield must be applied bare to the metal guide.
Fa5081f1.fh7

Fig. 17-4: Bus connection for all other slaves, bus connector INS0540, without 9-pin D-subminiature bushing



① Switch position for the first and final slave in the Profibus-DP
② The cable shield must be applied bare to the metal guide.
Fa5080f1.fh7

Fig. 17-5: Bus termination for the first and final slave, bus connector INS0541, with 9-pin D-subminiature bushing



① Matching resistor is switched off.
② The cable shield must be bare when placed against the metal guide.
Fa5078f1.fh7

Fig. 17-6: Bus connection for all other slaves, bus connector INS0541 with 9 pin D-subminiature bushing

Connect DPF05.1M to the control via a shielded two-wire line as per DIN 19245, section 1.

Notes

18 Analog signal interface DRF01.1M

18.1 General information

Plugin module DRF 01.1M supports:

- the measurement of voltages via the differential inputs S1/S3 and S2/S4 for evaluation in the drive controller.

18.2 Terminal diagram DRF01.1M

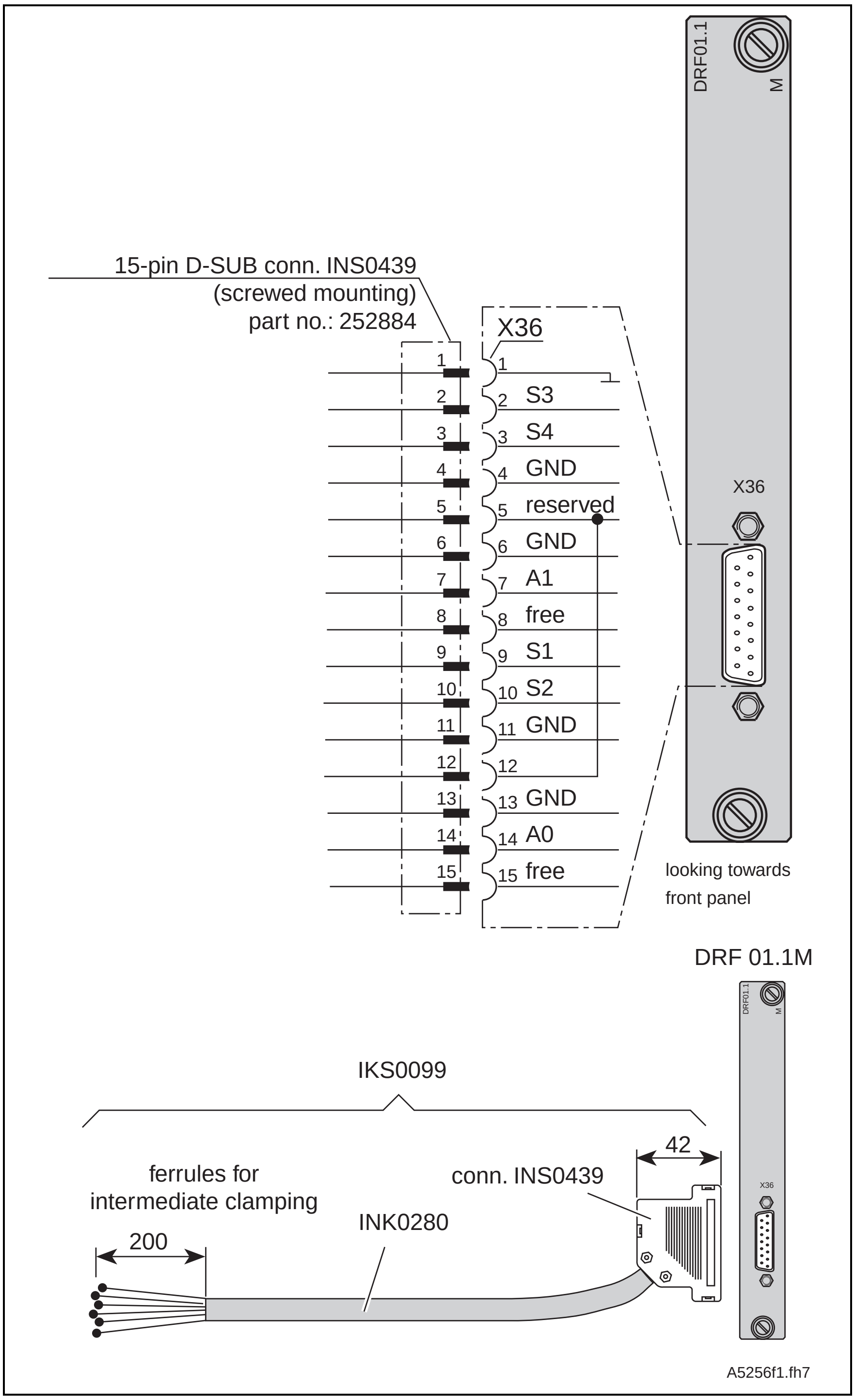


Fig. 18-1: Terminal diagram DRF01.1M

18.3 Technical data DRF01.1M

Block diagram input channels S1/S3 and S2/S4

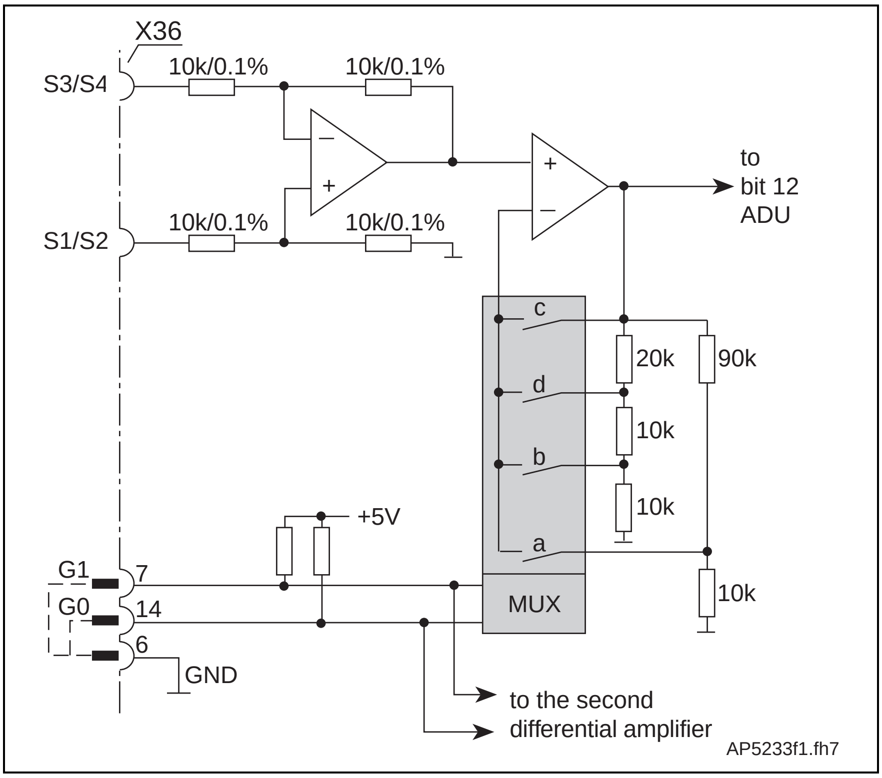


Fig. 18-2: Block diagram input channels S1/S3 and S2/S4

Setting desired amplification

Amplication is set by interconnecting pins 7 and 14 with pin 6 (GND).
If pins 7 and 14 are open, then amplification 2 has been set.

Interconnecting X36

Connection at	**X36**	**MUX channel**	**Desired amplificiation**
Pin 7	Pin 14		
free	free	d	2 (default)
free	GND	c	1
GND	frei	b	4
GND	GND	a	10

Fig. 18-3: Interconnecting X36

Voltage level and resolution of the input signals

Amplification	Input voltage	min.	resolution 12 bit	max.
1	S1, S2 S3, S4 |S1-S3| |S2-S4| resolution	-10 V -10 V	4.88 mV/bit	+10 V +10 V 10 V 10 V
2	S1, S2 S3, S4 |S1-S3| |S2-S4| resolution	-5 V -5 V	2.44 mV/bit	+5 V +5 V 5 V 5 V
4	S1, S2 S3, S4 |S1-S3| |S2-S4| resolution	-2,5 V -2,5 V	1.22 mV/bit	+2,5 V +2,5 V 2,5 V 2,5 V
10	S1, S2 S3, S4 |S1-S3| |S2-S4| resolution	-1 V -1 V	0.49 mV/bit	+1 V +1 V 1 V 1 V

Fig. 18-4: Voltage level and resolution of the input signals

The maximum permissible voltage at the differential amplification inputs S1 to S4 equals |±50 V|.

Note: The maximum permissible voltage at the differential amplification inputs S1 to S4 equals ± 50V.

Notes

19 Absolute encoder emulator DSA01.1M

19.1 General information

Plugin module "Absolute encoder emulator" generates absolute actual position values complying with SSI standards (Synchronous serial interface).

19.2 Terminal diagram DSA01.1M

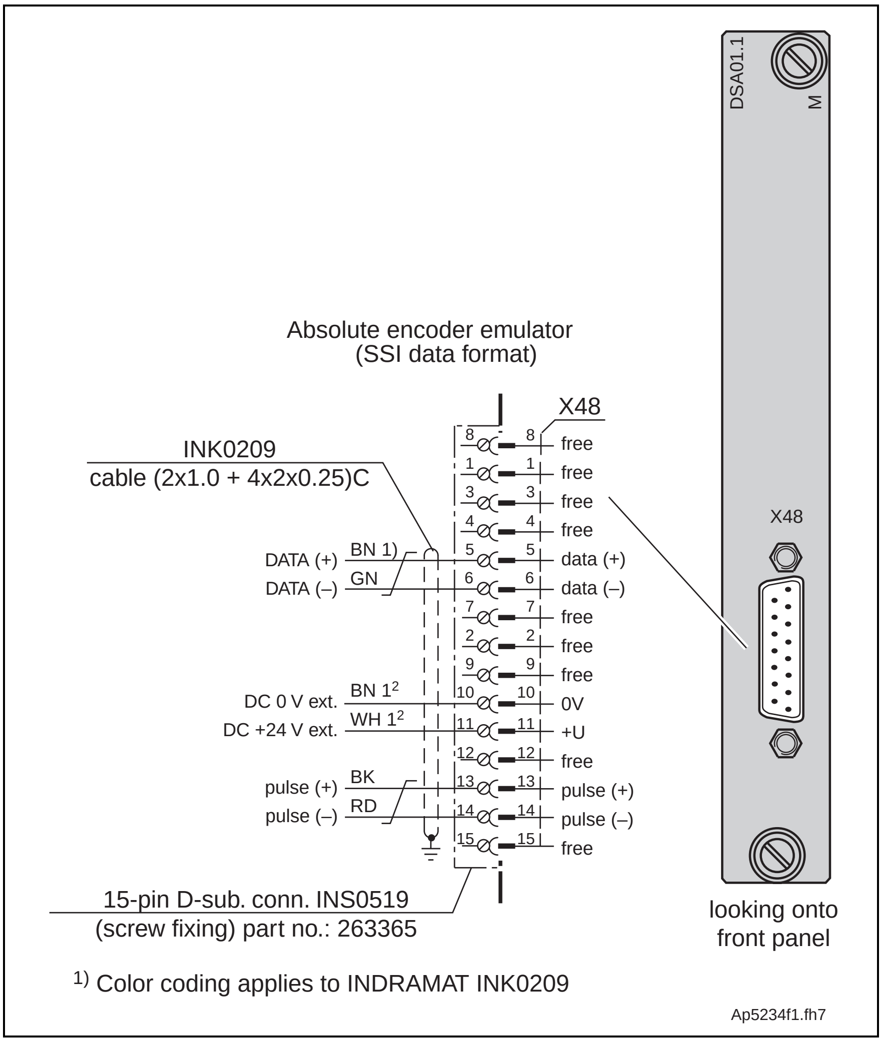


Fig. 19-1: Terminal diagram DSA01.1M

19.3 Technical data DSA01.1M

Power supply and signal level of the absolute encoder emulator

	Designation	Unit	min	typ	max
	Power source $+U_{ext}$	V	10	24	32
	current consumption of the $+U_{ext}$	mA		100	200
Transmitter	output current Low-Level $+I_{0L}$ High-Level $+I_{0L}$	 mA mA			 60 -60
	output voltage. V0 with Io=0	V	0		5.25
	Diff.-output voltage $\|V_{D01}\|$ with I0=0 $\|V_{D02}\|$ with $R_L = 54\ \Omega$	 V V	 1.5 1.5		 5.25 5.0
Receiver	Diff.-input voltage Low-Level V_{TL} High-Level V_{TL}	 V V	 0.2		 0.2
	Hysteresis V_{HVS}	mV		50	

Fig. 19-2: Power supply and signal level of the absolute encoder emulator

Absolute encoder output circuit

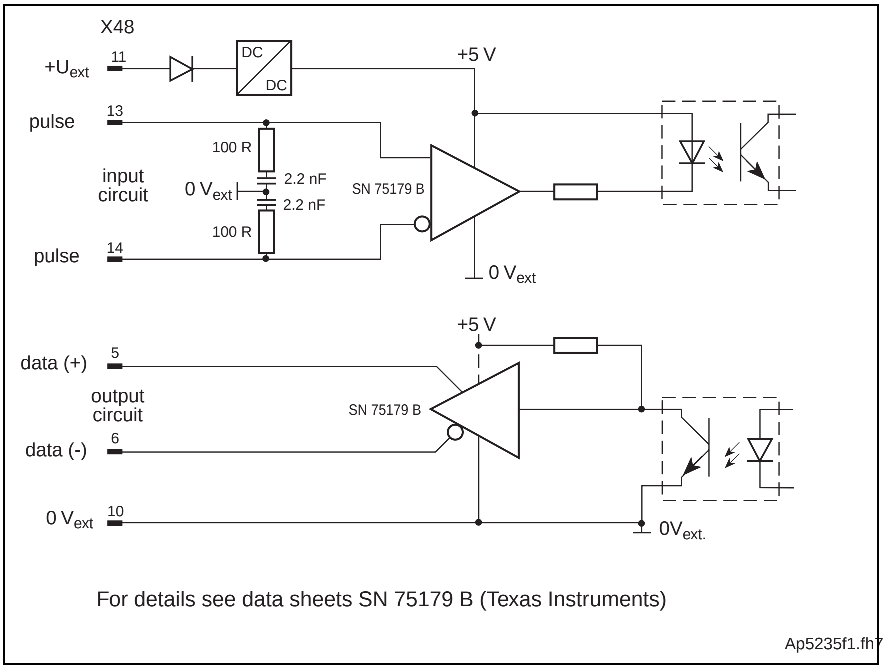


Fig. 19-3: Absolute encoder output circuit

Ready-made cable for X48

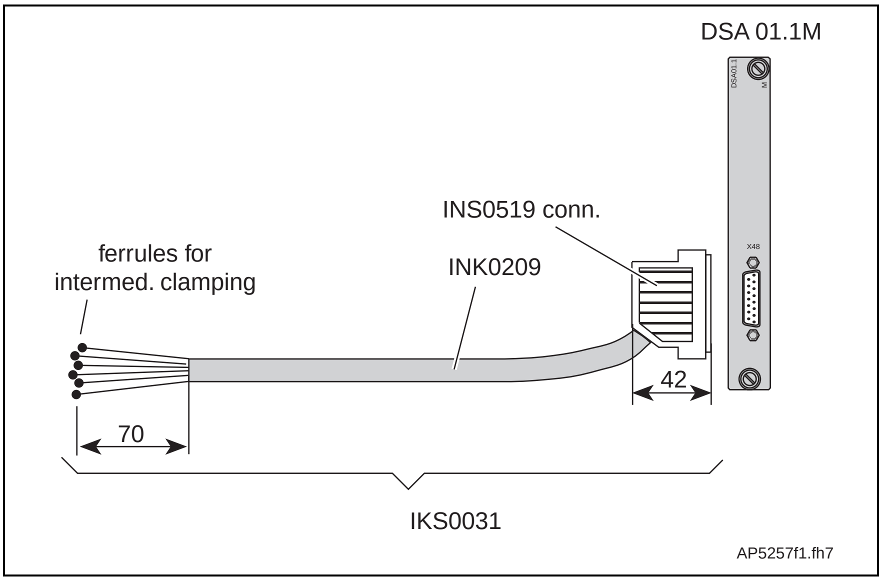


Fig. 19-4: Ready-made cable for X48

Recommended pulse frequency for data transmission

Line length in m	pulse frequency in kHz
< 50	< 400
< 100	< 300
< 200	< 200
< 400	< 100

Fig. 19-5: Recommended pulse frequency for data transmission

Actual position output in absolute format

probe code:	Gray Code
data scope:	4096 rotations
resolution:	4096 increments/360°
data format:	24 Bit + PFB (not used, always "0")
count direction:	switchable
data transmission:	synchronous, serial
input/output circuit:	driver per EIA RS 422 A (see block diagram)

Designation	Unit	min.	typ/Value	max.
monoflop time tm	µs		15...25	
pulse frequency f_T	MHz	0.1		1
pulse break T_p	µs	40		
period duration of pulse signal T	µs	1		10
decel time t_v	ns			540

Fig. 19-6: Actual position value output in absolute format

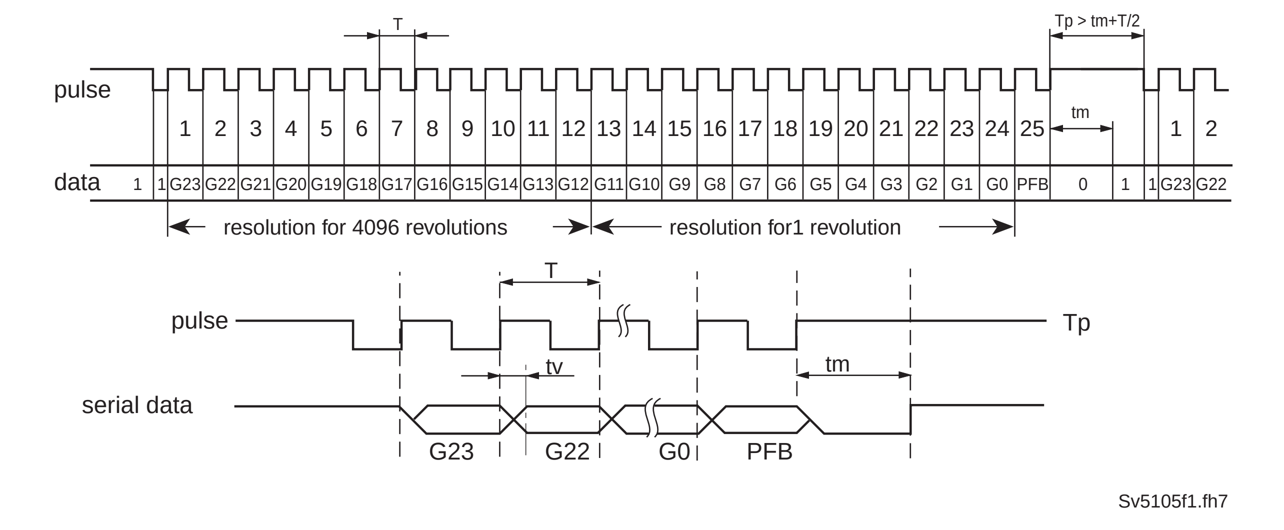


Fig. 19-7: Principle of signal paths illustrated

DANGER

Error in control of motor and moving parts

Bodily harm and property damage due to accidental axis movements.

If breaks in the power source $+U_{ext}$ of less than 10 V occur over periods longer than 100 µs, then encoder information may be inaccurate.

⇒ Active lag-distance monitoring in the control.

Actual position value output in modulo format

probe code:	Gray Code
data scope:	1 table rotation
resolution:	262 144 increments per table rotation
data format:	18 bit
count direction:	switchable
data transmission:	synchronous, serial
input/output circuit:	driver per EIA RS 422 A (see block diagram)

Designation	Unit	min.	type / value	max.
monoflop time tm	µs		15...25	
pulse frequency f_T	MHz	0,1		1
pulse break T_p	µs	40		
duration of pulse signal T	µs	1		10
delay time t_v	ns			540

Fig. 19-8: Actual position value output in modulo format

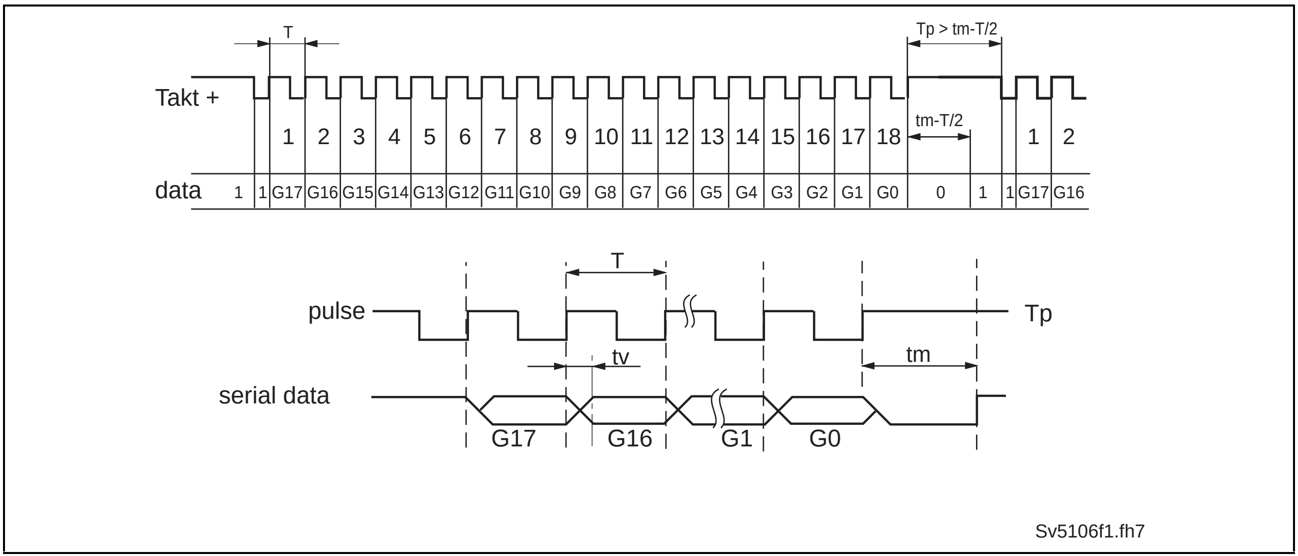


Fig. 19-9: Principle of signal paths illustrated

DANGER

Error in control of motor and moving parts

Bodily harm and property damage due to accidental axis movements.

If breaks in the power source $+U_{ext}$ of less than 10 V occur over periods longer than 100 µs, then encoder information may be inaccurate.

⇒ Active lag-distance monitoring in the control.

Notes

20 SERCOS interface DSS02.1M

20.1 General information

Plugin module "SERCOS interface DSS02.1 M" makes it possible to operate a digital drive with a SERCOS interface compatible control via a fiber optic cable (LWL). It also offers inputs for the evaluation of reference switches, travel range limit switches, probes and an E-STOP input.

20.2 Terminal diagram

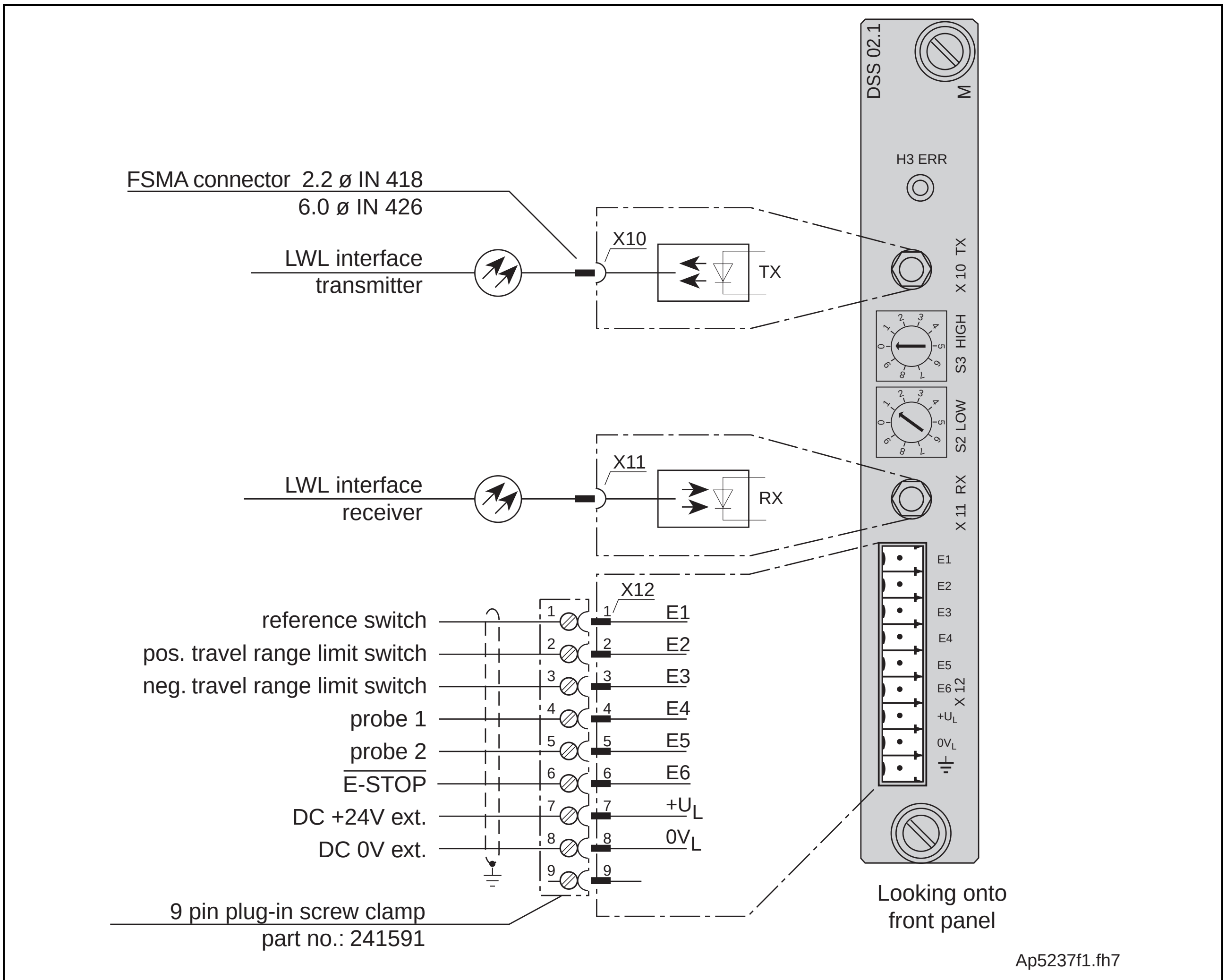


Fig. 20-1: Terminal diagram DSS02.1M

20.3 Technical data DSS02.1M

voltage level DSS02.1M

Designation		Unit	min	type /value	max
ext. power source $+U_L$		V	18	24	32
current consumption U_L		mA			100
inputs	U_{High}	V	16	24	32
E1…E6	U_{Low}	V	0		5,5

Fig. 20-2: Voltage level DSS02.1M

Block diagram of the digital input circuit

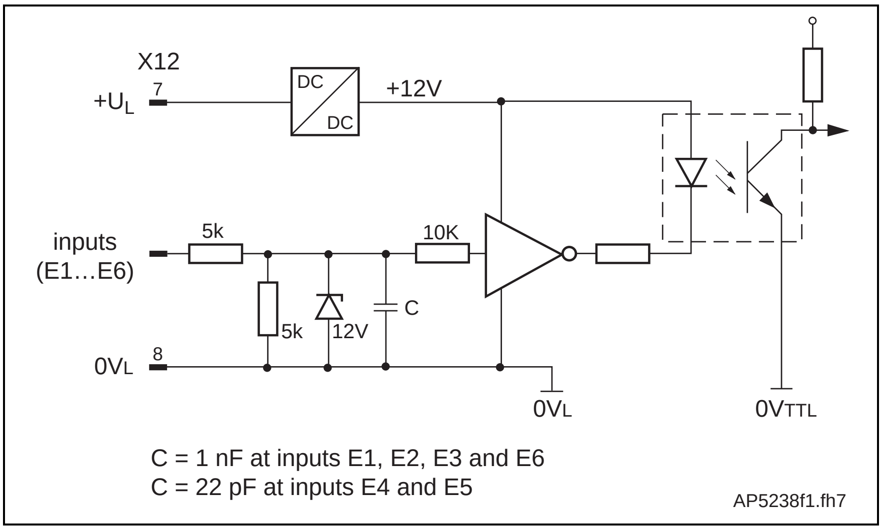


Fig. 20-3: Block diagram of the digital input circuits

	Name	Abbreviation	Unit	min. 1)	max. 1)
Sender data Tx	max. transmission output with opt. low level	P_{SmaxL}	dBm/µW	-31.2/0.75	-28.2/1.5
	min. transmission output with high level	P_{SminH}	dBm/µW	-10.5/90	-7.5/180
	max. transmission output with opt. high level	P_{SmaxH}	dBm/µW	-5.5/280	-3.5/450
	wavelength of the transmitter diode: peak wavelength spectral bandwidth	λp λp	nm nm	640…675 nm (0° C..55° C) - 30 nm (25° C)	
Receiver data Rx	max. input power for opt. low level	P_{EmaxL}	dBm/µW	-31.2/0,75	
	min. input power for opt. high level	P_{EminH}	dBm/µW	-20/10	
	max. input power for opt. high level	P_{EmaxH}	dBm/µW	-5/320	
	max. damping of the transmission distance	$P_{SminH}…P_{EminH}$	dB	9,5	12,5
1) The transmission output can be set via S5.					

Fig. 20-4: Technical data of the LWL interface

Setting transmission output

S5 position		Transmission output with opt. high level	
A	B	in dBm	in µW
OFF	OFF	-7	200
ON	OFF	-4.5	350
OFF	ON	-1	800
ON	ON	0	1000

Fig. 20-5: Setting transmission output

If a -4.5 dBm transmission output is delivered then a opt. high level is set.

Data rate

The data rate can be selected via S4/1 on the PCB.

S4/1 position	Data rate in MBaud
OFF	2
ON	4

Fig. 20-6: Data rate

A data rate of 2 MBaud is set at delivery.

Notes

21 Gearwheel encoder interface DZF02.1M

21.1 General information

Plugin module "Gearwheel encoder interface" support the evaluation of high-resolution main spindle position encoders (type SH2 / MH2) and of the feedback of 2AD / ADF motor with feedback type "3".

21.2 Terminal diagram

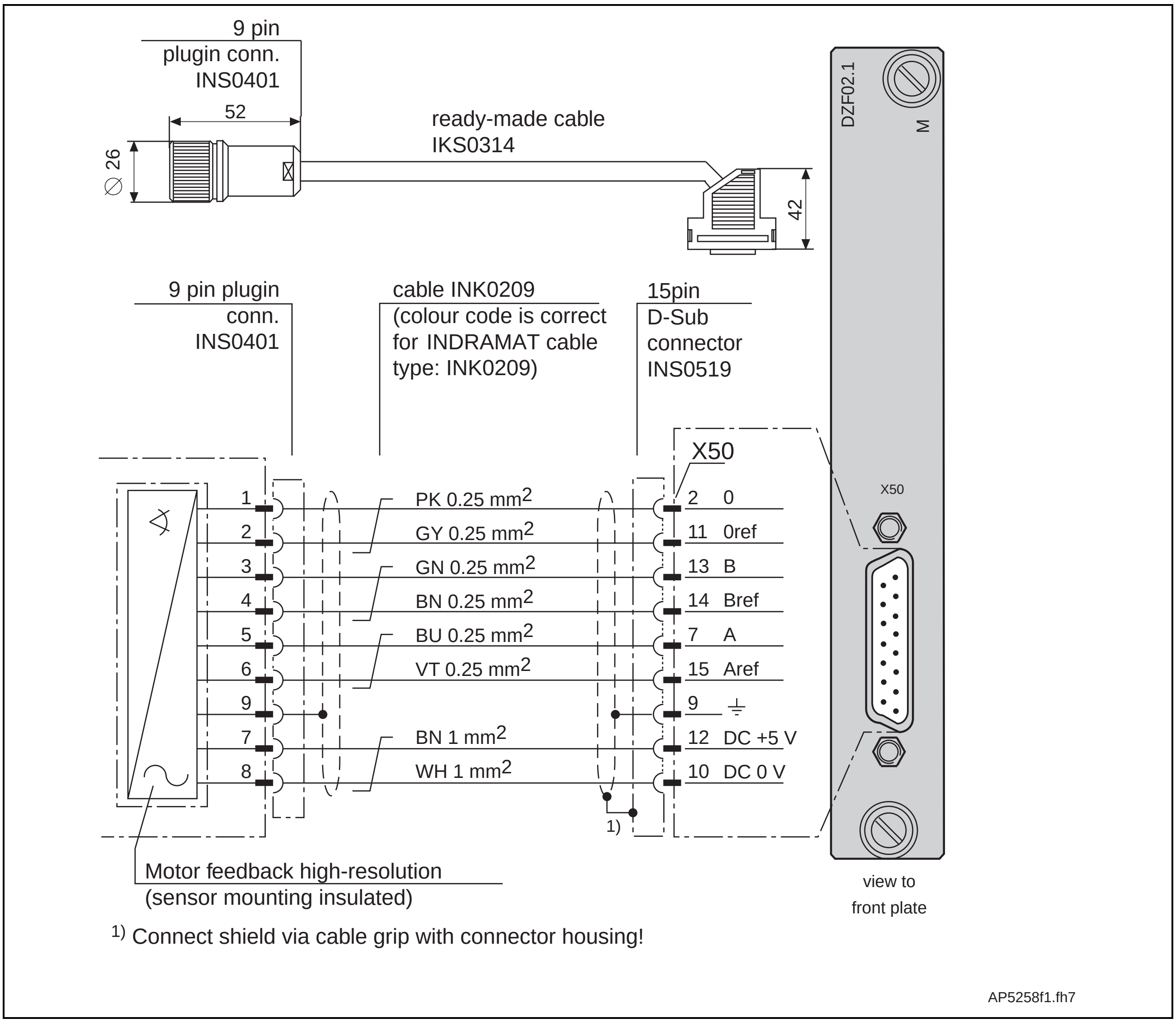


Fig. 21-1: Terminal diagram DZF02.1M

Warning

⇒ **The line to the high-resolution motor feedback may not be conducted via a terminal strip because of its sensitivity to interference!**

21.3 Power source of external measuring systems

Power source of external measuring systems

Designation	Unit	min.	type / value	max.
output voltage +5 V	V	3	5	5.25
output current +5 V	mA			200

Fig. 21-2: Power source of the external measuring system

22 Gearwheel encoder interface DZF03.1M

22.1 General information

Plugin module suports the evaluation of a $1V_{SS}$ - gearwheel encoder.

22.2 Terminal diagram

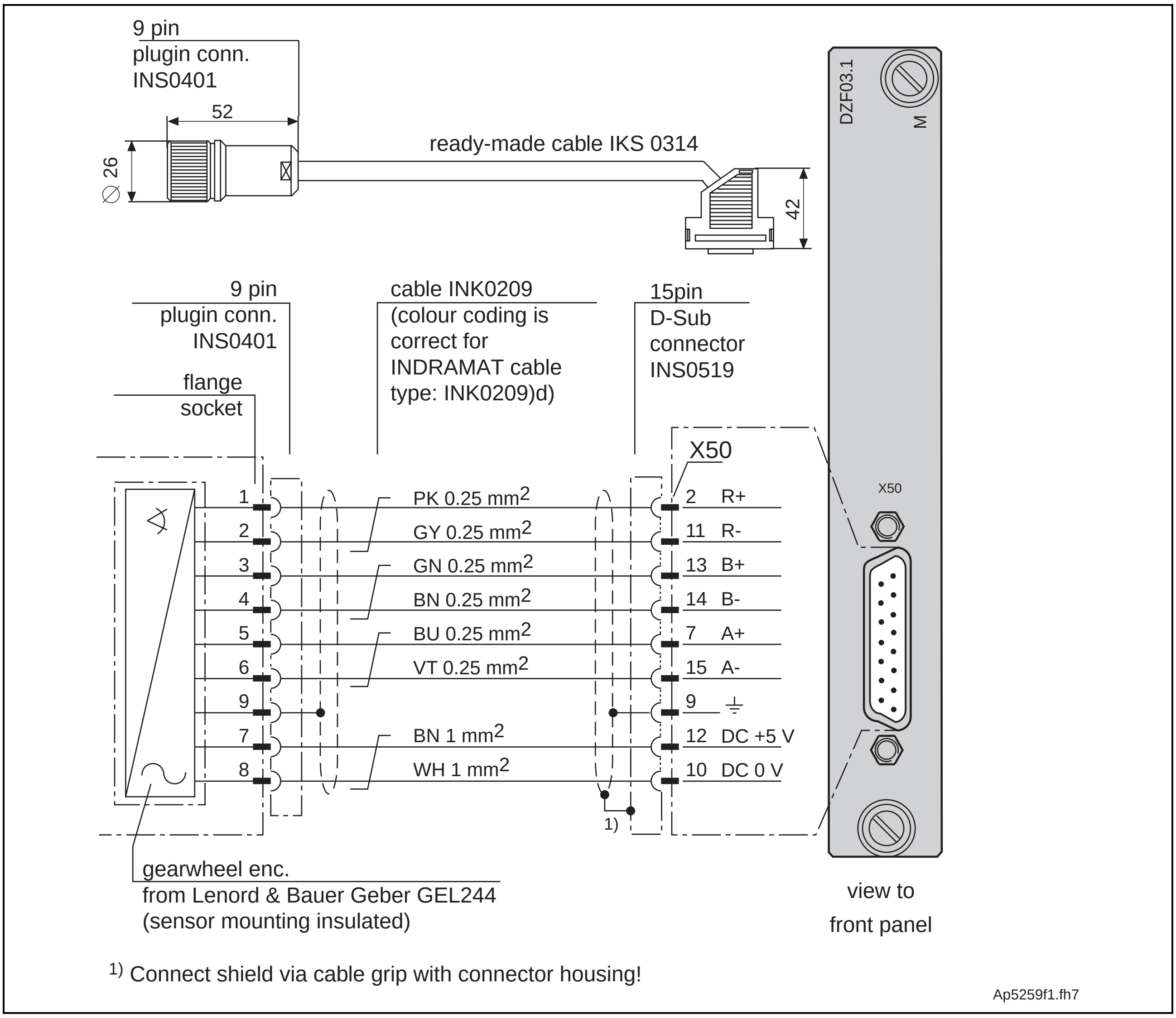


Fig. 22-1: Terminal diagram DZF03.1M

Warning

⇒ **The line to the high-resolution motor feedback may not be conducted via a terminal strip because of its sensitivity to interference!**

22.3 Technical data DZF03.1M

Power source for external measuring system	output voltage X50/12:	DC +5	V (±5%)
	maximum output load X50/12:	250	mA
Signal form	approximate sinusoidal signals		
Resolution	The signal periods from the measuring system have a 2048-fold resolution.		
Voltage signals	signal voltage:	A, B, R	1 V_{SS} (+10/-20%)
	max. signal voltage offset:		0,2 V
	max. frequency for measuring system signals:	A, B	250 kHz
	max. frequency for referencing signals:	R	15 kHz

Signal input circuit

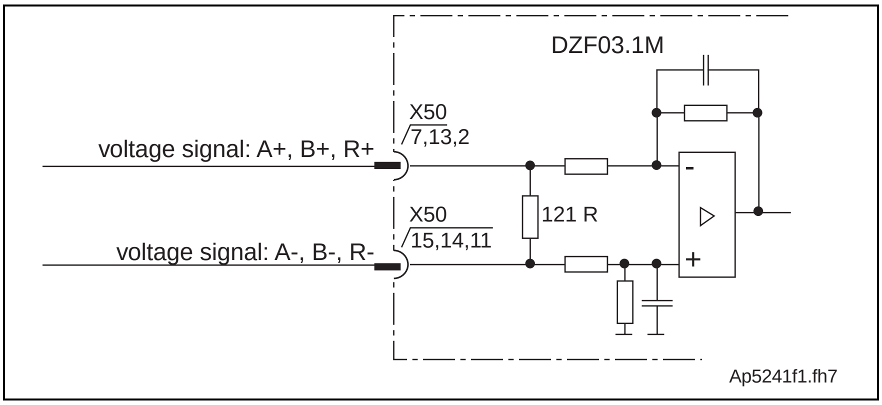


Fig. 22-2: Signal input circuit

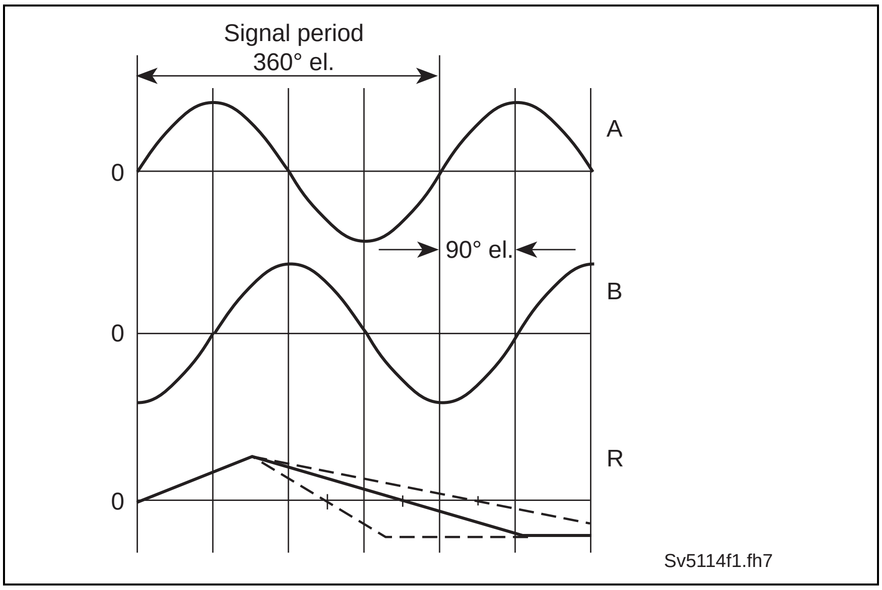


Fig. 22-3: Principle of signal paths illustrated

23 Plugin module accessories

23.1 Encoder branching DGA01.2 for encoders with sinusoidal voltage signals 1 V_{ss}

General information

The DGA makes it possible to distribute the signals of a measuring system to up to four measuring inputs of different drive controllers. DGA applications are:

- Parallel switching of linear motors using a measuring system
- position signals conducted to external controls for monitoring purposes or as a master axis position

All measuring systems can be connected if they have sinusoidal output signals and a signal level of 1 V_{ss} (Heidenhain voltage interface).

The DGA permits the connection of up to four drive controllers. There is also one output with square-wave signals.

Terminal diagram DGA01.2

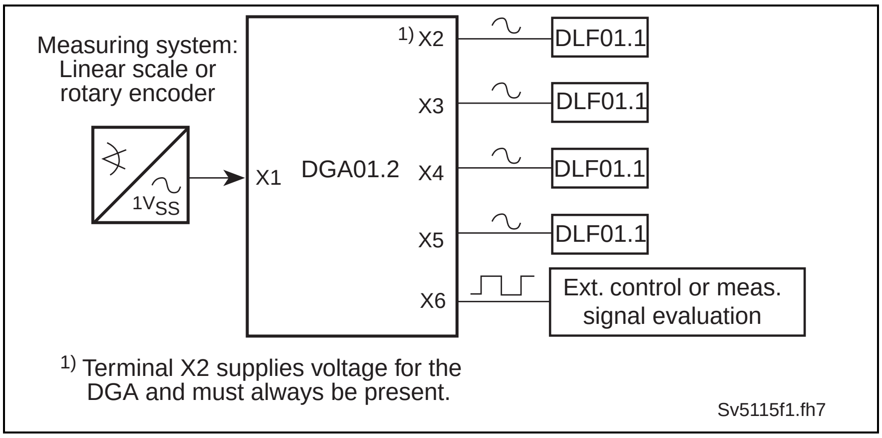


Fig. 23-1: Terminal diagram DGA01.2

Ready-made cables

Connection	Ready-made cable
DGA01.2 (X2, X3, X4, X5) to DLF01.1	IKS0131
DGA01.2 (X6) to DEF01.1	IKS0331

Fig. 23-2: Ready-made cable

Terminal diagram

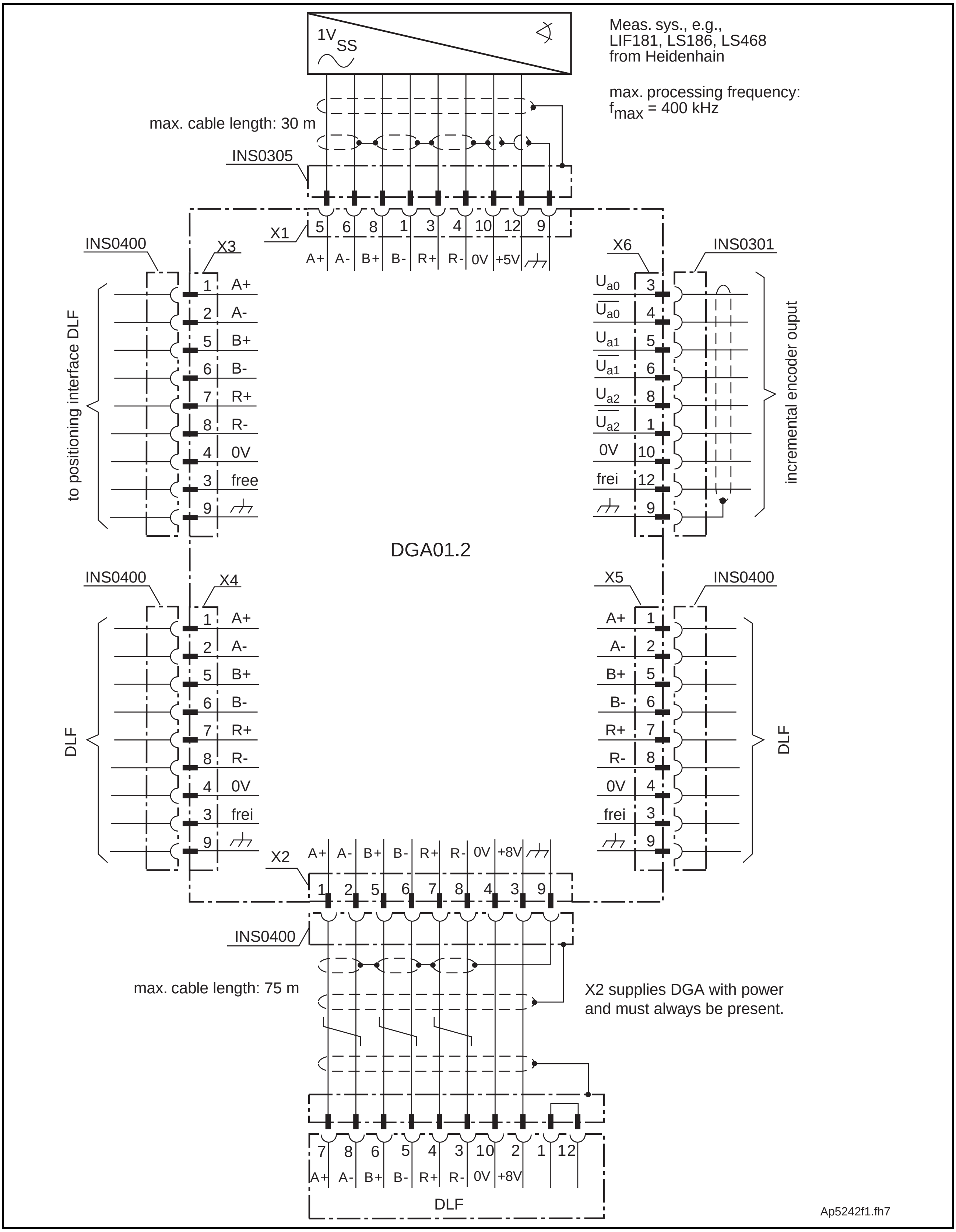


Fig. 23-3: Terminal diagram DGA01.2

Dimensions DGA01.2

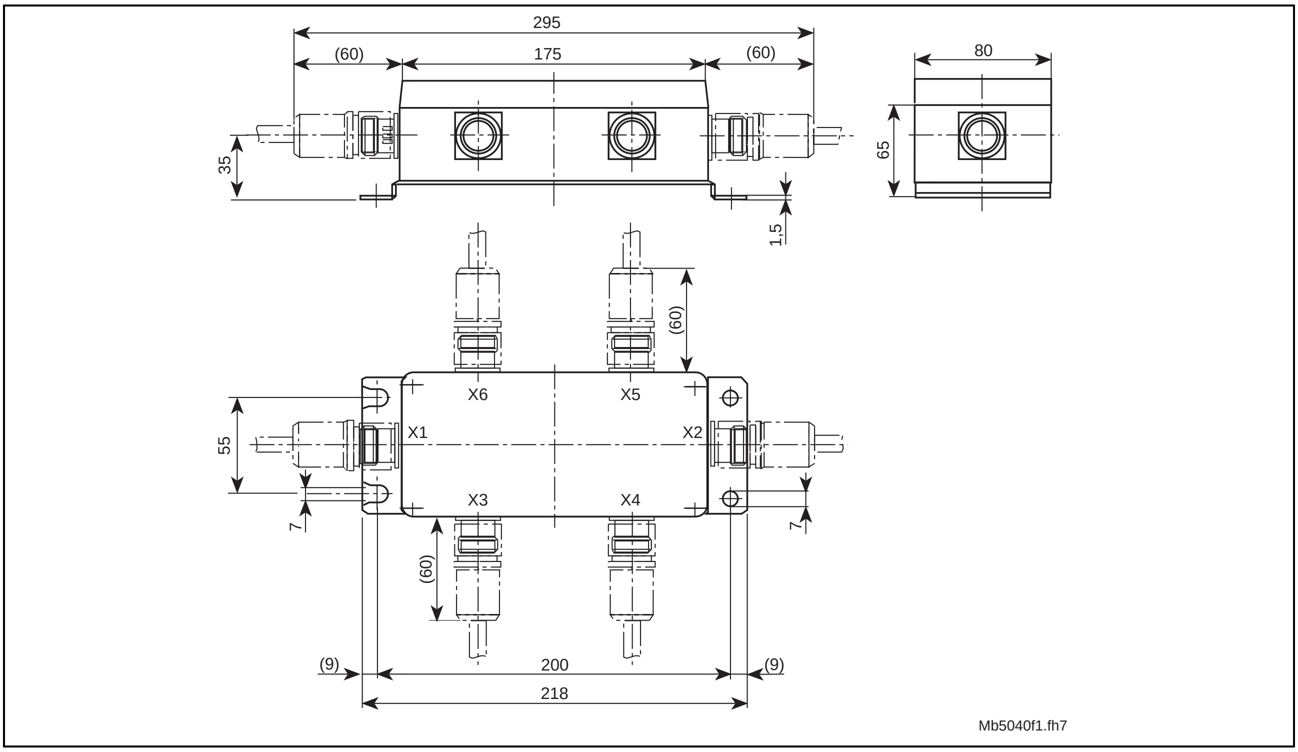


Fig. 23-4: Dimensions DGA01.2

Technical data

External measuring system

Power source for external measuring system
output voltage X1/12: DC +5 V (±5%)
maximum output load X1/12: 150 mA

Signal form
approximate sinusoidal signals

Voltage signals
signal voltage: A, B, R 1 V_{SS}
max. frequency for measuring system signals: A, B 400 kHz
max. frequency for Referenrsignal: R 15 kHz

Signal input circuit

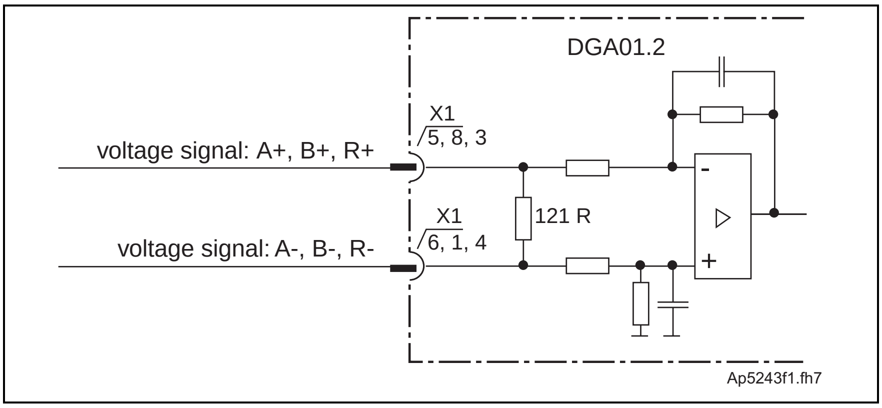


Fig. 23-5: Signal input circuit

Principle of signal paths illustrated

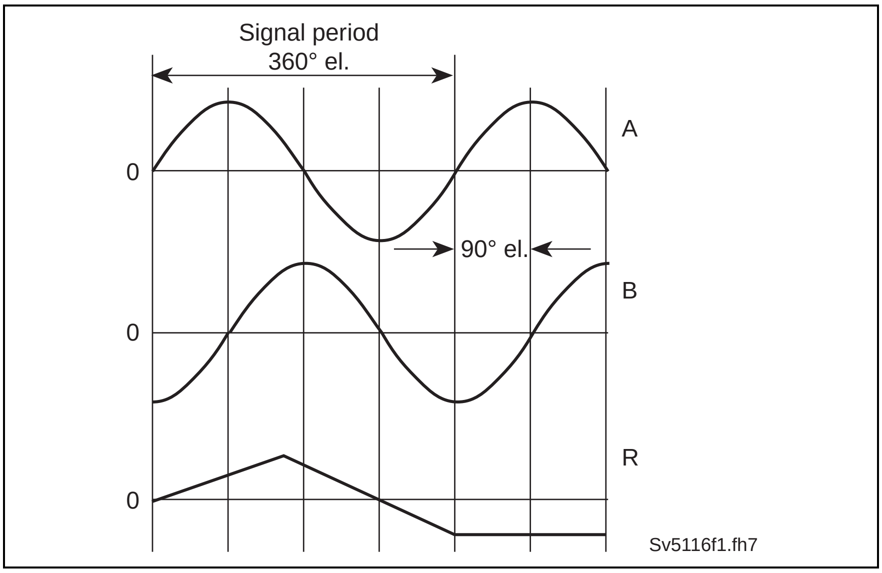


Fig. 23-6: Principle of signal paths illustrated

Branching of the measuring system signals to four connections

The signals from measuring systems are branched to X2, X3, X4 and X5.

Power for the DGA01.2

The DGA01.2 receives its power via X12.

supply voltage X2/3: DC +8 V (±5%)

maximum current consumption: 300 mA

Recommended signal input circuit

see Fig. 23-5

Output of measuring system signals as square-wave signals

Via X6, sinusoidal signals of the measuring system are output as square-wave incremental signals.

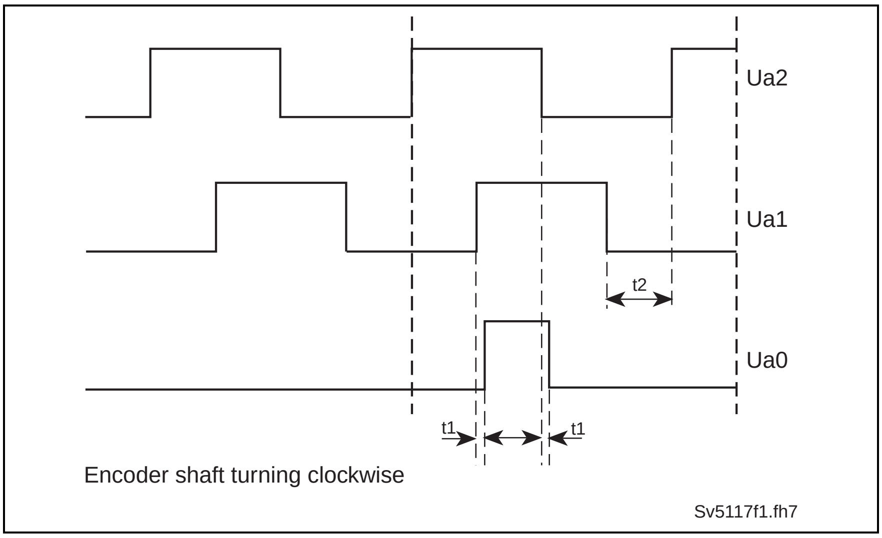


Fig. 23-7: Voltage level and phase position of incremental signals

Designation	Unit	min.	Type / value	max.
phase position Ua1	Grad		0	
phase position Ua2	Grad		90	
Signal amplitude Ua-(/Ua)	V_{SS}		7	
reference point delay t1	ns			50
edge distance t2	ns	500		

Fig. 23-8: Incremental signal data

Output circuit

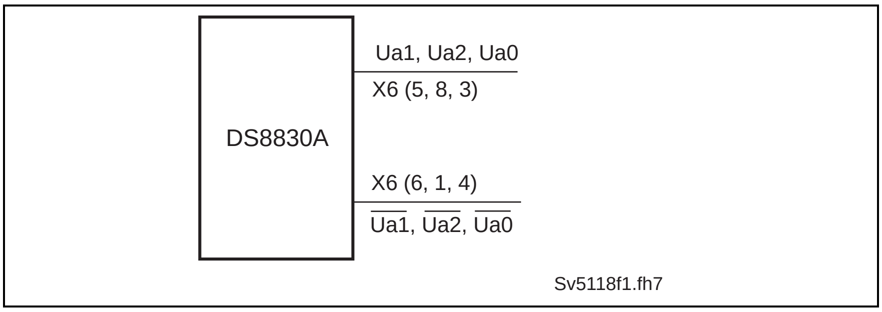


Fig. 23-9: Output circuit

Recommended input circuit

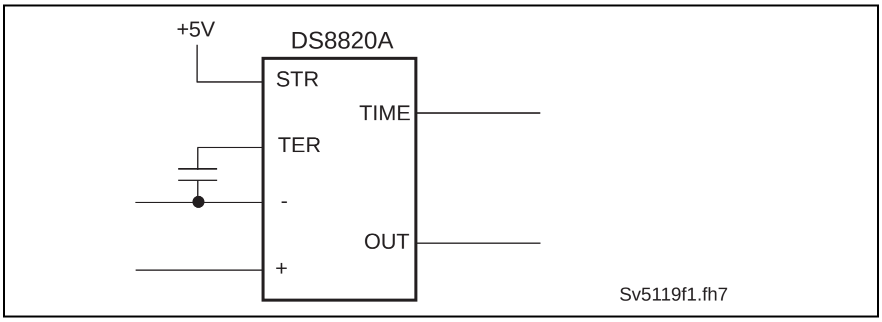
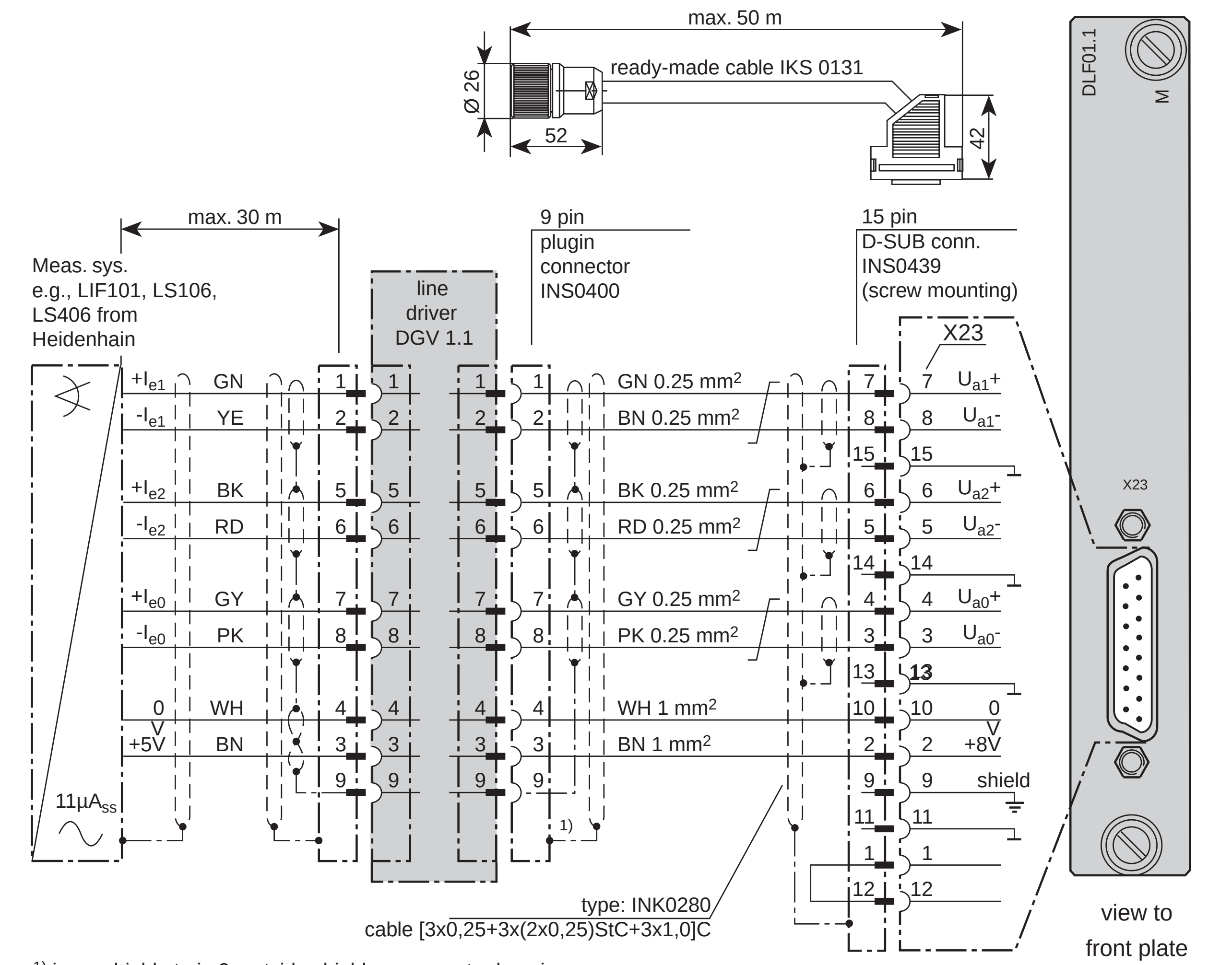


Fig. 23-10: Recommended input circuit

23.2 Line driver DGV01.1 for measuring systems with current signals

Terminal diagram - line driver DGV01.1



1) inner shield at pin 9, outside shield on connector housing

2) The colour code is correct for INDRAMAT cable type: INK0280

Fig. 23-11: Terminal diagram - line driver DGV01.1

Dimensions - line driver DGV01.1

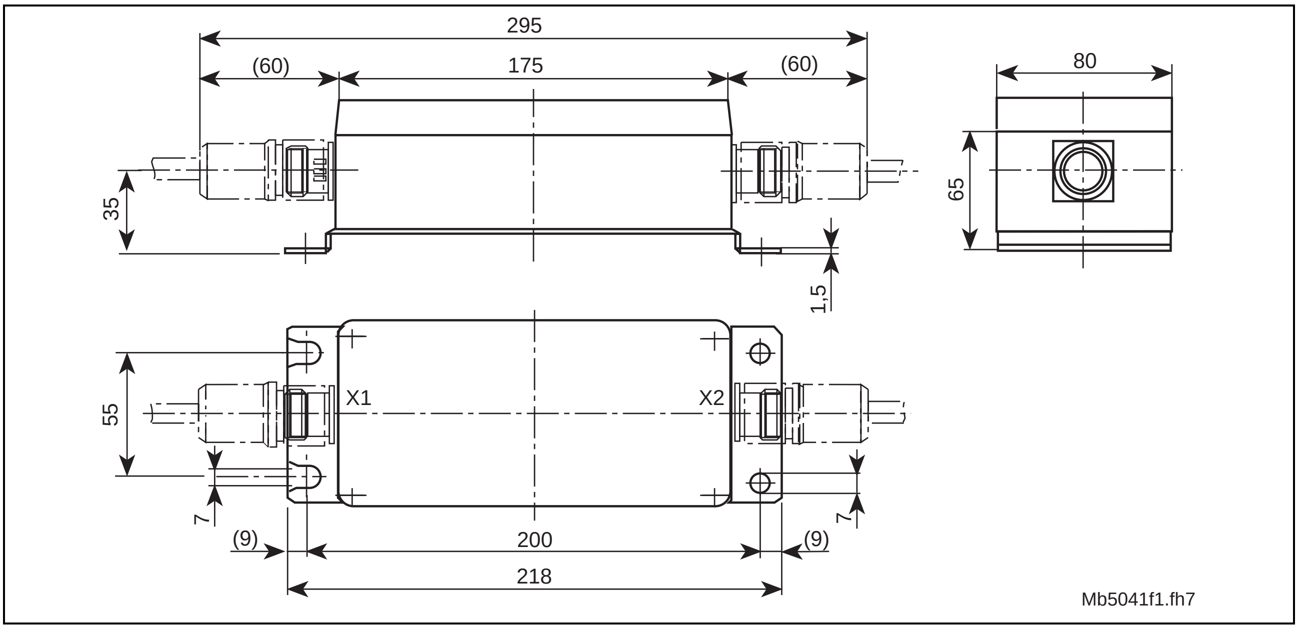


Fig. 23-12: Dimensions - line driver DGV01.1

Notes

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O

P

S

T

Kundenbetreuungsstellen - Sales & Service Facilities

Deutschland – Germany

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