SIEMENS

SIMATIC

High-availability systems S7-400H

System Manual

11/2011
A5E00267695-09

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A5E00267695-09
℗ 12/2011

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Preface 1

1.1 Preface

Purpose of this manual

This manual represents a useful reference and contains information on operator inputs, descriptions of functions, and technical specifications of the S7-400H CPUs.

For information on installing and wiring these and other modules in order to set up an S7-400H system, refer to the *S7-400 Automation System, Installation* manual.

Basic knowledge required

This manual requires general knowledge of automation engineering.

We assume that the reader has sufficient knowledge of computers or equipment similar to a PC, such as programming devices running under the Windows XP or Vista operating system. An S7-400H is configured using the STEP 7 basic software, and you should thus be familiar in the handling of this basic software. This knowledge is provided in the *Programming with STEP 7* manual.

In particular when operating an S7-400H system in potentially explosive atmospheres, you should always observe the information on the safety of electronic control systems provided in the appendix of the *S7-400 Automation System, Installation* manual.

Scope of the manual

The manual is relevant to the following components:

- CPU 412–3H; 6ES7 412–3HJ14–0AB0 firmware version V4.5 or higher
- CPU 414–4H; 6ES7 414–4HM14–0AB0 firmware version V4.5 or higher
- CPU 417–4H; 6ES7 417–4HT14–0AB0 firmware version V4.5 or higher

Installing the STEP 7 hardware update

In addition to STEP 7, you also need a hardware update. You can download the update files directly from STEP 7 via the Internet. Then run the "Options-> Install Hardware Updates" menu command under "STEP 7 -> Configuring Hardware".

Approvals

For details on certifications and standards, refer to the *S7-400 Automation System, Module Data* manual, Section 1.1, Standards and Certifications.

Online help

In addition to the manual, you will find detailed support on how to use the software in the integrated online help system of the software.

The help system can be accessed using various interfaces:

- The **Help** menu contains several commands: **Contents** opens the Help index. You will find help on H systems in **Configuring H-Systems**.
- **Using Help** provides detailed instructions on using the online help system.
- The context-sensitive help system provides information on the current context, for example, on an open dialog box or an active window. You can call this help by clicking "Help" or using the F1 key.
- The status bar provides a further form of context-sensitive help. It shows a short description of each menu command when you position the mouse pointer over a command.
- A short info text is also shown for the toolbar buttons when you hold the mouse pointer briefly over a button.

If you prefer to read the information of the online help in printed form, you can print individual topics, books or the entire help system.

Recycling and disposal

The S7-400H system contains environmentally compatible materials and can be recycled. For ecologically compatible recycling and disposal of your old device, contact a certificated disposal service for electronic scrap.

Additional support

If you have any questions relating to the products described in this manual, and do not find the answers in this documentation, please contact your Siemens partner at our local offices.

You will find information on who to contact at:

Contact partners (http://www.siemens.com/automation/partner)

A guide to the technical documents for the various SIMATIC products and systems is available at:

Documentation (http://www.automation.siemens.com/simatic/portal/html_76/techdoku.htm)

You can find the online catalog and order system under:

Catalog (http://mall.automation.siemens.com/)

H/F Competence Center

The H/F Competence Center in Nuremberg offers a special workshop on the topic of fault-tolerant SIMATIC S7 automation systems. The H/F Competence Center also offers configuration and commissioning support, and help in finding solutions for problems in your plant.
E-mail: hf-cc.aud@siemens.com

Training center

We offer a range of relevant courses to help you to get started with the SIMATIC S7 automation system. Please contact your local training center or the central training center.

Training (http://www.sitrain.com/index_en.html)

A&D Technical Support

For technical support of all Industry Automation products, fill in and submit the online Support Request:

Support Request (http://www.siemens.de/automation/support-request)

Additional information about our technical support is available on the Internet at:

Technical Support (http://support.automation.siemens.com)

Service & Support on the Internet

In addition to our documentation, we offer a comprehensive online knowledge base on the Internet at:

Service & Support (http://www.siemens.com/automation/service&support)

There you will find:

- The newsletter containing the latest information on your products.
- The latest documents via our search function in Service & Support.
- A forum for global information exchange by users and specialists.
- Your local Automation representative.
- Information on field service, repairs and spare parts. Much more can be found under "Services".

Fault-tolerant automation systems 2

2.1 Redundant SIMATIC automation systems

Operating objectives of redundant automation systems

Redundant automation systems are used in practice with the aim of achieving a higher degree of availability or fault tolerance.

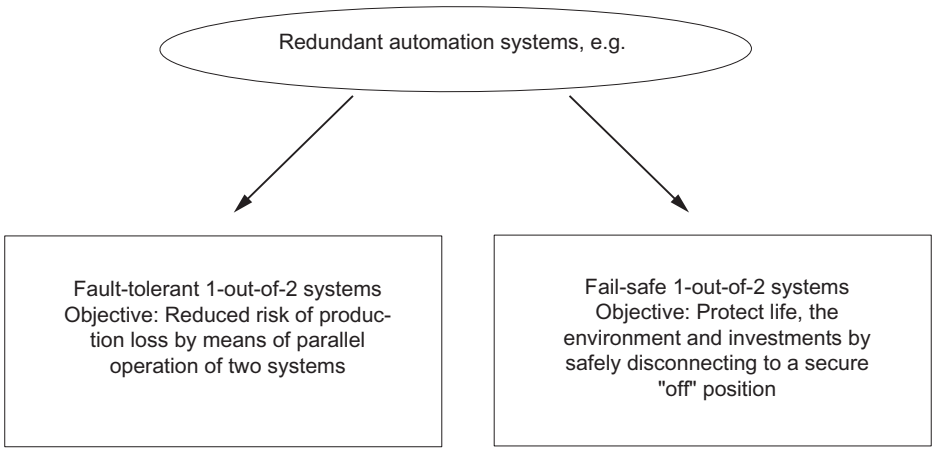


Figure 2-1 Operating objectives of redundant automation systems

Note the difference between fault-tolerant and fail-safe systems.
The S7–400H is a fault-tolerant automation system. You may only use it to control safety-related processes if you have programmed and configured it in accordance with the rules for F systems. You can find details in the following manual: SIMATIC Industrial Software S7 F/FH Systems (http://support.automation.siemens.com/WW/view/en/2201072)

Why fault-tolerant automation systems?

The purpose of using fault-tolerant automation systems is to reduce production downtimes, regardless of whether the failures are caused by an error/fault or are due to maintenance work.

The higher the costs of production stops, the greater the need to use a fault-tolerant system. The generally higher investment costs of fault-tolerant systems are soon recovered since production stops are avoided.

Software redundancy

For many applications, the requirements for redundancy quality or the extent of plant sections that may require redundant automation systems do not necessarily justify the implementation of a special fault-tolerant system. Frequently, simple software mechanisms are adequate to allow a failed control task to be continued on a substitute system if a problem occurs.

The optional "SIMATIC S7 Software Redundancy" software package can be implemented on S7-300 and S7-400 standard systems to control processes that tolerate switchover delays to a substitute system in the seconds range, e.g. in water works, water treatment plants, or traffic flows.

Redundant I/O

Input/output modules are termed redundant when they exist twice and they are configured and operated as redundant pairs. The use of redundant I/O provides the highest degree of availability, because the system tolerates the failure of a CPU or of a signal module. If you require a redundant I/O, you use the blocks of the "Functional I/O Redundancy" function block library, see section Connecting redundant I/O (Page 132).

2.2 Increasing the availability of plants

The S7-400H automation system satisfies the high demands on availability, intelligence, and decentralization placed on modern automation systems. It also provides all functions required for the acquisition and preparation of process data, including functions for the open-loop control, closed-loop control, and monitoring of assemblies and plants.

System-wide integration

The S7-400H automation system and all other SIMATIC components such as the SIMATIC PCS7 control system are matched to one another. The system-wide integration, ranging from the control room to the sensors and actuators, is implemented as a matter of course and ensures maximum system performance.

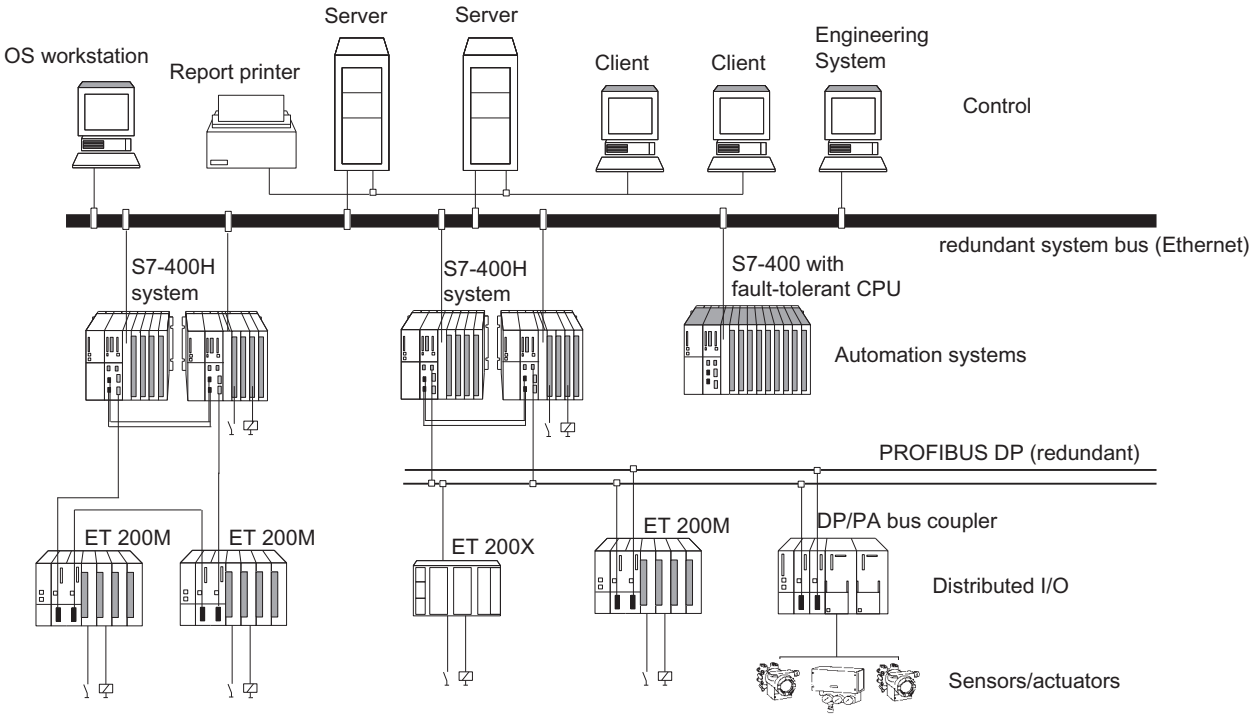


Figure 2-2 Integrated automation solutions with SIMATIC

Graduated availability by duplicating components

The redundant structure of the S7-400H ensures requirements to reliability at all times. This means: all essential components are duplicated.

This redundant structure includes the CPU, the power supply, and the hardware for linking the two CPUs.

You yourself decide on any other components you want to duplicate to increase availability depending on the specific process you are automating.

Redundancy nodes

Redundant nodes represent the fail safety of systems with redundant components. A redundant node can be considered as independent when the failure of a component within the node does not result in reliability constraints in other nodes or in the overall system.

The availability of the overall system can be illustrated simply in a block diagram. With a 1-out-of-2 system, **one** component of the redundant node may fail without impairing the operability of the overall system. The weakest link in the chain of redundant nodes determines the availability of the overall system

No error/fault

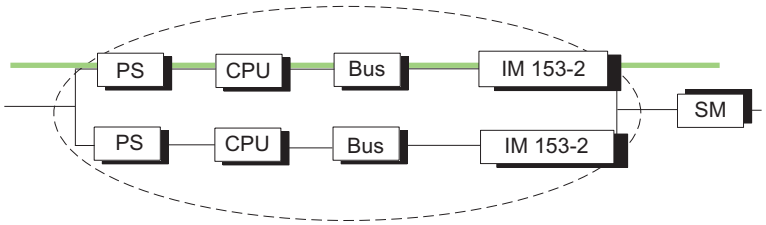


Figure 2-3 Example of redundancy in a network without error

With error/fault

The following figure shows how a component may fail without impairing the functionality of the overall system.

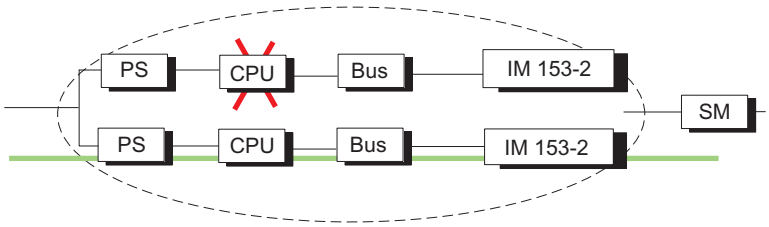


Figure 2-4 Example of redundancy in a 1-out-of-2 system with error

Failure of a redundancy node (total failure)

The following figure shows that the overall system is no longer operable, because both subunits have failed in a 1-out-of-2 redundancy node (total failure).

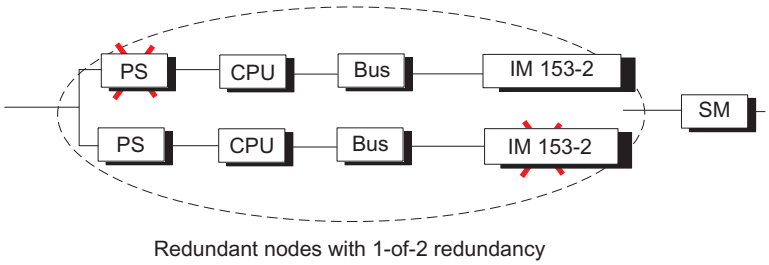


Figure 2-5 Example of redundancy in a 1-out-of-2 system with total failure

S7-400H setup options

3

3.1 S7-400H setup options

The first part of the description deals with the basic setup of the fault-tolerant S7-400H automation system, and with the components of an S7-400H basic system. We then describe the hardware components with which you can expand this basic system.

The second part deals with the software tools required for configuring and programming the S7-400H. Also included is a description of the extensions and functional expansions available for the S7-400 standard system which you need to create your user program to utilize all properties of your S7-400H in order to increase availability.

Important information on configuration

⚠ WARNING
Open equipment S7–400 modules are classified as open equipment, meaning you must install the S7-400 in an enclosure, cabinet, or switch room which can only be accessed by means of a key or tool. Such enclosures, cabinets, or switch rooms may only be accessed by instructed or authorized personnel.

The following figure shows an example of an S7-400H configuration with shared distributed I/O and connection to a redundant plant bus. The next pages deal with the hardware and software components required for the installation and operation of the S7-400H.

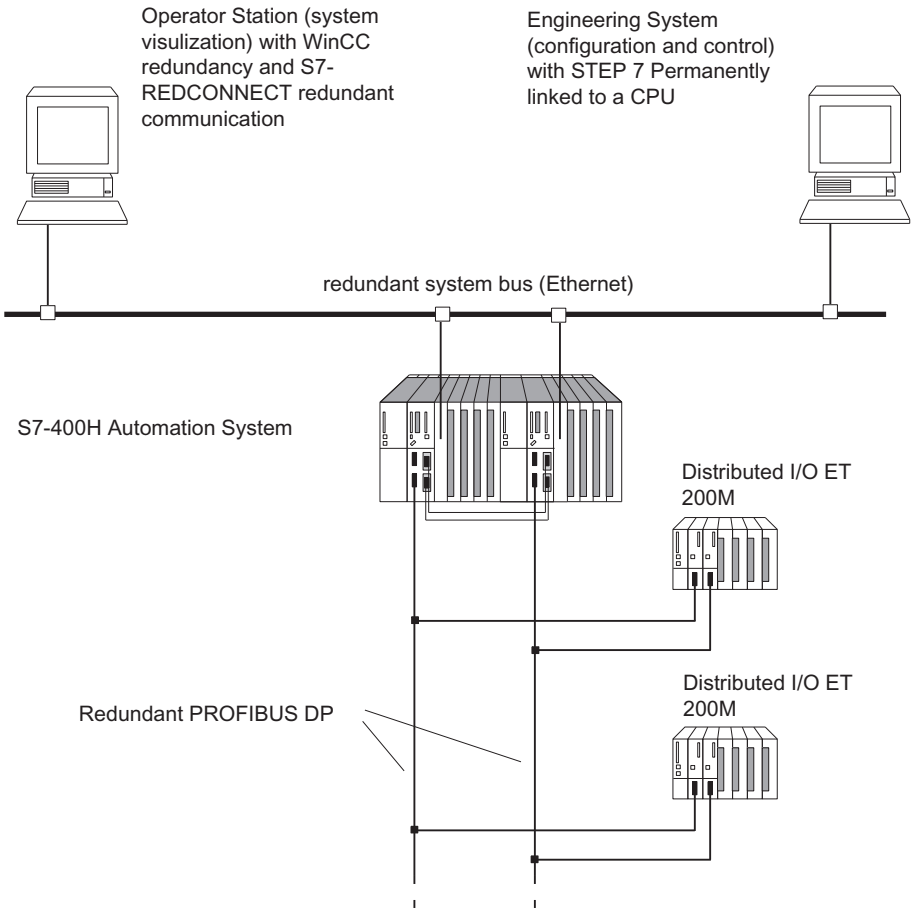


Figure 3-1 Overview

Additional information

The components of the S7-400 standard system are also used in the fault-tolerant S7–400H automation system. For a detailed description of all hardware components for S7–400, refer to the Reference Manual *S7-400 Automation System; Module Specifications*.

The rules governing the design of the user program and the use of function blocks laid down for the S7-400 standard system also apply to the fault-tolerant S7-400H automation system. Refer to the descriptions in the *Programming with STEP 7* manual, and to the *System Software for S7-300/400; Standard and System Functions* Reference Manual.

3.2 Rules for the assembly of fault-tolerant stations

The following rules have to be complied with for a fault-tolerant station, in addition to the rules that generally apply to the arrangement of modules in the S7-400:

- The CPUs have to be inserted in the same slots.
- Redundantly used external DP master interfaces or communication modules must be inserted in the same slots in each case.
- External DP master interfaces for redundant DP master systems must only be inserted in central devices rather than in expansion devices.
- Redundantly used modules (e.g. CPU 41x-4H, DP slave interface module IM 153-2) must be identical, i.e. they must have the same order number, the same version or firmware version.

3.3 The S7–400H basic system

Hardware of the basic system

The basic system consists of the hardware components required for a fault-tolerant controller. The following figure shows the components in the configuration.

The basic system can be expanded with S7–400 standard modules. Restrictions only apply to the function and communication modules; see Appendix Function modules and communication processors supported by the S7-400H (Page 355).

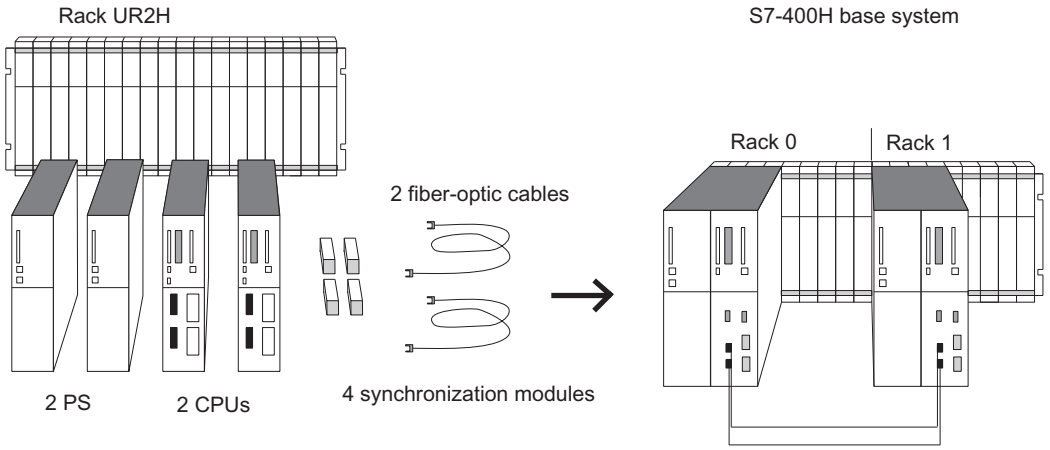


Figure 3-2 Hardware of the S7–400H basic system

Central processing units

The two CPUs are the heart of the S7-400H. Use the switch **on the rear** of the CPU to set the rack numbers. In the following sections, we will refer to the CPU in rack 0 as CPU 0, and to the CPU in rack 1 as CPU 1.

Rack for S7–400H

The UR2-H rack supports the installation of two separate subsystems with nine slots each, and is suitable for installation in 19" cabinets.

You can also set up the S7-400H in two separate racks. The racks UR1 and UR2 are available for this purpose.

Power supply

You require one power supply module from the standard range of the S7-400 for each H-CPU, or to be more precise, for each of the two subsystems of the S7-400H.

To increase availability of the power supply, you can also use two redundant power supplies in each subsystem. Use the power supply modules PS 405 R / PS 407 R for this purpose.

They can also be used together in redundant configurations (PS 405 R with PS 407 R).

Synchronization modules

The synchronization modules are used to link the two CPUs. They are installed in the CPUs and interconnected by means of fiber-optic cables.

There are two types of synchronization modules: one for distances up to 10 meters, and one for distances up to 10 km between the CPUs.

A fault-tolerant system requires 4 synchronization modules of the same type. For more information on synchronization modules, refer to section Synchronization modules for S7–400H (Page 267).

Fiber-optic cable

The fiber-optic cables are used to interconnect the synchronization modules for the redundant link between the two CPUs. They interconnect the upper and lower synchronization modules in pairs.

You will find the specifications of fiber-optic cables suitable for use in an S7-400H in section Selecting fiber-optic cables (Page 272).

3.4 I/O modules for S7–400H

I/O modules of the SIMATIC S7 series can be used for the S7-400H. The I/O modules can be used in the following devices:

- Central devices
- Expansion devices
- Distributed via PROFIBUS DP.

You will find the function modules (FMs) and communications modules (CPs) suitable for use in the S7-400H in Appendix Function modules and communication processors supported by the S7-400H (Page 355).

I/O design versions

The following I/O module design versions are available:

- Single-channel, one-sided configuration with standard availability

  With the single-channel, one-sided design, single input/output modules are available. The I/O modules are located in only one subsystem, and are only addressed by this subsystem.

  However, in redundant mode, both CPUs are interconnected via the redundant link and thus execute the user program identically.

- Single-channel, switched configuration with enhanced availability

  Switched single-channel distributed configurations contain only single I/O modules, but they can be addressed by both subsystems.

- Redundant dual-channel configuration with maximum availability

  A redundant dual-channel configuration contains two sets of the I/O modules which can be addressed by both subsystems.

Additional information

For detailed information on using the I/O, refer to section Using I/Os in S7–400H (Page 123).

3.5 Communication

The S7-400H supports the following communication methods and mechanisms:

- Plant buses with Industrial Ethernet
- Point-to-point connection

This equally applies to the central and distributed components. Communication modules that can be used are listed in Appendix Function modules and communication processors supported by the S7-400H (Page 355).

Communication availability

You can vary the availability of communication with the S7-400H. The S7-400H supports various solutions to meet your communication requirements. These range from a simple linear network structure to a redundant optical two-fiber loop.

Fault-tolerant communication via PROFIBUS or Industrial Ethernet is supported only by the S7 communication functions.

Programming and configuring

Apart from the use of additional hardware components, there are basically no differences with regard to configuration and programming compared to standard systems. Fault-tolerant connections only have to be configured; specific programming is not necessary.

All communication functions required for fault-tolerant communication are integrated in the operating system of the fault-tolerant CPU. These functions run automatically in the background, for example, to monitor the communication connection, or to automatically change over to a redundant connection in the event of error.

Additional information

For detailed information on communication with the S7-400H, refer to section Communication (Page 167).

3.6 Tools for configuration and programming

Like the S7-400, the S7-400H is also configured and programmed using STEP 7.

You only need to make allowances for slight restrictions when you write the user program. However, there are some additional details specific to the fault-tolerant configuration. The operating system automatically monitors the redundant components and switches over to the standby components when an error occurs. You have already configured the relevant information and communicated it to the system in your STEP 7 program.

Detailed information can be found in the online help, section Configuring with STEP 7 (Page 191), and Appendix Differences between fault-tolerant systems and standard systems (Page 351).

Optional software

All standard tools, engineering tools and runtime software used in the S7-400 system are also supported by the S7-400H system.

3.7 The user program

The rules of developing and programming the user program for the standard S7-400 system also apply to the S7-400H.

In terms of user program execution, the S7-400H behaves in exactly the same manner as a standard system. The integral synchronization functions of the operating system are executed automatically in the background. You do not need to consider these functions in your user program.

In redundant operation, the user programs are stored identically on both CPUs and are executed in event-synchronous mode.

However, we offer you several specific blocks for optimizing your user program, e.g. in order to improve its response to the extension of cycle times due to updates.

Specific blocks for S7–400H

In addition to the blocks supported both in the S7-400 and S7-400H systems, the S7-400H software provides further blocks which you can use to influence the redundancy functions.

You can react to redundancy errors of the S7-400H using the following organization blocks:

- OB 70, I/O redundancy errors
- OB 72, CPU redundancy errors

SFC 90 "H_CTRL" can be used to influence fault-tolerant systems as follows:

- You can disable interfacing in the master CPU.
- You can disable updating in the master CPU.
- You can remove, resume or immediately start a test component of the cyclic self-test.

NOTICE
Required OBs Always download these error OBs to the S7-400H CPU: OB 70, OB 72, OB 80, OB 82, OB 83, OB 85, OB 86, OB 87, OB 88, OB 121 and OB 122. If you do not download these OBs, the fault-tolerant system goes into STOP when an error occurs.

Additional information

For detailed information on programming the blocks listed above, refer to the *Programming with STEP 7* manual, and to the *System Software for S7-300/400; System and Standard Functions* Reference Manual.

3.8 Documentation

The figure below provides an overview of the descriptions of the various components and options in the S7-400H automation system.

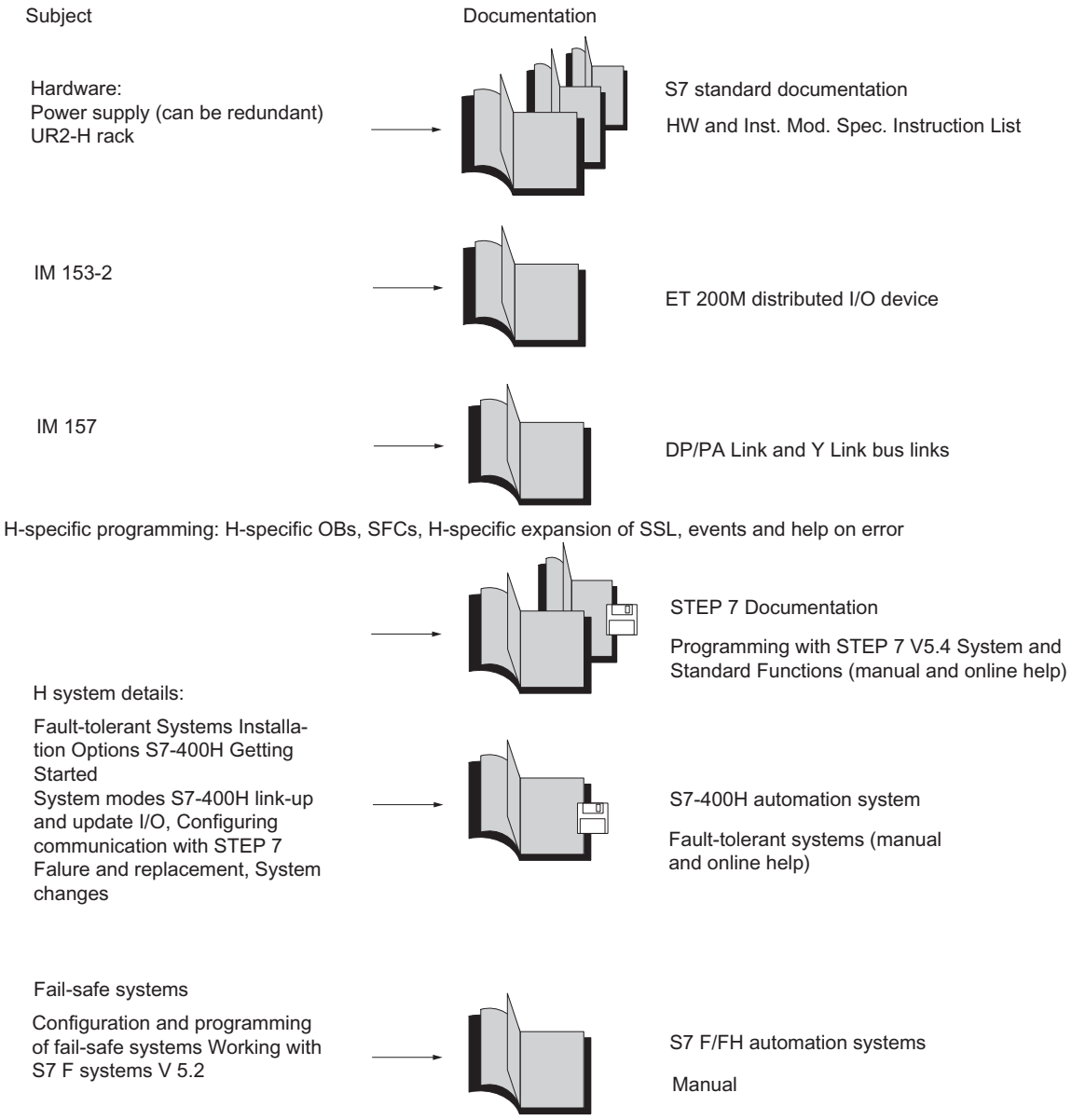


Figure 3-3 User documentation for fault-tolerant systems

Getting Started

4

4.1 Getting Started

Based on a specific example, these instructions guide you through the steps to implement commission all the way to a functional application. You will learn how an S7-400H automation system operates and become familiar with its response to a fault.

It takes about 1 to 2 hours to work through this example, depending on your previous experience.

4.2 Requirements

The following requirements must be met:

A correctly installed and valid version of the STEP 7 basic software on your programming device; see section Configuring with STEP 7 (Page 191). Any necessary hardware updates are installed.

The modules required for the hardware setup available:

- An S7-400H automation system consisting of:
  - 1 UR2–H rack
  - 2 PS 407 10 A power supply units
  - 2 H–CPUs
  - 4 synchronization modules
  - 2 fiber-optic cables
- An ET 200M distributed I/O device with active backplane bus with
  - 2 IM 153–2
  - 1 digital input module, SM321 DI 16 x DC24V
  - 1 digital output module, SM322 DO 16 x DC24V
- All necessary accessories such as PROFIBUS cables, etc.

4.3 Hardware assembly and commissioning of the S7–400H

Assembly of the hardware

Follow the steps below to assemble the S7-400H as shown in the following figure:

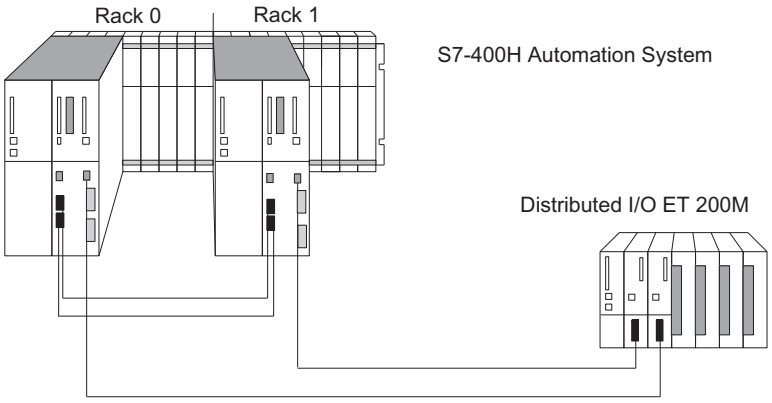


Figure 4-1 Hardware assembly

1. Assemble both modules of the S7-400H automation system as described in the *S7-400 Automation Systems, Installation* and *Module Specifications* manuals.
2. Set the rack numbers using the switch on the rear of the CPUs.

   An incorrectly set rack number prevents online access and the CPU might not start up.
3. Install the synchronization modules in the CPUs as described in the *S7-400 Automation System, Installation* manual.
4. Connect the fiber-optic cables.

   Always interconnect the two upper and the two lower synchronization modules of the CPUs. Route your fiber-optic cables so that they are reliably protected against any damage.

   You should also always make sure that the two fiber-optic cables are routed separately. This increases availability and protects the fiber-optic cables from potential double errors caused, for example, by interrupting both cables at the same time.

   Furthermore, always connect the fiber-optic cables to both CPUs before you switch on the power supply or the system. Otherwise both CPUs may execute the user program as master CPU.
5. Configure the distributed I/O as described in the *ET 200M Distributed I/O Device* manual.
6. Connect the programming device to the first fault-tolerant CPU (CPU0). This CPU will be the master of your S7-400H.
7. A high-quality RAM test is executed after POWER ON. This takes about 10 minutes. The CPU cannot be accessed and the STOP LED flashes for the duration of this test. If you use a backup battery, this test is no longer performed when you power up in future.

Commissioning the S7–400H

Follow the steps outlined below to commission the S7–400H:

1. In SIMATIC Manager, open the sample project "HProject". The configuration corresponds to the hardware configuration described in "Requirements".
2. Open the hardware configuration of the project by selecting the "Hardware" object, then by right-clicking and selecting the shortcut menu command "Object -> Open". If your configuration matches, continue with step 6.
3. If your hardware configuration does not match the project, e.g. there are different module types, MPI addresses or DP addresses, edit and save the project accordingly. For additional information, refer to the basic help of SIMATIC Manager.
4. Open the user program in the "S7 program" folder.

   In the offline view, this "S7 program" folder is only assigned to CPU0. The user program is executable with the described hardware configuration. It activates the LEDs on the digital output module (running light).
5. Edit the user program as necessary to adapt it to your hardware configuration, and then save it.
6. Select "PLC -> Download" to download the user program to CPU0.
7. Start up the S7-400H automation system by setting the mode selector switch of CPU0 to RUN and then the switch on CPU1. The CPU performs a restart and calls OB 100.

   Result: CPU0 starts up as the master CPU and CPU1 as the reserve CPU. After the reserve CPU is linked and updated, the S7-400H assumes redundant mode and executes the user program. It activates the LEDs on the digital output module (running light).

Note

You can also start and stop the S7-400H automation system using STEP 7.

For additional information, refer to the online help.

You can only initiate a cold restart using the programming device command "Cold restart". For this purpose, the CPU must be in STOP mode and the mode selector switch must be set to RUN. OB 102 is called in the cold restart routine.

4.4 Examples of the response of the fault-tolerant system to faults

Example 1: Failure of a CPU or power supply module

Initial situation: The S7-400H is in redundant system mode.

1. Simulate a CPU0 failure by turning off the power supply.

   Result: The LEDs REDF, IFM1F and IFM2F light up on CPU1. CPU1 goes into single mode and continues to process the user program.

2. Turn the power supply back on.

   Result:

   – CPU0 performs an automatic CONNECT and UPDATE.

   – CPU0 changes to RUN, and now operates as reserve CPU.

   – The S7-400H is now in redundant system mode.

Example 2: Failure of a fiber-optic cable

Initial situation: The S7-400H is in redundant system mode. The mode selector switch of each CPU is set to RUN.

1. Disconnect one of the fiber-optic cables.

   Result: The LEDs REDF and IFM1F or IFM2F (depending on which fiber-optic cable was disconnected) now light up on both CPUs. The reserve CPU changes to TROUBLESHOOTING mode. The other CPU remains master and continues operation in single mode.

2. Now, reconnect the withdrawn fiber-optic cable, provided that the CPU is still in TROUBLESHOOTING mode.

   Result: The reserve CPU performs starts a CONNECT and UPDATE. The S7–400H resumes redundant system mode.

   If you reconnect the withdrawn fiber-optic cable after the CPU has left TROUBLESHOOTING mode, you will need to manually start CONNECT and UPDATE.

Assembly of a CPU 41x–H

5

5.1 Operator controls and display elements of the CPUs

Operator controls and display elements on the CPU 412-3H

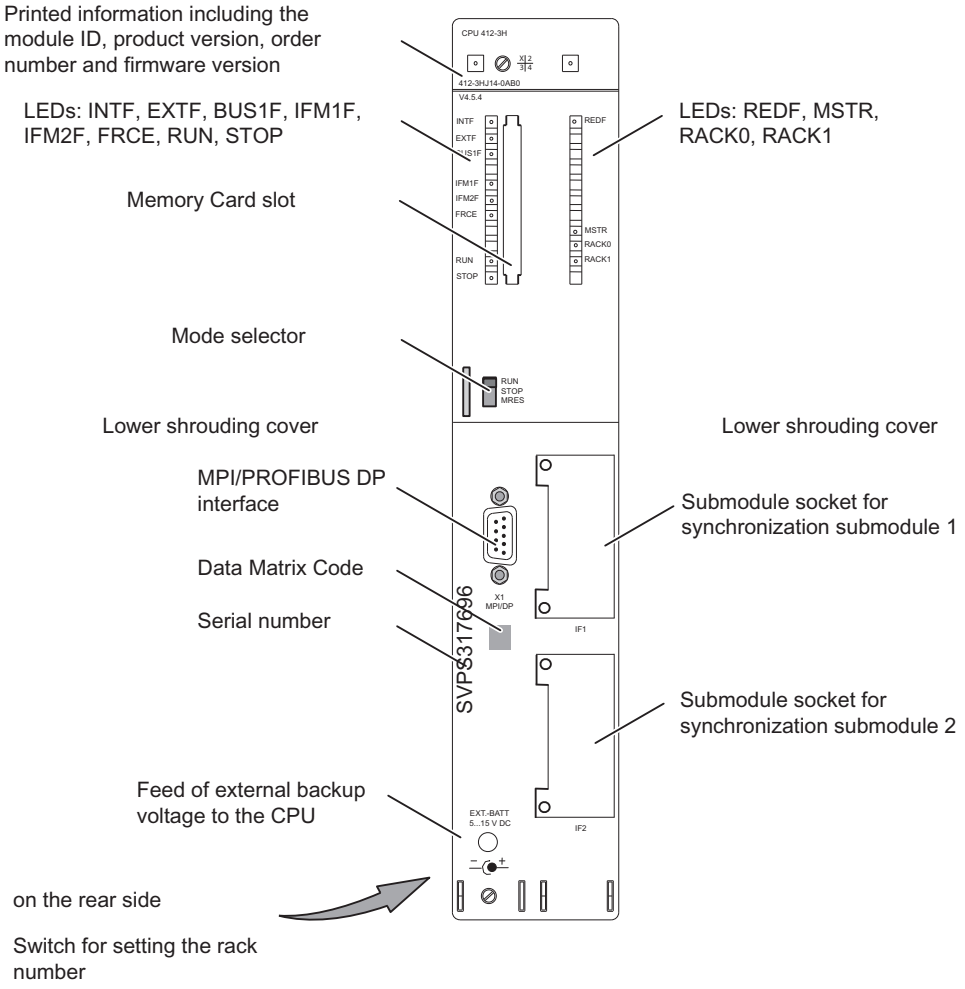


Figure 5-1 Arrangement of the operator controls and display elements on the CPU 412-3H

Operator controls and display elements of the CPU 414–4H/417–4H

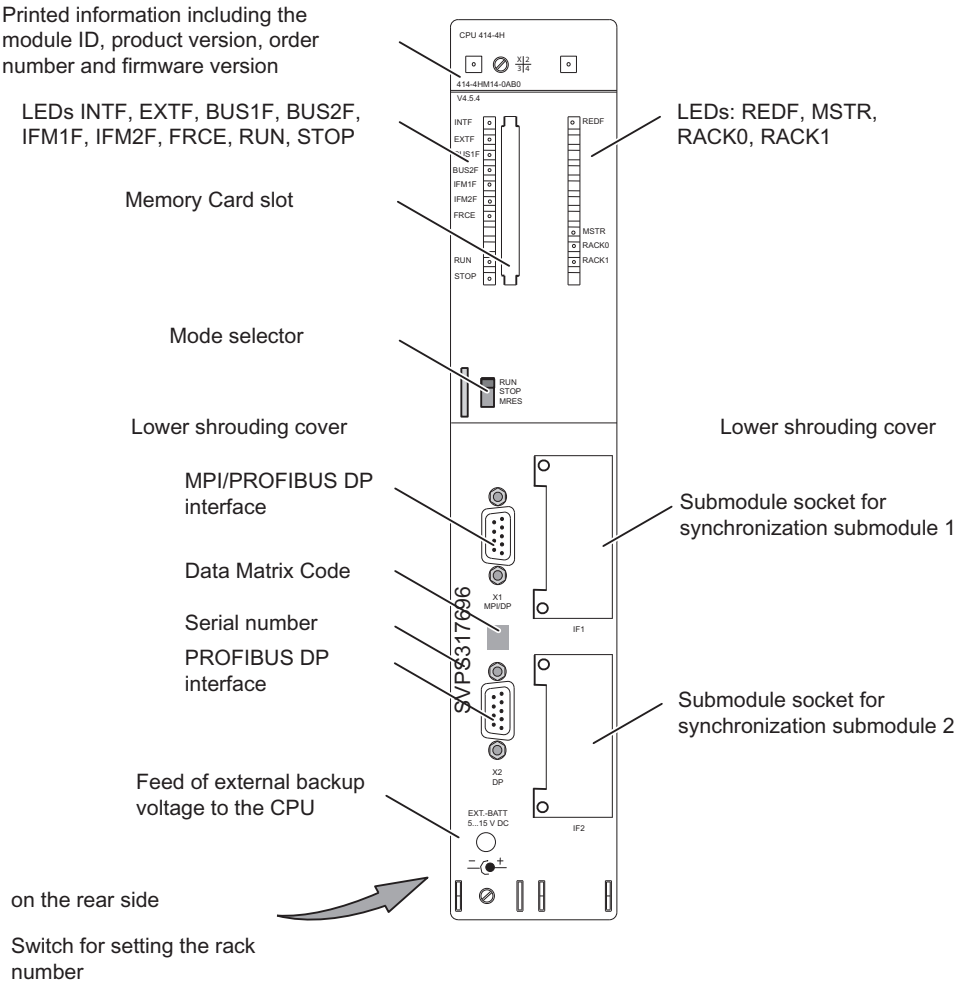


Figure 5-2 Layout of the operator controls and display elements of the CPU 414-4H/417-4H

LED displays

The following table shows an overview of the LED displays on the individual CPUs.

Sections Monitoring functions of the CPU (Page 42) and Status and error displays (Page 45) describe the states and errors/faults indicated by these LEDs.

Table 5- 1 LED displays on the CPUs

LED	Color	Meaning
INTF	red	Internal error
EXTF	red	External error
FRCE	yellow	Active force request
RUN	green	RUN mode
STOP	yellow	STOP mode
BUS1F	red	Bus fault on MPI/PROFIBUS DP interface 1
BUS2F	red	Bus fault on PROFIBUS DP interface 2
MSTR	yellow	CPU controls the process
REDF	red	Loss of redundancy/Redundancy fault
RACK0	yellow	CPU in rack 0
RACK1	yellow	CPU in rack 1
IFM1F	red	Error in synchronization module 1
IFM2F	red	Error in synchronization module 2

Mode selector

You can use the mode selector switch to set the current operating mode of the CPU. The mode selector switch is a toggle switch with three switching positions.

Section Mode selector (Page 48) describes the functions of the mode selector switch.

Memory card slot

You can insert a memory card into this slot.

There are two types of memory card:

- RAM cards

  You can expand the CPU load memory with a RAM card.

- FLASH cards

  A FLASH card can be used for fail-safe backup of the user program and data without a backup battery. You can program the FLASH card either on the programming device or in the CPU. The FLASH card also expands the load memory of the CPU.

  For detailed information on memory cards, refer to section Design and function of the memory cards (Page 53).

Slot for interface modules

You can insert an H-Sync module in this slot.

MPI/DP interface

You can, for example, connect the following devices to the MPI of the CPU:

- Programming devices
- Operator control and monitoring devices
- For further S7-400 or S7-300 controllers, see section Multi-point interface (MPI) (Page 57).

Use bus connectors with angled cable outlet, see the *S7–400 Automation System, Installation* manual.

The MPI can also be configured for operation as DP master and therefore as a PROFIBUS DP interface with up to 32 DP slaves.

PROFIBUS DP interface

The PROFIBUS DP interface supports the connection of distributed I/O, programming devices and OPs.

Setting the rack number

Use the switch on the rear panel of the CPU to set the rack number. The switch has two positions: 1 (up) and 0 (down). One CPU is allocated rack number 0, and the partner CPU is assigned rack number 1. The default setting of all CPUs is rack number 0.

Connecting an external backup voltage to the "EXT. BATT." socket

The S7–400H power supply modules support the use of two backup batteries. This allows you to implement the following:

- Back up the user program stored in RAM.
- Retain bit memories, timers, counters, system data and data in variable data blocks.
- Back up the internal clock.

You can achieve the same backup by connecting a DC voltage between 5 V DC and 15 V DC to the "EXT. BATT." socket of the CPU.

Properties of the "EXT. BATT." input:

- Reverse polarity protection
- Short-circuit current limiting to 20 mA

For incoming supply at the "EXT. BATT" socket, you require a connecting cable with a 2.5 mm ∅ jack connector as shown in the figure below. Observe the polarity of the jack connector.

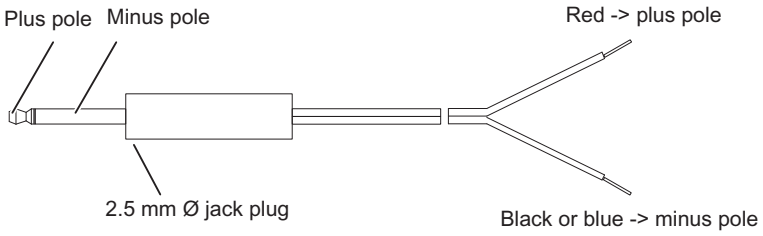


Figure 5-3 Jack connector

You can order an assembled jack connector and cable with the order number A5E00728552A.

Note

If you replace a power supply module and want to backup the user program and the data (as described above) in an RAM while doing so, you must connect an auxiliary power supply to the "EXT. BATT." socket.

5.2 Monitoring functions of the CPU

Monitoring functions and error messages

The hardware of the CPU and operating system provide monitoring functions to ensure proper operation and defined reactions to errors. Various errors may also trigger a reaction in the user program.

The table below provides an overview of possible errors and their causes, and the corresponding responses of the CPU.

Additional test and information functions are available in each CPU; they can be initiated in STEP 7.

Type of error	Cause of error	Response of the operating system	Error LED
Access error	Module failure (SM, FM, CP)	LED "EXTF" remains lit until the error is eliminated. In SMs: • Call of OB 122 with direct access, call of OB 85 in the event of a process image update • Entry in the diagnostic buffer • In the case of input modules: Entry of "null" as date in the accumulator or the process image In the case of other modules: • Call of OB 122 with direct access, call of OB 85 in the event of a process image update	EXTF
Time error	• The user program execution time (OB 1 and all interrupts and error OBs) exceeds the specified maximum cycle time. • OB request error • Overflow of the start information buffer • Time-of-day error interrupt	LED "INTF" remains lit until the error is eliminated. Call of OB 80. If the OB is not loaded: CPU changes to STOP mode.	INTF
Power supply module(s) fault (not power failure)	In the central or expansion rack: • at least one backup battery in the power supply module is flat. • the backup voltage is missing. • the 24 V supply to the power supply module has failed.	Call of OB 81 If the OB is not loaded: The CPU remains in RUN.	EXTF
Diagnostic interrupt	An I/O module with interrupt capability reports a diagnostic interrupt	Call of OB 82 If the OB is not loaded: CPU changes to STOP mode.	EXTF

Type of error	Cause of error	Response of the operating system	Error LED
Swapping interrupt	Removal or insertion of an SM, and insertion of a wrong module type.	Call of OB 83 If the OB is not loaded: CPU changes to STOP mode.	EXTF
CPU hardware fault	• A memory error was detected and eliminated • Redundant link: Data transfer errors.	Call of OB 84 If the OB is not loaded: The CPU remains in RUN.	INTF
Program execution error	• Priority class is called, but the corresponding OB is not available. • In the case of an SFB call: Missing or faulty instance DB • Process image update error	Call of OB 85 If the OB is not loaded: CPU changes to STOP mode.	INTF EXTF
Failure of a rack/station	• Power failure in an expansion rack • Failure of a PROFIBUS subnet • Failure of a coupling segment: Missing or defective IM, interrupted cable	Call of OB 86 If the OB is not loaded: CPU changes to STOP mode.	EXTF
Communication error	Communication error: • Clock synchronization • Access to DB when exchanging data via communications function blocks	Call of OB 87 If the OB is not loaded: CPU does not change to STOP mode.	INTF
Execution canceled	The execution of a program block was canceled. Possible reasons for the cancellation are: • Nesting depth of nesting levels too great • Nesting depth of master control relay too great • Nesting depth of synchronization errors too great • Nesting depth of block call commands (U stack) too great • Nesting depth of block call commands (B stack) too great • Error during allocation of local data	Call of OB 88 If the OB is not loaded: CPU changes to STOP mode.	INTF

Type of error	Cause of error	Response of the operating system	Error LED
Programming error	User program error: • BCD conversion error • Range length error • Range error • Alignment error • Write error • Timer number error • Counter number error • Block number error • Block not loaded	Call of OB 121 If the OB is not loaded: CPU changes to STOP mode.	INTF
MC7 code error	Error in the compiled user program, for example, illegal OP code or a jump beyond block end	CPU changes to STOP mode. Restart or memory reset required.	INTF

5.3 Status and error displays

RUN and STOP LEDs

The RUN and STOP LEDs provide information about the currently active CPU operating status.

LED		Meaning
RUN	STOP	
Lit	Dark	The CPU is in RUN mode.
Dark	Lit	The CPU is in STOP mode. The user program is not being executed. Cold restart/restart is possible. If the STOP status was triggered by an error, the error indicator (INTF or EXTF) is also set.
Flashes 2 Hz	Flashes 2 Hz	CPU is DEFECTIVE. All other LEDs also flash at 2 Hz.
Flashes 0.5 Hz	Lit	HOLD status has been triggered by a test function.
Flashes 2 Hz	Lit	A cold restart/restart was initiated. The cold restart/warm start may take a minute or longer, depending on the length of the called OB. If the CPU still does not change to RUN, there might be an error in the system configuration, for example.
Dark	Flashes 2 Hz	Self-test when unbuffered POWER ON is running. The self-test may take up to 10 minutes Memory is being reset
Irrelevant	Flashes 0.5 Hz	The CPU requests a memory reset.
Flashes 0.5 Hz	Flashes 0.5 Hz	Troubleshooting mode

MSTR, RACK0, and RACK1 LEDs

The three LEDs MSTR, RACK0, and RACK1 provide information about the rack number set on the CPU and show which CPU controls the switched I/O.

LED			Meaning
MSTR	RACK0	RACK1	
Lit	Irrelevant	Irrelevant	CPU controls switched I/O
Irrelevant	Lit	Dark	CPU on rack number 0
Irrelevant	Dark	Lit	CPU on rack number 1

INTF, EXTF, and FRCE LEDs

The three LEDs INTF, EXTF, and FRCE provide information about errors and special events in the user program execution.

LED			Meaning
INTF	EXTF	FRCE	
Lit	Irrelevant	Irrelevant	An internal error was detected (programming or parameter assignment error).
Irrelevant	Lit	Irrelevant	An external error was detected (i.e. an error whose cause is not in the CPU module).
Irrelevant	Irrelevant	Lit	A force request is active.

BUSF1 and BUSF2 LEDs

The BUSF1 and BUSF2 LEDs indicate errors on the MPI/DP and PROFIBUS DP interfaces.

LED		Meaning
BUS1F	BUS2F	
Lit	Irrelevant	An error was detected on the MPI/DP interface.
Irrelevant	Lit	An error was detected on the PROFIBUS DP interface.
Flashes	Irrelevant	DP master: No response from one or more slaves on PROFIBUS DP interface 1. DP slave: Not addressed by the DP master.
Irrelevant	Flashes	DP master: No response from one or more slaves on PROFIBUS DP interface 2. DP slave: Not addressed by the DP master.

IFM1F and IFM2F LEDs

The IFM1F and IFM2F LEDs indicate errors on the first or second synchronization module.

LED		Meaning
IFM1F	IFM2F	
Lit	Irrelevant	An error was detected on synchronization module 1.
Irrelevant	Lit	An error was detected on synchronization module 2

REDF LED

The REDF LED indicates specific system states and redundancy errors.

REDF LED	System state	Basic requirements
Flashes 0.5 Hz	Link-up	-
Flashes 2 Hz	Update	-
Dark	Redundant (CPUs are redundant)	No redundancy error
Lit	Redundant (CPUs are redundant)	There is an I/O redundancy error: • Failure of a DP master, or partial or total failure of a DP master system • Loss of redundancy on the DP slave

Diagnostic buffer

In STEP 7, you can select "PLC -> Module Information" to read the cause of an error from the diagnostic buffer.

5.4 Mode selector

Function of the mode selector switch

The mode selector can be used to set the CPU to RUN mode or STOP mode, or to reset the CPU memory. STEP 7 offers further options of changing the mode.

Positions

The mode selector is designed as toggle switch. The following figure shows all possible positions of the mode selector.

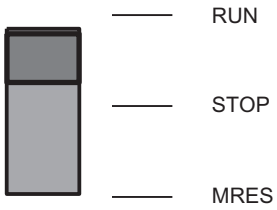


Figure 5-4 Mode selector positions

The following table explains the positions of the mode selector. If an error or a startup problem occurs, the CPU will either change to or stay in STOP mode regardless of the position of the mode selector switch.

Table 5- 2 Mode selector positions

Position	Explanations
RUN	If there is no startup problem or error and the CPU was able to switch to RUN, the CPU either executes the user program or remains idle. The I/O can be accessed.
STOP	The CPU does not execute the user program. In the default parameter setting, the output modules are disabled.
MRES (memory reset; master reset)	Toggle switch position for CPU memory reset, see section Operating sequence for memory reset (Page 50)

5.5 Security levels

You can define a security level for your project in order to prevent unauthorized access to the CPU programs. The objective of these security level settings is to grant a user access to specific programming device functions which are not protected by password, and to allow that user to execute those functions on the CPU. When logged on with a password, the user may execute all PG functions.

Setting security levels

You can set the CPU security levels 1 to 3 under "STEP 7/Configure Hardware".

If you do not know the password, you can clear the set security level by means of a manual memory reset using the mode selector. No Flash card must be inserted in the CPU when you perform such an operation.

The following table lists the security levels of an S7–400 CPU.

Table 5- 3 Security levels of a CPU

CPU function	Security level 1	Security level 2	Security level 3
Display of list of blocks	Access granted	Access granted	Access granted
Monitor variables	Access granted	Access granted	Access granted
Module status STACKS	Access granted	Access granted	Access granted
Operator control and monitoring functions	Access granted	Access granted	Access granted
S7 communication	Access granted	Access granted	Access granted
Reading the time	Access granted	Access granted	Access granted
Setting the time	Access granted	Access granted	Access granted
Status block	Access granted	Access granted	Password required
Load in PG	Access granted	Access granted	Password required
Load in CPU	Access granted	Password required	Password required
Delete blocks	Access granted	Password required	Password required
Compress memory	Access granted	Password required	Password required
Download user program to memory card	Access granted	Password required	Password required
Controlling selection	Access granted	Password required	Password required
Modify variable	Access granted	Password required	Password required
Breakpoint	Access granted	Password required	Password required
Clear breakpoint	Access granted	Password required	Password required
Memory reset	Access granted	Password required	Password required
Forcing	Access granted	Password required	Password required
Updating the firmware without a memory card	Access granted	Password required	Password required

Setting the security level with SFC 109 "PROTECT"

SFC 109 "PROTECT" is used to switch between security levels 1 and 2.

5.6 Operating sequence for memory reset

Case A: You want to download a new user program to the CPU.

1. Set the switch to the STOP position.

   Result: The STOP LED is lit.

2. Toggle the switch to MRES, and hold it in that position. In this position the mode selector acts as pushbutton.

   Result: The STOP LED is off for one second, then on for one second, then again off for one second, and then it remains lit.

3. Then release the switch, return it to MRES within the next 3 seconds, and then release it again.

   Result: The STOP LED flashes for at least 3 seconds at 2 Hz (memory is reset) and then remains lit.

Case B: The STOP LED is flashing slowly at 0.5 Hz. This indicates that the CPU is requesting a memory reset (memory reset requested by system, e.g. after a memory card has been removed or inserted).

Toggle the switch to MRES, and then release it again.

Result: The STOP LED flashes for at least 3 seconds at 2 Hz, the memory reset is executed, and the LED then remains lit.

Memory reset process in the CPU

During a memory reset, the following process occurs on the CPU:

- The CPU deletes the entire user program in the main memory.
- The CPU deletes the user program from the load memory. This process deletes the program from the integrated RAM and from any inserted RAM Card. The user program elements stored on a FLASH card will not be deleted if you have expanded the load memory with such a card.
- The CPU deletes all counters, bit memories, and timers, but not the time of day.
- The CPU tests its hardware.
- The CPU sets its parameters to default settings.
- If a FLASH card is inserted, the CPU copies the user program and the system parameters stored on the FLASH card into main memory after the memory reset.

Data retained after a memory reset...

The following values are retained after a memory reset:

- The content of the diagnostic buffer

  If no FLASH card was inserted during memory reset, the CPU resets the capacity of the diagnostic buffer to its default setting of 120 entries, i.e. the most recent 120 entries will be retained in the diagnostic buffer.

  You can read out the content of the diagnostic buffer using STEP 7.
- The MPI interface parameters. These define the MPI address and the highest MPI address. Note the special features shown in the table below.
- The time-of-day
- The status and value of the runtime meter

Special feature: MPI parameters

The MPI parameters play an exceptional role during memory reset. The table below lists the MPI parameters which are valid after a memory reset.

Memory reset ...	MPI parameters ...
with inserted FLASH card	... stored on the FLASH card are valid
without inserted FLASH card	...in the CPU are retained and valid

Cold restart

- A cold restart resets the process image, all bit memories, timers, counters, and data blocks to the initial values stored in the load memory, regardless of whether these data were parameterized as being retentive or not.
- Program execution resumes with OB 1, or with OB 102 if available.

Warm restart

- A warm restart resets the process image and the non-retentive bit memories, timers, times, and counters.

  Retentive bit memories, timers, counters, and all data blocks retain their last valid value.
- Program execution resumes with OB 1, or with OB 100 if available.
- If the power supply is interrupted, the warm restart function is only available in backup mode.

Operating sequence for warm restart

1. Set the switch to the STOP position.

Result: The STOP LED is lit.

2. Set the switch to RUN.

   Result: The STOP LED goes out, the RUN LED is lit.

Whether the CPU performs a warm restart or a hot restart is determined by its configuration.

Operating sequence for cold restart

You can only initiate a cold restart using the programming device command "Cold restart". For this purpose, the CPU must be in STOP mode and the mode selector switch must be set to RUN.

5.7 Design and function of the memory cards

Order numbers

The order numbers for memory cards are listed in the technical specifications, see section Technical data of memory cards (Page 330).

Design of a memory card

The memory card has the size of a PCMCIA card. It is inserted in a slot on the front side of the CPU.

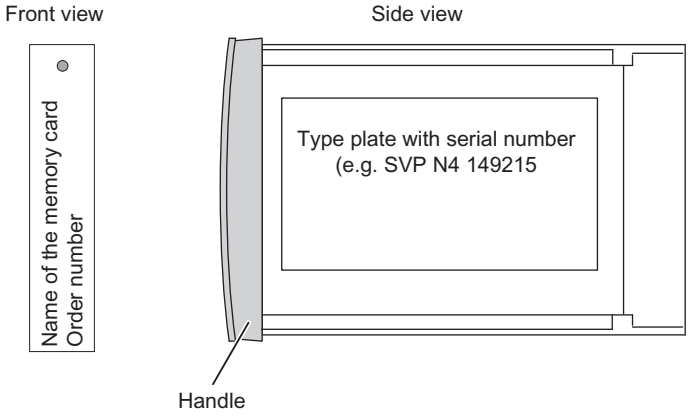


Figure 5-5 Design of the memory card

Function of the memory card

The memory card and an integrated memory area on the CPU together form the load memory of the CPU. During operation, the load memory contains the complete user program, including comments, symbols, and special additional information that enables decompilation of the user program, as well as all module parameters.

Data stored on the memory card

The following data can be stored on the memory card:

- The user program, i.e. OBs, FBs, FCs, DBs, and system data
- Parameters that determine the behavior of the CPU
- Parameters that determine the behavior of I/O modules
- The full set of project files on suitable memory cards.

Types of memory cards for the S7–400

Two types of memory card are used for the S7–400:

- RAM cards
- FLASH cards

What type of memory card should I use?

Whether you use a RAM card or a FLASH card depends on your application.

Table 5- 4 Types of memory card

If you ...	then ...
want to be able to edit your program in RUN mode,	use a **RAM card**
want to keep a permanent backup of your user program on the memory card, even when power is off, i.e. without backup or outside the CPU,	use a **FLASH card**

RAM card

Insert the RAM card to load the user program in the CPU. Load the user program in STEP 7 by selecting "PLC > Download user program to Memory Card".

You can load the entire user program or individual elements such as FBs, FCs, OBs, DBs, or SDBs in the load memory in STOP or RUN mode.

When you remove the RAM card from the CPU, the information stored on it will be lost. The RAM card is not equipped with an integrated backup battery.

If the power supply is equipped with an operational backup battery, or the CPU is supplied with an external backup voltage at the "EXT. BATT." socket, the RAM card memory contents are retained when power is switched off, provided the RAM card remains inserted in the CPU and the CPU remains inserted in the rack.

FLASH card

If you use a FLASH card, there are two ways of loading the user program:

- Use the mode selector to set the CPU to STOP. Insert the FLASH card into the CPU, and then download the user program to the FLASH card in STEP 7 by selecting "PLC > Download user program to Memory Card".
- Load the user program into the FLASH card in offline mode on the programming device/programming adapter, and then insert the FLASH card into the CPU.

The FLASH card is a non-volatile memory, i.e. its data are retained when it is removed from the CPU or your S7-400 is being operated without backup voltage (without a backup battery in the power supply module or external backup voltage at the "EXT. BATT." input of the CPU).

Automatic restart or cold restart without backup

If you operate your CPU without a backup battery, CPU memory reset followed by restart or cold restart, as configured, will automatically be carried out after switch-on or voltage recovery after power off. The user program must be available on the FLASH card and the battery indicator switch on the power supply module may not be set to battery monitoring.

If battery monitoring is set, you must carry out a restart or cold restart either with the mode selector or via a programming device after CPU switch on or voltage recovery following power off. The absence of or a defective backup battery is reported as an external fault and the LED EXTF lights up.

Downloading a user program

You can only download the full user program to a FLASH card.

NOTICE
Data block on FLASH card Do not transfer any data blocks to the FLASH card that are automatically generated when the CPU starts up. The CPU will not start up if this is the case. The automatically generated data blocks will only be available in an offline project, if you have downloaded them from the CPU to the offline project.

Downloading additional user program elements

You can download further elements of the user program from the programming device to the integrated load memory of the CPU. Note that the content of this integrated RAM will be deleted if the CPU performs a memory reset, i.e. the load memory is updated with the user program stored on the FLASH card after a memory reset.

What memory card capacity should I use?

The capacity of your memory card is determined by the scope of the user program.

Determining memory requirements using SIMATIC Manager

You can view the block lengths offline in the "Properties - Block folder offline" dialog box (Blocks > Object Properties > Blocks tab).

The offline view shows the following lengths:

- Size (sum of all blocks, without system data) in the load memory of the target system
- Size (sum of all blocks, without system data) in the work memory of the target system

Block lengths on the programming device (PG/PC) are not shown in the properties of the block container.

Block lengths are shown in "byte" units.

The following values are shown in the properties of a block:

- Required local data volume: Length of local data in bytes
- MC7: Length of MC7 code in bytes
- Length of DB user data
- Length in load memory of the target system
- Length in work memory of the target system (only if hardware assignment is known)

The views always show these block data, regardless whether it is located in the window of an online view or of an offline view.

When a block container is opened and "View Details" is set, the project window always indicates work memory requirements, regardless of whether the block container appears in the window of an online or offline view.

You can add up the block lengths by selecting all relevant blocks. SIMATIC Manager outputs the total length of the selected blocks in its status bar.

Lengths of blocks (VATs, for example) which can not be downloaded to the target system are not shown.

Block lengths on the programming device (PG/PC) are not shown in the Details view.

5.8 Multi-point interface (MPI)

Connectable devices

You can, for example, connect the following devices to the MPI:

- Programming devices (PG/PC)
- Operating and monitoring devices (OPs and TDs)
- Further SIMATIC S7 controllers

Various compatible devices take the 24 V supply from the interface. This voltage is non-isolated.

PG/OP–CPU communication

A CPU is capable of handling several online connections to PGs/OPs in parallel. By default, however, one of these connections is always reserved for a PG, and one for an OP/HMI device.

CPU–CPU communication

CPUs exchange data by means of S7 communication.

For additional information, refer to the *Programming with STEP 7* manual.

Connectors

Always use bus connectors with an angular cable outlet for PROFIBUS DP or PG cables to connect devices to the MPI (see *Installation Manual*).

MPI as DP interface

You can also parameterize the MPI for operation as DP interface. To do so, reparameterize the MPI under STEP 7 in the SIMATIC Manager. You can configure a DP segment with up to 32 slaves.

5.9 PROFIBUS DP interface

Connectable devices

You can connect any standard-compliant DP slaves to the PROFIBUS DP interface.

Here, the CPU represents the DP master, and is connected to the passive slave stations or, in stand-alone mode, to other DP masters via the PROFIBUS DP fieldbus.

Various compatible devices take the 24 V supply from the interface. This voltage is non-isolated.

Connectors

Always use bus connectors for PROFIBUS DP and PROFIBUS cables to connect devices to the PROFIBUS DP interface (*refer to the Installation Manual*).

Redundant mode

In redundant mode, the PROFIBUS DP interfaces have the same parameters.

5.10 Overview of the parameters for the S7-400H CPUs

Default values

You can determine the CPU-specific default values by selecting "Configuring Hardware" in STEP 7.

Parameter blocks

The responses and properties of the CPU are defined in parameters which are stored in system data blocks. The CPUs have a defined default setting. You can modify these default setting by editing the parameters in the hardware configuration.

The list below provides an overview of the parameterizable system properties of the CPUs.

- General properties such as the CPU name
- Start-up
- Cycle/clock memory, e.g. the scan cycle monitoring time
- Retentivity, i.e. the number of bit memories, timers, and counters retained
- Memory, e.g. local data

  Note: If you change the work memory allocation by modifying parameters, this work memory is reorganized when you download system data to the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

  If you change the following parameters, the work memory area available for logic blocks and data blocks will be modified when loading the system data:

  – Size of the process image, byte-oriented in the "Cycle/Clock memory" tab
  – Communication resources in the "Memory" tab
  – Size of the diagnostic buffer in the "Diagnostics/Clock" tab
  – Number of local data for all priority classes in the "Memory" tab
- Assignment of interrupts (hardware interrupts, time delay interrupts, asynchronous error interrupts) to the priority classes
- Time-of-day interrupts such as start, interval duration, priority
- Watchdog interrupts, e.g. priority, interval duration
- Diagnostics/clock, e.g. time-of-day synchronization
- Security levels
- Fault tolerance parameters

Parameter assignment tool

You can set the individual CPU parameters using "HW Config" in STEP 7.

Note

If you modify the parameters listed below, the operating system initializes the following:

- Size of the process input image
- Size of the process output image
- Size of the local data
- Number of diagnostic buffer entries
- Communication resources

These initializations are:

- Data blocks are initialized with the load values
- M, C, T, I, O will be deleted irrespective of the retentivity setting (0)
- DBs generated by SFC will be deleted
- Permanently configured dynamic connections will be terminated

The system starts up in the same way as with a cold restart.

Further settings

- The rack number of a fault-tolerant CPU, 0 or 1

  Use the selector switch on the rear panel of the CPU to change the rack number.
- The operating mode of a fault-tolerant CPU: Stand-alone or redundant mode

  For information on how to change the operating mode of a fault-tolerant CPU, refer to Appendix Stand-alone operation (Page 343).

Special functions of a CPU 41x-H

6

6.1 Updating the firmware without a memory card

Basic procedure

To update the firmware of a CPU, you will receive several files (*.UPD) containing the current firmware. Download these files to the CPU. You do not need a memory card to perform an online update. However, it is still possible to update the firmware using a memory card.

Requirement

The CPU whose firmware you want to update must be accessible online, e.g. via PROFIBUS, MPI, or Industrial Ethernet. The files containing the current firmware versions must be available in the programming device/PC file system. A folder may contain only the files of one firmware version. If security level 2 or 3 is set for the CPU, you require the password to update the firmware.

Note

You can update the firmware of the H-CPUs via Industrial Ethernet if the CPU is connected to the Industrial Ethernet via a CP. Updating the firmware over a MPI can take a long time if the transfer rate is low (e.g. approximately 10 minutes at 187.5 Kbit/s).

Procedure

Proceed as follows to update the firmware of a CPU:

1. Open the station containing the CPU you want to update in HW Config.
2. Select the CPU.
3. Select the "PLC -> Update Firmware" menu command.
4. In the "Update Firmware" dialog, select the path to the firmware update files (*.UPD) using the "Browse" button.

   After you have selected a file, the information in the bottom boxes of the "Update Firmware" dialog box indicate the modules for which the file is suitable and from which firmware version.
5. Click on "Run".

STEP 7 verifies that the selected file can be interpreted by the CPU and then downloads the file to the CPU. If this requires changing the operating state of the CPU, you will be prompted to do this in the relevant dialog boxes.

NOTICE

Power on/off without battery backup

If the firmware update is interrupted by a power cycle without battery backup, it is possible that the CPU no longer has a functioning operating system. You can recognize this by the LEDs INTF and EXTF both flashing. You can only correct this by reloading the firmware from a memory card.

6.2 Firmware update in RUN mode

Requirement

The size of the load memory on the master and reserve CPU is the same. Both Sync links exist and are working.

Procedure with STEP7 V5.4 SP3 or higher

Follow the steps below to update the firmware of the CPUs of an H system in RUN:

1. Set one of the CPUs to STOP using the programming device
2. Select this CPU in HW Config.
3. Select the "PLC -> Update Firmware" menu command.

   The "Update Firmware" dialog box opens. Select the firmware file from which the current firmware will be downloaded to the selected CPU.
4. In SIMATIC Manager or HW Config, select the "PLC -> Operating Mode -> Switch to CPU 41x-H" and select the "with altered operating system" check box.

   The fault-tolerant system switches the Master/Reserve roles, after which the CPU will be in RUN mode again.
5. Repeat steps 1 to 3 for the other CPU.
6. Restart the CPU. The fault-tolerant system will return to redundant mode.

Both CPUs have updated firmware (operating system) and are in redundant mode.

Procedure with STEP 7 V5.3 SP2 up to and including STEP 7 V5.4 SP2

Follow the steps below to update the firmware of the CPUs of an H system in RUN:

1. In SIMATIC Manager, set one of the CPUs to STOP with "PLC -> Operating Mode CPUs".
2. Select this CPU in HW Config.
3. Select the "PLC -> Update Firmware" menu command.

   The "Update Firmware" dialog box opens. Select the firmware file from which the current firmware will be downloaded to the selected CPU.
4. In SIMATIC Manager or HW Config, select the "PLC -> Operating Mode -> Switch to CPU 41xH" and select the "with altered operating system" check box.

   The fault-tolerant system switches the Master/Reserve roles, after which the CPU will be in RUN mode again.
5. Repeat steps 1 to 3 for the other CPU.
6. Restart the CPU. The fault-tolerant system will return to redundant mode.

Both CPUs have updated firmware (operating system) and are in redundant mode.

NOTICE
Note the following for STEP 7 V5.3 SP2 up to and including STEP 7 V5.4 SP2: With these STEP7 versions, if you run "PLC -> Update Firmware" from HW Config before you have set the CPU to STOP in SIMATIC Manager, **both** CPUs go to STOP.

Note

Only the third number of the firmware versions of the master and reserve CPU may differ by 1. You can only update to the newer version.

Example: From V4.5.0 to V4.5.1

Please take note of any information posted in the firmware download area.

The constraints described in section System and operating states of the S7–400H (Page 81) also apply to a firmware update in RUN

6.3 Reading service data

Application case

If you need to contact Customer Support due to a service event, the department may require specific diagnostic information on the CPU status of your system. This information is stored in the diagnostic buffer and in the actual service data.

Select the "PLC -> Save service data" command to read this information and save the data to two files. You can then send these to Customer Support.

Note the following:

- If possible, save the service data immediately after the CPU goes into STOP or the synchronization of a fault-tolerant system has been lost.
- Always save the service data of both CPUs in an H system.

Procedure

1. Select the "PLC > Save service data" command

   In the dialog box that opens up, select the file path and the file names.
2. Save the files.
3. Forward these files to Customer Support on request.

S7–400H in PROFIBUS DP mode

7

7.1 CPU 41x–H as PROFIBUS DP master

Introduction

This chapter describes how to use the CPU as DP master and configure it for direct data exchange.

Further references

For details and information on engineering, configuring a PROFIBUS subnet, and diagnostics in a PROFIBUS subnet, refer to the **STEP 7** Online Help.

Additional information

Details and information on migrating from PROFIBUS DP to PROFIBUS DPV1 can be found on the Internet at:

http://support.automation.siemens.com

under entry number 7027576

7.1.1 DP address areas of CPUs 41xH

Address areas of 41xH CPUs

Table 7- 1 CPUs 41x, MPI/DP interface as PROFIBUS DP

Address area	412-3H	414-4H	417–4H
MPI as PROFIBUS DP, inputs and outputs (bytes) in each case	2048	2048	2048
DP interface as PROFIBUS DP, inputs and outputs (bytes) in each case	-	6144	8192
Of those addresses you can configure up to x bytes for each I/O in the process image	-	0 to 8192	0 to 16384

DP diagnostics addresses occupy at least 1 byte for the DP master and each DP slave in the input address area. At these addresses, the DP standard diagnostics can be called for the relevant node by means of the LADDR parameter of SFC 13, for example. Define the DP diagnostics addresses when you configure the project data. If you do not specify any DP diagnostics addresses, STEP 7 automatically assigns the addresses as DP diagnostics addresses in descending order, starting at the highest byte address.

In DPV1 mode of the master, the slaves are usually assigned 2 diagnostics addresses.

7.1.2 CPU 41xH as PROFIBUS DP master

Requirement

You have to configure the relevant CPU interface for use as PROFIBUS DP master. This means you must make the following settings in **STEP 7**:

- Assign a network
- Configure the CPU as PROFIBUS DP master
- Assign a PROFIBUS address
- Select the operating mode, S7–compatible or DPV1

  The default setting is DPV1
- Link DP slaves to the DP master system

Note

Is one of the PROFIBUS DP slaves a CPU 31x or CPU 41x?

If yes, you will find it in the PROFIBUS DP catalog as "preconfigured station". Assign this DP slave CPU a slave diagnostics address in the PROFIBUS DP master. Link the PROFIBUS DP master to the DP slave CPU, and specify the address areas for data exchange with the DP slave CPU.

Monitor/Modify, programming via PROFIBUS

As an alternative to the MPI, you can use the PROFIBUS DP interface to program the CPU or execute the Monitor/Modify programming device functions.

NOTICE
The "Programming" or "Monitor/Modify" applications prolong the DP cycle if executed via the PROFIBUS DP interface.

DP master system startup

Use the following parameters to set startup time monitoring of the PROFIBUS DP master:

- Ready message from module
- Transfer of parameters to modules

This means the DP slaves must start up within the set time and be parameterized by the CPU (as PROFIBUS DP master).

PROFIBUS address of the PROFIBUS DP master

All PROFIBUS addresses are permissible.

From IEC 61158 to DPV1

The IEC 61158 standard for distributed I/Os has been enhanced. The enhancements were incorporated into IEC 61158/IEC 61784–1:2002 Ed1 CP 3/1. The SIMATIC documentation uses the term "DPV1" in this context. The new version features various expansions and simplifications.

SIEMENS automation components feature DPV1 functionality. In order to be able to use these new features, you first have to make some modifications to your system. A full description of the migration from IEC 61158 to DPV1 is available in the FAQ section titled "Migrating from IEC 61158 to DPV1", FAQ entry ID 7027576, on the Customer Support Internet site.

Components supporting PROFIBUS DPV1 functionality

DPV1 master

- The S7-400 CPUs with integrated DP interface.
- CP 443-5, order number 6GK7 443–5DX03–0XE0,
  6GK7 443–5DX04–0XE0.

DPV1 slaves

- DP slaves listed in the STEP 7 hardware catalog under their family names can be identified in the information text as DPV1 slaves.
- DP slaves integrated in STEP 7 by means of GSD files revision 3 or higher.

What operating modes are there for DPV1 components?

- S7-compatible mode

  In this mode, the component is compatible with IEC 61158. However, you cannot use the full DPV1 functionality.

- DPV1 mode

  In this mode the component can make full use of DPV1 functionality. Automation components in the station that do not support DPV1 can be used as before.

Compatibility between DPV1 and IEC 61158?

You can continue to use all existing slaves after converting to DPV1. These do not, however, support the enhanced functions of DPV1.

You can also use DPV1 slaves without a conversion to DPV1. In this case they behave like conventional slaves. SIEMENS DPV1 slaves can be operated in S7-compatible mode. To integrate DPV1 slaves from other manufacturers, you need a GSD file complying with IEC 61158 earlier than revision 3.

Determining the bus topology in a DP master system using SFC 103 "DP_TOPOL"

A diagnostic repeater is available to make it easier to localize disrupted modules or DP cable breaks when failures occur during operation. This module is a slave that discovers the topology of a PROFIBUS subnet and detects any problems caused by it.

You can use SFC 103 "DP_TOPOL" to trigger the determination of the bus topology of a DP master system by the diagnostic repeater. SFC 103 is described in the corresponding online help and in the *"System and Standard Functions* manual. For information on the diagnostic repeater refer to the *"Diagnostic Repeater for PROFIBUS DP* manual, order number 6ES7972–0AB00–8BA0.

7.1.3 Diagnostics of a CPU 41xH operating as PROFIBUS DP master

Diagnostics using LEDs

The following table shows the meaning of the BUSF LEDs. Always the BUSF LED assigned to the interface configured as PROFIBUS DP interface lights up or flashes when a problem occurs.

Table 7- 2 Meaning of the "BUSF" LED of the CPU 41x operating as DP master

BUSF	Meaning	What to do
Off	Configuration correct; all configured slaves are addressable	-
Lit	• DP interface error • Different Baud rates in multi-DP master operation (only in stand-alone mode)	• Evaluate the diagnosis. Reconfigure or correct the configuration.
Flashing	• Station failure • At least one of the assigned slaves is not addressable • Bus fault (physical fault)	• Check whether the bus cable is connected to the CPU 41x or whether the bus is interrupted. • Wait until the CPU 41x has powered up. If the LED does not stop flashing, check the DP slaves or evaluate the diagnosis of the DP slaves. • Check whether the bus cable has a short-circuit or a break.

Reading out the diagnostics information with STEP 7

Table 7- 3 Reading out the diagnostics information with STEP 7

DP master	Block or tab in STEP 7	Application	See ...
CPU 41x	"DP slave diagnostics" tab	Display the slave diagnosis as plain text on the **STEP 7** user interface	See "Hardware diagnostics" in the **STEP 7** Online Help, and *Configuring hardware and connections with* **STEP 7** in the manual
	SFC 13 "DPNRM_DG"	Reading slave diagnostics data, i.e. saving them to the data area of the user program The busy bit may not be set to "0" if an error occurs while SFC 13 is being processed. You should therefore check the RET_VAL parameter whenever SFC 13 was processed.	For information on the configuration of a CPU 41x, refer to the *CPU Data Reference Manual*; for information on the SFC, refer to the *System and Standard Functions Reference Manual*. For information on the configuration of other slaves, refer to the corresponding description
	SFC 59 "RD_REC"	Readout of data records of the S7 diagnosis (saving them to the data area of the user program)	Refer to the *System and Standard Functions Reference Manual*

DP master	Block or tab in STEP 7	Application	See ...
	SFC 51 "RDSYSST"	Readout of system status lists (SSL). Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	
	SFB 52 "RDREC"	for DPV1 slaves Reading data records of S7 diagnostics, i.e. saving them to the data area of the user program	
	SFB 54 "RALRM"	for DPV1 slaves: Readout of interrupt information within the associated interrupt OB	

Evaluating diagnostics data in the user program

The figure below shows how to evaluate the diagnostics data in the user program.

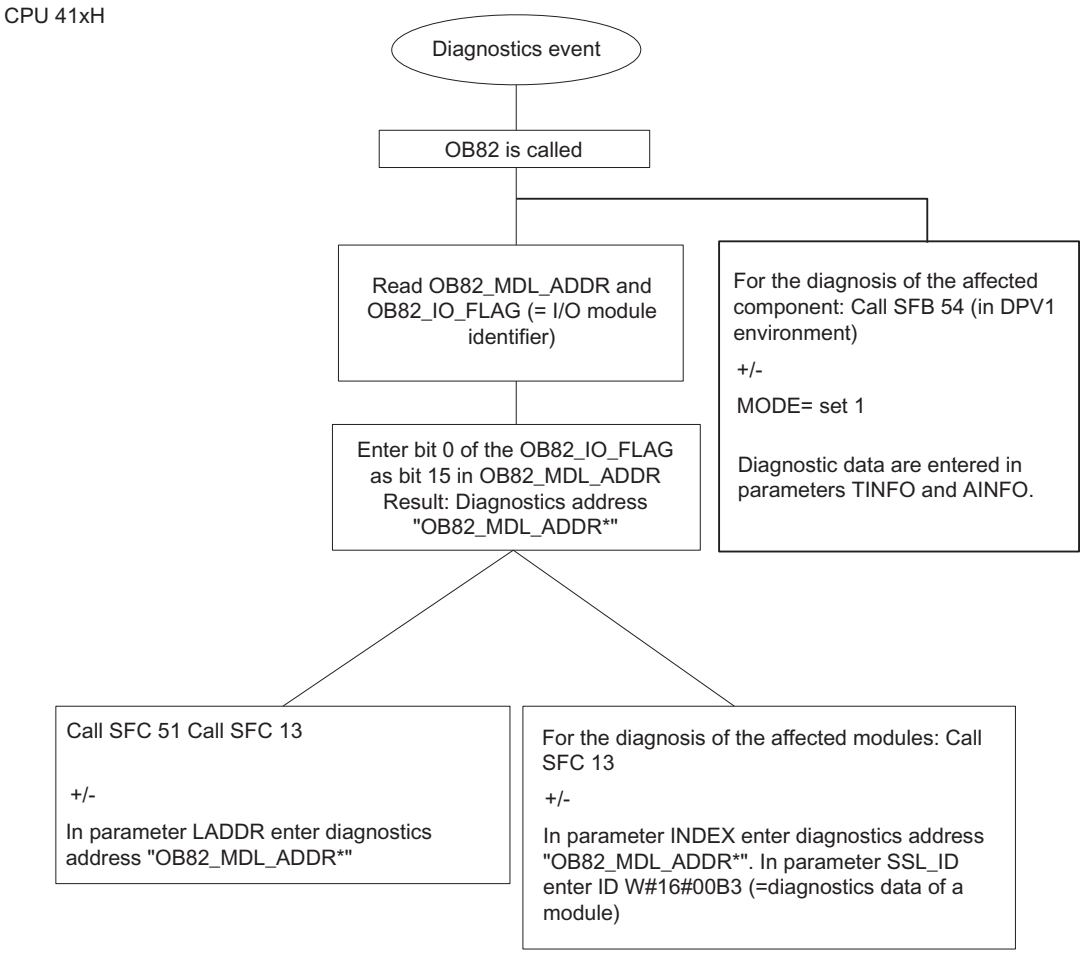


Figure 7-1 Diagnostics with CPU 41xH

Diagnostics addresses in connection with DP slave functionality

Assign the diagnostics addresses for PROFIBUS DP at the CPU 41xH. Verify in the configuration that the DP diagnostics addresses are assigned once to the DP master and once to the DP slave.

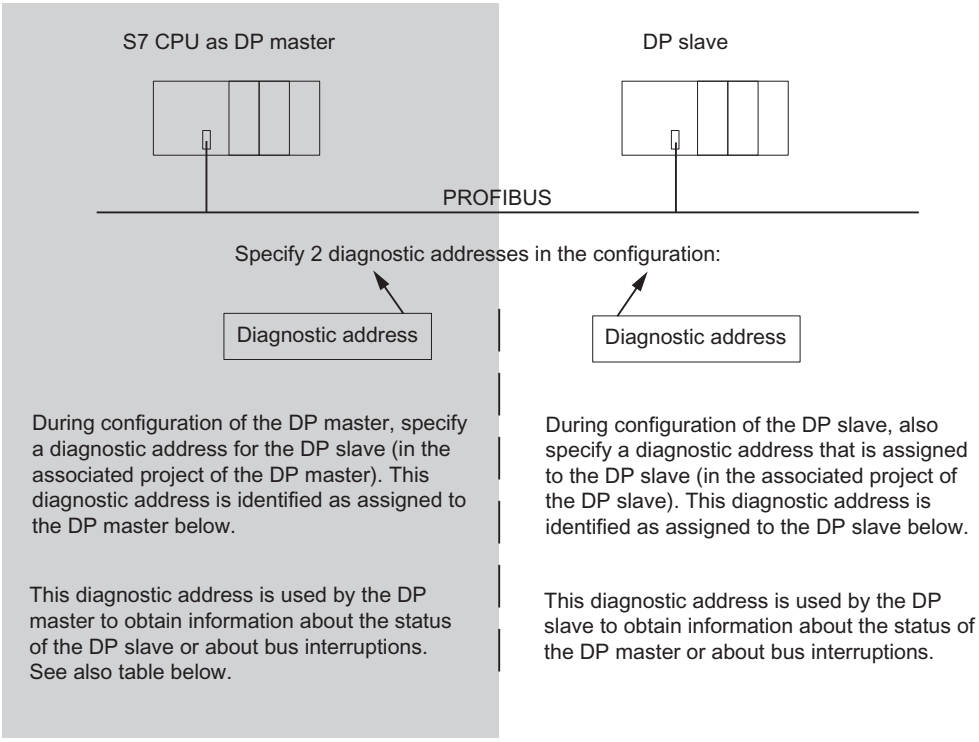


Figure 7-2 Diagnostics addresses for DP master and DP slave

Event detection

The following table shows how the CPU 41xH in DP master mode detects operating state changes on a DP slave or interruptions of the data transfer.

Table 7- 4 Event detection of the CPU 41xH as a DP master

Event	What happens in the DP master
Bus interruption due to short-circuit or disconnection of the connector	• OB 86 is called with the message **Station failure** as an incoming event; diagnostics address of the DP slave assigned to the DP master • With I/O access: Call of OB 122, I/O area access error
DP slave: RUN → STOP	• OB 82 is called with the message **Module error** as incoming event; diagnostic address of the DP slave assigned to the DP master; variable OB82_MDL_STOP=1
DP slave: STOP → RUN	• OB 82 is called with the message **Module OK** as incoming event; diagnostic address of the DP slave assigned to the DP master; variable OB82_MDL_STOP=0

Evaluation in the user program

The table below shows you how to evaluate RUN-STOP changes of the DP slave on the DP master. Also refer to previous table.

On the DP master	On the DP slave (CPU 41x)
• Example of diagnostics addresses: Master diagnostics address=1023 Slave diagnostics address in master system=1022	• Example of diagnostics addresses: Slave diagnostics address=422 Master diagnostics address=irrelevant
The CPU calls OB 82 with the following information, for example: • OB 82_MDL_ADDR:=1022 • OB82_EV_CLASS:=B#16#39 As incoming event • OB82_MDL_DEFECT:=module error The CPU diagnostic buffer also contains this information Your user program should also be set up to read the diagnostic data of the DP slave using SFC 13 "DPNRM_DG". Use SFB 54 in the DPV1 environment. This outputs the full interrupt information.	CPU: RUN → STOP CPU generates a DP slave diagnostics frame.

7.2 Consistent data

Data that belongs together in terms of its content and describe a process state at a specific point in time is known as consistent data. In order to maintain data consistency, do not modify or update the data during their transfer.

Example 1:

In order to provide a consistent image of the process signals to the CPU for the duration of cyclic program processing, the process signals are written to the process input image prior to program execution, or the processing results are written to the process output image after program execution. Subsequently, during program processing when the inputs (I) and outputs (O) operand areas are addressed, the user program addresses the internal memory area of the CPU on which the process image is located instead of directly accessing the signal modules.

Example 2:

Inconsistency may develop when a communication block, such as SFB 14 "GET" or SFB 15 "PUT", is interrupted by a process alarm OB of higher priority. If the user program modifies any data of this process alarm OB which in part have already been processed by the communication block, certain parts of the transferred data will have retained their original status which was valid prior to process alarm processing, while others represent data from after process alarm processing.

This results in inconsistent data, i.e. data which are no longer associated.

SFC 81 "UBLKMOV"

Use SFC 81 "UBLKMOV" to copy the content of a memory area, the source area, consistently to another memory area, the destination area. The copy operation cannot be interrupted by other operating system activities.

SFC 81 "UBLKMOV" enables you to copy the following memory areas:

- Bit memory
- DB contents
- Process input image
- Process output image

The maximum amount of data you can copy is 512 bytes. Make allowances for the CPU-specific restrictions listed in the instruction list.

Since copying cannot be interrupted, the alarm response times of your CPU may increase when using SFC 81 "UBLKMOV".

The source and destination areas must not overlap. If the specified destination area is larger than the source area, the function only copies the amount of data contained in the source area to the destination area. If the specified destination area is smaller than the source area, the function only copies as much data as can be written to the destination area.

7.2.1 Consistency of communication blocks and functions

With S7-400, communication jobs are not processed in the cycle control point but rather in fixed time slices during the program cycle.

The system can always process the data formats byte, word and double word consistently, i.e. the transfer or processing of 1 byte, 1 word = 2 bytes, or 1 double word = 4 bytes cannot be interrupted.

If the user program calls communication blocks such as SFB 12 "BSEND" and SFB 13 "BRCV", which are only used in pairs and access shared data, access to this data area can be coordinated by the user by means of the "DONE" parameter, for example. The consistency of data transmitted locally with these communication blocks can thus be ensured in the user program.

In contrast, S7 communication functions do not require a block such as SFB 14 "GET", SFB 15 "PUT", in the user program of the target device. Here, you must make allowance for the volume of consistent data in the programming phase.

7.2.2 Access to the work memory of the CPU

The communication functions of the operating system access the CPU's work memory in fixed block lengths. The block length is CPU-specific. The variables for S7-400 CPUs have a length of up to 472 bytes.

This ensures that the interrupt response time is not prolonged due to communication load. Since this access is performed asynchronously to the user program, you cannot transmit an unlimited number of bytes of consistent data.

The rules to ensure data consistency are described below.

7.2.3 Consistency rules for SFB 14 "GET" or read variable, and SFB 15 "PUT" or write variable

SFB 14

The data are received consistently if you observe the following points:

Evaluate the entire, currently used part of the receive area RD_i before you activate a new request.

SFB 15

When a send operation is initiated (rising edge at REQ), the data to be sent from the send areas SD_i are copied from the user program. You can write new data to these areas after the block call command without corrupting the current send data.

Note

Completion of transfer

The send operation is not completed until the status parameter DONE assumes value 1.

7.2.4 Reading data consistently from a DP standard slave and writing consistently to a DP standard slave

Reading data consistently from a DP standard slave using SFC 14 "DPRD_DAT"

Use SFC 14 "DPRD_DAT", "read consistent data of a DP standard slave", to read consistent data from a DP standard slave.

The data read is entered into the destination area defined by RECORD if no error occurs during data transfer.

The destination area must have the same length as the one you have configured for the selected module with STEP 7.

By calling SFC 14 you can only access the data of one module/DP identifier at the configured start address.

Writing data consistently to a DP standard slave using SFC 15 "DPWR_DAT"

Use SFC 15 "DPWR_DAT", "write consistent data to a DP standard slave", to transfer consistent data in RECORD to the addressed DP standard slave.

The source area must have the same length as the one you configured for the selected module with STEP 7.

Upper limits for the transfer of consistent user data to a DP slave

The PROFIBUS DP standard defines upper limits for the transfer of consistent user data to a DP slave.

For this reason a maximum of 64 words = 128 bytes of user data can be consistently transferred in a block to the DP standard slave.

You can define the length of the consistent area in your configuration. In the special identification format (SIF), you can define a maximum length of consistent data of 64 words = 128 bytes; 128 bytes for inputs and 128 bytes for outputs. A greater length is not possible.

This upper limit applies only to pure user data. Diagnostics and parameter data are grouped to form complete data records, and are thus always transferred consistently.

In the general identification format (GIF), you can define a maximum length of consistent data of 16 words = 32 bytes; 32 bytes for inputs, and 32 bytes for outputs. A greater length is not possible.

In this context, consider that a CPU 41x operating as DP slave generally has to support its configuration at an external master (implementation by means of GSD file) using the general identification format. A CPU 41x operated as DP slave thus supports only a maximum length of 16 words = 32 bytes in its transfer memory for PROFIBUS DP.

7.2.5 Consistent data access without using SFC 14 or SFC 15

Consistent data access > 4 bytes is also possible without using SFC 14 or SFC 15. The data area of a DP slave to be transferred consistently is transferred to a process image partition. The data in this area are thus always consistent. You can then access the process image partition using the load/transfer commands (L EW 1, for example). This represents a highly user-friendly and efficient (low runtime load) method to access consistent data Thus an efficient integration and parameterization of, for example, drives or other DP slaves is made possible.

Any direct access to a consistently configured data area,
e.g. L PEW or T PAW, does **not** result in an I/O area access error.

Important aspects in the conversion from the SFC14/15 solution to the process image solution are:

- When converting from the SFC14/15 method to the process image method, it is not advisable to use the system functions and the process image at the same time. Although the process image is updated when writing with the system function SFC15, this is not the case when reading. In other words, consistency between the values of the process image and of the system function SFC14 is not ensured.
- SFC 50 "RD_LGADR" outputs different address areas with the SFC 14/15 method as with the process image method.
- If you use a CP 443–5 ext, the parallel use of system functions and process image causes the following errors: Read/write access to the process image is blocked, and/or SFC 14/15 is no longer able to perform any read/write access operations.

Example:

The example of the process image partition 3 "PIP 3" below shows a possible configuration in HW Config:

- PIP 3 at output: Those 50 bytes are stored consistently in process image partition 3 (drop down list box "Consistent over > Total length"), and can thus be read by means of standard "Load input xy" commands.
- Selecting "Process image -> ---" under Input in the drop down list box means: no storage in a process image. You must work with the system functions SFC14/15.

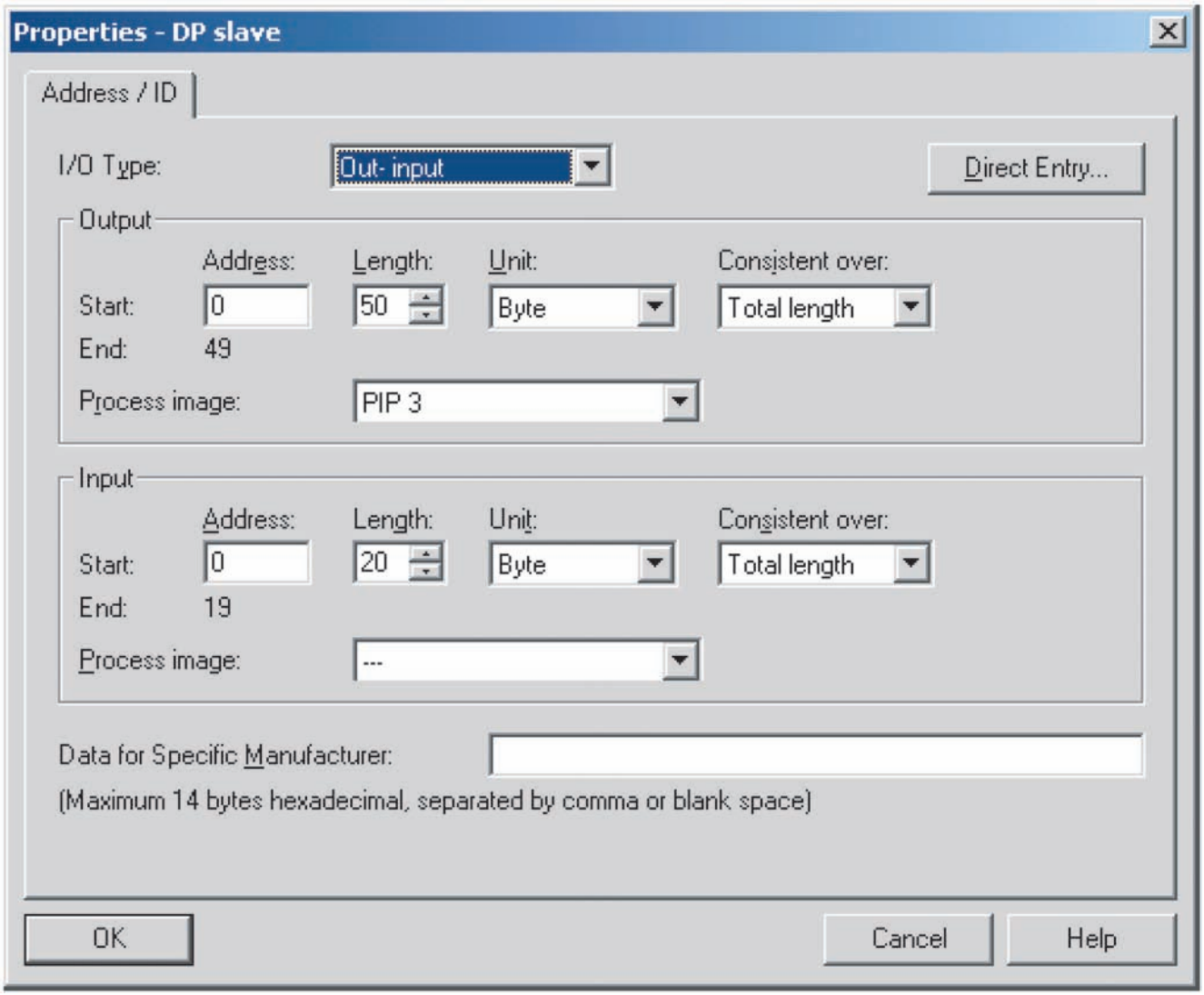


Figure 7-3 Properties - DP slave

System and operating states of the S7–400H 8

8.1 System and operating states of the S7–400H

This chapter features an introduction to the subject of S7-400H fault-tolerant systems.

You will learn the basic terms that are used in describing how fault-tolerant systems operate.

Following that, you will receive information on fault-tolerant system states. They depend on the operating states of the different fault-tolerant CPUs, which will be described in the next section.

In describing these operating states, this section concentrates on the behavior that differs from a standard CPU. You will find a description of the standard behavior of a CPU in the corresponding operating mode in the *Programming with STEP 7* manual.

The final section provides details on the modified time response of fault-tolerant CPUs.

8.2 Introduction

The S7-400H consists of two redundantly configured subsystems that are synchronized via fiber-optic cables.

Both subsystems create a fault-tolerant automation system operating with a two-channel (1-out-of-2) structure based on the "active redundancy" principle.

What does active redundancy mean?

Active redundancy means that all redundant resources are constantly in operation and simultaneously involved in the execution of the control task.

For the S7-400H this means that the user programs in both CPUs are identical and executed synchronously by the CPUs.

Convention

To identify the two subsystems, we use the traditional expressions of "master" and "reserve" for dual-channel fault-tolerant systems in this description. The reserve always processes events in synchronism with the master, and does not explicitly wait for any errors before doing so.

The distinction made between the master and reserve CPUs is primarily important for ensuring reproducible error reactions. For example, the reserve CPU may go into STOP when the redundant link fails, while the master CPU remains in RUN.

Master/reserve assignment

When the S7-400H is initially switched on, the CPU that started up first assumes master mode, and the partner CPU assumes reserve mode.

The preset master/reserve assignment is retained when both CPUs power up simultaneously.

The master/reserve assignment changes when:

1. The reserve CPU starts up before the master CPU (interval of at least 3 s)
2. The master CPU fails or goes into STOP in redundant system mode
3. No error was found in ERROR-SEARCH mode (see also section ERROR-SEARCH mode (Page 90))

Synchronizing the subsystems

The master and reserve CPUs are linked by fiber-optic cables. Both CPUs maintain event-synchronous program execution via this connection.

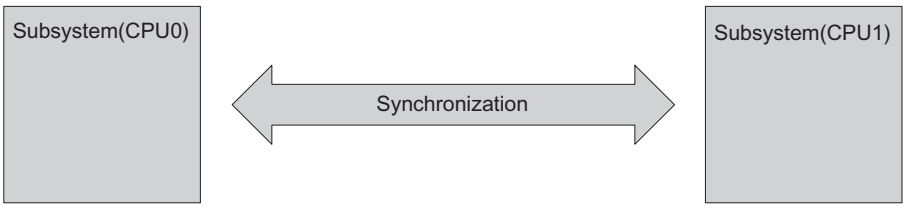


Figure 8-1 Synchronizing the subsystems

Synchronization is performed automatically by the operating system and has no effect on the user program. You create your program in the same way as for standard S7-400 CPUs.

Event-driven synchronization procedure

The "event-driven synchronization" procedure patented by Siemens was used for the S7-400H. This procedure has proved itself in practice and has already been used for the S5-115H and S5-155H controllers.

Event-driven synchronization means that the master and reserve always synchronize their data when an event occurs which may lead to different internal states of the subsystems.

The master and reserve CPUs are synchronized when:

- There is direct access to the I/O
- Interrupts occur
- User timers (e.g. S7 timers) are updated
- Data is modified by communication functions

Continued bumpless operation even if redundancy of a CPU is lost

The event-driven synchronization method ensures bumpless continuation of operation by the reserve CPU even if the master CPU fails.

Self-test

Malfunctions or errors must be detected, localized and reported as quickly as possible. Consequently, extensive self-test functions have been implemented in the S7-400H that run automatically and entirely in the background.

The following components and functions are tested:

- Coupling of the central racks
- Processor
- Internal memory of the CPU
- I/O bus

If the self-test detects an error, the fault-tolerant system tries to eliminate it or to suppress its effects.

For detailed information on the self-test, refer to section Self-test (Page 91).

8.3 The system states of the S7-400H

The system states of the S7-400H result from the operating states of the two CPUs. The term "system state" is used as a simplified term which identifies the concurrent operating states of the two CPUs.

Example: Instead of "the master CPU is in RUN and the reserve CPU is in LINK-UP mode" we say "the S7-400H system is in link-up mode".

Overview of system states

The table below provides an overview of the possible states of the S7-400H system.

Table 8- 1 Overview of S7-400H system states

System states of the S7–400H	Operating states of the two CPUs	
	Master	Reserve
Stop	STOP	STOP, power off, DEFECTIVE
Start-up	STARTUP	STOP, power off, DEFECTIVE, no synchronization
Single mode	RUN	STOP, ERROR-SEARCH, power off, DEFECTIVE, no synchronization
Link-up	RUN	STARTUP, LINK-UP
Update	RUN	UPDATE
Redundant	RUN	RUN
Hold	HOLD	STOP, ERROR-SEARCH, power off, DEFECTIVE, no synchronization

8.4 The operating states of the CPUs

Operating states describe the behavior of the CPUs at any given point in time. Knowledge of the operating states of the CPUs is useful for programming the startup, test, and error diagnostics.

Operating states from POWER ON to redundant system mode

Generally speaking, the two CPUs enjoy equal rights so that either can be the master or the reserve CPU. For reasons of legibility, the illustration presumes that the master CPU (CPU 0) is started up before the reserve CPU (CPU 1) is switched on.

The following figure shows the operating states of the two CPUs, from POWER ON to redundant system mode. The HOLD HOLD mode (Page 89) and ERROR-SEARCH ERROR-SEARCH mode (Page 90) modes are special modes and are not shown.

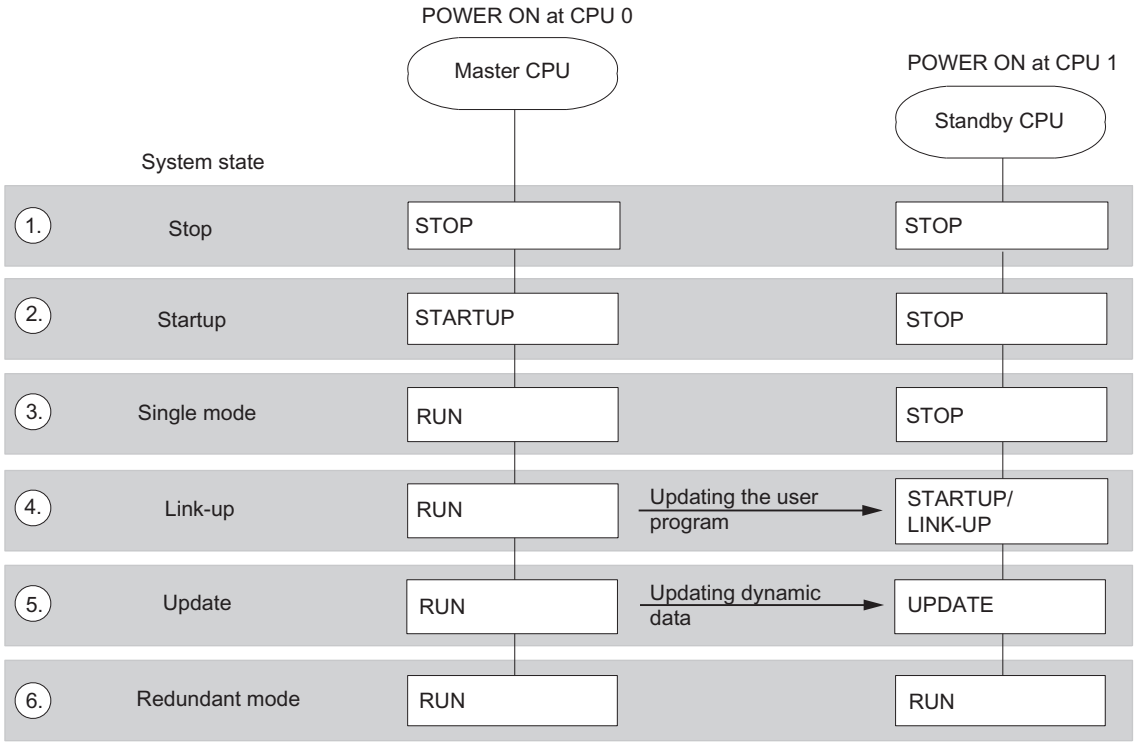


Figure 8-2 System and operating states of the fault-tolerant system

Explanation of the figure

Point	Description
1.	After the power supply has been turned on, the two CPUs (CPU 0 and CPU 1) are in STOP mode.
2.	CPU 0 changes to STARTUP and executes OB 100 or OB 102 according to the startup mode; see also section STARTUP mode (Page 87).
3.	If startup is successful, the master CPU (CPU 0) changes to single mode. The master CPU executes the user program alone. At the transition to the LINK-UP system mode, no block may be opened by the "Monitor" option, and no variable table may be active.
4.	If the reserve CPU (CPU 1) requests LINK-UP, the master and reserve CPUs compare their user programs. If any differences are found, the master CPU updates the user program of the reserve CPU, see also section LINK-UP and UPDATE modes (Page 87).
5.	After a successful link-up, updating is started, see section Update sequence (Page 103). The master CPU updates the dynamic data of the reserve CPU. Dynamic data are inputs, outputs, timers, counters, bit memories, and data blocks. Following the update, the memories of both CPUs have the same content, see also section LINK-UP and UPDATE modes (Page 87).
6.	The master and reserve CPUs are in RUN mode after the update. Both CPUs process the user program synchronized with each other. Exception: Master/reserve changeover for configuration/program modifications. The redundant system mode is only supported with CPUs of the same version and firmware version.

8.4.1 STOP mode

Except for the additions described below, the behavior of S7-400H CPUs in STOP mode corresponds to that of standard S7-400 CPUs.

When you download a configuration to one of the CPUs while both are in STOP mode, observe the points below:

- Start the CPU to which you downloaded the configuration first in order to set it up for master mode.
- By initiating the system startup request on the programming device, you first start the CPU to which an active connection exists, regardless of the master or reserve status.

NOTICE
A system startup may trigger a master–reserve changeover.

Memory reset

The memory reset function affects only the selected CPU. To reset both CPUs, you must reset one and then the other.

8.4.2 STARTUP mode

Except for the additions described below, the behavior of S7-400H CPUs in STARTUP mode corresponds to that of standard S7-400 CPUs.

Startup modes

The fault-tolerant CPUs distinguish between cold restart and warm restart.

Fault-tolerant CPUs do not support warm restarts.

Startup processing by the master CPU

The startup system mode of an S7-400H is always processed by the master CPU.

During STARTUP, the master CPU compares the existing I/O configuration with the hardware configuration that you created in STEP 7. If any differences are found, the master CPU reacts in the same way as a standard S7-400 CPU.

The master CPU checks and parameterizes the following:

- the switched I/O
- its assigned one-sided I/O

Startup of the reserve CPU

The reserve CPU startup routine does not call an OB 100 or OB 102.

The reserve CPU checks and parameterizes the following:

- its assigned one-sided I/O

Additional information

For detailed information on STARTUP mode, refer to the *Programming with STEP 7* manual.

8.4.3 LINK-UP and UPDATE modes

The master CPU checks and updates the memory content of the reserve CPU before the fault-tolerant system assumes redundant system mode. This is implemented in two successive phases: connect and update.

The master CPU is always in RUN mode and the reserve CPU is in CONNECT or UPDATE mode during the connect and update phases.

In addition to the connect and update functions, which are carried out to establish redundant system mode, the system also supports linking and updating in combination with master/reserve changeover.

For detailed information on connect and updating, refer to section Link-up and update (Page 95).

8.4.4 RUN mode

Except for the additions described below, the behavior of S7-400H CPUs in RUN mode corresponds to that of standard S7-400 CPUs.

The user program is executed by at least one CPU in the following system states:

- Single mode
- Link-up, update
- Redundant

Single mode, link-up, update

In the system states mentioned above, the master CPU is in RUN and executes the user program in single mode.

Redundant system mode

The master CPU and reserve CPU are always in RUN when operating in redundant system mode. Both CPUs execute the user program in synchronism, and perform mutual checks.

In redundant system mode it is not possible to test the user program with breakpoints.

The redundant system mode is only supported with CPUs of the same version and firmware version. Redundancy will be lost if one of the errors listed in the following table occurs.

Table 8- 2 Causes of error leading to redundancy loss

Cause of error	Reaction
Failure of one CPU	Failure and replacement of a CPU (Page 197)
Failure of the redundant link (synchronization module or fiber-optic cable)	Failure and replacement of a synchronization module or fiber-optic cable (Page 204)
RAM comparison error	ERROR-SEARCH mode (Page 90)

Redundant use of modules

The following rule applies to the redundant system mode:

Modules interconnected in redundant mode (e.g. DP slave interface module IM 153-2) must be in identical pairs, i.e. the two redundant linked modules have the same order number and product or firmware version.

8.4.5 HOLD mode

Except for the additions described below, the behavior of the S7-400H CPU in HOLD mode corresponds to that of a standard S7-400 CPU.

The HOLD mode has an exceptional role, as it is used only for test purposes.

When is the HOLD mode possible?

A transition to HOLD is only available during STARTUP and in RUN in single mode.

Properties

- Link-up and update operations are not available while the fault-tolerant CPU is in HOLD mode; the reserve CPU remains in STOP and outputs a diagnostics message.
- It is not possible to set breakpoints when the fault-tolerant system is in redundant system mode.

8.4.6 ERROR-SEARCH mode

The ERROR-SEARCH mode can only be adopted from the redundant system mode. During troubleshooting, the redundant system mode is exited, the other CPU can become master and continue to work in single mode.

Note

If the master CPU changes to STOP during troubleshooting, the troubleshooting is continued on the reserve CPU. However, once troubleshooting is completed, the reserve CPU does not start up again.

The self-test routine compares the master and reserve CPUs, and reports an error if any differences are found. Errors could be caused by hardware faults, checksum errors and RAM/POI comparison errors.

The following events will trigger ERROR-SEARCH mode:

1. If a one-sided call of OB 121 (on only one CPU) occurs in redundant mode, the CPU assumes a hardware fault and enters ERROR-SEARCH mode. The partner CPU assumes master mode as required, and continues operation in single mode.
2. If a checksum error occurs on only one CPU in redundant mode, that CPU enters ERROR-SEARCH mode. The partner CPU assumes master mode as required, and continues operation in single mode.
3. If a RAM/POI comparison error is detected in redundant mode, the reserve CPU enters ERROR-SEARCH mode (default response), and the master CPU continues operation in single mode.

   The response to RAM/POI comparison errors can be modified in the configuration (for example, the reserve CPU goes into STOP).
4. If a multiple-bit error occurs on a CPU in redundant mode, that CPU will enter ERROR-SEARCH mode. The partner CPU assumes master mode as required, and continues operation in single mode.

   But: OB 84 is called when a single-bit error occurs on a CPU in redundant mode. The CPU does not change to ERROR-SEARCH mode.
5. If synchronization is lost during redundant mode, the reserve CPU changes to ERROR-SEARCH mode. The other CPU remains master and continues operation in single mode.

The purpose of ERROR-SEARCH mode is to find a faulty CPU. The reserve CPU runs the full self-test, while the master CPU remains in RUN.

If a hardware fault is detected, the CPU changes to DEFECTIVE mode. If no fault is detected the CPU is linked up again. The fault-tolerant system resumes the redundant system mode. An automatic master-reserve changeover then takes place. This ensures that when the next error is detected in error-search mode, the hardware of the previous master CPU is tested.

No communication is possible with the CPU in ERROR-SEARCH mode, e.g. no access by a programming device is possible. The ERROR-SEARCH mode is indicated by the RUN and STOP LEDs, see section Status and error displays (Page 45).

For additional information on the self-test, refer to section Self-test (Page 91)

8.5 Self-test

Processing the self-test

The CPU executes the complete self-test program after POWER ON without backup, e.g. POWER ON after initial insertion of the CPU or POWER ON without backup battery, and in the ERROR-SEARCH mode.

The self-test takes at least 10 minutes. The larger the load memory used (e.g. the size of the inserted RAM memory card), the longer the self-test.

When the CPU of a fault-tolerant system requests a memory reset and is then shut down with backup power, it performs a self-test even though it was backed up. The CPU requests a memory reset when you remove the memory card, for example.

In RUN the operating system splits the self-test routine into several small program sections ("test slices") which are processed in multiple successive cycles. The cyclic self-test is organized to perform a single, complete pass in a certain time. The default time of 90 minutes can be modified in the configuration.

Response to errors during the self-test

If the self-test returns an error, the following happens:

Table 8- 3 Response to errors during the self-test

Type of error	System response
Hardware fault without one-sided call of OB 121	The faulty CPU enters the DEFECTIVE state. The fault-tolerant system switches to single mode. The cause of the error is written to the diagnostic buffer.
Hardware fault with one-sided call of OB 121	The CPU with the one-sided OB 121 enters ERROR-SEARCH mode. The fault-tolerant system switches to single mode (see below).
RAM/POI comparison error	The cause of the error is written to the diagnostic buffer. The CPU enters the configured system or operating state (see below).
Checksum errors	The response depends on the error situation (see below).
Multiple-bit errors	The faulty CPU enters ERROR-SEARCH mode.

Hardware fault with one-sided call of OB 121

If a hardware fault occurs with a one-sided OB 121 call for the first time since the previous POWER ON without backup, the faulty CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to single mode. The cause of the error is written to the diagnostic buffer.

RAM/POI comparison error

If the self-test returns a RAM/POI comparison error, the fault-tolerant system quits redundant mode and the reserve CPU enters ERROR-SEARCH mode (in default configuration). The cause of the error is written to the diagnostic buffer.

The response to a recurring RAM/POI comparison error depends on whether the error occurs in the subsequent self-test cycle after troubleshooting or not until later.

Table 8- 4 Response to a recurring comparison error

Comparison error recurs ...	Reaction
in the first self-test cycle after troubleshooting	The reserve CPU first enters ERROR-SEARCH mode, and then goes into STOP. The fault-tolerant system switches to single mode.
after two or more self-test cycles after troubleshooting	Reserve CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to single mode.

Checksum errors

When a checksum error occurs for the first time after the last POWER ON without backup, the system reacts as follows:

Table 8- 5 Reaction to checksum errors

Time of detection	System response
During the startup test after POWER ON	The faulty CPU enters the DEFECTIVE state. The fault-tolerant system switches to single mode.
In the cyclic self-test (STOP or single mode)	The error is corrected. The CPU remains in STOP or in single mode.
In the cyclic self-test (redundant system mode)	The error is corrected. The faulty CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to single mode.
In the ERROR-SEARCH mode	The faulty CPU enters the DEFECTIVE state.
Single-bit errors	The CPU calls OB 84 after detection and elimination of the error.

The cause of the error is written to the diagnostic buffer.

In an F system, the F program is informed that the self-test has detected an error the first time a checksum error occurs in STOP or single mode. The reaction of the F program to this is described in the *S7-400F and S7-400FH Automation Systems* manual.

Hardware fault with one-sided call of OB 121, checksum error, second occurrence

A CPU 41x–4H reacts to a second occurrence of a hardware fault with a one-sided call of OB 121 and to checksum errors as set out in the table below, based on the various operating modes of the CPU 41x–4H.

Table 8- 6 Hardware fault with one-sided call of OB 121, checksum error, second occurrence

Error	CPU in single mode	CPU in stand-alone mode	CPU in redundant mode
Hardware fault with one-sided call of OB 121	OB 121 is executed	OB 121 is executed	The faulty CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to single mode.
Checksum errors	The CPU enters the DEFECTIVE state if two errors occur within two successive test cycles (configure the length of the test cycle in HW Config).	The CPU enters the DEFECTIVE state if two errors occur within two successive test cycles (configure the length of the test cycle in HW Config).	The CPU enters the DEFECTIVE state if a second error triggered by the first error event occurs in ERROR-SEARCH mode.

If a second checksum error occurs in single/stand-alone mode after twice the test cycle time has expired, the CPU reacts as it did on the first occurrence of the error. If a second error (hardware fault with one-sided call of OB 121, checksum error) occurs in redundant mode when troubleshooting is finished, the CPU reacts as it did on the first occurrence of the error.

Multiple-bit errors

The CPU changes to ERROR-SEARCH mode when a multiple-bit error is detected while the fault-tolerant system is operating in redundant mode. When troubleshooting is finished, the CPU can automatically connect and update itself, and resume redundant operation. At the transition to error-search mode, the address of the errors is reported in the diagnostic buffer.

Single-bit errors

The CPU calls OB 84 after detection and elimination of the error.

Influencing the cyclic self-test

SFC 90 "H_CTRL" allows you to influence the scope and execution of the cyclic self-test. For example, you can remove various test components from the overall test and re-introduce them. In addition, you can explicitly call and process specific test components.

For detailed information on SFC 90 "H_CTRL", refer to the *System Software for S7-300/400, System and Standard Functions* manual.

NOTICE
In a fail-safe system, you are not allowed to disable and then re-enable the cyclic self-tests. For more details, refer to the *S7-400F and S7-400FH Automation Systems* manual.

8.6 Time response

Instruction run times

You will find the execution times of the STEP 7 commands in the instruction list for the S7-400 CPUs.

Processing direct I/O access

Please note that any I/O access requires a synchronization of the two units and thus extends the cycle time.

You should therefore avoid direct I/O access in your user program, and instead access using process images (or process image partitions, e.g. for watchdog interrupts). This automatically increases performance, because in process images you can synchronize a whole set of values at once.

Response time

For detailed information on calculating response times, refer to section S7-400 cycle and response times (Page 277).

Note that any update of the reserve CPU extends the alarm response time.

The alarm response time depends on the priority class, because a graduated delay of the interrupts is performed during an update.

8.7 Evaluation of hardware interrupts in the S7-400H system

When using a hardware interrupt-triggering module in the S7-400H system, it is possible that the process values which can be read from the hardware interrupt OB by direct access do not match the process values valid at the time of the interrupt. Evaluate the temporary variables (start information) in the hardware interrupt OB instead.

When using the process interrupt-triggering module SM 321-7BH00, it is not advisable to have different responses to rising or falling edges at the same input, because this would require direct access to the I/O. If you want to respond differently to the two edge changes in your user program, assign the signal to two inputs from different channel groups and parameterize one input for the rising edge and the other for the falling edge.

Link-up and update

9

9.1 Effects of link-up and updating

Link-up and updating are indicated by the REDF LEDs on the two CPUs. During link-up, the LEDs flash at a frequency of 0.5 Hz, and when updating at a frequency of 2 Hz.

Link-up and update have various effects on user program execution and on communication functions.

Table 9- 1 Properties of link-up and update functions

Process	Link-up	Update
Execution of the user program	All priority classes (OBs) are processed.	Processing of the priority classes is delayed section by section. All requests are caught up with after the update. For details, refer to the sections below.
Deleting, loading, generating, and compressing of blocks	Blocks cannot be deleted, loaded, created or compressed. When such actions are busy, link-up and update operations are inhibited.	Blocks cannot be deleted, loaded, created or compressed.
Execution of communication functions, PG operation	Communication functions are executed.	Execution of the functions is restricted section by section and delayed. All the delayed functions are caught up with after the update. For details, refer to the sections below.
CPU self-test	Not performed	Not performed
Test and commissioning functions, such as "Monitor and modify variable", "Monitor (On/Off)"	Test and commissioning functions are disabled. When such actions are busy, link-up and update operations are inhibited.	Test and commissioning functions are disabled.
Handling of the connections on the master CPU	All connections are retained; no new connections can be made.	All connections are retained; no new connections can be made. Interrupted connections are not restored until the update is completed
Handling of the connections on the reserve CPU	All the connections are cancelled; no new connections can be made.	All connections are already down. They were cancelled during link-up.

9.2 Conditions for link-up and update

Which commands you can use on the programming device to initiate a link-up and update operation is determined by the current conditions on the master and reserve CPU. The table below shows the correlation between those conditions and available programming device commands for link-up and update operations.

Table 9- 2 Conditions for link-up and update

Link-up and update as PG command:	Size and type of load memory in the master and reserve CPUs	FW version in the master and reserve CPUs	Available sync connections	Hardware version on master and reserve CPU
Restart of the reserve	Are identical	Are identical	2	Are identical
Switch to CPU with modified configuration	RAM and EPROM mixed	Are identical	2	Are identical
Switchover to CPU with expanded memory configuration	Size of load memory in the reserve CPU is larger than that of the master	Are identical	2	Are identical
Switchover to CPU with modified operating system	Are identical	Are different	2	Are identical
CPUs with changed hardware version	Are identical	Are identical	2	Are different
Only one synchronization link-up is available over only one intact redundant link	Are identical	Are identical	1	Are identical

9.3 Link-up and update sequence

There are two types of link-up and update operation:

- Within a "normal" link-up and update operation, the fault-tolerant system should change over from single mode to redundant mode. The two CPUs then process the same program synchronized with each other.
- When the CPUs link up and update with master/reserve changeover, the second CPU with modified components can assume control over the process. Either the hardware configuration, or the memory configuration, or the operating system may have been modified.

  In order to return to redundant system mode, a "normal" link-up and update operation must be performed subsequently.

How to start the link-up and update operation?

Initial situation: Single mode, i.e. only one of the CPUs of a fault-tolerant system connected via fiber-optic cables is in RUN.

To establish system redundancy, initiate the link-up and update operation as follows:

- Toggle the mode selector switch of the reserve CPU from STOP to RUN.
- POWER ON the reserve (mode selector in RUN position) if prior to POWER OFF the CPU was not in STOP mode.
- Operator input on the PG/ES.

A link-up and update operation with master/reserve changeover is always started on the PG/ES.

NOTICE
If a link-up and update operation is interrupted on the reserve CPU (for example due to POWER OFF, STOP), this may cause data inconsistency and lead to a memory reset request on this CPU. The link-up and update functions are possible again after a memory reset on the reserve.

Flow chart of the link-up and update operation

The figure below outlines the general sequence of the link-up and update. In the initial situation, the master is operating in single mode. In the figure, CPU 0 is assumed to be the master.

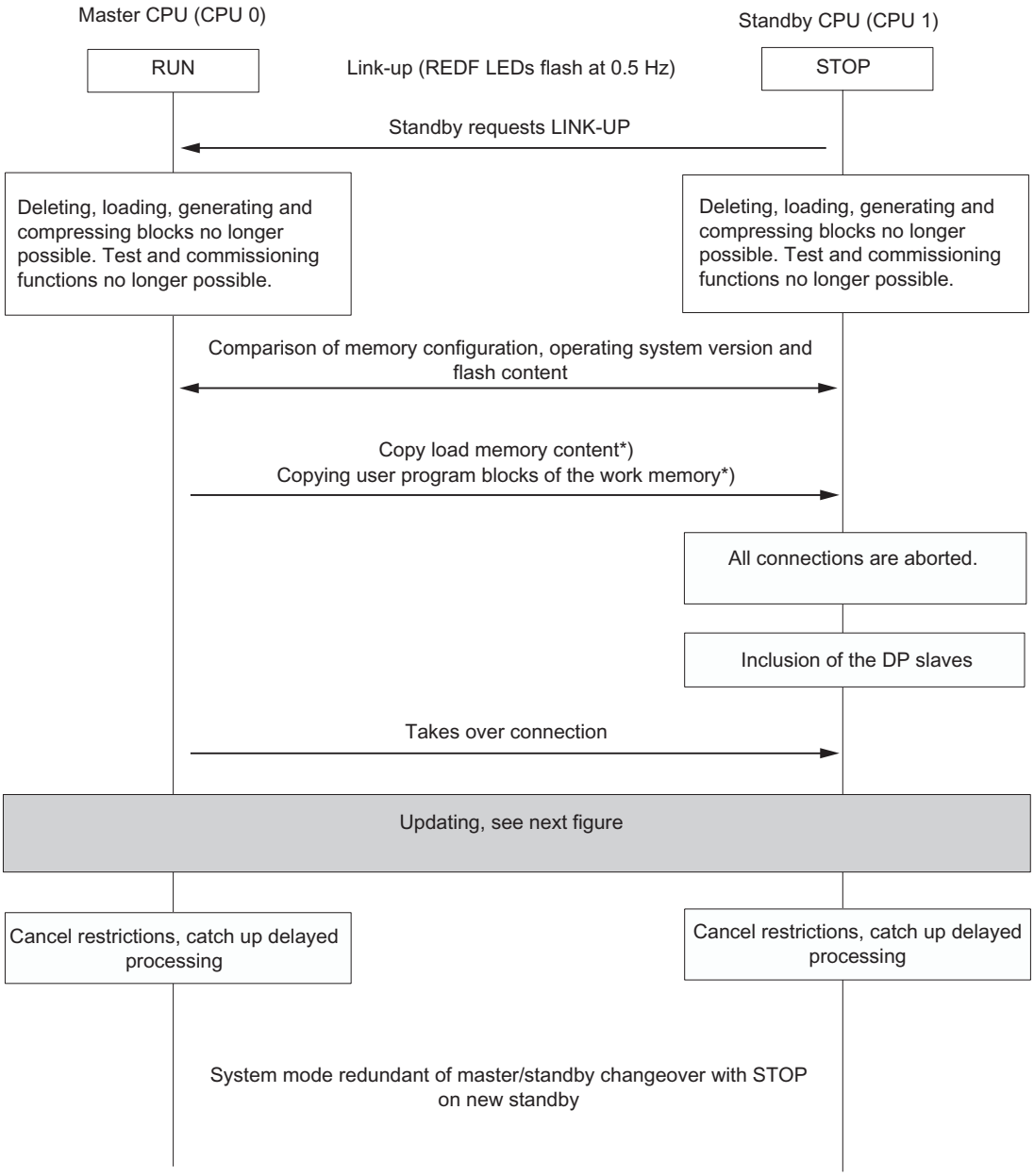


Figure 9-1 Sequence of link-up and update

*) If the "Switchover to CPU with altered configuration" option is set, the content of the load memory is not copied; what is copied from the user program blocks of the work memory (OBs, FCs, FBs, DBs, SDBs) of the master CPU is listed in section Switch to CPU with modified configuration or expanded memory configuration (Page 106)

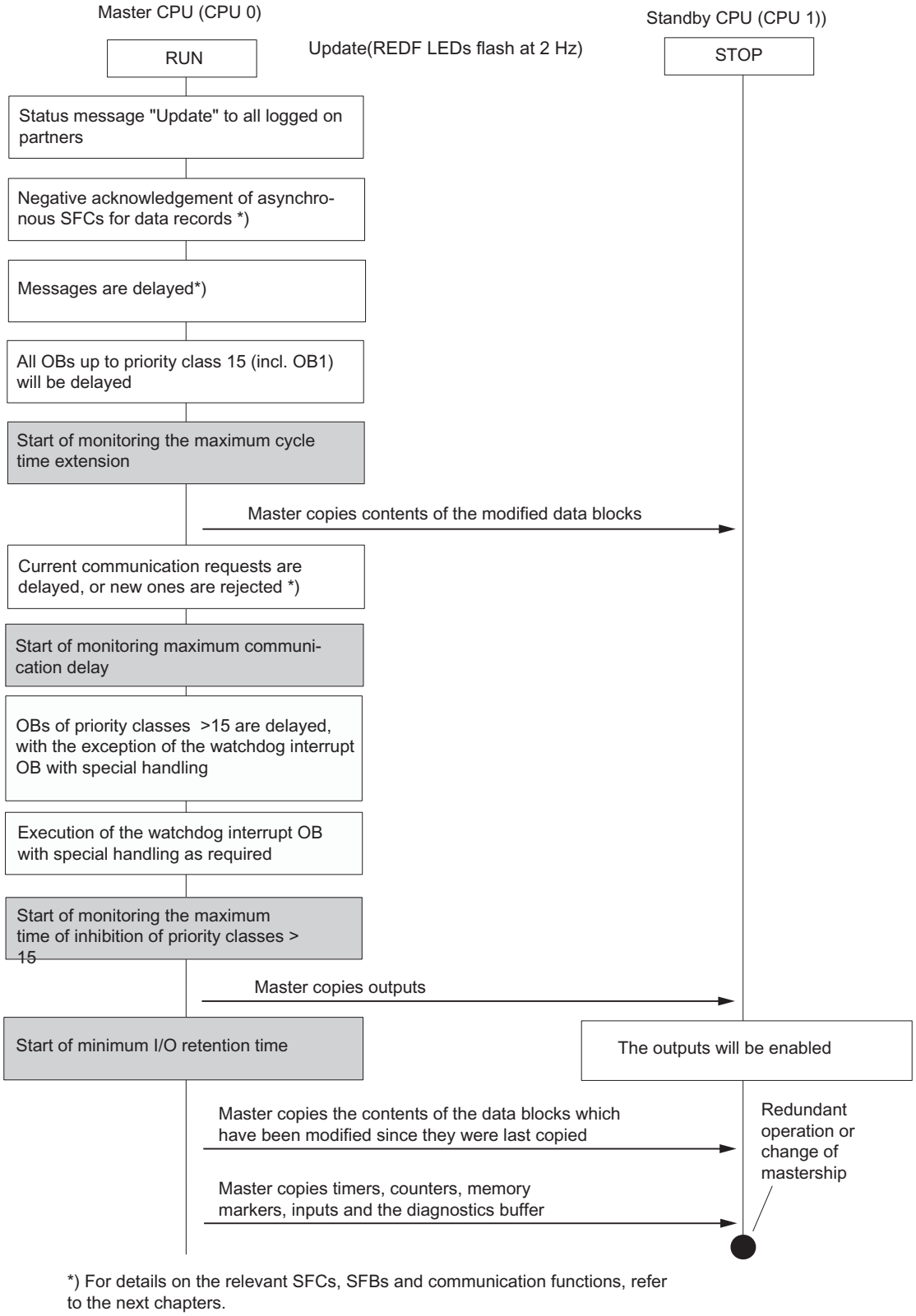


Figure 9-2 Update sequence

Minimum duration of input signals during update

Program execution is stopped for a certain time during the update (the sections below describe this in greater detail). To ensure that the CPU can reliably detect changes to input signals during the update, the following condition must be satisfied:

Min. signal duration > 2 x the time required for I/O update (DP only)
+ call interval of the priority class
+ program execution time of the priority class
+ time required for the update
+ program execution time of higher-priority classes

Example:

Minimum signal duration of an input signal that is evaluated in a priority class > 15 (e.g. OB 40).

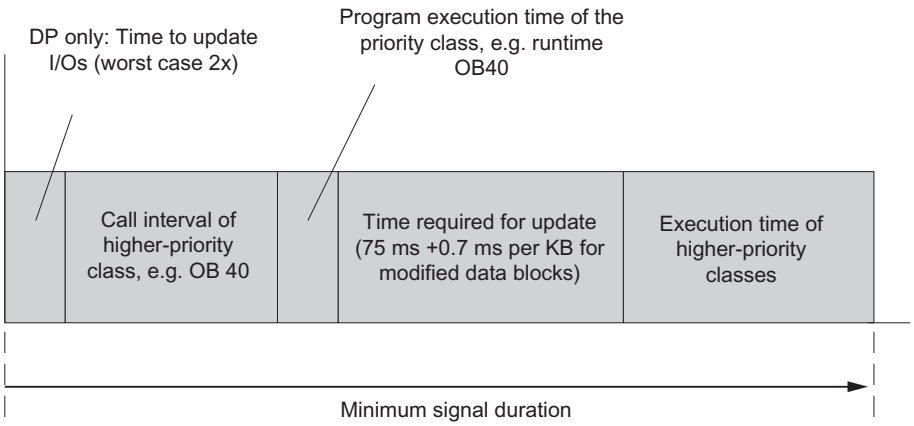


Figure 9-3 Example of minimum signal duration of an input signal during the update

9.3.1 Link-up sequence

For the connect sequence, you need to decide whether to carry out a master/reserve changeover, or whether redundant system mode is to be achieved after that.

Connect with the objective of setting up system redundancy

To exclude differences in the two subsystems, the master and the reserve CPU run the following comparisons.

The following are compared:

1. Consistency of the memory configuration
2. Consistency of the operating system version
3. Consistency of the load memory (FLASH card) content
4. Consistency of load memory (integrated RAM and RAM card) content

If 1., 2., or 3. are inconsistent, the reserve CPU changes to STOP mode and outputs an error message.

If 4. is inconsistent, the master CPU copies the user program from its load memory in RAM to the reserve CPU.

The user program stored in load memory on the FLASH card is not transferred.
It must be identical before initiating connect.

Connect with master/reserve changeover

In STEP 7 you can select one of the following options:

- "Switch to CPU with modified configuration"
- "Switchover to CPU with expanded memory configuration"
- "Switchover to CPU with modified operating system"
- "Switchover to CPU with modified hardware version"
- "Switchover to CPU via only one intact redundant link"

Switch to CPU with modified configuration

You may have modified the following elements on the reserve CPU:

- The hardware configuration
- The type of load memory (for example, you have replaced a RAM card with a FLASH card). The new load memory may be larger or smaller than the old one.

The master does not transfer any blocks to the reserve during the connect. For detailed information, refer to section Switch to CPU with modified configuration or expanded memory configuration (Page 106).

For information on the required steps based on the scenarios described above (alteration of the hardware configuration, or of the type of load memory), refer to section Failure and replacement of components during operation (Page 197).

Note

Even though you have not modified the hardware configuration or the type of load memory on the reserve CPU, there is nevertheless a master/reserve changeover and the previous master CPU changes to STOP.

Switchover to CPU with expanded memory configuration

You may have expanded the load memory on the reserve CPU. The memory media for storing load memory must be identical, i.e. either RAM cards or FLASH cards. The contents of FLASH cards must be identical.

During the connect, the user program blocks (OBs, FCs, FBs, DBs, SDBs) of the master are transferred from the load memory and work memory to the reserve. Exception: If the load memory modules are FLASH cards, the system only transfers the blocks from work memory.

For information on changing the type of memory or on load memory expansions, refer to section Changing the CPU memory configuration (Page 255).

NOTICE
Assuming you have implemented a different type of load memory or operating system on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer. Assuming you have not expanded load memory on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer. The system does not perform a master/reserve changeover, and the previous master CPU remains in RUN.

9.3.2 Update sequence

What happens during updating?

The execution of communication functions and OBs is restricted section by section during updating. Likewise, all the dynamic data (content of the data blocks, timers, counters, and bit memories) are transferred to the reserve CPU.

Update procedure:

1. Until the update is completed, all asynchronous SFCs which access data records of I/O modules (SFCs 13, 51, 52, 53, 55 to 59) are acknowledged as "negative" with the return values W#16#80C3 (SFCs 13, 55 to 59) or W#16#8085 (SFC 51). When these values are returned, the jobs should be repeated by the user program.
2. Message functions are delayed until the update is completed (see list below).
3. The execution of OB 1 and of all OBs up to priority class 15 is delayed.

   In the case of watchdog interrupts, the generation of new OB requests is disabled, so no new watchdog interrupts are stored and as a result no new request errors occur.

   The system waits until the update is completed, and then generates and processes a maximum of one request per watchdog interrupt OB. The time stamp of delayed watchdog interrupts cannot be evaluated.
4. Transfer of all data block contents modified since link-up.
5. The following communication jobs are acknowledged negatively:
   - Reading/writing of data records using HMI functions
   - Reading diagnostic information using STEP 7
   - Disabling and enabling messages
   - Logon and logoff for messages
   - Acknowledgement of messages
6. Initial calls of communication functions are acknowledged negatively. These calls manipulate the work memory, see also *System Software for S7-300/400, System and Standard Functions*. All remaining communication functions are executed with delay, after the update is completed.
7. The system disables the generation of new OB requests for all OBs of priority class > 15, so new interrupts are not saved and as a result do not generate any request errors.

   Queued interrupts are not requested again and processed until the update is completed. The time stamp of delayed interrupts cannot be evaluated.

   The user program is no longer processed and there are no more I/O updates.

8. Generation of the start event for the watchdog interrupt OB with special handling if its priority class is > 15, and execution of this OB as required.

   Note

   The watchdog interrupt OB with special handling is particularly important in situations where you need to address certain modules or program parts within a specific time. This is a typical scenario in fail-safe systems. For details, refer to the *S7-400F and S7-400FH Automation Systems* and *S7-300 Automation Systems, Fail-safe Signal Modules* manuals.

9. Transfer of outputs and of all data block contents modified again. Transfer of timers, counters, bit memories, and inputs. Transfer of the diagnostic buffer.

   During this data synchronization, the system interrupts the clock pulse for watchdog interrupts, time-delay interrupts and S7 timers. This results in the loss of any synchronism between cyclic and time-of-day interrupts.

10. Cancel all restrictions. Delayed interrupts and communication functions are executed. All OBs are executed again.

    A constant bus cycle time compared with previous calls can no longer be guaranteed for delayed watchdog interrupt OBs.

    Note

    Process and diagnostic interrupts are stored by the I/O. Such interrupt requests issued by distributed I/O modules are executed when the block is re-enabled. Any such requests by central I/O modules can only be executed provided the same interrupt request did not occur repeatedly while the status was disabled.

If the PG/ES requested a master/reserve changeover, the previous reserve CPU assumes master mode and the previous master CPU goes into STOP when the update is completed. Both CPUs will otherwise go into RUN (redundant system mode) and execute the user program in synchronism.

When there is a master/reserve changeover, in the first cycle after the update OB 1 is assigned a separate identifier (see *System Software for S7-300/400, System and Standard Functions* Reference Manual). For information on other aspects resulting from modifying the configuration, refer to section Switch to CPU with modified configuration or expanded memory configuration (Page 106).

Delayed message functions

The listed SFCs, SFBs and operating system services trigger the output of messages to all logged-on partners. These functions are delayed after the start of the update:

- SFC 17 "ALARM_SQ", SFC 18 "ALARM_S", SFC 107 "ALARM_DQ", SFC 108 "ALARM_D"
- SFC 52 "WR_USMSG"
- SFB 31 "NOTIFY_8P", SFB 33 "ALARM", SFB 34 "ALARM_8", SFB 35 "ALARM_8P", SFB 36 "NOTIFY", SFB 37 "AR_SEND"
- Process control messages
- System diagnostics messages

From this time on, any requests to enable and disable messages by SFC 9 "EN_MSG" and SFC 10 "DIS_MSG" are rejected with a negative return value.

Communication functions and resulting jobs

After it has received one of the jobs specified below, the CPU must in turn generate communication jobs and output them to other modules. These include, for example, jobs for reading or writing parameterization data records from/to distributed I/O modules. These jobs are rejected until the update is completed.

- Reading/writing of data records using HMI functions
- Reading data records using SSL information
- Disabling and enabling messages
- Logon and logoff for messages
- Acknowledgement of messages

Note

The last three of the functions listed are registered by a WinCC system, and automatically repeated when the update is completed.

9.3.3 Switch to CPU with modified configuration or expanded memory configuration

Switch to CPU with modified configuration

You may have modified the following elements on the reserve CPU:

- The hardware configuration
- The type of load memory. You may have replaced a RAM card with a FLASH card, for example. The new load memory may be larger or smaller than the old one.

For information on steps required in the scenarios mentioned above, refer to section Failure and replacement of components during operation (Page 197).

Note

Even though you have not modified the hardware configuration or the type of load memory on the reserve CPU, there is nevertheless a master/reserve changeover and the previous master CPU changes to STOP.

Note

If you have downloaded connections using NETPRO, you can no longer change the memory type of the load memory from RAM to FLASH.

When you initiate a connect and update operation with the "Switch to CPU with modified configuration" option in STEP 7, the system reacts as follows with respect to handling of the memory contents.

Load memory

The contents of the load memory are not copied from the master to the reserve CPU.

Work memory

The following components are transferred from the work memory of the master CPU to the reserve CPU:

- Contents of all data blocks assigned the same interface time stamp in both load memories and whose attributes "read only" and "unlinked" are not set.
- Data blocks generated in the master CPU by SFCs.

  The DBs generated in the reserve CPU by means of SFC are deleted.

  If a data block with the same number is also found in the load memory of the reserve CPU, connect is cancelled with an entry in the diagnostic buffer.
- Process images, timers, counters, and bit memories

If there is insufficient memory, connect is cancelled with an entry in the diagnostic buffer.

The status of SFB instances of S7 communication contained in modified data blocks is restored to the status prior to their initial call.

Note

When changing over to a CPU with modified configuration, the size of load memories in the master and reserve may be different.

Switchover to CPU with expanded memory configuration

You may have expanded the load memory on the reserve CPU. The memory media for storing load memory must be identical, i.e. either RAM cards or FLASH cards. The contents of FLASH cards must be identical.

NOTICE
Assuming you have implemented a different type of load memory or operating system on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer. Assuming you have not expanded load memory on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer. The system does not perform a master/reserve changeover, and the previous master CPU remains in RUN.

For information on changing the type of memory or on load memory expansions, refer to section Failure and replacement of components during operation (Page 197).

When you initiate a connect and update with the "Switchover to CPU with expanded memory configuration" option in STEP 7, the system reacts as follows with respect to the handling of memory contents.

RAM and load memory

During the connect, the user program blocks (OBs, FCs, FBs, DBs, SDBs) of the master are transferred from the load memory and work memory to the reserve. Exception: If the load memory modules are FLASH cards, the system only transfers the blocks from work memory.

9.3.4 Disabling of link-up and update

Connect and update entails a cycle time extension. This includes a period during which the I/O is not updated; see section Time monitoring (Page 109). Make allowances for this feature in particular when using distributed I/Os and on master/reserve changeover after updating (that is, when modifying the configuration during operation).

CAUTION
Always perform connect and update operations when the process is not in a critical state.

You can set specific start times for connect and update operations at SFC 90 "H_CTRL". For detailed information on this SFC, refer to the *System Software for S7-300/400, System and Standard Functions* manual.

NOTICE
If the process tolerates cycle time extensions at any time, you do not need to call SFC 90 "H_CTRL". The CPU does not perform a self-test during connect and updating. If you use a fail-safe user program, you should avoid any excessive delay for the update operation. For more details, refer to the *S7-400F and S7-400FH Automation Systems* manual.

Example of a time-critical process

A slide block with a 50 mm cam moves on an axis at a constant velocity v = 10 km/h = 2.78 m/s = 2.78 mm/ms. A switch is located on the axis. So the switch is actuated by the cam for the duration of Δt = 18 ms.

For the CPU to detect the actuation of the switch, the inhibit time for priority classes > 15 (see below for definition) must be significantly below 18 ms.

With respect to maximum inhibit times for operations of priority class > 15, STEP 7 only supports settings of 0 ms or between 100 and 60000 ms, so you need to work around this by taking one of the following measures:

- Shift the start time of connect and updating to a time at which the process state is non-critical . Use SFC 90 "H_CTRL" to set this time (see above).
- Use a considerably longer cam and/or substantially reduce the approach velocity of the slide block to the switch.

9.4 Time monitoring

Program execution is interrupted for a certain time during updating. This section is relevant to you if this period is critical in your process. If this is the case, configure one of the monitoring times described below.

During updating, the fault-tolerant system monitors the cycle time extension, communication delay and inhibit time for priority classes > 15 in order to ensure that their configured maximum values are not exceeded, and that the configured minimum I/O retention time is maintained.

NOTICE
If you have not defined any default values for the monitoring times, make allowance for the update in the scan cycle monitoring time. If in this case the update is cancelled, the fault-tolerant system switches to single mode: The previous master CPU remains in RUN, and the reserve CPU goes into STOP. You can either configure all the monitoring times or none at all.

You made allowances for the technological requirements in your configuration of monitoring times.

The monitoring times are described in detail below.

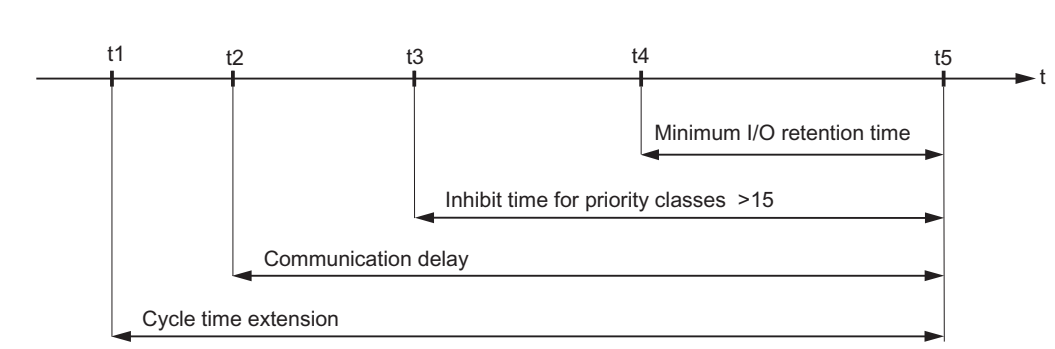
- Maximum cycle time extension
  - Cycle time extension: The time during the update in which neither OB 1 nor any other OBs up to priority class 15 are executed. "Normal" cycle time monitoring is disabled within this time span.
  - Max. cycle time extension: The maximum permissible cycle time extension configured by the user.
- Maximum communication delay
  - Communication delay: The time span during the update during which no communication functions are processed. Note: The master CPU, however, maintains all existing communication links.
  - Maximum communication delay: The maximum permissible communication delay configured by the user.
- Maximum inhibit time for priority classes > 15
  - Inhibit time for priority classes > 15: The time span during an update during which no OBs (and thus no user program) are executed nor any I/O updates are implemented.
  - Maximum inhibit time for priority classes > 15: The maximum permissible inhibit time for priority classes > 15 configured by the user.

- Minimum I/O retention time:

  This represents the interval between copying of the outputs from the master CPU to the reserve CPU, and the time of the transition to the redundant system mode or master/reserve changeover (time at which the previous master CPU goes into STOP and the new master CPU goes into RUN). Both CPUs control the outputs within this period, in order to prevent the I/O from going down when the system performs an update with master/reserve changeover.
  The minimum I/O retention time is of particular importance when updating with master/reserve changeover. If you set the minimum I/O retention time to 0, the outputs could possibly shut down when you modify the system during operation.

The monitoring start times are indicated in the highlighted boxes in Figure 9-2. These times expire when the system enters the redundant system mode or when there is a master/reserve changeover, i.e. on the transition of the new master to RUN when the update is completed.

The figure below provides an overview of the relevant update times.



t1: End of current OBs up to priority class 15
t2: Stop all communication functions
t3: End of watchdog interrupt OB with special handling
t4: End of copying of outputs to the standby CPU
t5: Redundant system status, or master/standby changeover

Figure 9-4 Meanings of the times relevant for updates

Response to time-outs

If one of the times monitored exceeds the configured maximum value, the following procedure is started:

1. Cancel update
2. Fault-tolerant system remains in single mode, with the previous master CPU in RUN
3. Cause of cancelation is entered in diagnostic buffer
4. Call OB 72 (with corresponding start information)

The reserve CPU then reevaluates its system data blocks.
Then, but after at least one minute, the CPU tries again to perform the link-up and update. If still unsuccessful after a total of 10 retries, the CPU abandons the attempt. You yourself will then need to start the link-up and update again.

A monitoring timeout can be caused by:

- High interrupt load (e.g. from I/O modules)
- High communication load causing prolonged execution times for active functions
- In the final update phase, the system needs to copy large amounts of data to the reserve CPU.

9.4.1 Time response

Time response during link-up

The influence of link-up operations on your plant's control system should be kept to an absolute minimum. The current load on your automation system is therefore a decisive factor in the increase of link-up times. The time required for link-up is in particular determined by

- the communication load
- the cycle time

The following applies to no-load operation of the automation system:

Link-up runtime = size of load memory and work memory in MB × 1 s + base load

The base load is a few seconds.

Whenever your automation system is subject to high load, the memory-specific share may increase up to 1 minute per MB.

Time response during updating

The update transfer time is determined by the number and overall length of modified data blocks, rather than by the modified volume of data within a block. It is also determined by the current process status and communication load.

As a simple approximation, we can interpret the maximum inhibit time to be configured for priority classes > 15 as a function of the data volume in the work memory. The volume of code in the work memory is irrelevant.

9.4.2 Determining the monitoring times

Determination using STEP 7 or formulas

STEP 7 automatically calculates the monitoring times listed below for each new configuration. You can also calculate these times using the formulas and procedures described below. They are equivalent to the formulas provided in STEP 7.

- Maximum cycle time extension
- Maximum communication delay
- Maximum inhibit time for priority classes
- Minimum I/O retention time

You can also start automatic calculation of monitoring times with Properties CPU > H Parameters in HW Config.

Monitoring time accuracy

Note

The monitoring times determined by STEP 7 or by using formulas merely represent recommended values.

These times are based on a fault-tolerant system with two communication peers and an average communication load.

Your system profile may differ considerably from those scenarios, therefore the following rules must be observed.

- The cycle time extension factor may increase sharply at a high communication load.
- Any modification of the system in operation may lead to a significant increase in cycle times.
- Any increase in the number of programs executed in priority classes > 15 (in particular processing of communication blocks) automatically increases the communication delay and cycle time extension.
- You can even undercut the calculated monitoring times in small plants with high-performance requirements.

Configuration of the monitoring times

When configuring monitoring times, always make allowances for the following dependencies; conformity is checked by STEP 7:

Max. cycle time extension
> max. communication delay
> (max. inhibit time for priority classes > 15)
> min. I/O retention time

If you have configured different monitoring times in the CPUs and perform a link-up and update operation with master/reserve changeover, the system always applies the higher of the two values.

Calculating the minimum I/O retention time (T_{PH})

The following applies to the calculation of the minimum I/O retention time:

- With central I/O: T_{PH} = 30 ms
- With distributed I/O: T_{PH} = 3 x T_{TRmax}

  Where T_{TRmax} = maximum target rotation time
  all DP master systems of the fault-tolerant station

When using central and distributed I/Os, the resultant minimum I/O retention time is:

T_{PH} = MAX (30 ms, 3 x T_{TRmax})

The following figure shows the correlation between the minimum I/O retention time and the maximum inhibit time for priority classes > 15.

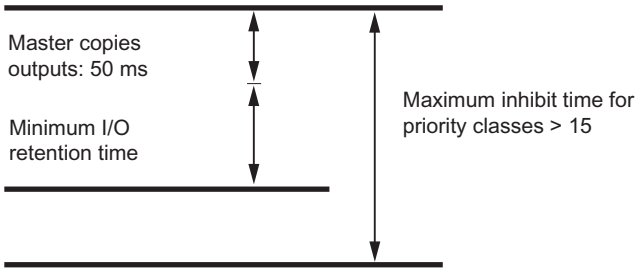


Figure 9-5 Correlation between the minimum I/O retention time and the maximum inhibit time for priority classes > 15

Note the following condition:

50 ms + minimum I/O retention time ≤
(maximum inhibit time for priority classes > 15)

It follows that a high minimum I/O retention time can determine the maximum inhibit time for priority classes > 15.

Calculating the maximum inhibit time for priority classes > 15 (T_{P15})

The maximum inhibit time for priority classes > 15 is determined by 4 main factors:

- As shown in Figure 8–2, all the contents of data blocks modified since the last copy to the reserve CPU are transferred to the reserve CPU again when the update is completed. **The number and structure of the DBs** you write to in the high-priority classes is a decisive factor in the duration of this operation, and thus in the maximum inhibit time for priority classes > 15. Relevant information is available in the remedies described below.
- In the final update phase, all OBs are either delayed or inhibited. To avoid any unnecessary extension of the maximum inhibit time for priority classes > 15 due to unfavorable programming, you should always process the time-critical I/O components in a **selected watchdog interrupt**. This is particularly relevant in fail-safe user programs. You can define this watchdog interrupt in your configuration. It is then executed again right after the start of the maximum inhibit time for priority classes > 15, provided you have assigned it a priority class > 15.
- In link-up and update operations with master/reserve changeover (see section Link-up sequence (Page 101)), you also need to change over the active communication channel on the switched DP slaves when the update is completed. This operation prolongs the time within which valid values can neither be read nor output. How long this process takes is determined by your **hardware configuration**.
- The **technological conditions in your process** also decide how long an I/O update can be delayed. This is particularly important in time-monitored processes in fail-safe systems.

Note

For details, refer to the *S7-400F and S7-400FH Automation Systems* and *S7-300 Automation Systems, Fail-safe Signal Modules* manuals. This applies in particular to the internal execution times of fail-safe modules.

1. Based on the bus parameters in STEP 7, for each DP master system you must define:
   - T_{TR} for the DP master system
   - DP changeover time (referred to below as T_{DP_UM})
2. Based on the technical data of the switched DP slaves, define for each DP master system:
   - The maximum changeover time of the active communication channel (referred to below as T_{SLAVE_UM}).
3. Based on the technological settings of your system, define:
   - The maximum permissible time during which there is no update of your I/O modules (referred to below as T_{PTO}).
4. Based on your user program, determine:
   - The cycle time of the highest-priority or selected (see above) watchdog interrupt (T_{WA})
   - The execution time of your program in this watchdog interrupt (T_{PROG})

5. For each DP master system this results in:

   T_{P15} (DP master system) = T_{PTO} - (2 x T_{TR} + T_{WA} + T_{PROG} + T_{DP_UM} + T_{SLAVE_UM}) [1]

NOTICE
If T_{P15}(DP master system) < 0, stop the calculation here. Possible remedies are shown below the following example calculation. Make appropriate changes and then restart the calculation at 1.

6. Select the minimum of all T_{P15} (DP master system) values.

   This time is then known as TP15_HW.

7. Define the share of the maximum inhibit time for I/O classes > 15 determined by the minimum I/O retention time (T_{P15_OD}):

   T_{P15_OD} = 50 ms + min. I/O retention time [2]

NOTICE
If T_{P15_OD} > T_{P15_HW}, stop the calculation here. Possible remedies are shown below the following example calculation. Make appropriate changes and then restart the calculation at 1.

8. Using the information in section Link-up sequence (Page 101), calculate the share of the maximum inhibit time for priority classes > 15 defined by the user program (T_{P15_AWP}).

NOTICE
If T_{P15_AWP} > T_{P15_HW}, stop the calculation here. Possible remedies are shown below the following example calculation. Make appropriate changes and then restart the calculation at 1.

9. The recommended value for the maximum inhibit time for priority classes > 15 is now obtained from:

   T_{P15} = MAX (T_{P15_AWP}, T_{P15_OD}) [3]

Example of the calculation of T_{P15}

In the next steps, we take an existing system configuration and define the maximum permitted time span of an update, during which the operating system does not execute any programs or I/O updates.

We assume two DP master systems: DP master system_1 is "connected" to the CPU via the MPI/DP interface of the CPU, and DP master system_2 via an external DP master interface.

1. Based on the bus parameters in STEP 7:

   T_{TR_1} = 25 ms

   T_{TR_2} = 30 ms

   $T_{DP\_UM\_1}$ = 100 ms

   $T_{DP\_UM\_2}$ = 80 ms

2. Based on the technical data of the DP slaves used:

   $T_{SLAVE\_UM\_1}$ = 30 ms

   $T_{SLAVE\_UM\_2}$ = 50 ms

3. Based on the technological settings of your system:

   T_{PTO_1} = 1250 ms

   T_{PTO_2} = 1200 ms

4. Based on the user program:

   T_{WA} = 300 ms

   T_{PROG} = 50 ms

5. Based on the formula [1]:

   T_{P15} (DP master system_1)

   = 1250 ms - (2 x 25 ms + 300 ms + 50 ms + 100 ms + 30 ms) = 720 ms

   T_{P15} (DP master system_2)

   = 1200 ms - (2 x 30 ms + 300 ms + 50 ms + 80 ms + 50 ms) = 660 ms

Check: Since $T_{P15} > 0$, continue with

1. T_{P15_HW} = MIN (720 ms, 660 ms) = 660 ms
2. Based on the formula [2]:

$T_{P15\_OD} = 50 \text{ ms} + T_{PH} = 50 \text{ ms} + 90 \text{ ms} = 140 \text{ ms}$

Check: Since $T_{P15\_OD} = 140 \text{ ms} < T_{P15\_HW} = 660 \text{ ms}$, continue with

1. Based on section 7.4.4 with 170 KB of user program data:

   T_{P15_AWP} = 194 ms

Check: Since $T_{P15\_AWP} = 194 \text{ ms} < T_{P15\_HW} = 660 \text{ ms}$, continue with

1. Based on formula [3], we obtain the recommended max. inhibit time for priority classes > 15:

T_{P15} = MAX (194 ms, 140 ms)

T_{P15} = 194 ms

This means that by setting a maximum inhibit time of 194 ms for priority classes > 15 in STEP 7, you ensure that any signal changes during the update are detected with a signal duration of 1250 ms or 1200 ms.

Remedies if it is not possible to calculate T_{P15}

If no recommendation results from calculating the maximum inhibit time for priority classes > 15, you can remedy this by taking various measures:

- Reduce the watchdog interrupt cycle of the configured watchdog interrupt.
- If T_{TR} times are particularly high, distribute the slaves across several DP master systems.
- Increase the baud rate on the affected DP master systems.
- Configure the DP/PA links and Y links in separate DP master systems.
- If there is a great difference in changeover times on the DP slaves, and thus (generally) great differences in T_{PTO}, distribute the slaves involved across several DP master systems.
- If you do not expect any significant load caused by interrupts or parameter assignments in the various DP master systems, you can also reduce the calculated T_{TR} times by around 20% to 30%. However, this increases the risk of a station failure in the distributed I/O.
- The time value T_{P15_AWP} represents a guideline and depends on your program structure. You can reduce it by taking the following measures, for example:
  - Save data that changes often in different DBs than data that does not change as often.
  - Specify a smaller DB sizes in the work memory.

If you reduce the time T_{P15_AWP} without taking the measures described, you run the risk that the update operation will be canceled due to a monitoring timeout.

Calculation of the maximum communication delay

Use the following formula:

Maximum communication delay =
4 x (maximum inhibit time for priority classes > 15)

Decisive factors for determining this time are the process status and the communication load in your system. This can be understood as the absolute load or as the load relative to the size of your user program. You may have to adjust this time.

Calculation of the maximum cycle time extension

Use the following formula:

Maximum cycle time extension =
10 x (maximum inhibit time for priority classes > 15)

Decisive factors for determining this time are the process status and the communication load in your system. This can be understood as the absolute load or as the load relative to the size of your user program. You may have to adjust this time.

See also

Performance values for link-up and update (Page 120)

9.4.3 Performance values for link-up and update

User program share T_{P15_AWP} of the maximum inhibit time for priority classes > 15

The user program share T_{P15_AWP} of the maximum inhibit time for priority classes > 15 can be calculated using the following formula:

T_{P15_AWP} in ms = 0.7 x size of DBs in work memory in KB + 75

The table below shows the derived times for some typical values in work memory data.

Table 9- 3 Typical values for the user program part

Work memory data	T_{P15_AWP}
500 KB	220 ms
1 MB	400 ms
2 MB	0.8 s
5 MB	1.8 s
10 MB	3.6 s

The following assumptions were made for this formula:

- 80% of the data blocks are modified prior to delaying the interrupts of priority classes > 15.
  In particular for fail-safe systems, this calculated value must be more precise to avoid any timeout of driver blocks (see section Determining the monitoring times (Page 113)).
- For active or queued communication functions, allowance is made for an update time of approximately 100 ms per MB in the work memory occupied by data blocks.
  Depending on the communication load of your automation system, you will need to add or deduct a value when you set T_{P15_AWP}.

9.4.4 Influences on time response

The period during which no I/O updates take place is primarily determined by the following influencing factors:

- The number and size of data blocks modified during the update
- The number of instances of SFBs in S7 communication and of SFBs for generating block-specific messages
- System modifications during operation
- Settings by means of dynamic quantity structures
- Expansion of distributed I/Os (a lower baud rate and higher number of slaves increases the time required for I/O updates).

In the worst case, this period is extended by the following amounts:

- Maximum watchdog interrupt cycle used
- Duration of all watchdog interrupt OBs
- Duration of high-priority interrupt OBs executed until the start of interrupt delays

Explicit delay of the update

Delay the update using SFC 90 "H_CTRL", and re-enable it only when the system state shows less communication or interrupt load.

⚠ CAUTION
The update delay increases the time of single mode operation of the fault-tolerant system.

9.5 Special features in link-up and update operations

Requirement for input signals during the update

Any process signals read previously are retained and not included in the update. The CPU only recognizes changes of process signals during the update if the changed signal state remains after the update is completed.

The CPU does not detect pulses (signal transitions "0 → 1 → 0" or "1 → 0 →1") which are generated during the update.

You should therefore ensure that the interval between two signal transitions (pulse period) is always greater than the required update period.

Communication links and functions

Connections on the master CPU are not be shut down. However, associated communication jobs are not executed during updates. They are queued for execution as soon as one of the following cases occurs:

- The update is completed, and the system is in the redundant state.
- The update and master/reserve changeover are completed, the system is in single mode.
- The update was canceled (e.g. due to timeout), and the system has returned to single mode.

An initial call of communication blocks is not possible during the update.

Memory reset request on cancelation of link-up

If the link-up operation is canceled while the content of load memory is being copied from the master to the reserve CPU, the reserve CPU requests a memory reset. This indicated in the diagnostic buffer by event ID W#16#6523.

Using I/Os in S7–400H

10

10.1 Using I/Os in S7–400H

This section provides an overview of the different I/O installations in the S7-400H automation system and their availability. It also provides information on configuration and programming of the selected I/O installation.

10.2 Introduction

I/O installation types

In addition to the power supply module and CPUs, which are always redundant, the operating system supports the following I/O installations:

I/O type	Setup	Availability
Digital input	Single-channel one-sided Single-channel switched Dual-channel redundant	normal enhanced high
Digital output	Single-channel one-sided Single-channel switched Dual-channel redundant	normal enhanced high
Analog input	Single-channel one-sided Single-channel switched Dual-channel redundant	normal enhanced high
Analog output	Single-channel one-sided Single-channel switched Dual-channel redundant	normal enhanced high

A dual-channel redundant configuration at user level is also possible. You nevertheless need to implement the high availability in the user program (see section Other options for connecting redundant I/Os (Page 160)).

Addressing

No matter whether you are using a single-channel one-sided or switched I/O, you always access the I/O via the same address.

Limits of I/O configuration

If there are insufficient slots in the central racks, you can add up to 20 expansion units to the S7-400H configuration.

Module racks with even numbers are always assigned to central rack 0, and racks with odd numbers are always assigned to central rack 1.

For applications with distributed I/O, each of the subsystems supports the connection of up to 12 DP master systems (2 DP master systems on the integrated interfaces of the CPU and 10 via external DP master systems).

The integrated MPI/DP interface supports the operation of up to 32 slaves. You can connect up to 125 distributed I/O devices to the integrated DP master interface and to the external DP master systems.

10.3 Using single-channel, one-sided I/Os

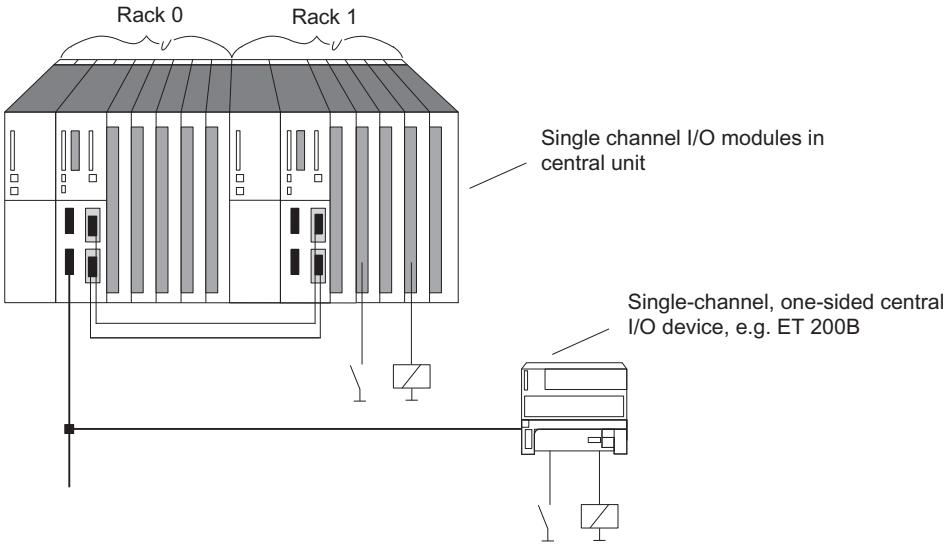
What is single-channel one-sided I/O?

In the single-channel one-sided configuration, the input/output modules exist only once (single-channel). The I/O modules are located in only one subsystem, and are only addressed by this subsystem.

A single-channel, one-sided I/O configuration is possible in:

- Central and expansion devices
- Distributed I/O devices

A configuration with single-channel one-sided I/O is useful for single I/O channels up to system components which only require standard availability.



Single-channel one-sided I/O configuration

Single-channel one-sided I/O and user program

In redundant system mode, the data read from one-sided components (such as digital inputs) is transferred automatically to the second subsystem.

When the transfer is completed, the data read from the single-channel one-sided I/O is available on both subsystems and can be evaluated in their identical user programs. For data processing in the redundant system mode, it is therefore irrelevant whether the I/O is connected to the master or to the reserve CPU.

In single mode, access to one-sided I/O assigned to the partner subsystem is not possible. This must be considered as follows when programming: Assign functions to the single-channel one-sided I/O that can only be executed conditionally. This ensures that specific I/O access functions are only called in redundant system mode and when the relevant subsystem is in single mode.

NOTICE
The user program also has to update the process image for single-channel, one-sided output modules when the system is in single mode (direct access, for example). If you use process image partitions, the user program must update them (SFC 27 "UPDAT_PO") in OB 72 (recovery of redundancy). The system would otherwise first output old values on the single-channel one-sided output modules of the reserve CPU when the system changes to redundant mode.

Failure of the single-channel one-sided I/O

The fault-tolerant system with single-channel one-sided I/O responds to errors just like a standard S7-400 system.

- The I/O is no longer available after it fails.
- If the subsystem to which the I/O is connected fails, the entire process I/O of this subsystem is no longer available.

10.4 Using single-channel switched I/O

What is single-channel switched I/O?

In the single-channel switched configuration, the input/output modules are present singly (single-channel).

In redundant mode, these can addressed by both subsystems.

In single mode, the master subsystem can always address **all switched I/Os** (in contrast to one-sided I/O).

The system supports single-channel switched I/O configurations containing an ET 200M distributed I/O module with active backplane bus and a redundant PROFIBUS DP slave interface module.

You can use the following interfaces:

Table 10- 1 Interfaces for the use of single-channel switched I/O

Interface	Order number
IM 153–2	6ES7 153–2BA81–0XB0 6ES7 153–2BA02–0XB0 6ES7 153–2BA01–0XB0 6ES7 153–2BA00–0XB0
IM 153–2FO	6ES7 153–2AB02–0XB0 6ES7 153–2AB01–0XB0 6ES7 153–2AB00–0XB0 6ES7 153–2AA02–0XB0

Each S7–400H subsystem is interconnected with one of the two DP slave interfaces of the ET 200M via a DP master interface.

PROFIBUS PA can be connected to a redundant system via a DP/PA link.

You can use the following DP/PA links:

DP/PA link	Order number
IM 157	6ES7 157–0BA82–0XA0 6ES7 157–0AA82–0XA0 6ES7 157–0AA81–0XA0 6ES7 157–0AA80–0XA0
ET 200M as DP/PA link with	6ES7 153–2BA02–0XB0 6ES7 153–2BA01–0XB0 6ES7 153–2BA81–0XB0

A single-channel DP master system can be connected to a redundant system via a Y coupler.
Supported IM 157 Y coupler: 6ES7 197-1LB00 0XA0

The single-channel switched I/O configuration is recommended for system components which tolerate the failure of individual modules within the ET 200M.

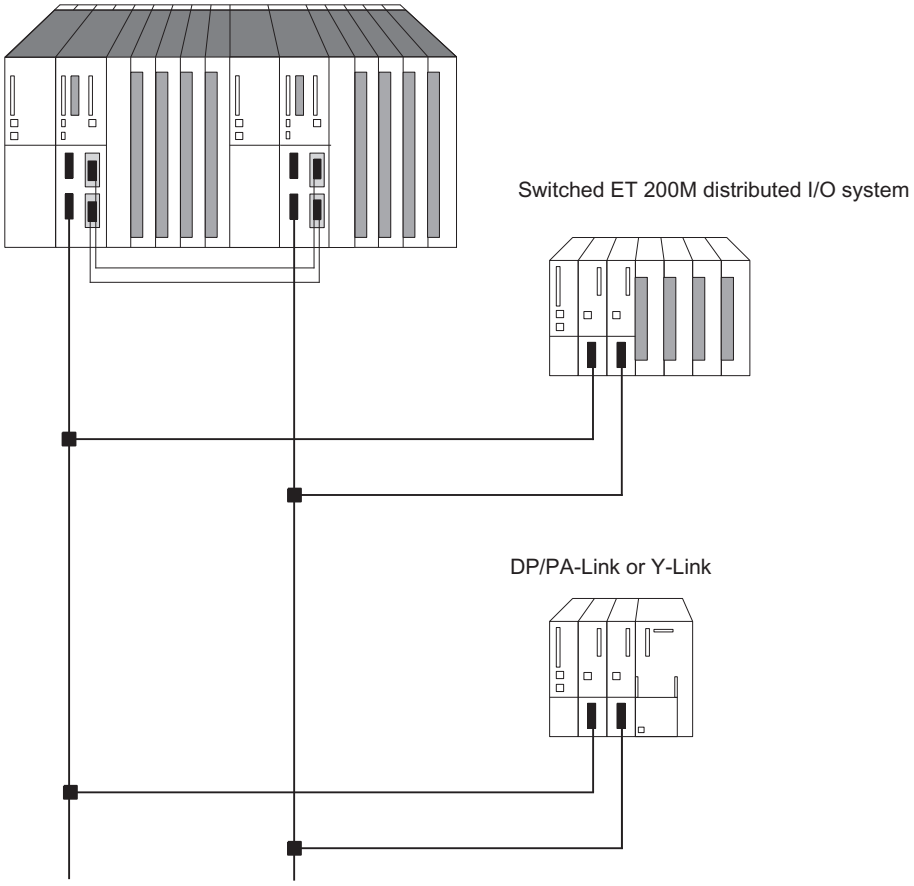


Figure 10-1 ET 200M single-channel switched distributed I/O

Rule

A single-channel switched I/O configuration must always be symmetrical.

- This means, the fault-tolerant CPU and other DP masters must be installed in the same slots in both subsystems (e.g. slot 4 in both subsystems)
- Or the DP masters must be connected to the same integrated interface in both subsystems (e.g. to the PROFIBUS DP interfaces of both fault-tolerant CPUs)

Single-channel switched I/O and user program

In redundant mode, in principle any subsystem can access single-channel switched I/O. The data is automatically transferred via the synchronization link and compared. An identical value is available to the two subsystems at all times owing to the synchronized access.

The fault-tolerant system uses only one of the interfaces at any given time. The active interface is indicated by the ACT LED on the corresponding IM IM 153–2 or IM 157.

The path via the currently active interface (IM 153-2 or IM 157) is called the **active channel** and the path via the other interface as the **passive channel**. The DP cycle is always active on both channels. However, only the input and output values of the active channel are processed in the user program or output to the I/O. The same applies to asynchronous activities, such as interrupt processing and the exchange of data records.

Failure of the single-channel switched I/O

The fault-tolerant system with single-channel switched I/O responds to errors as follows:

- The I/O is no longer available after it fails.
- In certain failure situations (such as the failure of a subsystem, DP master system or DP slave interface module IM153-2 or IM 157; see section Communication (Page 167)), the single-channel switched I/O remains available to the process.
  This is achieved by a switchover between the active and passive channel. This switchover takes place separately for each DP station. A distinction is made between the following types of failure:
  - Failures affecting only one station (such as failure of the DP slave interface of the currently active channel)
  - Failures affecting all stations of a DP master system.
    This includes unplugging of the connector at the DP master interface, shutdown of the DP master system (e.g. RUN-STOP change on a CP 443-5), and short-circuits on the cable harness of a DP master system.

The following applies to each station affected by a failure: If both DP slave interfaces are currently functional and the active channel fails, the previously passive channel automatically becomes active. A redundancy loss is reported to the user program when OB 70 starts (event W#16#73A3).

Once the problem is eliminated, redundant mode is restored. This also starts OB 70 (event W#16#72A3). In this situation, there is no changeover between the active and passive channel.

If one channel has already failed, and the remaining (active) channel also fails, then there is a complete station failure. This starts OB 86 (event W#16#39C4).

Note

If the DP master interface module can detect failure of the entire DP master system (due to short-circuit, for example), it reports only this event ("Master system failure entering state" W#16#39C3). The operating system no longer reports individual station failures. This feature can be used to accelerate the changeover between the active and passive channel.

Duration of a changeover of the active channel

The maximum changeover time is

DP error detection time + DP changeover time + changeover time of the DP slave interface

You can determine the first two values from the bus parameters of your DP master system in STEP 7. You can obtain the last value from the manuals of the relevant DP slave interface module *(distributed I/O device ET 200M* or *DP/PA bus link*).

NOTICE

When using fail-safe modules, always set a monitoring time for each fail-safe module that is longer than the changeover time of the active channel in the fault-tolerant system. If you ignore this rule, you risk failure of the fail-safe modules during the changeover of the active channel.

NOTICE

The above calculation also includes the processing time in OB 70 or OB 86. Make sure that the processing time for a DP station **does not last longer than 1 ms**. In situations requiring extensive processing, exclude this processing from direct execution of the OBs mentioned.

Note that the CPU can only detect a signal change if the signal duration is greater than the specified changeover time.
When there is a changeover of the entire DP master system, the changeover time of the slowest component applies to all DP components. A DP/PA link or Y link usually determines the changeover time and the associated minimum signal duration. We therefore recommend that you connect DP/PA and Y links to a separate DP master system.

When using fail-safe modules, always set a monitoring time for each fail-safe module that is longer than the changeover time of the active channel in the fault-tolerant system. If you ignore this, you risk failure of the fail-safe modules during the changeover of the active channel.

Changeover of the active channel during connect and updating

During connect and update with master/reserve changeover (see section Link-up sequence (Page 101)), the active and passive channels are changed over on all stations of the switched I/O. At the same time OB 72 is called.

Bumpless changeover of the active channel

To prevent the I/O failing temporarily or outputting substitute values during the changeover between the active and passive channel, the DP stations of the switched I/O put their outputs on hold until the changeover is completed and the new active channel has taken over.

To ensure that total failures of a DP station are detected during the changeover, the changeover is monitored by the various DP stations and by the DP master system.

Provided the minimum I/O retention time is set correctly (see section Time monitoring (Page 109)), no interrupts or data records will be lost due to a changeover. There is an automatic repetition when necessary.

System configuration and project engineering

You should allocate switched I/O with different changeover times to separate chains. This, for example, simplifies the calculation of monitoring times.

10.5 Connecting redundant I/O

10.5.1 Connecting redundant I/O

What is redundant I/O?

Input/output modules are termed redundant when they exist twice and they are configured and operated as redundant pairs. The use of redundant I/O provides the highest degree of availability, because the system tolerates the failure of a CPU or of a signal module.

Configurations

The following redundant I/O configurations are supported:

1. Redundant signal modules in the central and expansion devices
   For this purpose, the signal modules are installed in pairs in the CPU 0 and CPU 1 subsystems. Redundant I/O in central and expansion devices

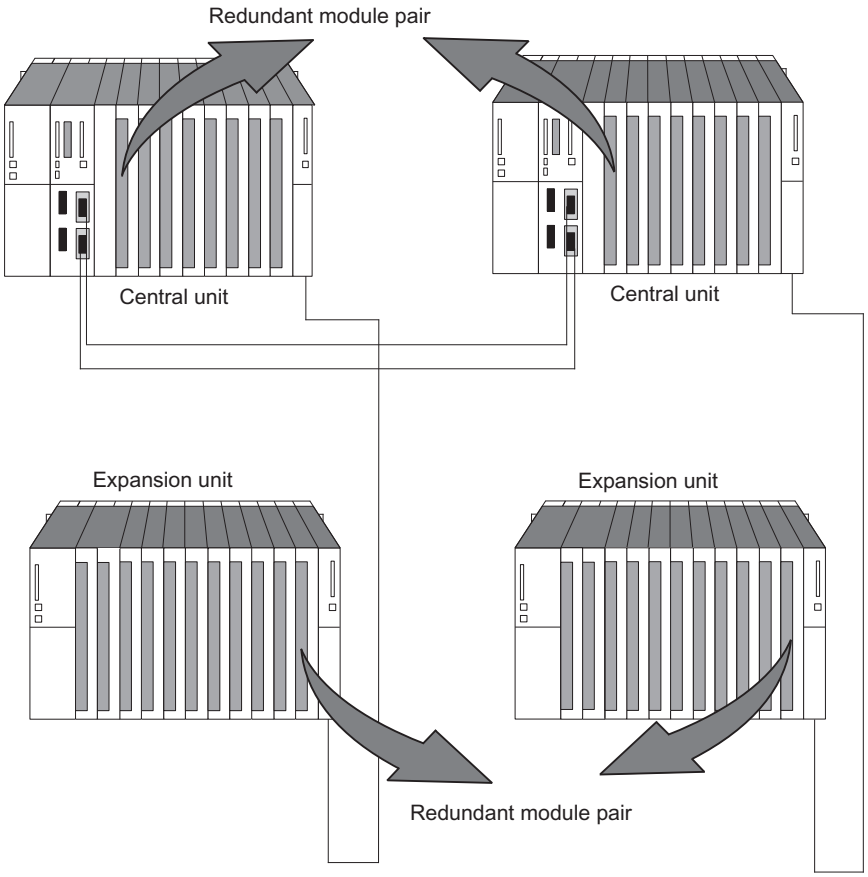


Figure 10-2 Redundant I/O in central and expansion devices

2. Redundant I/O in the one-sided DP slave

   To achieve this, the signal modules are installed in pairs in ET 200M distributed I/O devices with active backplane bus.

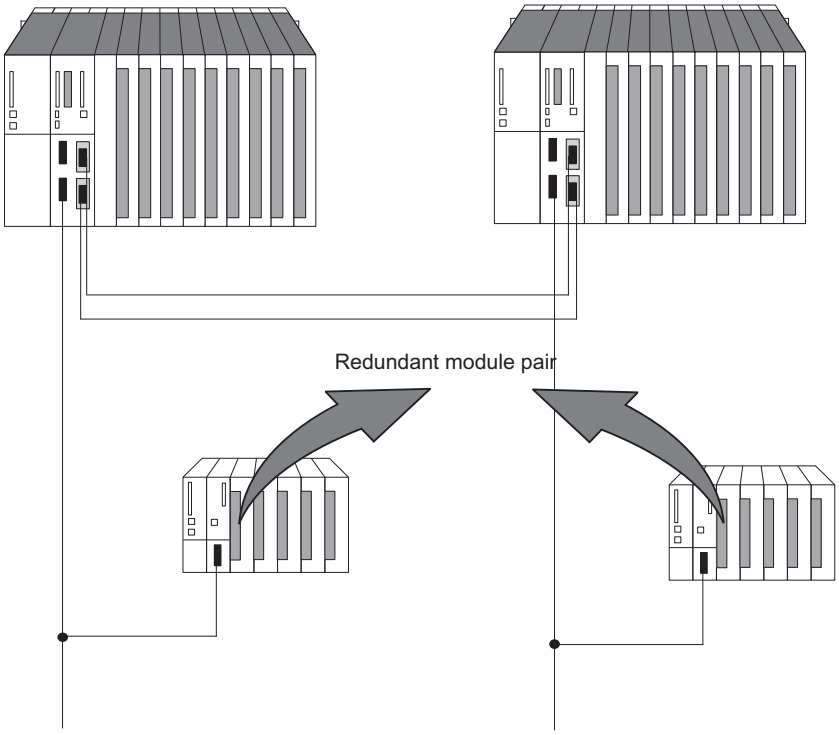


Figure 10-3 Redundant I/O in the one-sided DP slave

3. Redundant I/O in the switched DP slave

   To achieve this, the signal modules are installed in pairs in ET 200M distributed I/O devices with active backplane bus.

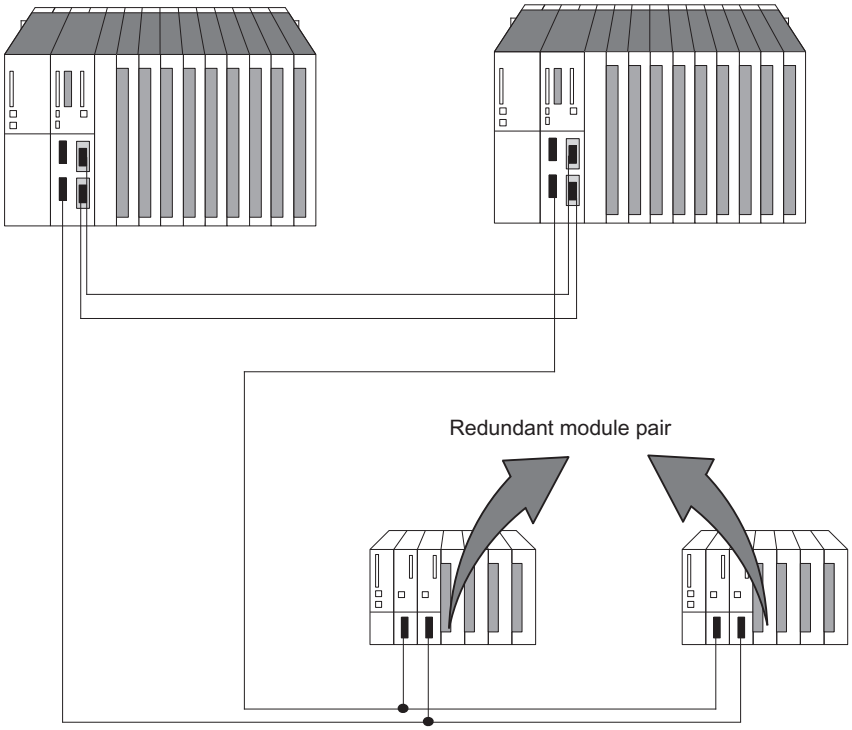


Figure 10-4 Redundant I/O in the switched DP slave

4. Redundant I/O connected to a fault-tolerant CPU in single mode

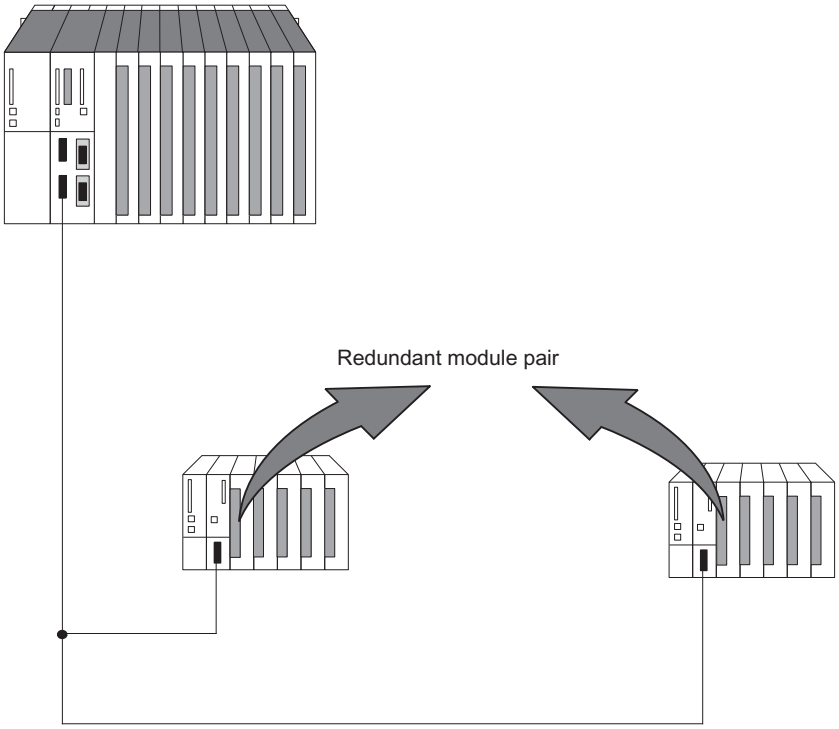


Figure 10-5 Redundant I/O in stand-alone mode

Principle of channel group-specific redundancy

Channel errors due to discrepancy cause the passivation of the respective channel. Channel errors due to diagnostic interrupts (OB82) cause the passivation of the channel group affected. Depassivation depassivates all affected channels as well as the modules passivated due to module errors. Channel group-specific passivation significantly increases availability in the following situations:

- Relatively frequent encoder failures
- Repairs that take a long time
- Multiple channel errors on one module

Note

Channel and channel group

Depending on the module, a channel group contains a single channel, a group of several channels, or all channels of the module. You can therefore operate all modules with redundancy capability in channel group-specific redundancy mode.

An up-to-date list of modules with redundancy capability can be found in section Signal modules for redundancy (Page 140).

Principle of module-specific redundancy

Redundancy always applies to the entire module, rather than to individual channels. When a channel error occurs in the first redundant module, the entire module and all of its channels are passivated. If an error occurs on another channel on the second module before the first error has been eliminated and the first module has been depassivated, this second error cannot be handled by the system.

An up-to-date list of modules with redundancy capability can be found in section Signal modules for redundancy (Page 140).

"Functional I/O redundancy" block libraries

The blocks you use for channel group-specific redundancy are located in the "Redundant IO CGP V50" library. The blocks in the library "Redundant IO CGP V40" can also be set for channel group-specific redundancy but only for a limited range of modules.

The blocks you use for module-specific redundancy are located in the "Redundant IO MGP V30" library. Module-specific redundancy is a special form of redundant module operation; see above.

Note

Operating redundant modules

When you are operating signal modules for the first time, use channel group-specific redundancy with the blocks in the "Redundant IO CGP V50" library. This ensures maximum flexibility when using redundant modules.

The "Functional I/O redundancy" block libraries that support the redundant I/O each contain the following blocks:

- FC 450 "RED_INIT": Initialization function
- FC 451 "RED_DEPA": Initiate depassivation
- FB 450 "RED_IN": Function block for reading redundant inputs
- FB 451 "RED_OUT": Function block for controlling redundant outputs
- FB 452 "RED_DIAG": Function block for diagnostics of redundant I/O
- FB 453 "RED_STATUS": Function block for redundancy status information

Configure the numbers of the management data blocks for the redundant I/O in HW Config "Properties CPU -> H Parameter". Assign free DB numbers to these data blocks. The data blocks are created by FC 450 "RED_INIT" during CPU startup. The default setting for the numbers of the management data blocks is 1 and 2. These data blocks are not the instance data blocks of FB 450 "RED_IN" or FB 451 "RED_OUT".

You can open the libraries in the SIMATIC Manager with "File -> Open -> Libraries"

The functions and use of the blocks are described in the corresponding online help.

NOTICE
Blocks from various libraries Only use blocks from one library. Simultaneous use of blocks from different libraries is not permitted. If you wish to replace one of the earlier libraries Redundant IO (V1) or Redundant IO CGP with the Redundant IO CGP V5.0, you must first of all edit your user program accordingly. Refer to the context-sensitive block help or the STEP 7 Readme for more information.

Switching to channel group-specific redundancy

To activate channel group-specific passivation, you have to stop the automation system (memory reset and reload user program in STOP).

Observe the following:

Mixing blocks from various libraries in one CPU is not permitted and can lead to unpredictable behavior.

When converting a project, make sure that all library blocks named FB450–453 and FC450-451 have been deleted from the block folder and replaced by the blocks from Red-IO CGP V5.0. Perform this step in every relevant program. Compile and load your project.

Using the blocks

Before you use the blocks, parameterize the redundant modules as redundant in HW Config.

The OBs into which you need to link the various blocks are listed in the table below:

Block	OB
FC 450 "RED_INIT"	• OB 72 "CPU redundancy error" (only with fault-tolerant systems) FC 450 is only executed after the start event B#16#33:"Reserve-master changeover by operator" • OB 80 "Timeout error" (only in single mode) FC 450 is only executed after the start event "Resume RUN after reconfiguring" • OB 100 "Restart" (the administration DBs are recreated, see the online help) • OB 102 "Cold restart"

Block	OB
FC 451 "RED_DEPA"	If you call FC 451 in OB 83 while inserting modules or in OB 85 during alarm output, depassivation is delayed by approximately 3 seconds. In addition the FC 451 should be executed after the removal of the error response as specific call in OB 1 and/or OB 30 to 38. The FC451 only depassivates modules in the corresponding process image partition. Depassivation is delayed by 10 seconds with Version 3.5 or higher of FB 450 "RED_IN" in the library "Redundant IO MGP" and Version 5.8 or higher of FB 450 "RED_IN" in the library "Redundant IO CGP" V50.
FB 450 "RED_IN"	• OB 1 "Cyclic program" • OB 30 to OB 38 "Watchdog interrupt"
FB 451 "RED_OUT"	• OB 1 "Cyclic program" • OB 30 to OB 38 "Watchdog interrupt"
FB 452 "RED_DIAG"	• OB 72 "CPU redundancy error" • OB 82 "Diagnostic interrupt" • OB 83 "Swapping interrupt" • OB 85 "Program execution error"
FB 453 "RED_STATUS"	• OB 1 "Cyclic program" (fault-tolerant systems only) • OB 30 to OB 38 "Watchdog interrupt"

To be able to address redundant modules using process image partitions in watchdog interrupts, the relevant process image partition must be assigned to this pair of modules and to the watchdog interrupt. Call FB 450 "RED_IN" in this watchdog interrupt before you call the user program. Call FB 451 "RED_OUT" in this watchdog interrupt after you call the user program.

The valid values that can be processed by the user program are always located at the lower address of both redundant modules. This means that only the lower address can be used for the application; the values of the higher address are not relevant for the application.

Note

Use of FB 450 "RED_IN" and 451 "RED_OUT" when using process image partitions

For each priority class used (OB 1, OB 30 ... OB 38), you must use a separate process image partition.

Hardware configuration and project engineering of the redundant I/O

Follow the steps below to use redundant I/O:

1. Insert all the modules you want to operate redundantly. Remember the following basic rules for configuration.

2. Configure the module redundancy using HW Config in the object properties of the relevant module.

   Either browse for a partner module for each module, or accept the default settings

   In a centralized configuration: If the module is in slot X of the even-numbered rack, the module at the same slot position in the next odd-numbered rack is proposed.
   If the module is in slot X of the odd-numbered rack, the module at the same slot position in the previous even-numbered rack is proposed.

   Distributed configuration in a one-sided DP slave: If the module is inserted in slot X of the slave, the module at the same slot X of the slave at the same PROFIBUS address in the partner DP subsystem is proposed, provided the DP master system is redundant.

   Distributed configuration in a switched DP slave, stand-alone mode: If the module in the slave with a DP address is inserted in slot X, the module in the slave with the next PROFIBUS address at slot X is proposed.

3. Enter the remaining redundancy parameters for the input modules.

Note

System modifications during operation are also supported with redundant I/O. You are not permitted to change the parameter settings for a redundant module per SFC.

NOTICE

Always switch off power to the station or rack before you remove a redundant digital input module that does not support diagnostics functions and is not passivated. You might otherwise passivate the wrong module. This procedure is necessary, for example, when replacing the front connector of a redundant module.

Redundant modules must be in the process image of the inputs or outputs. Redundant modules are always accessed using the process image.

When using redundant modules, select the "Cycle/Clock Memory" tab from "HW Config -> Properties CPU 41x-H" and set the following:

"OB 85 call on I/O area access error > Only incoming and outgoing errors"

10.5.2 Signal modules for redundancy

Signal modules as redundant I/O

The signal modules listed below can be used as redundant I/O. Refer to the latest information about the use of modules available in the readme file and in the SIMATIC FAQ at http://www.siemens.com/automation/service&support under the keyword "Redundant I/O".

Take into account that you can only use modules of the same product version and same firmware version as redundant pairs.

Table 10- 2 Signal modules for redundancy

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
Central: Redundant DI dual-channel				
X	X		DI 16xDC 24V interrupt	6ES7 421–7BH0x–0AB0
			Use with non-redundant encoder • This module supports the "wire break" diagnostic function. To implement this function, make sure that a total current between 2.4 mA and 4.9 mA flows even at signal state "0" when you use an encoder that is evaluated at two inputs in parallel. You achieve this by connecting a resistor via the encoder. Its value depends on the type of switch and usually ranges between 6800 and 8200 ohms for contacts. For BEROS, calculate the resistance based on this formula: (30 V/(4.9 mA – I_R_Bero) < R < (20 V/(2.4 mA – I_R_Bero)	
X	X		DI 32xDC 24V	6ES7 421–1BL0x–0AA0
X	X		DI 32xUC 120V	6ES7 421–1EL00–0AA0
Distributed: Redundant DI dual-channel				
X	X		DI16xDC 24 V, interrupt	6ES7 321–7BH00–0AB0
X	X	X	DI16xDC 24 V	6ES7 321–7BH01–0AB0
			In the event of an error on one channel, the entire group (2 channels) is passivated. Use with non-redundant encoder • This module supports the "wire break" diagnostic function. To implement this function, make sure that a total current between 2.4 mA and 4.9 mA flows even at signal state "0" when you use an encoder that is evaluated at two inputs in parallel. You achieve this by connecting a resistor via the encoder. Its value depends on the type of switch and usually ranges between 6800 and 8200 ohms for contacts. For BEROS, calculate the resistance based on this formula: (30 V/(4.9 mA – I_R_Bero) < R < (20 V/(2.4 mA – I_R_Bero)	

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
X	X		DI16xDC 24 V	6ES7 321–1BH02–0AA0
			In some system states, it is possible that an incorrect value of the first module is read in briefly when the front connector of the second module is removed. This is prevented by using series diodes like those shown in figure F.1.	
X	X		DI32xDC 24 V	6ES7 321–1BL00–0AA0
			In some system states, it is possible that an incorrect value of the first module is read in briefly when the front connector of the second module is removed. This is prevented by using series diodes like those shown in figure F.2.	
X	X		DI 8xAC 120/230V	6ES7 321–1FF01–0AA0
X	X		DI 4xNamur [EEx ib]	6ES7 321–7RD00–0AB0
			You cannot use the module for applications in hazardous areas in redundant mode. Use with non-redundant encoder • You can only connect 2-wire NAMUR encoders or contact makers. • Equipotential bonding of the encoder circuit should always be at one point only (preferably encoder negative). • When selecting encoders, compare their properties with the specified input characteristics. Remember that this function must always be available, regardless of whether you are using one or two inputs. Example of valid values for NAMUR encoders: for "0" current > 0.2 mA; for "1" current > 4.2 mA.	
X	X		DI 16xNamur	6ES7321–7TH00–0AB0
			Use with non-redundant encoder • Equipotential bonding of the encoder circuit should always be at one point only (preferably encoder negative). • Operate the two redundant modules on a common load power supply. • When selecting encoders, compare their properties with the specified input characteristics. Remember that this function must always be available, regardless of whether you are using one or two inputs. Example of valid values for NAMUR encoders: for "0" current > 0.7 mA; for "1" current > 4.2 mA.	
X	X		DI 24xDC 24 V	6ES7326–1BK0x–0AB0
			F module in standard mode	
X	X		DI 8xNAMUR [EEx ib]	6ES7326–1RF0x–0AB0
			F module in standard mode	
Central: Redundant DO dual-channel				
X	X		DO 32xDC 24V/0.5A	6ES7422–7BL00–0AB0
			A clear evaluation of the diagnostics information "P short-circuit", "M short-circuit" and wire break is not possible. Deselect these individually in your configuration.	
X	X		DO 16xAC 120/230V/2A	6ES7422–1FH00–0AA0

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
Distributed: Redundant DO dual-channel				
X	X		DO8xDC 24 V/0.5 A	6ES7322–8BF00–0AB0
			A definite evaluation of the diagnostics information "P short-circuit" and "wire break" is not possible. Deselect these individually in your configuration.	
X	X		DO8xDC 24 V/2 A	6ES7322–1BF01–0AA0
X	X		DO32xDC 24 V/0.5 A	6ES7322–1BL00–0AA0
X	X		DO8xAC 120/230 V/2 A	6ES7322–1FF01–0AA0
X	X		DO 4x24 V/10 mA [EEx ib]	6ES7322–5SD00–0AB0
			You cannot use the module for applications in hazardous areas in redundant mode.	
X	X		DO 4x24 V/10 mA [EEx ib]	6ES7322–5RD00–0AB0
			You cannot use the module for applications in hazardous areas in redundant mode.	
X	X	X	DO 16xDC 24 V/0.5 A	6ES7322–8BH01–0AB0
			• The equipotential bonding of the load circuit should always take place from one point only (preferably load minus). • Diagnostics of the channels is not possible.	
X	X	X	DO 16xDC 24 V/0.5 A	6ES7322–8BH10–0AB0
			• The equipotential bonding of the load circuit should always take place from one point only (preferably load minus). • Diagnostics of the channels is not possible.	
X	X	X	DO 10xDC 24 V/2 A, product version 3 or higher	6ES7326–2BF0x–0AB0
			The inputs and outputs must have the same address.	

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
Central: Redundant AI dual-channel				
X	X		AI 16x16Bit	6ES7431–7QH00–0AB0
			Use in voltage measurement • The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected. Use in indirect current measurement • Use a 50 ohm resistor (measuring range +/- 1 V) or 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage, see figure 10-9. The tolerance of the resistor must be added on to the module error. Use in direct current measurement • Suitable Zener diode: BZX85C6v2 • Load capability of 4-wire transmitters: R_B > 325 ohms (determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to $R_B = (R_E * I_{max} + U_{z\,max})/I_{max)}$ • Input voltage in the circuit when operating with a 2-wire transmitter: $U_{e\text{-}2w}$ < 8 V (determined for worst case: 1 input + 1 Zener diode at an S7 overshoot value 24 mA to $U_{e\text{-}2w} = R_E * I_{max} + U_{z\,max}$) **Note:** The circuit shown in figure 10–10 works only with active (4-wire) transmitters or with passive (2-wire) transmitters with external power supply. Always parameterize the module channels for operation as "4-wire transmitter", and set the measuring range cube to position "C". It is not possible to power the transmitters via the module (2DMU).	

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
Distributed: Redundant AI dual-channel				
X	X		AI8x12Bit	6ES7331–7KF02–0AB0
			Use in voltage measurement • The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected. Use for indirect current measurement • When determining the measuring error, observe the following: The total input resistance in measuring ranges > 2.5 V is reduced from a nominal 100 kOhm to 50 kOhm when operating two inputs connected in parallel. • The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected. • Use a 50 ohm resistor (measuring range +/- 1 V) or 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage, see figure 10-9. The tolerance of the resistor must be added on to the module error. • This module is not suitable for direct current measurement. Use of redundant encoders: • You can use a redundant encoder with the following voltage settings: +/- 80 mV (only without wire break monitoring) +/- 250 mV (only without wire break monitoring) +/- 500 mV (wire break monitoring not configurable) +/- 1 V (wire break monitoring not configurable) +/- 2.5 V (wire break monitoring not configurable) +/- 5 V (wire break monitoring not configurable) +/- 10 V (wire break monitoring not configurable) 1...5 V (wire break monitoring not configurable)	

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
X	X	X	AI 8x16Bit	6ES7 331–7NF00–0AB0
			Use in voltage measurement • The "wire break" diagnostics function in HW Config must not be activated when operating the modules with transmitters. Use in indirect current measurement • When using indirect current measurement, ensure a reliable connection between the sensor resistances and the actual inputs, because a reliable wire break detection cannot be guaranteed in the case of a wire break of individual cables of this connection. • Use a 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage; see figure 10-9. Use in direct current measurement • Suitable Zener diode: BZX85C8v2 • Circuit-specific additional error: If one module fails, the other may suddenly show an additional error of approx. 0.1%. • Load capability of 4-wire transmitters: R_B > 610 ohms (determined for worst case scenario: 1 input + 1 Zener diode at an S7 overload value 24 mA to $R_B = (R_E * I_{max} + U_{z\,max})/I_{max)}$ • Input voltage in the circuit when operating with a 2-wire transmitter: $U_{e\text{-}2w}$ < 15 V (determined for worst case: 1 input + 1 Zener diode at an S7 overshoot value 24 mA to $U_{e\text{-}2w} = R_E * I_{max} + U_{z\,max}$)	
X	X		AI 8x16Bit	6ES7 331–7NF10–0AB0
			Use in voltage measurement • The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected. Use in indirect current measurement • Use a 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage; see figure 10-9. Use in direct current measurement • Suitable Zener diode: BZX85C8v2 • Load capability of 4-wire transmitters: R_B > 610 ohms (determined for worst case scenario: 1 input + 1 Zener diode at an S7 overload value 24 mA to $R_B = (R_E * I_{max} + U_{z\,max})/I_{max)}$ • Input voltage in the circuit when operating with a 2-wire transmitter: $U_{e\text{-}2w}$ < 15 V (determined for worst case: 1 input + 1 Zener diode at an S7 overshoot value 24 mA to $U_{e\text{-}2w} = R_E * I_{max} + U_{z\,max}$)	

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
X	X		AI 6xTC 16Bit iso, 6ES7331-7PE10-0AB0	6ES7331-7PE10-0AB0
			Notice: These modules must only be used with redundant encoders. You can use this module with Version 3.5 or higher of FB 450 "RED_IN" in the library "Redundant IO MGP" and Version 5.8 or higher of FB 450 "RED_IN" in the library "Redundant IO CGP" V50. This FB is available in STEP 7 V5.4.4 HF6 or higher. Observe the following when measuring temperatures by means of thermocouples and parameterized redundancy: The value specified in "Redundancy" under "Tolerance window" is always based on 2764.8 °C. For example, a tolerance of 27 °C is checked if "1" is entered, or a tolerance of 138 °C is checked if "5" is entered. A firmware update is not possible in redundant mode. Online calibration is not possible in redundant mode. Use in voltage measurement • The "wire break" diagnostics function in HW Config must not be activated when operating the modules with thermocouples. Use in indirect current measurement • Due to the maximum voltage range +/- 1 V, the indirect current measurement can be carried out exclusively via a 50 ohm resistor. Mapping that conforms to the system is only possible for the area +/- 20 mA.	
X	X		AI 4x15Bit [EEx ib]	6ES7331-7RD00-0AB0
			You cannot use the module for applications in hazardous areas in redundant mode. It is not suitable for indirect current measurement. Use in direct current measurement • Suitable Zener diode: BZX85C6v2 • Load capability of 4-wire transmitters: RB > 325 ohms determined for worst case: 1 input + 1 Zener diode at an S7 overshoot value 24 mA to RB = (RE * I_{max} + $U_{z\ max}$)/I_{max} • Input voltage for 2-wire transmitters: Ue–2w < 8 V determined for worst case: 1 input + 1 Zener diode at an S7 overshoot value 24 mA to Ue–2w = RE * I_{max} + $U_{z\ max}$ **Note:** You can only connect 2-wire transmitters with a 24 V external supply or 4-wire transmitters. The internal power supply for transmitters cannot be used in the circuit shown in figure 8-10, because this outputs only 13 V, and thus in the worst case it would supply only 5 V to the transmitter.	
X	X		AI 6x13Bit	6ES7 336–1HE0x–0AB0
			F module in standard mode	
X	X	X	AI 8x0/4...20mA HART	6ES7 331–7TF01-0AB0
			A firmware update is not possible in redundant mode. Online calibration is not possible in redundant mode. See *Distributed I/O Device ET 200M; HART Analog Modules* manual	

Channel group-specific (V5.x)	Channel group-specific (V3.x)	Channel-specific (V 4.x)	Module	Order number
Distributed: Redundant AO dual-channel				
X	X		AO4x12 Bit	6ES7332–5HD01–0AB0
X	X	X	AO8x12 Bit	6ES7332–5HF00–0AB0
X	X		AO4x0/4...20 mA [EEx ib]	6ES7332–5RD00–0AB0
			You cannot use the module for applications in hazardous areas in redundant mode.	
X	X	X	AO 8x0/4...20mA HART	6ES7 332–8TF01-0AB0
			A firmware update is not possible in redundant mode. Online calibration is not possible in redundant mode. If there is a CPU passivation or CPU STOP, this module outputs a minimum current of approx. 240 µA. See *Distributed I/O Device ET 200M; HART Analog Modules* manual	

NOTICE

You need to install the F ConfigurationPack for F modules.
The F ConfigurationPack can be downloaded free of charge from the Internet.
You can get it from Customer Support at:
http://www.siemens.com/automation/service&support.

Quality levels in the redundant configuration of signal modules

The availability of modules in the case of an error depends on their diagnostics possibilities and the fine granularity of the channels.

Using digital input modules as redundant I/O

The following parameters were set to configure digital input modules for redundant operation:

- Discrepancy time (maximum permitted time in which the redundant input signals may differ). The configured discrepancy time must be a multiple of the update time of the process image and therefore also the basic conversion time of the channels.
  When there is still a discrepancy in the input values after the configured discrepancy time has expired, an error has occurred.
- Response to a discrepancy in the input values

First, the input signals of the paired redundant modules are checked for consistency. If the values match, the uniform value is written to the lower memory area of the process input image. If there is a discrepancy and it is the first, it is marked accordingly and the discrepancy time is started.

During the discrepancy time, the most recent matching (non-discrepant) value is written to the process image of the module with the lower address. This procedure is repeated until the values once again match within the discrepancy time or until the discrepancy time of a bit has expired.

If the discrepancy continues past the expiration of the configured discrepancy time, an error has occurred.

The defective side is localized according to the following strategy:

1. During the discrepancy time, the most recent matching value is retained as the result.
2. Once the discrepancy time has expired, the following error message is displayed:
   Error code 7960: "Redundant I/O: discrepancy time at digital input expired, error not yet localized". Passivation is not performed and no entry is made in the static error image. Until the next signal change occurs, the configured response is performed after the discrepancy time expires.
3. If another signal change occurs, the module/channel in which the signal change occurred is the intact module/channel and the other module/channel is passivated.

NOTICE
The time that the system actually needs to determine a discrepancy depends on various factors: Bus delay times, cycle and call times in the user program, conversion times, etc. Redundant input signals can therefore be different for a longer period than the configured discrepancy time.

Modules with diagnostics capability are also passivated by calling OB 82.

Using redundant digital input modules with non-redundant encoders

With non-redundant encoders, you use digital input modules in a 1-out-of-2 configuration:

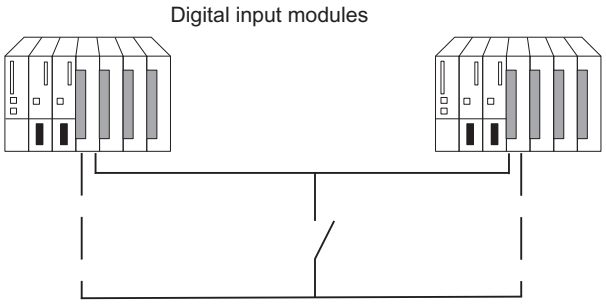


Figure 10-6 Fault-tolerant digital input module in 1-out-of-2 configuration with one encoder

The use of redundant digital input modules increases their availability.

Discrepancy analysis detects "Continuous 1" and "Continuous 0" errors of the digital input modules. A "Continuous 1" error means the value 1 is applied permanently at the input, a "Continuous 0" error means that the input is not energized. This can be caused, for example, by a short-circuit to L+ or M.

The current flow over the chassis ground connection between the modules and the encoder should be the minimum possible.

When connecting an encoder to several digital input modules, the redundant modules must operate at the same reference potential.

If you want to replace a module during operation and are not using redundant encoders, you will need to use decoupling diodes.

You will find connection examples in Appendix Connection examples for redundant I/Os (Page 359).

Note

Remember that the proximity switches (Beros) must provide the current for the channels of both digital input modules. The technical data of the respective modules, however, specify only the required current per input.

Using redundant digital input modules with redundant encoders

With redundant encoders you use digital input modules in a 1-out-of-2 configuration:

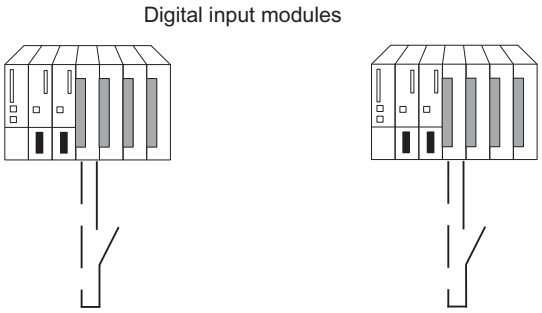


Figure 10-7 Fault-tolerant digital input modules in 1-out-of-2 configuration with two encoders

The use of redundant encoders also increases their availability. A discrepancy analysis detects all errors, except for the failure of a non-redundant load voltage supply. You can enhance availability by installing redundant load power supplies.

You will find connection examples in Appendix Connection examples for redundant I/Os (Page 359).

Redundant digital output modules

Fault-tolerant control of a final controlling element can be achieved by connecting two outputs of two digital output modules or fail-safe digital output modules in parallel (1-out-of-2 configuration).

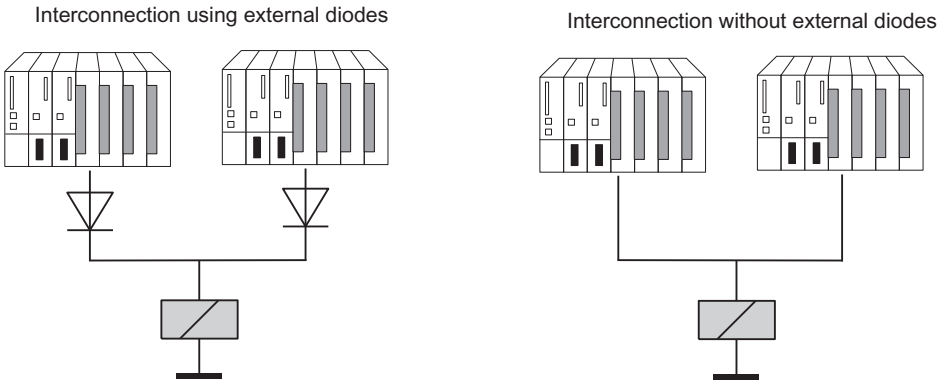


Figure 10-8 Fault-tolerant digital output modules in 1-out-of-2 configuration

The digital output modules must be connected to a common load voltage supply.

You will find connection examples in Appendix Connection examples for redundant I/Os (Page 359).

Interconnection using external diodes <-> without external diodes

The table below lists the redundant digital output modules which in redundant mode you should interconnect using external diodes:

Table 10- 3 Interconnecting digital output modules with/without diodes

Module	with diodes	without diodes
6ES7 422–7BL00–0AB0	X	-
6ES7 422–1FH00–0AA0	-	X
6ES7 326–2BF0x–0AB0	X	X
6ES7 322–1BL00–0AA0	X	-
6ES7 322–1BF01–0AA0	X	-
6ES7 322–8BF00–0AB0	X	X
6ES7 322–1FF01–0AA0	-	X
6ES7 322–8BH01–0AB0	-	X
6ES7 322–8BH10–0AB0	-	X
6ES7 322–5RD00–0AB0	X	-
6ES7 322–5SD00–0AB0	X	-

Information on connecting with diodes

- Suitable diodes are diodes with U_r >=200 V and I_F >= 1 A (e.g. types from the series 1N4003 ... 1N4007).
- It is advisable to separate the ground of the module and the ground of the load. There must be equipotential bonding between both.

Using analog input modules as redundant I/O

You specified the following parameters when you configured the analog input modules for redundant mode:

- Tolerance window (configured as a percentage of the end value of the measuring range) Two analog values are considered equal if they are within the tolerance window.
- Discrepancy time (maximum permitted time in which the redundant input signals can be outside the tolerance window). The configured discrepancy time must be a multiple of the update time of the process image and therefore also the basic conversion time of the channels.
  An error is generated when there is an input value discrepancy after the configured discrepancy time has expired.
  If you connect identical sensors to both analog input modules, the default value for the discrepancy time is usually sufficient. If you use different sensors, in particular temperature sensors, you will have to increase the discrepancy time.
- Applied value
  The applied value represents the value of the two analog input values that is accepted in the user program.

The system verifies that the two read-in analog values are within the configured tolerance window. If they are, the applied value is written to the lower data memory area of the process input image. If there is a discrepancy and it is the first, it is marked accordingly and the discrepancy time is started.

When the discrepancy time is running, the most recent valid value is written to the process image of the module with the lower address and made available to the current process. If the discrepancy time expires, the module/channel with the configured standard value is declared as valid and the other module/channel is passivated. If the maximum value from both modules is parameterized as the standard value, this value is then taken for further program execution and the other module/channel is passivated. If the minimum value is configured, this module/channel supplies the data to the process and the module with the maximum value is passivated. In any case, the passivated modules/channels are entered in the diagnostic buffer.

If the discrepancy is eliminated within the discrepancy time, analysis of the redundant input signals is still carried out.

NOTICE
The time that the system actually needs to determine a discrepancy depends on various factors: Bus delay times, cycle and call times in the user program, conversion times, etc. Redundant input signals can therefore be different for a longer period than the configured discrepancy time.

Note

There is no discrepancy analysis when a channel reports an overflow with 16#7FFF or an underflow with 16#8000. The relevant module/channel is passivated immediately.

You should therefore disable all unused inputs in HW Config using the "Measurement type" parameter.

Redundant analog input modules with non-redundant encoder

With non-redundant encoders, analog input modules are used in a 1-out-of-2 configuration:

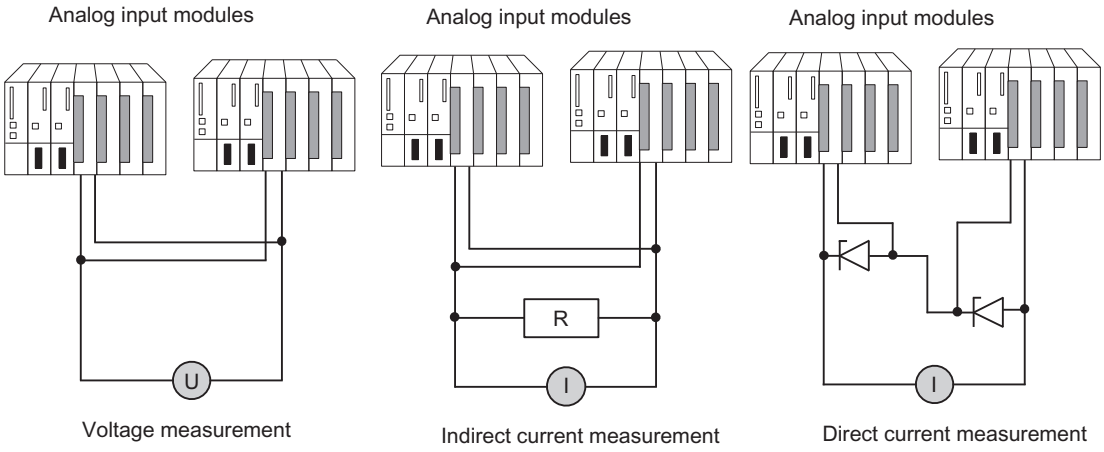


Figure 10-9 Fault-tolerant analog input modules in 1-out-of-2 configuration with one encoder

Remember the following when connecting an encoder to multiple analog input modules:

- Connect the analog input modules in parallel for voltage sensors (left in figure).
- You can convert a current into voltage using an external load to be able to use voltage analog input modules connected in parallel (center in the figure).
- 2-wire transmitters are powered externally to allow you to repair the module online.

The redundancy of the fail-safe analog input modules enhances their availability.

You will find connection examples in Appendix Connection examples for redundant I/Os (Page 359).

Redundant analog input modules for indirect current measurement

The following applies to the wiring of analog input modules:

- Suitable encoders for this circuit are active transmitters with voltage output and thermocouples.
- The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected.
- Suitable encoder types are active 4-wire and passive 2-wire transmitters with output ranges +/-20 mA, 0...20 mA, and 4...20 mA. 2-wire transmitters are powered by an external auxiliary voltage.
- Criteria for the selection of resistance and input voltage range are the measurement accuracy, number format, maximum resolution and possible diagnostics.
- In addition to the options listed, other input resistance and voltage combinations according to Ohm’s law are also possible. Note, however, that such combinations may lead to loss of the number format, diagnostics function and resolution. The measurement error also depends largely on the size of the measure resistance of certain modules.
- Use a measure resistance with a tolerance of +/- 0.1% and TC 15 ppm.

Additional conditions for specific modules

AI 8x12bit 6ES7 331–7K..02–0AB0

- Use a 50 ohm or 250 ohm resistor to map the current on a voltage:

Resistor	50 ohms	250 ohms	
Current measuring range	+/-20 mA	+/-20 mA *)	4...20 mA
Input range to be parameterized	+/-1 V	+/-5 V	1...5 V
Measuring range cube position	"A"	"B"	
Resolution	12 bits + sign	12 bits + sign	12 bits
S7 number format	x	x	
Circuit-specific measuring error - 2 parallel inputs - 1 input	- -	0,5% 0,25%	
"Wire break" diagnostics	-	-	x *)
Load for 4-wire transmitters	50 ohms	250 ohms	
Input voltage for 2-wire transmitters	> 1.2 V	> 6 V	
*) The AI 8x12bit outputs diagnostic interrupt and measured value "7FFF" in the event of wire break.			

The listed measuring error results solely from the interconnection of one or two voltage inputs with a measure resistance. Allowance has neither been made here for the tolerance nor for the basic/operational limits of the modules.

The measuring error for one or two inputs shows the difference in the measurement result depending on whether two inputs or, in case of error, only one input acquires the current of the transmitter.

AI 8x16bit 6ES7 331–7NF00–0AB0

- Use a 250 ohm resistor to map the current on a voltage:

Resistor	250 ohms *)	
Current measuring range	+/-20 mA	4...20 mA
Input range to be parameterized	+/-5 V	1...5 V
Resolution	15 bits + sign	15 bits
S7 number format	x	
Circuit-specific measuring error - 2 parallel inputs - 1 input	- -	
"Wire break" diagnostics	-	x
Load for 4-wire transmitters	250 ohms	
Input voltage for 2-wire transmitters	> 6 V	
*) It may be possible to use the freely connectable internal 250 ohm resistors of the module		

AI 16x16bit 6ES7 431–7QH00–0AB0

- Use a 50 ohm or 250 ohm resistor to map the current on a voltage:

Resistor	50 ohms	250 ohms	
Current measuring range	+/-20 mA	+/-20 mA	4...20 mA
Input range to be configured	+/-1 V	+/-5 V	1...5 V
Measuring range cube position	"A"	"A"	
Resolution	15 bits + sign	15 bits + sign	15 bits
S7 number format	x	x	
Circuit-specific measuring error 1) - 2 parallel inputs - 1 input	- -	- -	
"Wire break" diagnostics	-	-	x
Load for 4-wire transmitters	50 ohms	250 ohms	
Input voltage for 2-wire transmitters	> 1.2 V	> 6 V	

Redundant analog input modules for direct current measurement

Requirements for wiring analog input modules according to Figure 8-10:

- Suitable encoder types are active 4-wire and passive 2-wire transmitters with output ranges +/-20 mA, 0...20 mA, and 4...20 mA. 2-wire transmitters are powered by an external auxiliary voltage.
- The "wire break" diagnostics function supports only the 4...20 mA input range. All other unipolar or bipolar ranges are excluded in this case.
- Suitable diodes include the types of the BZX85 or 1N47..A series (Zener diodes 1.3 W) with the voltages specified for the modules. When selecting other elements, make sure that the reverse current is as low as possible.
- A fundamental measuring error of max. 1 µA results from this type of circuit and the specified diodes due to the reverse current. In the 20 mA range and at a resolution of 16 bits, this value leads to an error of < 2 bits. Individual analog inputs in the circuit above lead to an additional error, which may be listed in the constraints. The errors specified in the manual must be added to these errors for all modules.
- The 4-wire transmitters used must be capable of driving the load resulting from the circuit above. You will find details in the technical specifications of the individual modules.
- When connecting up 2-wire transmitters, note that the Zener diode circuit weighs heavily in the power budget of the transmitter. The required input voltages are therefore included in the technical specifications of the individual modules. Together with the inherent supply specified on the transmitter data sheet, the minimum supply voltage is calculated to $L+ > U_{e-2w} + U_{IS-TR}$

Redundant analog input modules with redundant encoders

With double-redundant encoders, it is better to use fail-safe analog input modules in a 1-out-of-2 configuration:

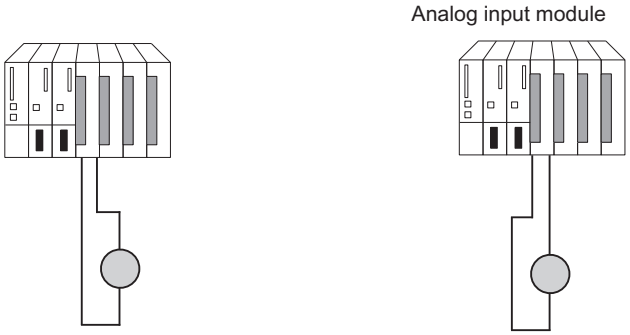


Figure 10-10 Fault-tolerant analog input modules in 1-out-of-2 configuration with two encoders

The use of redundant encoders also increases their availability.

A discrepancy analysis also detects external errors, except for the failure of a non-redundant load voltage supply.

You will find connection examples in Appendix Connection examples for redundant I/Os (Page 359).

The general comments made at the beginning of this documentation apply.

Redundant encoders <-> non-redundant encoders

The table below shows you which analog input modules you can operate in redundant mode with redundant or non-redundant encoders:

Table 10- 4 Analog input modules and encoders

Module	Redundant encoders	Non-redundant encoders
6ES7 431–7QH00–0AB0	X	X
6ES7 336–1HE0x–0AB0	X	-
6ES7 331–7KF02–0AB0	X	X
6ES7 331–7NF00–0AB0	X	X
6ES7 331–7RD00–0AB0	X	X

Redundant analog output modules

You implement fault-tolerant control of a final controlling element by wiring two outputs of two analog output modules in parallel (1-out-of-2 structure).

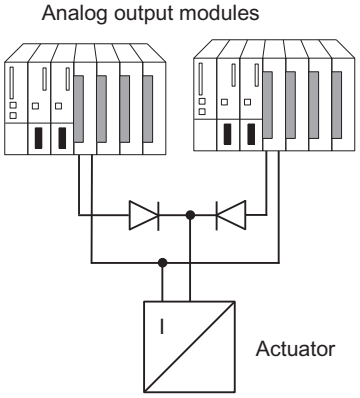


Figure 10-11 Fault-tolerant analog output modules in 1-out-of-2 configuration

The following applies to the wiring of analog output modules:

- Wire the ground connections in a star structure to avoid output errors (limited common-mode suppression of the analog output module).

Information on connecting with diodes

- Suitable diodes are diodes with U_r >=200 V and I_F >= 1 A (e.g. types from the series 1N4003 ... 1N4007).
- A separate load supply is advisable. There must be equipotential bonding between both load supplies.

Analog output signals

Only analog output modules with current outputs (0 to 20 mA, 4 to 20 mA) can be operated redundantly.

The output value is divided by 2, and each of the two modules outputs half. If one of the modules fails, the failure is detected and the remaining module outputs the full value. As a result, the surge at the output module in the event of an error is not as high.

Note

The output value drops briefly to half, and after the reaction in the program it is returned to the proper value. The duration that the output value drops is specified by the following time periods:

- Time period between the initial occurrence of an alarm and the alarm report reaching the CPU.
- Time period until the next FB 453 call.
- Time period until the intact analog output module has doubled the output value.

In the case of passivation or a CPU STOP, redundant analog outputs output a minimum current of approximately 120 µA per module (or 240 µA for HART analog output modules), meaning a total of approximately 240 µA (or 480 µA for HART analog output modules). Considering the tolerance, this means that the output value is always positive. A configured substitute value of 0 mA will produce at least these output values. In redundant mode, in the event of a CPU STOP the response of the current outputs is automatically set to "zero current and zero voltage" in their configuration.

NOTICE
If both channels of a channel pair were passivated (e.g. by OB 85), then nevertheless the respective half current value is output to both storage locations in the process output image. If one channel is depassivated, then the full value is output on the available channel. If this is not required, a substitute value must be written to the lower channels of both modules prior to executing FB 451 "RED_OUT".

Depassivation of modules

Passivated modules are depassivated by the following events:

- When the fault-tolerant system starts up
- When the fault-tolerant system changes over to "redundant" mode
- After system modifications during operation
- If you call FC 451 "RED_DEPA" and at least one redundant channel or module is passivated.

The depassivation is executed in FB 450 "RED IN" after one of these events has occurred. Completion of the depassivation of all modules is logged in the diagnostic buffer.

Note

When a redundant module is assigned a process image partition and the corresponding OB is not available on the CPU, the complete passivation process may take approximately 1 minute.

10.5.3 Evaluating the passivation status

Procedure

First, determine the passivation status by evaluating the status byte in the status/control word "FB_RED_IN.STATUS_CONTROL_W". If you see that one or more modules have been passivated, determine the status of the respective module pairs in MODUL_STATUS_WORD.

Evaluating the passivation status using the status byte

The status word "FB_RED_IN.STATUS_CONTROL_W" is located in the instance DB of FB 450 "RED_IN". The status byte returns information on the status of the redundant I/Os. The assignment of the status byte is described in the online help for the respective block library.

Evaluating the passivation status of individual module pairs by means of MODUL_STATUS_WORD

MODUL_STATUS_WORD is an output parameter of FB 453 and can be interconnected accordingly. It returns information on the status of individual module pairs.

The assignment of the MODUL_STATUS_WORD status byte is described in the online help for the respective function block library.

10.6 Other options for connecting redundant I/Os

Redundant I/O at user level

If you cannot use the redundant I/O supported by your system (section Connecting redundant I/O (Page 132)), for example because the relevant module may not be listed among the supported components, you can implement the use of redundant I/O at the user level.

Configurations

The following redundant I/O configurations are supported:

1. Redundant configuration with one-sided central and/or distributed I/O.

   For this purpose, one signal module each is inserted into the CPU 0 and CPU 1 subsystems.

2. Redundant configuration with switched I/O

   One signal module each is inserted into two ET 200M distributed I/O devices with active backplane bus.

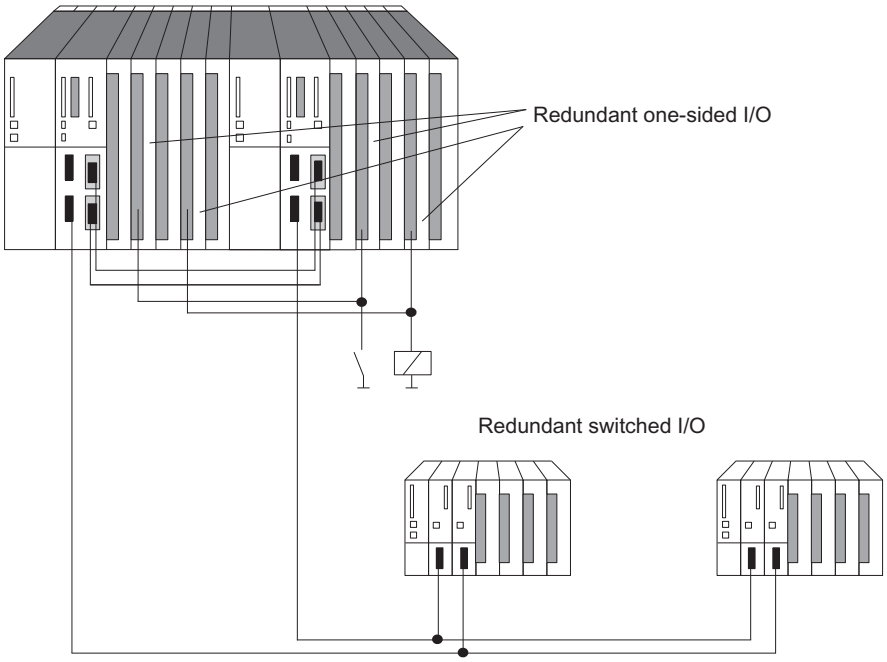


Figure 10-12 Redundant one-sided and switched I/O

NOTICE
When using redundant I/O, you may need to add time to the calculated monitoring times; see section Determining the monitoring times (Page 113)

Hardware configuration and project engineering of the redundant I/O

Strategy recommended for use of redundant I/O:

1. Use the I/O as follows:
   - in a one-sided configuration, one signal module in each subsystem
   - in a switched configuration, one signal module each in two ET 200M distributed I/O devices.
2. Wire the I/O in such a way that it can be addressed by both subsystems.
3. Configure the signal modules so that they have different logical addresses.

NOTICE
It is not advisable to configure the input and output modules with the same logical addresses. Otherwise, in addition to the logical address, you will also need to query the type (input or output) of the defective module in OB 122. The user program also has to update the process image for redundant one-sided output modules when the system is in single mode (direct access, for example). If you use process image partitions, the user program must update them (SFC 27 "UPDAT_PO") in OB 72 (recovery of redundancy). The system would otherwise first output old values on the single-channel one-sided output modules of the reserve CPU when the system changes to redundant mode.

Redundant I/O in the user program

The sample program below shows the use of two redundant digital input modules:

- Module A in rack 0 with logical start address 8 and
- module B in rack 1 with logical start address 12.

One of the two modules is read in OB 1 by direct access. For the following it is generally assumed that the module in question is A (value of variable MODA is TRUE). If no error occurred, processing continues with the value read.

If an I/O area access error has occurred, module B is read by direct access ("second try" in OB 1). If no error occurred, processing of module B continues with the value read. However, if an error has also occurred here, both modules are currently defective, and operation continues with a substitute value.

The sample program is based on the fact that following an access error on module A and its replacement, module B is always processed first in OB 1. Module A is not processed first again in OB 1 until an access error occurs on module B.

NOTICE
The MODA and IOAE_BIT variables must also be valid outside OB 1 and OB 122. The ATTEMPT2 variable, however, is used only in OB 1.

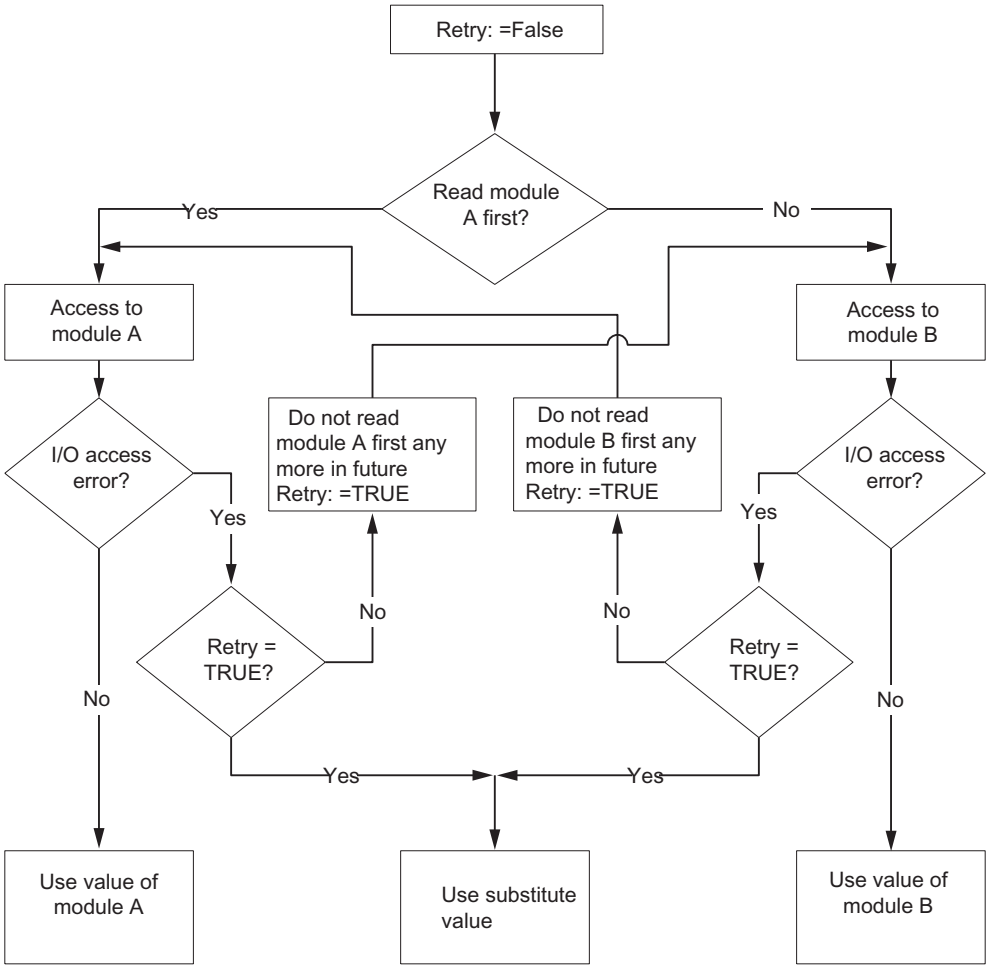


Figure 10-13 Flow chart for OB 1

Example in STL

The required elements of the user program (OB 1, OB 122) are listed below.

Table 10- 5 Example of redundant I/O, OB 1 part

STL	Description
NOP 0;	
SET;	
R ATTEMPT2;	//Initialization
A MODA;	//Read module A first?
JCN CMOB;	//If not, continue with module B
CMOA: SET;	
R IOAE_BIT;	//Delete IOAE bit
L PID 8;	//Read from CPU 0
A IOAE_BIT;	//Was IOAE detected in OB 122?
JCN IOOK;	//If not, process access OK
A ATTEMPT2;	//Was this access the second attempt?
JC CMO0;	//If yes, use substitute value
SET;	
R MODA;	//Do not read module A first any more //in future
S ATTEMPT2;	
CMOB: SET;	
R IOAE_BIT;	//Delete IOAE bit
L PID 12;	//Read from CPU 1
A IOAE_BIT;	//Was IOAE detected in OB 122?
JCN IOOK;	//If not, process access OK
A ATTEMPT2;	//Was this access the second attempt?
JC CMO0;	//If yes, use substitute value
SET;	
S MODA;	//Read module A first again in future
S ATTEMPT2;	
JU CMOA;	
CMO0: L SUBS;	//Substitute value
IOOK:	//The value to be used is in ACCU1

Table 10- 6 Example of redundant I/O, OB 122 part

STL	Description
	// Does module A cause IOAE?
L OB122_MEM_ADDR;	//Relevant logical start address
L W#16#8;	
== I;	//Module A?
JCN M01;	//If not, continue with M01
	//IOAE during access to module A
SET;	
= IOAE_BIT;	//Set IOAE bit
JU CONT;	
	// Does module B cause an IOAE?
M01: NOP 0;	
L OB122_MEM_ADDR;	//Relevant logical start address
L W#16#C;	
== I;	//Module B?
JCN CONT;	//If not, continue with CONT
	//IOAE during access to module B
SET;	
= IOAE_BIT;	//Set IOAE bit
CONT: NOP 0;	

Monitoring times during connect and update

NOTICE
If you have made I/O modules redundant and have taken account of this in your program, you may need to add an overhead to the calculated monitoring times so that no bumps occur at output modules (in HW Config -> Properties CPU -> H Parameter).

An overhead is only required if you operate modules from the following table as redundant modules.

Table 10- 7 For the monitoring times with redundant I/O

Module type	Overhead in ms
ET200M: Standard output modules	2
ET200M: HART output modules	10
ET200M: F output modules	50
ET200L–SC with analog outputs	≤ 80
ET200S with analog outputs or technology modules	≤ 20

Follow the steps below:

- Calculate the overhead from the table. If you use several module types from the table redundantly, apply the largest overhead.
- Add this to all of the monitoring times calculated so far.

Communication 11

11.1 Communication

This section provides an introduction to communications with fault-tolerant systems and their specific characteristics.

It sets out the basic concepts, the bus systems you can use for fault-tolerant communication, and the available types of connection.

It contains information on communication functions using fault-tolerant and standard connections, and explains how to configure and program them.

- You will also find examples of communication over **fault-tolerant S7 connections** and learn about the advantages it offers.
- By way of comparison, you will learn how communication takes place over **S7 connections** and how you can also communicate in redundant mode by means of S7 connections.

11.2 Fundamentals and basic concepts

Overview

Increased demands on the availability of an overall system require increased reliability of the communication systems, which means implementing redundant communication.

Below you will find an overview of the fundamentals and basic concepts which you ought to know with regard to using fault-tolerant communications.

Redundant communication system

The availability of the communication system can be enhanced by redundancy of the media, duplication of component units, or duplication of all bus components.

On failure of a component, the various monitoring and synchronization mechanisms ensure that the communication functions are taken over by the reserve components during operation.

A redundant communication system is essential if you want to use fault-tolerant S7 connections.

Fault-tolerant communication

Fault-tolerant communication is the deployment of S7 communication SFBs over fault-tolerant S7 connections.

Fault-tolerant S7 connections are only possible when using redundant communication systems.

Redundancy nodes

Redundancy nodes represent extreme reliability of communication between two fault-tolerant systems. A system with multi-channel components is represented by redundancy nodes. Redundancy nodes are independent when the failure of a component within the node does not result in any reliability impairment in other nodes.

Even with fault-tolerant communication, only single errors/faults can be tolerated. If more than one error occurs between communication endpoints, communication can no longer be guaranteed.

Connection (S7 connection)

A connection represents the logical assignment of two communication peers for executing a communication service. Every connection has two end points containing the information required for addressing the communication peer as well as other attributes for establishing the connection.

An S7 connection is the communication link between two standard CPUs or from a standard CPU to a CPU in a fault-tolerant system.

In contrast to a fault-tolerant S7 connection, which contains at least two partial connections, an S7 connection actually consists of just one connection. If that connection fails, communication is terminated.

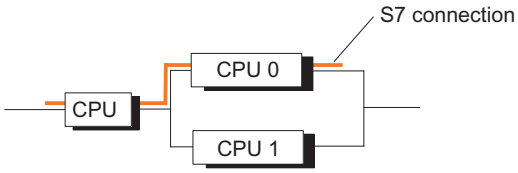


Figure 11-1 Example of an S7 connection

Note

Generally speaking, "connection" in this manual means a "configured S7 connection". For other types of connection, please refer to the *SIMATIC NET NCM S7 for PROFIBUS* and *SIMATIC NET NCM S7 for Industrial Ethernet* manuals.

Fault-tolerant S7 connections

The requirement for higher availability with communication components (for example CPs and buses) means that redundant communication connections are necessary between the systems involved.

Unlike an S7 connection, a fault-tolerant S7 connection consists of at least two underlying subconnections. From the user program, configuration and connection diagnostics perspective, the fault-tolerant S7 connection with its underlying subconnections is represented by exactly one ID (just like a standard S7 connection). Depending on the configuration, it can consist of up to four subconnections, of which two are always established (active) to maintain communication in the event of an error. The number of subconnections depends on the possible alternative paths (see figure below) and is determined automatically.

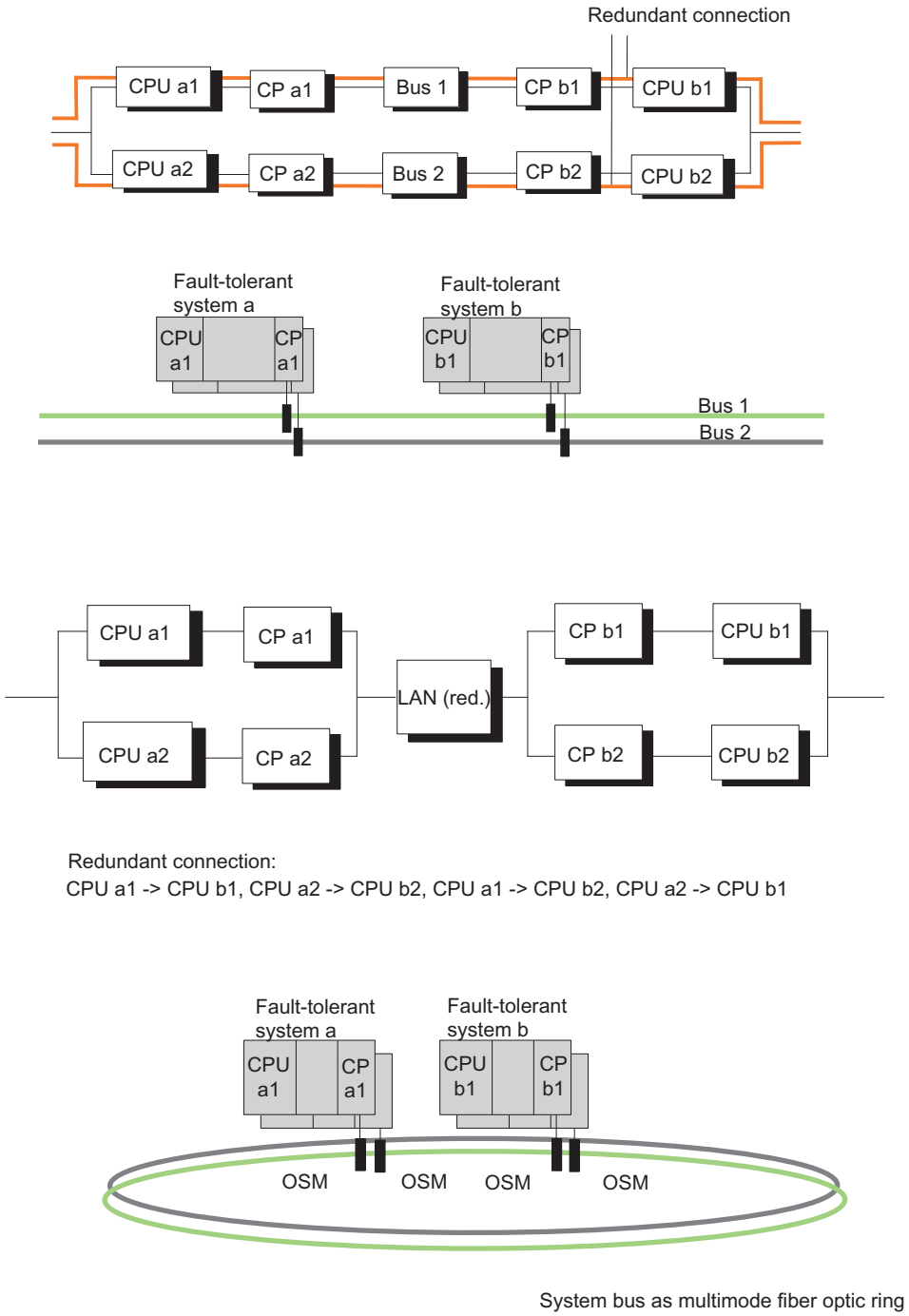


Figure 11-2 Example that shows that the number of resulting partial connections depends on the configuration

If the active subconnection fails, the already established second subconnection automatically takes over communication.

Resource requirements of fault-tolerant S7 connections

The fault-tolerant CPU supports the operation of 62/30/14 (see the technical specifications) fault-tolerant S7 connections. On the CP each subconnection requires a connection resource.

NOTICE
If you have configured several fault-tolerant S7 connections for a fault-tolerant station, establishing them may take a considerable time. If the configured maximum communication delay is set too short, link-up and updating is canceled and the redundant system mode is no longer reached (see section Time monitoring (Page 109)).

11.3 Usable networks

Your choice of the physical transmission medium depends on the required expansion, targeted fault tolerance, and transfer rate. The following bus systems are used for communication with fault-tolerant systems:

- Industrial Ethernet (fiber-optic cable, triaxial or twisted-pair copper cable)
- PROFIBUS (fiber-optic cable or copper cable)

For additional information on suitable networks, refer to the "*Communication with SIMATIC*", "*Industrial Twisted Pair Networks*", and "*PROFIBUS Networks*" manuals.

11.4 Usable communication services

The following services can be used:

- S7 communication using fault-tolerant S7 connections via PROFIBUS and Industrial Ethernet. Fault-tolerant S7 connections are possible only between SIMATIC S7 stations. Fault-tolerant communication is possible over Industrial Ethernet only with the ISO protocol
- S7 communication using S7 connections via MPI, PROFIBUS, and Industrial Ethernet
- Standard communication (e.g. FMS) via PROFIBUS
- S5-compatible communication (e.g. SEND and RECEIVE blocks) via PROFIBUS and Industrial Ethernet

The following are not supported:

- S7 basic communication
- Global data communication
- Open communication via Industrial Ethernet

11.5 Communication via fault-tolerant S7 connections

Availability of communicating systems

Fault-tolerant communication expands the overall SIMATIC system by additional, redundant communication components such as CPs and bus cables. To illustrate the actual availability of communicating systems when using an optical or electrical network, a description is given below of the possibilities for communication redundancy.

Requirement

The essential requirement for the configuration of fault-tolerant connections with STEP 7 is a configured hardware installation.

The hardware configuration in both subsystems of a fault-tolerant system **must** be identical. This applies in particular to the slots.

Depending on the network used, CPs can be used for fault-tolerant and fail-safe communication, see Appendix Function modules and communication processors supported by the S7-400H (Page 355)
Only Industrial Ethernet with the ISO protocol or PROFIBUS without distributed I/O is supported. You require a suitable CP for fault-tolerant S7 connections via PROFIBUS. These connections are not possible via the internal PROFIBUS-DP interface.

To be able to use fault-tolerant S7 connections between a fault-tolerant system and a PC, you must install the "S7-REDCONNECT" software package on the PC. Please refer to the Product Information on "S7-REDCONNECT" to learn more about the CPs you can use at the PC end.

Configuration

The availability of the system, including the communication, is set during configuration. Refer to the STEP 7 documentation to find out how to configure connections.

Only S7 communication is used for fault-tolerant S7 connections. To set this up, open the "New Connection" dialog box, then select "S7 Connection Fault-Tolerant" as the type.

The number of required redundant connections is determined by STEP 7 as a function of the redundancy nodes. Up to four redundant connections can be generated, if supported by the network. Higher redundancy cannot be achieved even by using more CPs.

In the "Properties - Connection" dialog box you can also modify specific properties of a fault-tolerant connection if necessary. When using more than one CP, you can also route the connections in this dialog box. This may be practical, because by default all connections are routed initially through the first CP. If all the connections are busy there, any further connections are routed via the second CP, etc.

Programming

Fault-tolerant communication can be implemented on the fault-tolerant CPU and is implemented by means of S7 communication.

This is possible only within an S7 project/multiproject.

Fault-tolerant communication is programmed in STEP 7 by means of communication SFBs. Those blocks can be used to transfer data on subnets (Industrial Ethernet, PROFIBUS). The standard communication SFBs integrated into the operating system offer you the option of acknowledged data transfer. In addition to data transfer, you can also use other communication functions for controlling and monitoring the communication peer.

User programs written for standard communication can also be run for fault-tolerant communication without modification. Cable and connection redundancy has no effect on the user program.

Note

For information on programming the communication, refer to the STEP 7 documentation (e.g. *Programming with STEP 7*).

The START and STOP communication functions act on exactly one CPU or on all CPUs of the fault-tolerant system (for more details refer to the *System Software for S7-300/400, System and Standard Functions* Reference Manual).

Any disruption of subconnections while communication jobs are active over fault-tolerant S7 connections leads to extended delay times.

NOTICE
Downloading the connection configuration during operation If you download a connection configuration during operation, any established connections could be canceled.

11.5.1 Communication between fault-tolerant systems

Availability

The easiest way to enhance availability between linked systems is to implement a redundant plant bus, using a duplex fiber-optic ring or a dual electrical bus system. The connected nodes may consist of simple standard components.

Availability can best be enhanced using a duplex fiber-optic ring. If the one of the multimode fiber-optic cables breaks, communication between the systems involved is maintained. The systems then communicate as if they were connected to a bus system (line). A ring topology basically contains two redundant components and automatically forms a 1-out-of-2 redundancy node. A fiber-optic network can be set up as a line or star topology. However, the line topology does not permit cable redundancy.

If one electrical cable segment fails, communication between the participating systems is also upheld (1-out-of-2 redundancy).

The examples below illustrate the differences between the two variants.

Note

The number of connection resources required on the CPs depends on the network used.

If you implement a duplex fiber-optic ring (see figure below), two connection resources are required per CP. In contrast, only one connection resource is required per CP if a double electrical network (see figure after next) is used.

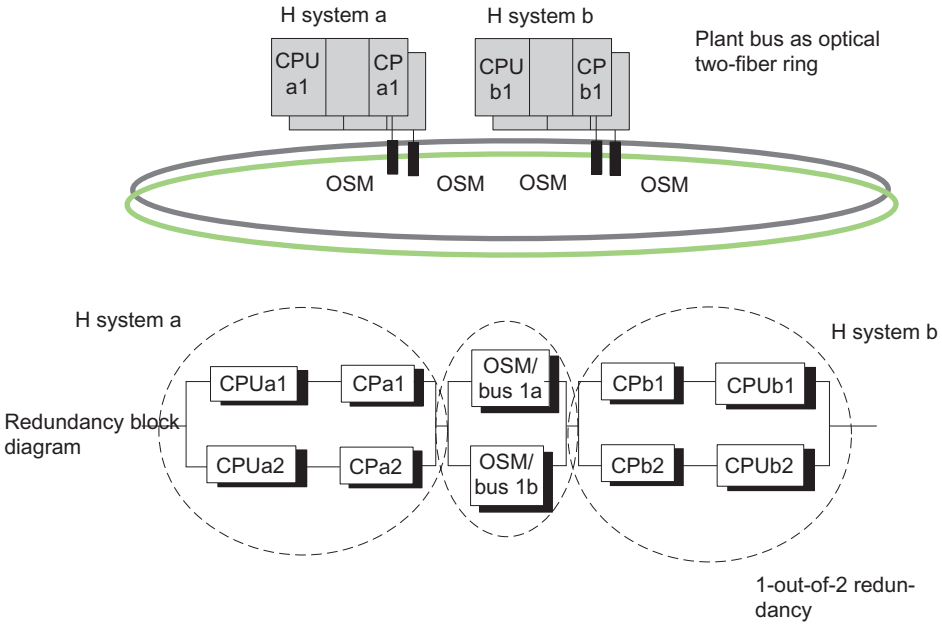


Figure 11-3 Example of redundancy with fault-tolerant system and redundant ring

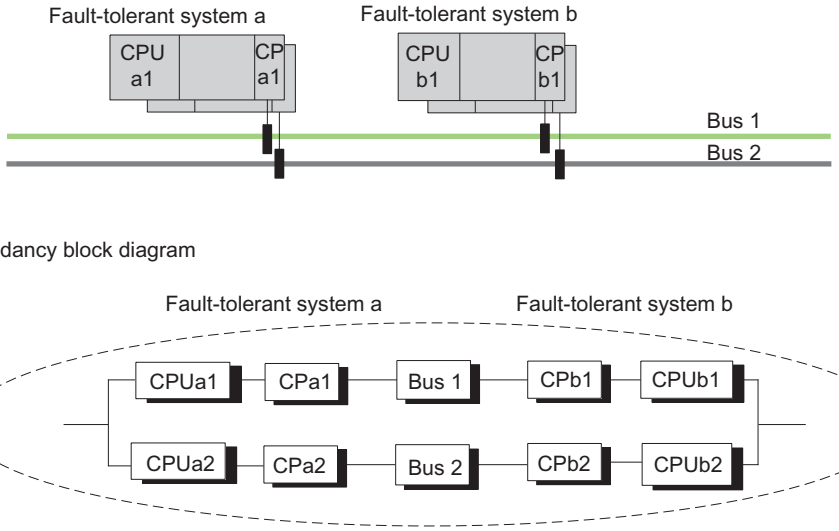


Figure 11-4 Example of redundancy with fault-tolerant system and redundant bus system

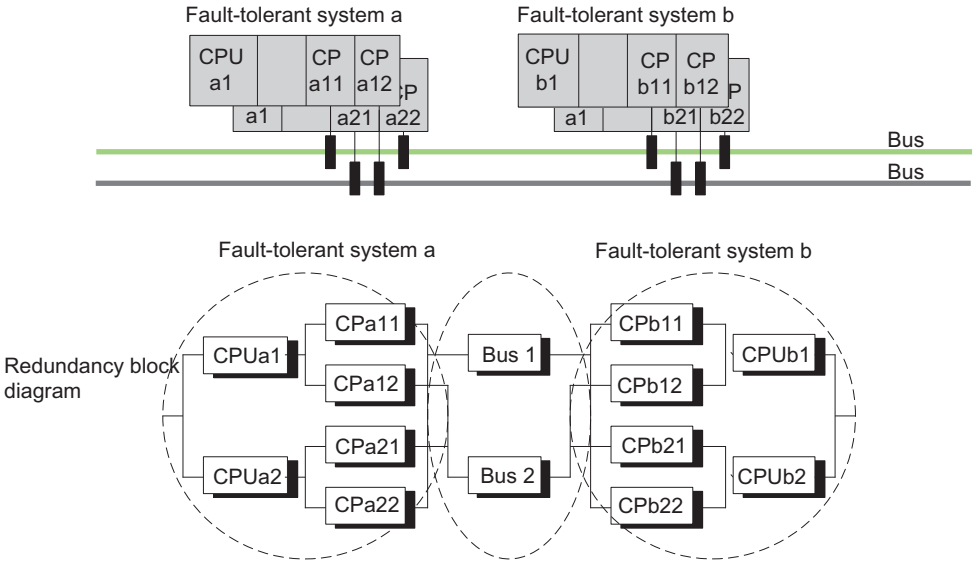


Figure 11-5 Example of fault-tolerant system with additional CP redundancy

Response to failure

If a duplex fiber-optic ring is used, only a double error within a fault-tolerant system (e.g. CPUa1 and CPa2 in one system) leads to total failure of communication between the systems involved (see first figure).

If a double error (e.g. CPUa1 and CPb2) occurs in the first case of a redundant electrical bus system (see second figure), this results in a total failure of communication between the systems involved.

In the case of a redundant electrical bus system with CP redundancy (see third figure), only a double error within a fault-tolerant system (e.g. CPUa1 and CPUa2) or a triple error (e.g. CPUa1, CPa22, and bus2) will result in a total failure of communication between the systems involved.

Fault-tolerant S7 connections

Any disruption of subconnections while communication jobs are active over fault-tolerant S7 connections leads to extended delay times.

11.5.2 Communication between fault-tolerant systems and a fault-tolerant CPU

Availability

Availability can be enhanced by using a redundant plant bus and by using a fault-tolerant CPU in a standard system.

If the communication peer is a fault-tolerant CPU, redundant connections can also be configured, in contrast to systems with a CPU 416, for example.

Note

Fault-tolerant connections use two connection resources on CP b1 for the redundant connections. One connection resource each is occupied on CP a1 and CP a2 respectively. In this case, the use of further CPs in the standard system only serves to increase the resources.

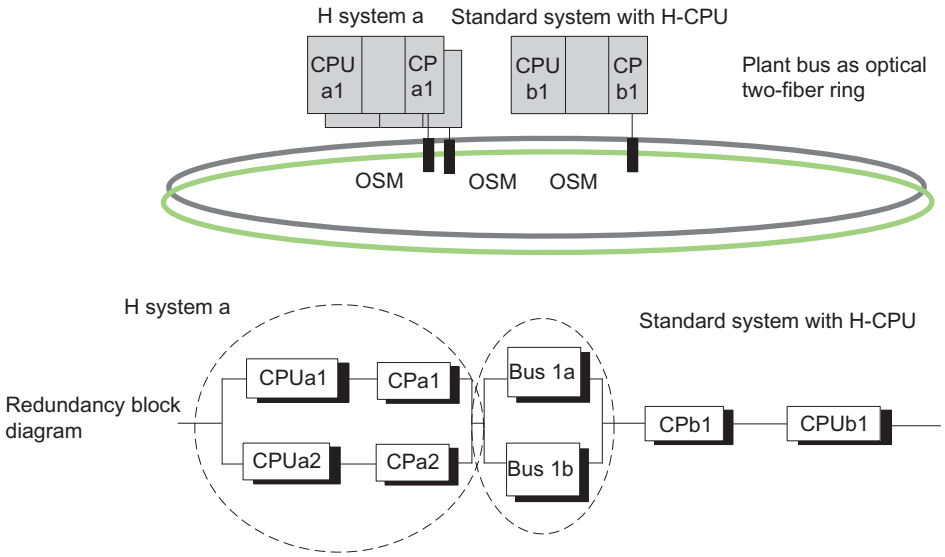


Figure 11-6 Example of redundancy with fault-tolerant system and fault-tolerant CPU

Response to failure

Double errors in the fault-tolerant system (i.e. CPUa1 and CPa2) or single errors in a standard system (CPUb1) lead to a total failure of communication between the systems involved; see previous figure.

11.5.3 Communication between fault-tolerant systems and PCs

Availability

When fault-tolerant systems are linked to a PC, the availability of the overall system is concentrated not only on the PCs (OS) and their data management, but also on data acquisition in the automation systems.

PCs are not fault-tolerant due to their hardware and software characteristics. They can be arranged redundantly within a system, however. The availability of such a PC (OS) system and its data management is ensured by means of suitable software such as WinCC Redundancy.

Communication takes place via fault-tolerant connections.

The "S7-REDCONNECT" software package, V1.3 or higher, is essential for fault-tolerant communication on a PC. It supports the connection of a PC to a fiber-optic network with one CP, or to a redundant bus system with 2 CPs.

Configuring connections

The PC must be engineered and configured as a SIMATIC PC station. Additional configuration of fault-tolerant communication is not necessary at the PC end. Connection configuration is handled by the STEP 7 project in the form of an XDB file at the PC end.

You can find out how to use STEP 7 to integrate fault-tolerant S7 communication for a PC into your OS system in the WinCC documentation.

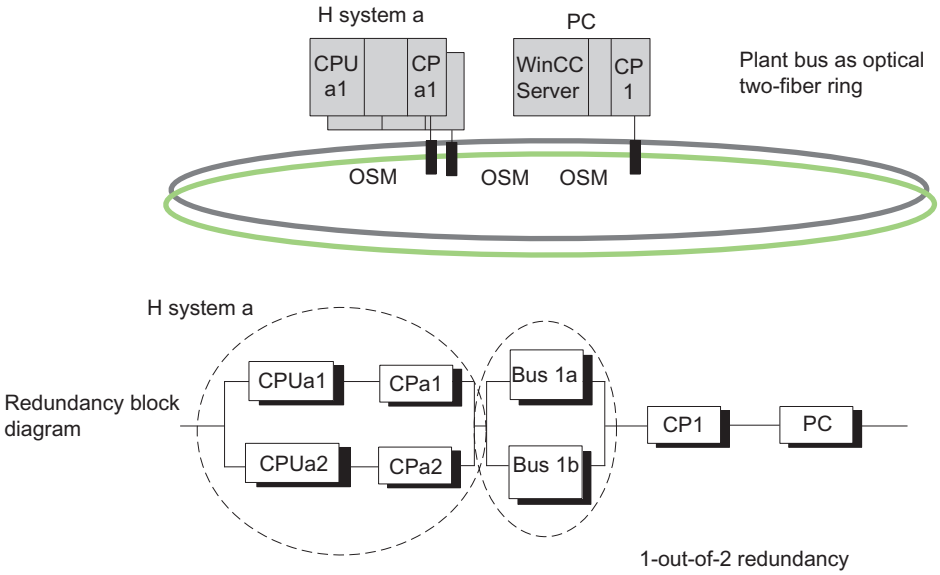


Figure 11-7 Example of redundancy with fault-tolerant system and redundant bus system

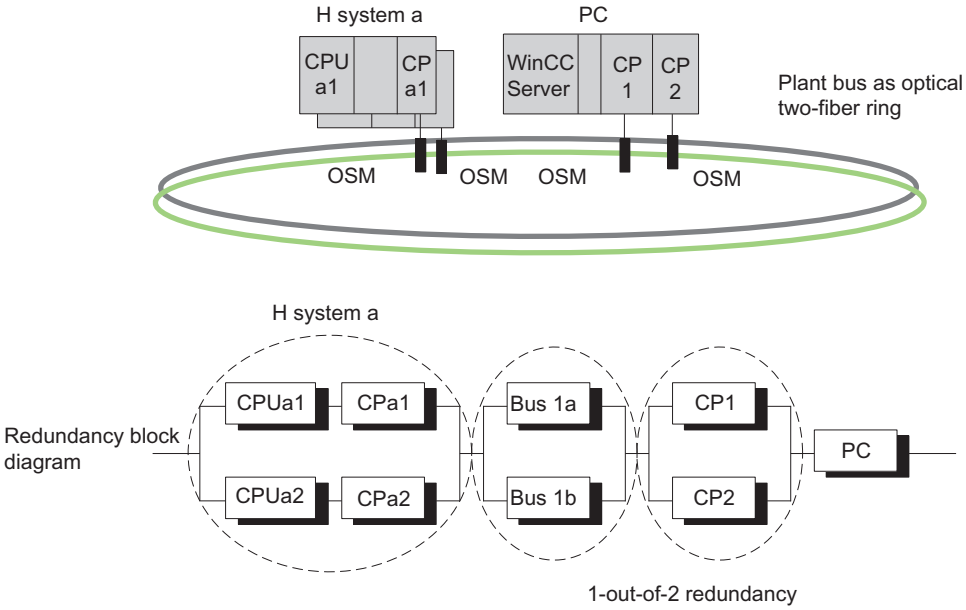


Figure 11-8 Example of redundancy with a fault-tolerant system, redundant bus system, and CP redundancy on PC.

Response to failure

Double errors in the fault-tolerant system (i.e. CPUa1 and CPa2) and failure of the PC result in a total failure of communication between the systems involved (see previous figures).

PC/PG as Engineering System (ES)

To be able to use a PC as Engineering System, you need to configure it under its name as a PC station in HW Config. The ES is assigned to a CPU and is capable of executing STEP 7 functions on that CPU.

If the CPU fails, communication between the ES and the fault-tolerant system is no longer possible.

11.6 Communication via S7 connections

Communication with standard systems

Fault-tolerant communication between fault-tolerant and standard systems is not supported. The following examples illustrate the actual availability of the communicating systems.

Configuration

S7 connections are configured in STEP 7.

Programming

All communication functions are supported for standard communication on a fault-tolerant system.

The communication SFBs are used in STEP 7 to program communication.

Note

The START and STOP communication functions act on exactly one CPU or on all CPUs of the fault-tolerant system (for more details refer to the *System Software for S7-300/400, System and Standard Functions* Reference Manual).

NOTICE
Downloading the connection configuration during operation If you download a connection configuration during operation, any established connections could be canceled.

11.6.1 Communication via S7 connections - one-sided mode

Availability

Availability is also enhanced by using a redundant plant bus instead of a simple bus (see image below) for communication between a fault-tolerant system and a standard system.

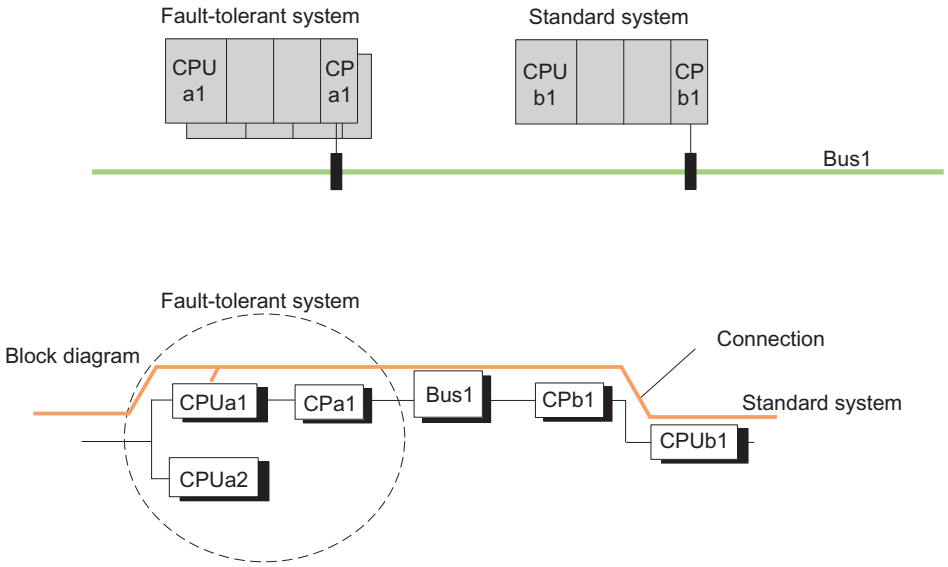


Figure 11-9 Example of linking standard and fault-tolerant systems in a simple bus system

In this configuration, the CPUa2 is connected to the standard system in redundant mode via the reserve CPU and CPb1. This applies no matter which CPU is the master CPU.

On a plant bus configured as duplex fiber-optic ring, communication between the partner systems is maintained if the duplex fiber-optic cable breaks. The systems then communicate as if they were connected to a bus system (linear structure); see following figure.

For linked fault-tolerant and standard systems, the availability of communication cannot be improved by means of a dual electrical bus system. To use the second bus system as a redundant system, you will have to use and manage a second S7 connection in the user program (see figure after next one).

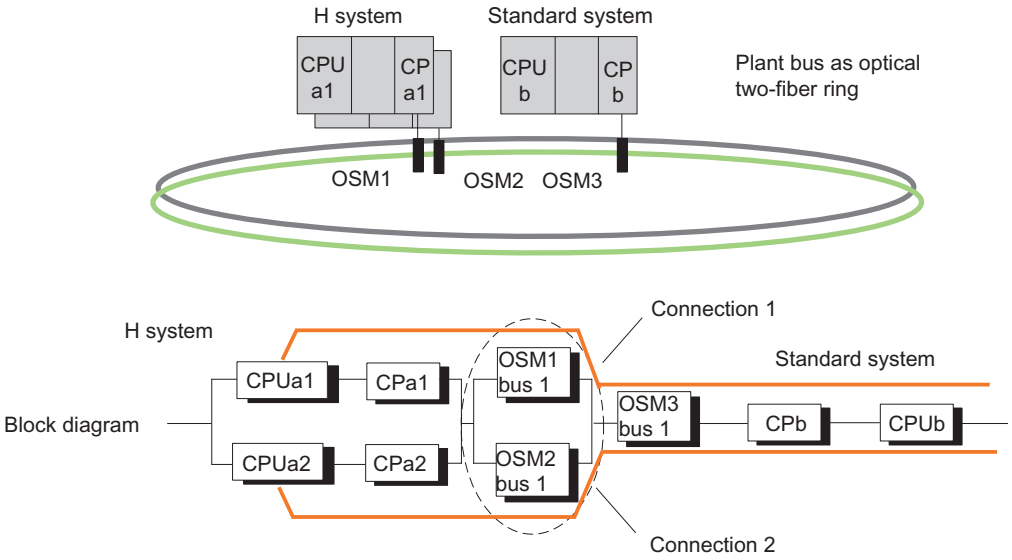


Figure 11-10 Example of linking of standard and fault-tolerant systems in a redundant ring

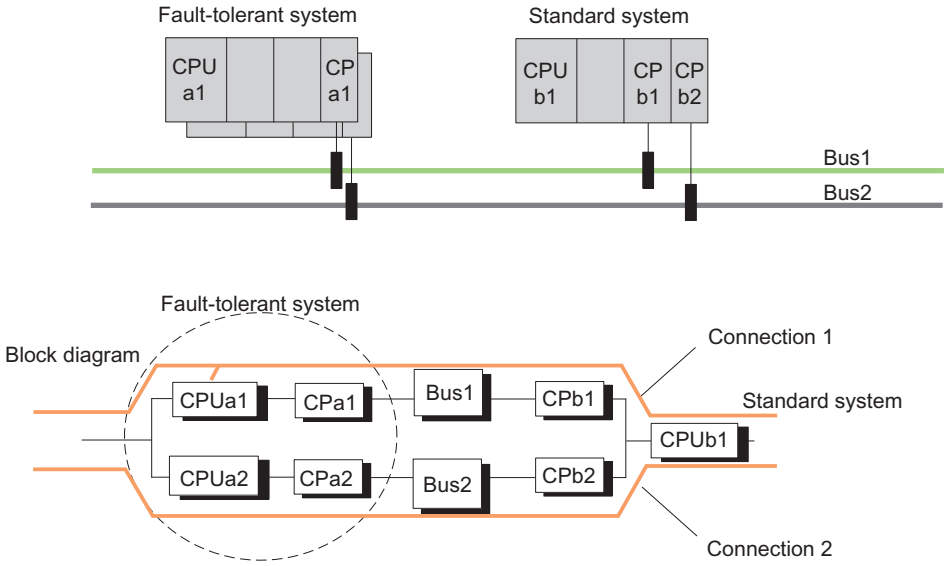


Figure 11-11 Example of linking standard and fault-tolerant systems in a redundant bus system

Response to failure

Duplex fiber-optic ring and bus system

Because standard S7 connections are used here (the connection ends at the CPU of the subsystem, in this case CPUa1), an error in the fault-tolerant system (e.g. CPUa1 or CPa1) or an error in system b (e.g. CP b) results in total failure of communication between the systems involved (see previous figures).

There are no bus system-specific differences in the response to failure.

Linking standard and fault-tolerant systems

Driver block "S7H4_BSR": You can link a fault-tolerant system to an S7-400 / S7-300 using the "S7H4_BSR" driver block. For more detailed information, contact the H/F Competence Center
E-mail: hf-cc.aud@siemens.com

Alternative: SFB 15 "PUT" and SFB 14 "GET" in the fault-tolerant system: As an alternative, use two SFB 15 "PUT" blocks over two standard connections. First call the first block. If there was no error message when the block executed, the transfer is assumed to have been successful. If there was an error message, the data transfer is repeated via the second block. If a connection cancelation is detected later, the data is also transferred again to exclude possible information losses. You can use the same method with an SFB 14 "GET".

If possible, use the mechanisms of S7 communication for communication.

11.6.2 Communication via redundant S7 connections

Availability

Availability can be enhanced by using a redundant plant bus and two separate CPs in a standard system.

Redundant communication can also be operated with standard connections. For this two separate S7 connections must be configured in the program in order to implement connection redundancy. In the user program, both connections require the implementation of monitoring functions in order to allow the detection of failures and to change over to the standby connection.

The following figure shows such a configuration.

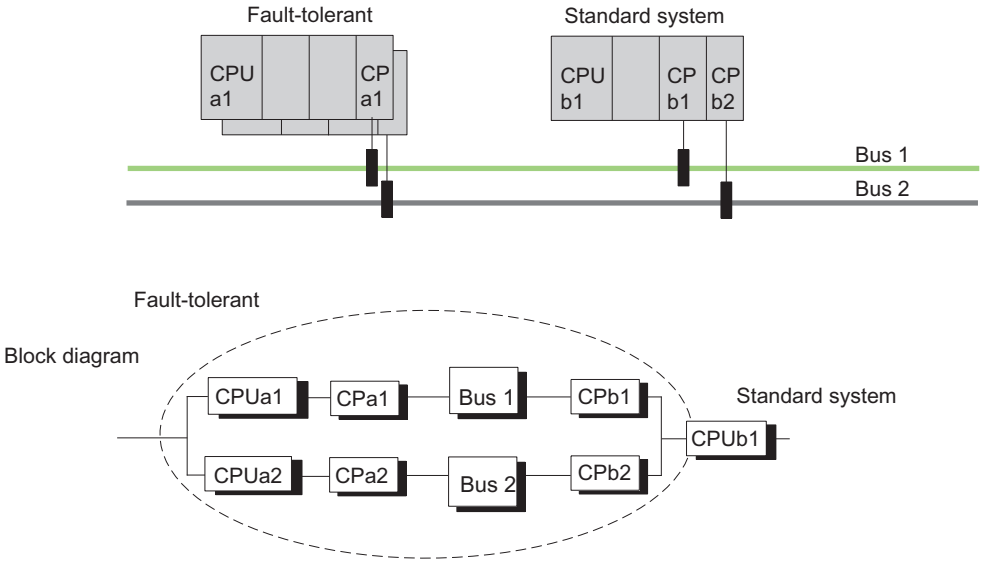


Figure 11-12 Example of redundancy with fault-tolerant systems and a redundant bus system with redundant standard connections

Response to failure

Double errors in the fault-tolerant system (i.e. CPUa1 and CPa 2) or in the standard system (CPb1 and CPb2), and single errors in the standard system (CPUb1) lead to a total failure of communication between the systems involved (see previous figure).

11.6.3 Communication via point-to-point CP on the ET 200M

Connection via ET 200M

Links from fault-tolerant systems to single-channel systems are often possible only by way of point-to-point connections, as many systems offer no other connection options.

In order to make the data of a single-channel system available to CPUs of the fault-tolerant system as well, the point-to-point CP (CP 341) must be installed in a distributed rack along with two IM 153-2 modules.

Configuring connections

Redundant connections between the point-to-point CP and the fault-tolerant system are not necessary.

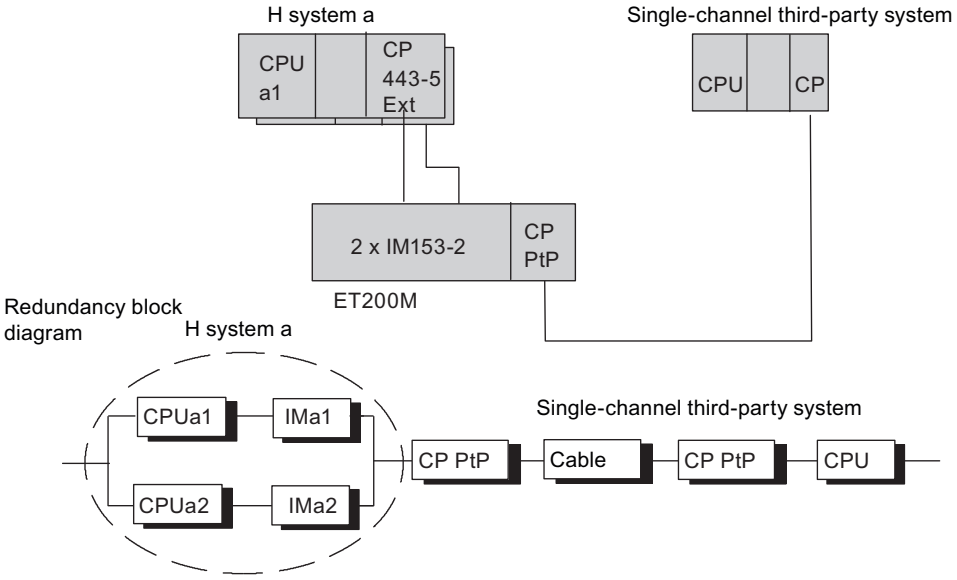


Figure 11-13 Example of connecting a fault-tolerant system to a single-channel third-party system

Response to failure

Double errors in the fault-tolerant system (i.e. CPUa1 and IM 153-2) and single errors in the third-party system lead to a total failure of communication between the systems involved (see previous figure).

The point-to-point CP can also be inserted centrally in "Fault-tolerant system a". However, in this configuration even the failure of the CPU, for example, will cause a total failure of communication.

11.6.4 Custom connection to single-channel systems

Connection via PC as gateway

Fault-tolerant systems and single-channel systems can also be via a gateway (no connection redundancy). The gateway is connected to the system bus by one or two CPs, depending on availability requirements. Fault-tolerant connections can be configured between the gateway and the fault-tolerant systems. The gateway allows you to link any kinds of single-channel system (e.g. TCP/IP with a manufacturer-specific protocol).

A user-programmed software instance in the gateway implements the single-channel transition to the fault-tolerant systems, and so allows any single-channel systems to be linked to a fault-tolerant system.

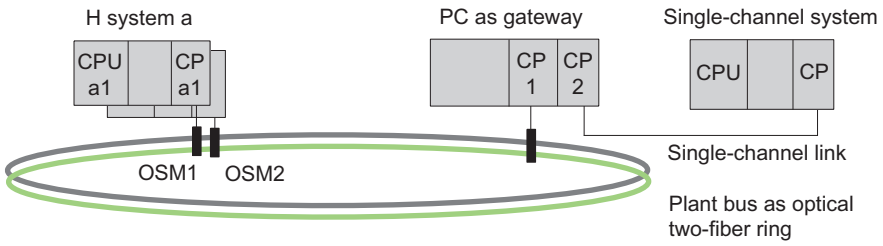
Configuring connections

Redundant connections between the gateway CP and the single-channel system are not required.

The gateway CP is located on a PC system which has fault-tolerant connections to the fault-tolerant system.

To configure fault-tolerant S7 connections between fault-tolerant system A and the gateway, you first need to install S7-REDCONNECT on the gateway. The functions for preparing data for their transfer via the single-channel link must be implemented in the user program.

For additional information, refer to the "*Industrial Communications IK10*" Catalog.



Redundancy block diagram

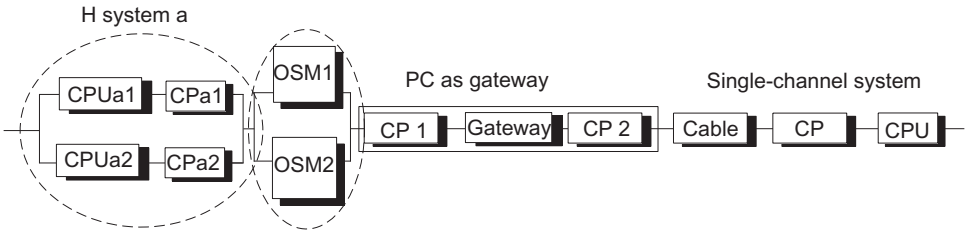


Figure 11-14 Example of linking a fault-tolerant system to a single-channel third-party system

11.7 Communication performance

Compared to a fault-tolerant CPU in stand-alone mode or standard CPU, the communication performance (response time or data throughput) of a fault-tolerant system operating in redundant mode is significantly lower.

The aim of this description is to provide you with criteria which allow you to assess the effects of the various communication mechanisms on communication performance.

Definition of communication load

Communication load is the sum of requests per second issued to the CPU by the communication mechanisms, plus the requests and messages issued by the CPU.

Higher communication load increases the response time of the CPU, meaning the CPU takes more time to respond to a request (such as a read job) or to output requests and messages.

Operating range

In every automation system there is a linear operating range in which an increase in communication load will also lead to an increase in data throughput. This then results in reasonable response times which are acceptable for the automation task at hand.

A further increase in communication load will push data throughput into the saturation range. Under certain conditions, the automation system therefore may no longer be capable of processing the request volume within the response time demanded. Data throughput reaches its maximum, and the reaction time rises exponentially; see the figures below.

Data throughput may even be reduced somewhat due to additional internal loads inside the device.

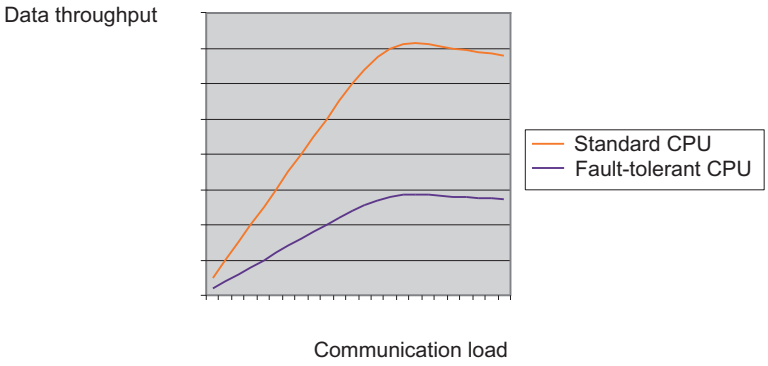


Figure 11-15 Communication load as a variable of data throughput (basic profile)

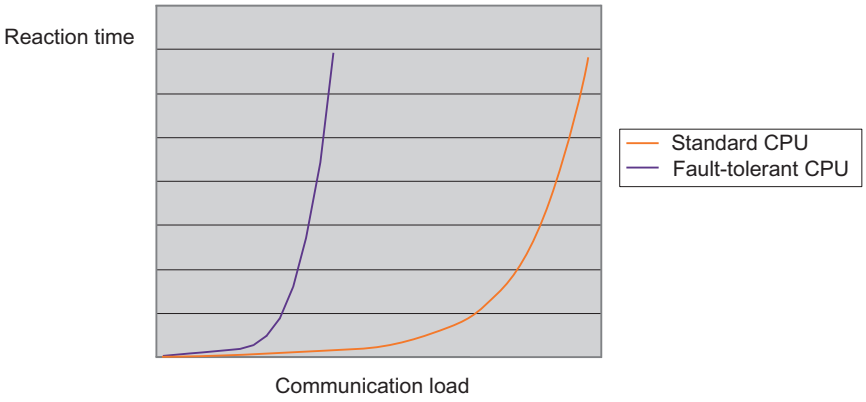


Figure 11-16 Communication load as a variable of response time (basic profile)

Standard and fault-tolerant systems

The information above applies to standard and fault-tolerant systems. Since communication performance in standard systems is clearly higher than that of redundant, fault-tolerant systems, the saturation point is rarely reached in today's plants.

In contrast, fault-tolerant systems require synchronization to maintain synchronous operation. This increases block execution times and reduces communication performance, This means that performance limits are reached earlier. If the redundant, fault-tolerant system is not operating at its performance limits, the performance benchmark compared to the standard system will be lower by the factor 2 to 3.

Which variables influence communication load?

The communication load is affected by the following variables:

- Number of connections/connected HMI systems
- Number of tags, or number of tags in screens displayed on OPs or using WinCC.
- Communication type (HMI, S7 communication, S7 message functions, S5-compatible communication, ...)
- The configured maximum cycle time extension as a result of communication load

The sections below show the factors that influence communication performance.

11.8 General issues regarding communication

Reduce the rate of communication jobs per second as far as possible. Utilize the maximum user data length for communication jobs, for example by grouping several tags or data areas in one read job.

Each request requires a certain processing time, and its status should therefore not be checked before this process is completed.

You can download a tool for the assessment of processing times free of charge from the Internet at:

Service & Support (http://www.siemens.com/automation/service&support) ID 1651770

Your calls of communication jobs should allow the event-driven transfer of data. Check the data transfer event only until the job is completed.

Call the communication blocks sequentially and stepped down within the cycle in order to obtain a balanced distribution of communication load.

You can by-pass the block call command by means of a conditional jump if you do not want to transfer any user data.

A significant increase in communication performance between S7 components is achieved by using S7 communication functions, rather than S5-compatible communication functions.

As S5-compatible communication functions (FB "AG_SEND", FB "AG_RECV", AP_RED) generate a significantly higher communication load, you should only deploy these for the communication of S7 components with non-S7 components.

AP_RED software package

When using the "AP_RED" software package, limit the user data length to 240 bytes. If larger data volumes are necessary, transfer those by means of sequential block calls.

The "AP_RED" software package uses the mechanisms of FB "AG_SEND" and FB "AG_RCV". Use AP_RED only to link SIMATIC S5/S5-H controllers or third-party devices which only support S5-compatible communication.

S7 communication (SFB 12 "BSEND" and SFB 13 "BRCV")

Do not call SFB 12 "BSEND" in the user program more often than the associated SFB 13 "BRCV" at the communication peer.

S7 communication (SFB 8 "USEND" and SFB 9 "URCV")

SFB 8 "USEND" should always be event-driven, because this block may generate a high communication load.

Do not call SFB 8 "USEND" in the user program more often than the associated SFB 9 "URCV" at the communication peer.

SIMATIC OPs, SIMATIC MPs

Do not install more than 4 OPs or 4 MPs in a fault-tolerant system. If you do need more OPs/MPs, your automation task may have to be revised. Contact your SIMATIC sales partner for support.

Do not select a screen refresh cycle time of less than 1 s, and increase it to 2 s as required.

Verify that all screen tags are requested within the same cycle time in order to form an optimized group for read jobs.

OPC servers

When OPC is used to connect several HMI devices for your visualization tasks to a fault-tolerant system, you should keep the number of OPC servers accessing the fault-tolerant system as low as possible. OPC clients should address a shared OPC server, which then fetches the data from the fault-tolerant system.

You can optimize data exchange by using WinCC and its client/server concept.

Various HMI devices of third-party vendors support the S7 communication protocol. You should utilize this option.

Configuring with STEP 7

12

12.1 Configuring with STEP 7

This section provides an overview of fundamental issues to be observed when you configure a fault-tolerant system.

The second section covers the PG functions in STEP 7.

For detailed information, refer to *Configuring fault-tolerant systems* in the basic help.

12.2 Configuring with STEP 7

The basic approach to configuring the S7-400H is no different from that used to configure the S7-400:

- Creating projects and stations
- Configuring hardware and networking
- Loading system data onto the target system

Even the individual steps that are required for this are identical for the most part to those familiar from the S7-400.

NOTICE
OBs required Always download these error OBs to the S7-400H CPU: OB 70, OB 72, OB 80, OB 82, OB 83, OB 85, OB 86, OB 87, OB 88, OB 121 and OB 122. If you do not download these OBs, the fault-tolerant system goes into STOP when an error occurs.

Creating a fault-tolerant station

The SIMATIC fault-tolerant station represents a separate station type in SIMATIC Manager. It allows the configuration of two central units, each having a CPU and therefore a redundant station configuration.

12.2.1 Rules for arranging fault-tolerant station components

The following rules have to be complied with for a fault-tolerant station, in addition to the rules that generally apply to the arrangement of modules in the S7-400:

- The CPUs have to be inserted in the same slots.
- Redundantly used external DP master interfaces or communication modules must be inserted in the same slots in each case.
- External DP master interfaces for redundant DP master systems must only be inserted in central devices rather than in expansion devices.
- Redundantly used modules (for example, CPU 417-4H, DP slave interface module IM 153-2) must be identical, i.e. they must have the same order number, the same product version, and the same firmware version.

Layout rules

- A fault-tolerant station may contain up to 20 expansion racks.
- Even-numbered mounting racks can be assigned only to central rack 0, whereas odd-numbered mounting racks can be assigned only to central rack 1.
- Modules with communication bus interface can be operated only in racks 0 through 6.
- Communication-bus capable modules are not permissible in switched I/O.
- Pay attention to the mounting rack numbers when operating CPs for fault-tolerant communication in expansion racks:

  The numbers must be directly sequential and begin with the even number, e.g. rack numbers 2 and 3, but not rack numbers 3 and 4.
- A rack number is also assigned for DP master no. 9 onwards if the central rack contains DP master modules. The number of possible expansion racks is reduced as a result.

Compliance with the rules is monitored automatically by STEP 7 and considered accordingly during configuration.

12.2.2 Configuring hardware

The simplest way of achieving a redundant hardware configuration consists in initially equipping **one** rack with all the redundant components, assigning parameters to them and then copying them.

You can then specify the various addresses (for one-sided I/O only!) and arrange other, non-redundant modules in individual racks.

Special features in presenting the hardware configuration

In order to enable quick recognition of a redundant DP master system, it is represented by two parallel DP cables.

12.2.3 Assigning parameters to modules in a fault-tolerant station

Introduction

Assigning parameters to modules in a fault-tolerant station is no different from assigning parameters to modules in S7-400 standard stations.

Procedure

All the parameters of the redundant components (with the exception of MPI and communication addresses) must be identical.

The special case of CPUs

You can only set the CPU0 parameters (CPU on rack 0). Any values that you specify are automatically allocated to CPU1 (CPU on rack 1). The settings of CPU1 cannot be changed, with the exception of the following parameters:

- MPI parameters of the CPU
- CPU name, higher level designation of item, location designation

Configuring modules addressed in the I/O address space

Always configure a module that is addressed in the I/O address space so that it is located either entirely in the process image or entirely outside.

Otherwise, consistency cannot be guaranteed, and the data may be corrupted.

I/O access using word or double word operations

The system loads the values to accumulator "0" if the word or double word for I/O access contains only the first or the first three bytes, but not the remaining bytes of the addressed space.

Example: The I/O with address 8 and 9 is available in the S7-400H; addresses 10 and 11 are not used. Access L ID 8 causes the system to load the value DW#16#00000000 into the accumulator.

12.2.4 Recommendations for setting the CPU parameters

CPU parameters that determine cyclic behavior

You specify the CPU parameters that determine the cyclic behavior of the system on the "Cycle/Clock memory" tab.

Recommended settings:

- As long a scan cycle monitoring time as possible (e.g. 6000 ms)
- OB 85 call when there is an I/O area access error: only with incoming and outgoing errors

Number of messages in the diagnostic buffer

You specify the number of messages in the diagnostic buffer on the "Diagnostics/Clock" tab.

We recommend that you set a large number (1500, for example).

Monitoring time for transferring parameters to modules

You specify this monitoring time on the "Startup" tab. It depends on the configuration of the fault-tolerant station. If the monitoring time is too short, the CPU enters the W#16#6547 event in the diagnostic buffer.

For some slaves (e.g. IM 157) these parameters are packed in system data blocks. The transmission time of the parameters depends on the following factors:

- Baud rate of the bus system (high baud rate => short transmission time)
- Size of the parameters and the system data blocks (long parameter => long transmission time)
- Load on the bus system (many slaves => long transmission time);
  Note: The bus load is at its peak during restart of the DP master, for example, following Power OFF/ON

Recommended setting: 600 corresponds to 60 s.

Note

The specific fault-tolerant CPU parameters, and thus also the monitoring times, are calculated automatically. The work memory allocation of all data blocks is based on a CPU-specific default value. If your fault-tolerant system does not link up, check the data memory allocation (HW Config > CPU Properties > H Parameters > Work memory used for all data blocks).

NOTICE
A CP 443-5 Extended (order number 6GK7443–5DX03) may only be used for transfer rates of up to 1.5 MBaud in an S7–400H or S7–400FH when a DP/PA or Y link is connected (IM157, order number 6ES7157-0AA00-0XA0, 6ES7157-0AA80-0XA0, 6ES7157-0AA81-0XA0). Remedy: see FAQ 11168943 in Service & Support (http://www.siemens.com/automation/service&support)

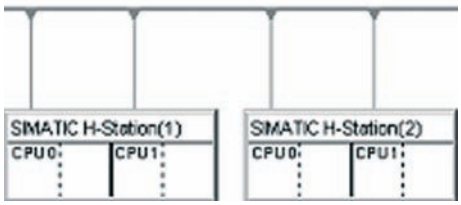
12.2.5 Networking configuration

The fault-tolerant S7 connection is a separate connection type of the "Configure Networks" application. It permits that the following communication peers can communicate with each other:

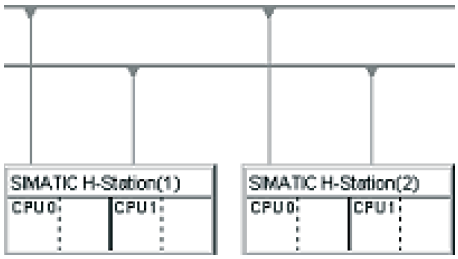
- S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)->S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)
- S7–400 station (with 1 fault-tolerant CPU)->S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)
- S7–400 station (with 1 fault-tolerant CPU)->S7–400 station (with 1 fault-tolerant CPU)
- SIMATIC PC stations > S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)

When this connection type is configured, the application automatically determines the number of possible connecting paths:

- If two independent but identical subnets are available and they are suitable for an S7 connection (DP master systems), two connecting paths are used. In practice, they are usually electrical power systems, one CP in each subnet:



- If only one DP master system is available (in practice usually fiber-optic cables), four connecting paths are used for a connection between two fault-tolerant stations. All CPs are in this subnet:



Downloading the network configuration into a fault-tolerant station

The complete network configuration can be downloaded into the fault-tolerant station in one operation. The same requirements that apply for downloads into standard stations must be met.

12.3 Programming device functions in STEP 7

Display in SIMATIC Manager

In order to do justice to the special features of a fault-tolerant station, the way in which the system is visualized and edited in SIMATIC Manager differs from that of a S7-400 standard station as follows:

- In the offline view, the S7 program appears only under CPU0 of the fault-tolerant station. No S7 program is visible under CPU1.
- In the online view, the S7 program appears under both CPUs and can be selected in both locations.

Communication functions

For programming device (PG) functions that establish online connections (e.g. downloading and deleting blocks), one of the two CPUs has to be selected even if the function affects the entire system over the redundant link.

- Data which is modified in one of the central processing units in redundant operation affect the other CPUs over the redundant link.
- Data which is modified when there is no redundant link (i.e. in single mode) initially affects only the processed CPU. The blocks are applied by the master CPU to the reserve CPU during the next link-up and update. Exception: After a configuration modification no new blocks are applied (only the unchanged data blocks). Loading the blocks is then the responsibility of the user.

Failure and replacement of components during operation 13

13.1 Failure and replacement of components during operation

One factor that is crucial to the uninterrupted operation of the fault-tolerant controller is the replacement of failed components during operation. Quick repairs will recover fault-tolerant redundancy.

We will show you in the following sections how simple and fast it can be to repair and replace components in the S7-400H. Also refer to the tips in the corresponding sections of the manual *S7-400 Automation Systems, Installation*

13.2 Failure and replacement of components during operation

Which components can be replaced?

The following components can be replaced during operation:

- Central processing units (e.g. CPU 417–4H)
- Power supply modules (e.g. PS 405, PS 407)
- Signal and function modules
- Communication processors
- Synchronization modules and fiber-optic cables
- Interface modules (e.g. IM 460, IM 461)

13.2.1 Failure and replacement of a CPU

Complete replacement of the CPU is not always necessary. If only the load memory fails, it is enough to replace the corresponding memory card. Both cases are described below.

Starting situation for replacement of the CPU

Failure	How does the system react?
The S7-400H is in redundant system mode and a **CPU** fails.	• The partner CPU switches to single mode. • The partner CPU reports the event in the diagnostic buffer and in OB 72.

Requirements for replacement

The module replacement described below is possible only if the "new" CPU

- has the same operating system version as the failed CPU and
- if it is equipped with the same load memory as the failed CPU.

NOTICE
New CPUs are always shipped with the latest operating system version. If this differs from the version of the operating system of the remaining CPU, you will have to equip the new CPU with the same version of the operating system. Either create an operating system update card for the new CPU and use this to load the operating system on the CPU or load the required operating system in HW Config with "PLC -> Update Firmware", see section Updating the firmware without a memory card (Page 61).

Procedure

Follow the steps below to **replace a CPU**:

Step	What has to be done?	How does the system react?
1	Turn off the power supply module.	• The entire subsystem is switched off (system operates in single mode).
2	Replace the CPU. Make sure the rack number is set correctly on the CPU.	–
3	Insert the synchronization modules.	–
4	Plug in the fiber-optic cable connections of the synchronization modules.	–
5	Switch the power supply module on again.	• CPU runs the self-tests and changes to STOP.
6	Perform a CPU memory reset on the replaced CPU.	–
7	Start the replaced CPU (for example STOP³RUN or Start using the PG).	• The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN and operates as the reserve CPU.

Starting situation for replacement of the load memory

Failure	How does the system react?
The S7-400H is in redundant system mode and a **load memory access error** occurs.	• The relevant CPU changes to STOP and requests a memory reset. • The partner CPU switches to single mode.

Procedure

Follow the steps below to **replace the load memory**:

Step	What has to be done?	How does the system react?
1	Replace the memory card on the stopped CPU.	–
2	Perform a memory reset on the CPU with the replaced memory card.	–
3	Start the CPU.	• The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN and operates as the reserve CPU.

13.2.2 Failure and replacement of a power supply module

Starting situation

Both CPUs are in RUN.

Failure	How does the system react?
The S7-400H is in redundant system mode and a power supply module fails.	• The partner CPU switches to single mode. • The partner CPU reports the event in the diagnostic buffer and in OB 72.

Procedure

Proceed as follows to replace a power supply module in the central rack:

Step	What has to be done?	How does the system react?
1	Turn off the power supply (24 V DC for PS 405 or 120/230 V AC for PS 407).	• The entire subsystem is switched off (system operates in single mode).
2	Replace the module.	–
3	Switch the power supply module on again.	• The CPU executes the self-tests. • The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN (redundant system mode) and operates as reserve CPU.

Note

Redundant power supply

If you use a redundant power supply (PS 407 10A R), two power supply modules are assigned to one fault-tolerant CPU. If a part of the redundant PS 407 10A R power supply module fails, the associated CPU keeps on running. The defective part can be replaced during operation.

Other power supply modules

If the failure concerns a power supply module outside the central rack (e.g. in the expansion rack or in the I/O device), the failure is reported as a rack failure (central) or station failure (remote). In this case, simply switch off the power supply to the power supply module concerned.

13.2.3 Failure and replacement of an input/output or function module

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and an input/output or function module fails.	• Both CPUs report the event in the diagnostic buffer and via appropriate OBs.

Procedure

⚠ CAUTION

Note the different procedures.

Minor injury or damage to equipment is possible.

The procedure for replacing and input/output or function module differs for modules of the S7-300 and S7-400.

Use the correct procedure when replacing a module. The correct procedure is described below for the S7-300 and the S7-400.

To replace signal and function modules of an S7-300, perform the following steps:

Step	What has to be done?	How does the system react?
1	Remove the failed module (in RUN mode).	• Both CPUs process the swapping interrupt OB 83 synchronized with each other.
2	Disconnect the front connector and wiring.	• Call OB 82 if the module concerned is capable of diagnostic interrupts and diagnostic interrupts are enabled in the configuration. • Call OB 122 if you are accessing the module by direct access • Call OB 85 if you are accessing the module using the process image
3	Plug the front connector into the new module.	• Call OB 82 if the module concerned is capable of diagnostic interrupts and diagnostic interrupts are enabled in the configuration.
4	Insert the new module.	• Both CPUs process the swapping interrupt OB 83 synchronized with each other. • Parameters are assigned automatically to the module by the CPU concerned and the module is addressed again.

To replace signal and function modules of an S7-400, perform the following steps:

Step	What has to be done?	How does the system react?
1	Disconnect the front connector and wiring.	• Call OB 82 if the module concerned is capable of diagnostic interrupts and diagnostic interrupts are enabled in the configuration. • Call OB 122 if you are accessing the module by direct access • Call OB 85 if you are accessing the module using the process image
2	Remove the failed module (in RUN mode).	• Both CPUs process the swapping interrupt OB 83 synchronized with each other.
3	Insert the new module.	• Both CPUs process the swapping interrupt OB 83 synchronized with each other. • Parameters are assigned automatically to the module by the CPU concerned and the module is addressed again.
4	Plug the front connector into the new module.	• Call OB 82 if the module concerned is capable of diagnostic interrupts and diagnostic interrupts are enabled in the configuration.

13.2.4 Failure and replacement of a communication module

This section describes the failure and replacement of communication modules for PROFIBUS and Industrial Ethernet.

The failure and replacement of communication modules for PROFIBUS DP are described in section Failure and replacement of a PROFIBUS DP master (Page 208).

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and a communication module fails.	• Both CPUs report the event in the diagnostic buffer and via appropriate OBs. • In communication via standard connections: Connection failed • In communication via redundant connections: Communication is maintained without interruption over an alternate channel.

Procedure

Proceed as follows to replace a communication module for PROFIBUS or Industrial Ethernet:

Step	What has to be done?	How does the system react?
1	Remove the module.	• Both CPUs process the swapping interrupt OB 83 synchronized with each other.
2	Make sure that the new module has no parameter assignment data in its integrated FLASH EPROM and plug it in.	• Both CPUs process the swapping interrupt OB 83 synchronized with each other. • The module is automatically configured by the appropriate CPU.
3	Turn the module back on.	• The module resumes communication (system establishes communication connection automatically).

13.2.5 Failure and replacement of a synchronization module or fiber-optic cable

In this section, you will see three different error scenarios:

- Failure of a synchronization module or fiber-optic cable
- Successive failure of both synchronization modules or fiber-optic cables
- Simultaneous failure of both synchronization modules or fiber-optic cables

The CPU indicates by means of LEDs and diagnostics whether the lower or upper redundant link has failed. After the defective parts (fiber-optic cable or synchronization module) have been replaced, LEDs IFM1F and IFM2F must go out.

Starting situation

Failure	How does the system react?
Failure of a fiber-optic cable or synchronization module: The S7-400H is in redundant system mode and a fiber-optic cable or synchronization module fails.	• The master CPU reports the event in the diagnostic buffer and with OB 72. • The reserve CPU changes to ERROR-SEARCH mode for some minutes. If the error is eliminated during this time, the reserve CPU switches to redundant system mode, otherwise it switches to STOP. • The diagnostic LED on the synchronization module is lit

Procedure

Follow the steps below to replace a synchronization module or fiber-optic cable:

Step	What has to be done?	How does the system react?
1	First, check the fiber-optic cable.	–
2	Start the reserve CPU (for example, STOP-RUN or Start using the programming device).	The following responses are possible: 1. CPU changes to RUN mode. 2. CPU changes to STOP mode. In this case continue at step 3.
3	Remove the faulty synchronization module from the reserve CPU.	–
4	Insert the new synchronization module in the reserve CPU.	–
5	Plug in the fiber-optic cable connections of the synchronization modules.	• The diagnostic LED on the synchronization module goes off • Both CPUs report the event in the diagnostic buffer

Step	What has to be done?	How does the system react?
6	Start the reserve CPU (for example, STOP-RUN or Start using the programming device).	The following responses are possible: 1. CPU changes to RUN mode. 2. CPU changes to STOP mode. In this case continue at step 7.
7	If the reserve CPU changed to STOP in step 6: Remove the synchronization module from the master CPU.	• The master CPU processes swapping interrupt OB 83 and redundancy error OB 72 (entering state).
8	Insert the new synchronization module into the master CPU.	• The master CPU processes swapping interrupt OB 83 and redundancy error OB 72 (exiting state).
9	Plug in the fiber-optic cable connections of the synchronization modules.	–
10	Start the reserve CPU (for example, STOP-RUN or Start using the programming device).	• The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN (redundant system mode) and operates as reserve CPU.

Note

If both fiber-optic cables or synchronization modules are damaged or replaced one after the other, the system responses are the same as described above.

The only exception is that the reserve CPU does not change to STOP but instead requests a memory reset.

Starting situation

Failure	How does the system react?
Failure of both fiber-optic cables or synchronization modules: The S7-400H is in redundant system mode and **both** fiber-optic cables or synchronization modules fail.	• Both CPUs report the event in the diagnostic buffer and via OB 72. • Both CPUs become the master CPU and remain in RUN mode. • The diagnostic LED on the synchronization module is lit

Procedure

The double error described results in loss of redundancy. In this event proceed as follows:

Step	What has to be done?	How does the system react?
1	Switch off one subsystem.	–
2	Replace the faulty components.	–
3	Turn the subsystem back on.	• LEDs IFM1F and IFMF2F go off. The reserve LED lights up.
4	Start the CPU (for example Start from programming device or STOP³RUN).	• The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN (redundant system mode) and operates as reserve CPU.

Failure and replacement of an IM 460 and IM 461 interface module

The IM 460 and IM 461 interface modules provide permit the connection of expansion modules.

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and an interface module fails.	• The connected expansion unit is turned off. • Both CPUs report the event in the diagnostic buffer and via OB 86.

Procedure

Follow the steps below to replace an interface module:

Step	What has to be done?	How does the system react?
1	Turn off the power supply of the central rack.	• The partner CPU switches to single mode.
2	Turn off the power supply of the expansion unit in which you want to replace the interface module.	–
3	Remove the interface module.	–
4	Insert the new interface module and turn the power supply of the expansion unit back on.	–
5	Switch the power supply of the central unit back on and start the CPU.	• The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN and operates as the reserve CPU.

13.2.6 Failure and replacement of an IM 460 and IM 461 interface module

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and an interface module fails.	• The connected expansion unit is turned off. • Both CPUs report the event in the diagnostic buffer and via OB 86.

Procedure

Follow the steps below to replace an interface module:

Step	What has to be done?	How does the system react?
1	Turn off the power supply of the central rack.	• The partner CPU switches to single mode.
2	Turn off the power supply of the expansion unit in which you want to replace the interface module.	–
3	Remove the interface module.	–
4	Insert the new interface module and turn the power supply of the expansion unit back on.	–
5	Switch the power supply of the central unit back on and start the CPU.	• The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN and operates as the reserve CPU.

13.3 Failure and replacement of components of the distributed I/Os

Which components can be replaced?

The following components of the distributed I/Os can be replaced during operation:

- PROFIBUS DP master
- PROFIBUS DP interface module (IM 153-2 or IM 157)
- PROFIBUS DP slave
- PROFIBUS DP cable

Note

Replacing I/O and function modules located in a distributed station is described in section Failure and replacement of an input/output or function module (Page 200).

13.3.1 Failure and replacement of a PROFIBUS DP master

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and a DP master module fails.	• With single-channel one-sided I/O: The DP master can no longer process connected DP slaves. • With switched I/O: DP slaves are addressed via the DP master of the partner.

Procedure

Proceed as follows to replace a PROFIBUS DP master:

Step	What has to be done?	How does the system react?
1	Turn off the power supply of the central rack.	The fault-tolerant system switches to single mode.
2	Unplug the Profibus DP cable of the affected DP master module.	–
3	Replace the module.	–
4	Plug the Profibus DP back in.	–
5	Turn on the power supply of the central rack.	• The CPU performs an automatic LINK-UP and UPDATE. • The CPU changes to RUN and operates as the reserve CPU.

13.3.2 Failure and replacement of a redundant PROFIBUS DP interface module

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and a PROFIBUS DP interface module (IM 153–2, IM 157) fails.	Both CPUs report the event in the diagnostic buffer and via OB 70.

Replacement procedure

Proceed as follows to replace the PROFIBUS DP interface module:

Step	What has to be done?	How does the system react?
1	Turn off the supply for the affected DP interface module.	–
2	Remove the bus connector.	–
3	Insert the new PROFIBUS DP interface module and turn the power supply back on.	–
4	Plug the bus connector back in.	• The CPUs process the rack failure OB 70 synchronized with each other (outgoing event). • Redundant access to the station by the system is now possible again.

13.3.3 Failure and replacement of a PROFIBUS DP slave

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and a DP slave fails.	Both CPUs report the event in the diagnostic buffer and via the appropriate OB.

Procedure

Proceed as follows to replace a DP slave:

Step	What has to be done?	How does the system react?
1	Turn off the supply for the DP slave.	–
2	Remove the bus connector.	–
3	Replace the DP slave.	–
4	Plug the bus connector back in and turn the power supply back on.	• The CPUs process the rack failure OB 86 synchronized with each other (outgoing event) • The associated DP master can address the DP slave.

13.3.4 Failure and replacement of PROFIBUS DP cables

Starting situation

Failure	How does the system react?
The S7-400H is in redundant system mode and the PROFIBUS DP cable is defective.	• With single-channel one-sided I/O: Rack failure OB (OB 86) is started (incoming event). The DP master can no longer process connected DP slaves (station failure). • With switched I/O: I/O redundancy error OB (OB 70) is started (incoming event). DP slaves are addressed via the DP master of the partner.

Replacement procedure

Proceed as follows to replace PROFIBUS DP cables:

Step	What has to be done?	How does the system react?
1	Check the cabling and localize the interrupted PROFIBUS DP cable.	–
2	Replace the defective cable.	–
3	Switch the failed modules to RUN mode.	The CPUs process the error OBs synchronized with each other • With one-sided I/O: Rack failure OB 86 (outgoing event) The DP slaves can be addressed via the DP master system. • With switched I/O: I/O redundancy error OB 70 (outgoing event). The DP slaves can be addressed via both DP master systems.

System modifications during operation 14

14.1 System modifications during operation

In addition to the options of hot swapping failed components as described in section Failure and replacement of components during operation (Page 197), you can also make changes to the system in a fault-tolerant system without interrupting the running program.

The procedure partially depends on whether you are working with your user software in PCS 7 or STEP 7.

The procedures described below for changes during operation are designed so that you start with the redundant system mode (see section The system states of the S7-400H (Page 84)) with the aim of returning to this mode when the procedures are completed.

NOTICE
Keep strictly to the rules described in this section with regard to modifications of the system in runtime. If you contravene one or more rules, the response of the fault-tolerant system can result in its availability being restricted or even failure of the entire automation system. Only perform a system change in runtime when there is no redundancy error, i.e. when the REDF LED is not lit. The automation system may otherwise fail. The cause of a redundancy error is listed in the diagnostic buffer.

Safety-related components are not taken into account in this description. For more information on dealing with fail-safe systems refer to the *S7-400F and S7-400FH Automation Systems* manual.

14.2 Possible hardware modifications

How is a hardware modification made?

If the hardware components concerned are suitable for unplugging or plugging in live, the hardware modification can be carried out in redundant system mode. However, the fault-tolerant system must be operated temporarily in single mode, because any download of new hardware configuration data in redundant system mode would inevitably cause it to stop. In single mode the process is then controlled only by one CPU while you can carry out the relevant configuration changes at the partner CPU.

⚠ WARNING
During a hardware modification, you can either remove or add modules. If you want to alter your fault-tolerant system such that you remove modules and add others, you have to make two hardware changes.

NOTICE
Always download configuration changes to the CPU using the "Configure hardware" function.

Load memory data of both CPUs must be updated several times in the process. It is therefore advisable to expand the integrated load memory with a RAM card (at least temporarily).

You may only change the FLASH card to a RAM card as required for this if the FLASH card has as much maximum storage space as the largest RAM card available. If you cannot obtain a RAM card with a capacity to match the FLASH card memory space, split the relevant configuration and program modifications into several smaller steps in order to provide sufficient space in the integrated load memory.

Synchronization link

Whenever you make hardware modifications, make sure that the synchronization link between the two CPUs is established **before** you start or turn on the reserve CPU. If the power supply to the CPUs is on, the LEDs IFM1F and IFM2F that indicate errors on the module interfaces on the two CPUs should **go off**.

If one of the IFM LEDs continues to be lit even after you have replaced the relevant synchronization modules, the synchronization cables and even the reserve CPU, there is an error in the master CPU. In this case, you can, however, switch to the reserve CPU by selecting the "via only one intact redundancy link" option in the "Switch" STEP 7 dialog box.

Which components can be modified?

The following modifications can be made to the hardware configuration during operation:

- Adding or removing modules in the central or expansion units (e.g. one-sided I/O module).

NOTICE
Always switch off power before you add or remove IM460 and IM461 interface modules, external CP443-5 Extended DP master interface modules, and their connecting cables.

- Adding or removing components of the distributed I/Os such as
  - DP slaves with a redundant interface module (e.g. ET 200M, DP/PA link, or Y link)
  - One-sided DP slaves (in any DP master system)
  - Modules in modular DP slaves
  - DP/PA links
  - PA devices
- Changing specific CPU parameters
- Changing the CPU memory configuration
- Re-parameterization of a module
- Assigning a module to another process image partition
- Upgrading the CPU version
- Changing the master with only one available redundant link

When you make any modifications, keep to the rules for the configuration of a fault-tolerant station (see section Rules for the assembly of fault-tolerant stations (Page 25)).

What should I consider during system planning?

For switched I/O to be expanded during operation, the following points must be taken into account already at the system planning stage:

- In both cables of a redundant DP master system, sufficient numbers of branching points are to be provided for spur lines or isolating points (spur lines are not permitted for transmission rates of 12 Mbit/s). These branching points can be spaced or implemented at any points that can be accessed easily.
- Both cables must be uniquely identified so that the line which is currently active is not accidentally cut off. This identification should be visible not only at the end points of a line, but also at each possible new connection point. Different colored cables are especially suitable for this.
- Modular DP slave stations (ET 200M), DP/PA links and Y links must always be installed with an active backplane bus and fitted with all the bus modules required wherever possible, because the bus modules cannot be installed and removed during operation.

- Always terminate both ends of PROFIBUS DP and PROFIBUS PA bus cables using active bus terminating elements in order to ensure proper termination of the cables while you are reconfiguring the system.
- PROFIBUS PA bus systems should be built up using components from the SpliTConnect product range (see interactive catalog CA01) so that separation of the lines is not required.
- Loaded data blocks must not be deleted and created again. In other words, SFC 22 (CREATE_DB) and SFC 23 (DEL_DB) may not be applied to DB numbers occupied by loaded DBs.
- Always ensure that the current status of the user program is available as STEP 7 project in block format at the PG/ES when you modify the system configuration. It is not enough to upload the user program back from one of the CPUs to the PG/ES or to compile it again from an STL source.

Modification of the hardware configuration

With a few exceptions, all elements of the configuration can be modified during operation. Usually configuration changes will also affect the user program.

The following must not be changed by means of system modifications during operation:

- Certain CPU parameters (for details refer to the relevant subsections)
- The transmission rate (baud rate) of redundant DP master systems
- S7 and S7 H connections

Modifications to the user program and the connection configuration

The modifications to the user program and connection configuration are loaded into the target system in redundant system mode. The procedure depends on the software used. For more details refer to the *Programming with STEP 7* manual and the *PCS 7, Configuration Manual*.

Note

After reloading connections/gateways, it is no longer possible to change from a RAM card to a FLASH card.

Special features

- Keep changes to a manageable extent. We recommend that you modify only one DP master and/or a few DP slaves (e.g. no more than 5) per reconfiguration run.
- When using an IM 153-2, active bus modules can only be plugged in if the power supply is off.

NOTICE
Remember the following when using redundant I/O that you have implemented as one-sided I/O at the user level (see section Other options for connecting redundant I/Os (Page 160)): Due to the link-up and update process carried out after a system modification, the I/O data of the previous master CPU may be temporarily deleted from the process image until all (changed) I/Os of the "new" master CPU are written to the process image. During the first update of the process image after a system modification, you may (incorrectly) have the impression that the redundant I/O has failed completely or that a redundant I/O exists. So correct evaluation of the redundancy status is not possible until the process image has been fully updated. This does not apply for modules that have been enabled for redundant operation (see section Connecting redundant I/O (Page 132)).

Preparations

To minimize the time during which the fault-tolerant system has to run in single mode, perform the following steps **before** making the hardware change:

- Check whether the CPUs provide sufficient memory capacity for the new configuration data and user program. If necessary, first expand the memory configuration (see section Changing the CPU memory configuration (Page 255)).
- Always ensure that plugged modules which are not configured yet do not have any unwanted influence on the process.

14.3 Adding components in PCS 7

Starting situation

You have verified that the CPU parameters (e.g. monitoring times) match the planned new program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters (Page 250)).

The fault-tolerant system is operating in redundant system mode.

Procedure

Carry out the steps listed below to add hardware components to a fault-tolerant system in PCS 7. Details of each step are described in a subsection.

Step	What has to be done?	See section
1	Modification of hardware	PCS 7, step 1: Modification of hardware (Page 219)
2	Editing the hardware configuration offline	PCS 7, step 2: Offline modification of the hardware configuration (Page 220)
3	Stopping the reserve CPU	PCS 7, step 3: Stopping the reserve CPU (Page 220)
4	Downloading a new hardware configuration to the reserve CPU	PCS 7, step 4: Loading a new hardware configuration in the reserve CPU (Page 221)
5	Switch to CPU with modified configuration	PCS 7, step 5: Switch to CPU with modified configuration (Page 221)
6	Transition to redundant system mode	PCS 7, step 6: Transition to redundant system mode (Page 222)
7	Editing and downloading the user program	PCS 7, step 7: Editing and downloading the user program (Page 223)

Exceptions

This procedure for system modification does not apply in the following cases:

- To use free channels on an existing module
- For adding interface modules (see section Adding interface modules in PCS 7 (Page 225))

Note

As of STEP 7 V5.3 SP2, after changing the hardware configuration, the load operation runs largely automatically. This means that you no longer need to perform the steps described in sections PCS 7, step 3: Stopping the reserve CPU (Page 220) to PCS 7, step 6: Transition to redundant system mode (Page 222). The system behavior remains as described.

You will find more information in the HW Config online help, "Download to module -> Download station configuration in RUN mode".

14.3.1 PCS 7, step 1: Modification of hardware

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Add the new components to the system.
   - Plug new central modules into the racks.
   - Plug new module into existing modular DP stations
   - Add new DP stations to existing DP master systems.

NOTICE
With switched I/O: Always complete all changes on **one** segment of the redundant DP master system before you modify the next segment.

2. Connect the required sensors and actuators to the new components.

Result

The insertion of non-configured modules will have no effect on the user program. The same applies to adding DP stations.

The fault-tolerant system continues to operate in redundant system mode.

New components are not yet addressed.

14.3.2 PCS 7, step 2: Offline modification of the hardware configuration

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Perform all the modifications to the hardware configuration relating to the added hardware offline. Assign appropriate icons to the new channels to be used.
2. Compile the new hardware configuration, but do **not** load it into the target system just yet.

Result

The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.

Configuring connections

The interconnections with added CPs must be configured on both connection partners **after** you complete the HW modification.

14.3.3 PCS 7, step 3: Stopping the reserve CPU

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

Although I/O access errors of the one-sided I/O will result in OB 85 being called, due to the higher-priority CPU redundancy loss (OB 72) they will not be reported. OB 70 (I/O redundancy loss) is not called.

14.3.4 PCS 7, step 4: Loading a new hardware configuration in the reserve CPU

Starting situation

The fault-tolerant system is operating in single mode.

Procedure

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

NOTICE
The user program and connection configuration cannot be downloaded in single mode.

Result

The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.

14.3.5 PCS 7, step 5: Switch to CPU with modified configuration

Starting situation

The modified hardware configuration is downloaded to the reserve CPU.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.

In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.

1. Acknowledge the prompt for confirmation with "OK".

Result

The reserve CPU links up, is updated (see section Link-up and update (Page 95)) and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system operates with the new hardware configuration in single mode.

Reaction of the I/O

Type of I/O	One-sided I/O of previous master CPU	One-sided I/O of new master CPU	Switched I/O
Added I/O modules	are not addressed by the CPU.	Are assigned new parameters and updated by the CPU. Driver blocks are not yet present. Process or diagnostic interrupts are detected, but are not reported.	
I/O modules still present	are no longer addressed by the CPU. Output modules output the configured substitute or holding values.	Are assigned new parameters[1] and updated by the CPU.	continue operation without interruption.
Added DP stations	are not addressed by the CPU.	as for added I/O modules (see above)	
[1] Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 109).

14.3.6 PCS 7, step 6: Transition to redundant system mode

Starting situation

The fault-tolerant system is operating with the new hardware configuration in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU connects and is updated. The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Reaction of the I/O

Type of I/O	One-sided I/O of reserve CPU	One-sided I/O of master CPU	Switched I/O
Added I/O modules	Are assigned new parameters and updated by the CPU. Driver blocks are not yet present. Any interrupts occurring are not reported.	are updated by the CPU. Driver blocks are not yet present. Process or diagnostic interrupts are detected, but are not reported.	
I/O modules still present	Are assigned new parameters[1)] and updated by the CPU.	continue operation without interruption.	
Added DP stations	as for added I/O modules (see above)	Driver blocks are not yet present. Any interrupts occurring are not reported.	
1) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the connect and update later. For additional information, refer to section Time monitoring (Page 109).

14.3.7 PCS 7, step 7: Editing and downloading the user program

Starting situation

The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

⚠ CAUTION

The following program modifications are not possible in redundant system mode and result in the system mode Stop (both CPUs in STOP mode):

- Structural modifications to an FB interface or the FB instance data.
- Structural modifications to global DBs.
- Compression of the CFC user program.

Before the entire program is recompiled and reloaded due to such modifications the parameter values must be read back into the CFC, otherwise the modifications to the block parameters could be lost. You will find more detailed information on this topic in the *CFC for S7, Continuous Function Chart* manual.

Procedure

1. Adapt the program to the new hardware configuration. You can add the following components:
   - CFCs and SFCs
   - Blocks in existing charts
   - Connections and parameter settings
2. Assign parameters for the added channel drivers and interconnect them with the newly assigned icons (see section PCS 7, step 2: Offline modification of the hardware configuration (Page 220)).
3. In SIMATIC Manager, select the charts folder and choose the "Options > Charts > Generate Module Drivers" menu command.
4. Compile only the modifications in the charts and download them to the target system.

NOTICE
Until an FC is called the first time, the value of its output is undefined. This must be taken into account in the interconnection of the FC outputs.

5. Configure the interconnections for the new CPs on both communication partners and download them to the target system.

Result

The fault-tolerant system processes the entire system hardware with the new user program in redundant system mode.

14.3.8 Adding interface modules in PCS 7

Always switch off power before you install the IM460 and IM461 interface modules, external CP443-5 Extended DP master interface module and their connecting cables.

Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

Procedure

1. Change the hardware configuration offline (see section PCS 7, step 2: Offline modification of the hardware configuration (Page 220))
2. Stop the reserve CPU (see section PCS 7, step 3: Stopping the reserve CPU (Page 220))
3. Download the new hardware configuration to the reserve CPU (see section PCS 7, step 4: Loading a new hardware configuration in the reserve CPU (Page 221))
4. Proceed as follows to expand the subsystem of the present reserve CPU:
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.

     or
   - Add a new expansion unit to an existing chain.

     or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.
5. Switch to CPU with altered configuration (see section PCS 7, step 5: Switch to CPU with modified configuration (Page 221))
6. Proceed as follows to expand the subsystem of the original master CPU (currently in STOP mode):
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.

     or
   - Add a new expansion unit to an existing chain.

     or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.
7. Change to redundant system mode (see section PCS 7, step 6: Transition to redundant system mode (Page 222))
8. Modify and download the user program (see section PCS 7, step 7: Editing and downloading the user program (Page 223))

14.4 Removing components in PCS 7

Starting situation

You have verified that the CPU parameters (e.g. monitoring times) match the planned new program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters (Page 250)).

The modules to be removed and their connected sensors and actuators are no longer of any significance to the process being controlled. The fault-tolerant system is operating in redundant system mode.

Procedure

Carry out the steps listed below to remove hardware components from a fault-tolerant system in PCS 7. Details of each step are described in a subsection.

Step	What has to be done?	See section
1	Editing the hardware configuration offline	PCS 7, step 1: Editing the hardware configuration offline (Page 227)
2	Editing and downloading the user program	PCS 7, step 2: Editing and downloading the user program (Page 228)
3	Stopping the reserve CPU	PCS 7, step 3: Stopping the reserve CPU (Page 229)
4	Downloading a new hardware configuration to the reserve CPU	PCS 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 229)
5	Switch to CPU with modified configuration	PCS 7, step 5: Switching to CPU with modified configuration (Page 230)
6	Transition to redundant system mode	PCS 7, step 6: Transition to redundant system mode (Page 231)
7	Modification of hardware	PCS 7, step 7: Modification of hardware (Page 232)

Exceptions

This general procedure for system modifications does not apply to removing interface modules (see section Removing interface modules in PCS 7 (Page 233)).

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections PCS 7, step 3: Stopping the reserve CPU (Page 229) to PCS 7, step 6: Transition to redundant system mode (Page 231). The system behavior remains as described.

You will find more information in the HW Config online help, "Download to module -> Download station configuration in RUN mode".

14.4.1 PCS 7, step 1: Editing the hardware configuration offline

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Perform offline only the configuration modifications relating to the hardware being removed. As you do, delete the icons to the channels that are no longer used.
2. Compile the new hardware configuration, but do **not** load it into the target system just yet.

Result

The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.

14.4.2 PCS 7, step 2: Editing and downloading the user program

Starting situation

The fault-tolerant system is operating in redundant system mode.

CAUTION

The following program modifications are not possible in redundant system mode and result in the system mode Stop (both CPUs in STOP mode):

- Structural modifications to an FB interface or the FB instance data.
- Structural modifications to global DBs.
- Compression of the CFC user program.

Before the entire program is recompiled and reloaded due to such modifications the parameter values must be read back into the CFC, otherwise the modifications to the block parameters could be lost. You will find more detailed information on this topic in the *CFC for S7, Continuous Function Chart* manual.

Procedure

1. Edit only the program elements related to the hardware removal. You can delete the following components:
   - CFCs and SFCs
   - Blocks in existing charts
   - Channel drivers, interconnections and parameter settings
2. In SIMATIC Manager, select the charts folder and choose the "Options > Charts > Generate Module Drivers" menu command.

   This removes the driver blocks that are no longer required.
3. Compile only the modifications in the charts and download them to the target system.

NOTICE

Until an FC is called the first time, the value of its output is undefined. This must be taken into account in the interconnection of the FC outputs.

Result

The fault-tolerant system continues to operate in redundant system mode. The modified user program will no longer attempt to access the hardware being removed.

14.4.3 PCS 7, step 3: Stopping the reserve CPU

Starting situation

The fault-tolerant system is operating in redundant system mode. The user program will no longer attempt to access the hardware being removed.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

14.4.4 PCS 7, step 4: Downloading a new hardware configuration to the reserve CPU

Starting situation

The fault-tolerant system is operating in single mode.

Procedure

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

NOTICE
The user program and connection configuration cannot be downloaded in single mode.

Result

The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.

14.4.5 PCS 7, step 5: Switching to CPU with modified configuration

Starting situation

The modified hardware configuration is downloaded to the reserve CPU.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result

The reserve CPU links up, is updated (see section Link-up and update (Page 95)) and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system operates with the new hardware configuration in single mode.

Reaction of the I/O

Type of I/O	One-sided I/O of previous master CPU	One-sided I/O of new master CPU	Switched I/O
I/O modules to be removed[1)]	are no longer addressed by the CPU. Driver blocks are no longer present.		
I/O modules still present	are no longer addressed by the CPU. Output modules output the configured substitute or holding values.	Are assigned new parameters[2)] and updated by the CPU.	continue operation without interruption.
DP stations to be removed	as for I/O modules to be removed (see above)		
1) No longer included in the hardware configuration, but still plugged in 2) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 109).

14.4.6 PCS 7, step 6: Transition to redundant system mode

Starting situation

The fault-tolerant system is operating with the new hardware configuration in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU connects and is updated. The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Reaction of the I/O

Type of I/O	One-sided I/O of reserve CPU	One-sided I/O of master CPU	Switched I/O
I/O modules to be removed[1)]	are no longer addressed by the CPU. Driver blocks are no longer present.		
I/O modules still present	Are assigned new parameters[2)] and updated by the CPU.	continue operation without interruption.	
DP stations to be removed	as for I/O modules to be removed (see above)		
1) No longer included in the hardware configuration, but still plugged in 2) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the connect and update later. For additional information, refer to section Time monitoring (Page 109).

14.4.7 PCS 7, step 7: Modification of hardware

Starting situation

The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Procedure

1. Disconnect all the sensors and actuators from the components you want to remove.
2. Unplug modules of the one-sided I/Os that are no longer required from the racks.
3. Unplug components that are no longer required from the modular DP stations.
4. Remove DP stations that are no longer required from the DP master systems.

NOTICE
With switched I/O: Always complete all changes on **one** segment of the redundant DP master system before you modify the next segment.

Result

The removal of non-configured modules does not influence the user program. The same applies to removing DP stations.

The fault-tolerant system continues to operate in redundant system mode.

14.4.8 Removing interface modules in PCS 7

Always switch off the power before you remove the IM460 and IM461 interface modules, external CP 443-5 Extended DP master interface module, and their connecting cables.

Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

Procedure

1. Change the hardware configuration offline (see section PCS 7, step 1: Editing the hardware configuration offline (Page 227))
2. Modify and download the user program (see section PCS 7, step 2: Editing and downloading the user program (Page 228))
3. Stop the reserve CPU (see section PCS 7, step 3: Stopping the reserve CPU (Page 229))
4. Download the new hardware configuration to the reserve CPU (see section PCS 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 229))
5. Follow the steps below to remove an interface module from the subsystem of the reserve CPU:
   - Switch off the power supply of the reserve subsystem.
   - Remove an IM460 from the central unit.

     or
   - Remove an expansion unit from an existing chain.

     or
   - Remove an external DP master interface module.
   - Switch on the power supply of the reserve subsystem again.
6. Switch to CPU with altered configuration (see section PCS 7, step 5: Switching to CPU with modified configuration (Page 230))
7. Proceed as follows to remove an interface module from the subsystem of the original master CPU (currently in STOP mode):
   - Switch off the power supply of the reserve subsystem.
   - Remove an IM460 from the central unit.

     or
   - Remove an expansion unit from an existing chain.

     or
   - Remove an external DP master interface module.
   - Switch on the power supply of the reserve subsystem again.
8. Change to redundant system mode (see section PCS 7, step 6: Transition to redundant system mode (Page 231))

14.5 Adding components in STEP 7

Starting situation

You have verified that the CPU parameters (e.g. monitoring times) match the planned new program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters (Page 250)).

The fault-tolerant system is operating in redundant system mode.

Procedure

Carry out the steps listed below to add hardware components to a fault-tolerant system in STEP 7. Details of each step are described in a subsection.

Step	What has to be done?	See section
1	Modification of hardware	STEP 7, step 1: Adding hardware (Page 235)
2	Editing the hardware configuration offline	STEP 7, step 2: Offline modification of the hardware configuration (Page 236)
3	Expanding and downloading OBs	STEP 7, step 3: Expanding and downloading OBs (Page 236)
4	Stopping the reserve CPU	STEP 7, step 4: Stopping the reserve CPU (Page 237)
5	Downloading a new hardware configuration to the reserve CPU	STEP 7, step 5: Loading a new hardware configuration in the reserve CPU (Page 237)
6	Switching to CPU with modified configuration	STEP 7, step 6: Switch to CPU with modified configuration (Page 238)
7	Transition to redundant system mode	STEP 7, step 7: Transition to redundant system mode (Page 239)
8	Editing and downloading the user program	STEP 7, step 8: Editing and downloading the user program (Page 240)

Exceptions

This procedure for system modification does not apply in the following cases:

- To use free channels on an existing module
- For adding interface modules (see section Adding interface modules in STEP 7 (Page 241))

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections STEP 7, step 4: Stopping the reserve CPU (Page 237) to STEP 7, step 8: Editing and downloading the user program (Page 240). The system behavior remains as described.

You will find more information in the HW Config online help, "Download to module -> Download station configuration in RUN mode".

14.5.1 STEP 7, step 1: Adding hardware

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Add the new components to the system.
   - Plug new central modules into the racks.
   - Plug new module into existing modular DP stations
   - Add new DP stations to existing DP master systems.

NOTICE
With switched I/O: Always complete all changes on **one** segment of the redundant DP master system before you modify the next segment.

2. Connect the required sensors and actuators to the new components.

Result

The insertion of non-configured modules will have no effect on the user program. The same applies to adding DP stations.

The fault-tolerant system continues to operate in redundant system mode.

New components are not yet addressed.

14.5.2 STEP 7, step 2: Offline modification of the hardware configuration

Starting situation

The fault-tolerant system is operating in redundant system mode. The modules added are not yet addressed.

Procedure

1. Perform all the modifications to the hardware configuration relating to the added hardware offline.
2. Compile the new hardware configuration, but do **not** load it into the target system just yet.

Result

The modified hardware configuration is in the PG. The target system continues operation with the old configuration in redundant system mode.

Configuring connections

The interconnections with added CPs must be configured on both connection partners **after** you complete the HW modification.

14.5.3 STEP 7, step 3: Expanding and downloading OBs

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Verify that the interrupt OBs 4x, 82, 83, 85, 86, OB 88 and 122 react to any interrupts of the new components as intended.
2. Download the modified OBs and the corresponding program elements to the target system.

Result

The fault-tolerant system is operating in redundant system mode.

14.5.4 STEP 7, step 4: Stopping the reserve CPU

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed. OB 70 (I/O redundancy loss) is not called due to the higher-priority CPU redundancy loss (OB72).

14.5.5 STEP 7, step 5: Loading a new hardware configuration in the reserve CPU

Starting situation

The fault-tolerant system is operating in single mode.

Procedure

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

NOTICE
The user program and connection configuration cannot be downloaded in single mode.

Result

The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.

14.5.6 STEP 7, step 6: Switch to CPU with modified configuration

Starting situation

The modified hardware configuration is downloaded to the reserve CPU.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result

The reserve CPU links up, is updated and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system operates with the new hardware configuration in single mode.

Reaction of the I/O

Type of I/O	One-sided I/O of previous master CPU	One-sided I/O of new master CPU	Switched I/O
Added I/O modules	are not addressed by the CPU.	Are assigned new parameters and updated by the CPU. The output modules temporarily output the configured substitution values.	
I/O modules still present	are no longer addressed by the CPU. Output modules output the configured substitute or holding values.	Are assigned new parameters[1)] and updated by the CPU.	continue operation without interruption.
Added DP stations	are not addressed by the CPU.	as for added I/O modules (see above)	
1) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 109).

14.5.7 STEP 7, step 7: Transition to redundant system mode

Starting situation

The fault-tolerant system is operating with the new hardware configuration in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU connects and is updated. The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Reaction of the I/O

Type of I/O	One-sided I/O of reserve CPU	One-sided I/O of master CPU	Switched I/O
Added I/O modules	Are assigned new parameters and updated by the CPU. The output modules temporarily output the configured substitution values.	are updated by the CPU.	are updated by the CPU. Generate insertion interrupt; must be ignored in OB 83.
I/O modules still present	Are assigned new parameters[1)] and updated by the CPU.	continue operation without interruption.	
Added DP stations	as for added I/O modules (see above)	are updated by the CPU.	
1) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the connect and update later. For additional information, refer to section Time monitoring (Page 109).

14.5.8 STEP 7, step 8: Editing and downloading the user program

Starting situation

The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Restrictions

CAUTION
Any attempts to modify the structure of an FB interface or the instance data of an FB in redundant system mode will lead to stop system mode (both CPUs in STOP mode).

Procedure

1. Adapt the program to the new hardware configuration.

   You can add, edit or remove OBs, FBs, FCs and DBs.
2. Download only the program changes to the target system.
3. Configure the interconnections for the new CPs on both communication partners and download them to the target system.

Result

The fault-tolerant system processes the entire system hardware with the new user program in redundant system mode.

14.5.9 Adding interface modules in STEP 7

Always switch off power before you install the IM460 and IM461 interface modules, external CP443-5 Extended DP master interface module and their connecting cables.

Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

Procedure

1. Change the hardware configuration offline (see section STEP 7, step 2: Offline modification of the hardware configuration (Page 236))
2. Expand and download the organization blocks (see section STEP 7, step 3: Expanding and downloading OBs (Page 236))
3. Stop the reserve CPU (see section STEP 7, step 4: Stopping the reserve CPU (Page 237))
4. Download the new hardware configuration to the reserve CPU (see section STEP 7, step 5: Loading a new hardware configuration in the reserve CPU (Page 237))
5. Proceed as follows to expand the subsystem of the present reserve CPU:
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.

     or
   - Add a new expansion unit to an existing chain.

     or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.
6. Switch to CPU with altered configuration (see section STEP 7, step 6: Switch to CPU with modified configuration (Page 238))
7. Proceed as follows to expand the subsystem of the original master CPU (currently in STOP mode):
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.

     or
   - Add a new expansion unit to an existing chain.

     or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.

8. Change to redundant system mode (see section STEP 7, step 7: Transition to redundant system mode (Page 239))
9. Modify and download the user program (see section STEP 7, step 8: Editing and downloading the user program (Page 240))

14.6 Removing components in STEP 7

Starting situation

You have verified that the CPU parameters (e.g. monitoring times) match the planned new program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters (Page 250)).

The modules to be removed and their connected sensors and actuators are no longer of any significance to the process being controlled. The fault-tolerant system is operating in redundant system mode.

Procedure

Carry out the steps listed below to remove hardware components from a fault-tolerant system in STEP 7. Details of each step are described in a subsection.

Step	What has to be done?	See section
1	Editing the hardware configuration offline	STEP 7, step 1: Editing the hardware configuration offline (Page 243)
2	Editing and downloading the user program	STEP 7, step 2: Editing and downloading the user program (Page 244)
3	Stopping the reserve CPU	STEP 7, step 3: Stopping the reserve CPU (Page 244)
4	Downloading a new hardware configuration to the reserve CPU	STEP 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 245)
5	Switching to CPU with modified configuration	STEP 7, step 5: Switching to CPU with modified configuration (Page 245)
6	Transition to redundant system mode	STEP 7, step 6: Transition to redundant system mode (Page 246)
7	Modification of hardware	STEP 7, step 7: Modification of hardware (Page 248)
8	Editing and downloading organization blocks	STEP 7, step 8: Editing and downloading organization blocks (Page 248)

Exceptions

This general procedure for system modifications does not apply to removing interface modules (see section Removing interface modules in STEP 7 (Page 249)).

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections STEP 7, step 3: Stopping the reserve CPU (Page 244) to STEP 7, step 6: Transition to redundant system mode (Page 246). The system behavior remains as described.

You will find more information in the HW Config online help, "Download to module -> Download station configuration in RUN mode".

14.6.1 STEP 7, step 1: Editing the hardware configuration offline

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Perform all the modifications to the hardware configuration relating to the hardware being removed offline.
2. Compile the new hardware configuration, but do **not** load it into the target system just yet.

Result

The modified hardware configuration is in the PG. The target system continues operation with the old configuration in redundant system mode.

14.6.2 STEP 7, step 2: Editing and downloading the user program

Starting situation

The fault-tolerant system is operating in redundant system mode.

Restrictions

CAUTION
Any attempts to modify the structure of an FB interface or the instance data of an FB in redundant system mode will lead to stop system mode (both CPUs in STOP mode).

Procedure

1. Edit only the program elements related to the hardware removal.

   You can add, edit or remove OBs, FBs, FCs and DBs.
2. Download only the program changes to the target system.

Result

The fault-tolerant system continues to operate in redundant system mode. The modified user program will no longer attempt to access the hardware being removed.

14.6.3 STEP 7, step 3: Stopping the reserve CPU

Starting situation

The fault-tolerant system is operating in redundant system mode. The user program will no longer attempt to access the hardware being removed.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

14.6.4 STEP 7, step 4: Downloading a new hardware configuration to the reserve CPU

Starting situation

The fault-tolerant system is operating in single mode.

Procedure

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

NOTICE
The user program and connection configuration cannot be downloaded in single mode.

Result

The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.

14.6.5 STEP 7, step 5: Switching to CPU with modified configuration

Starting situation

The modified hardware configuration is downloaded to the reserve CPU.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result

The reserve CPU links up, is updated (see section Link-up and update (Page 95)) and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system continues operating in single mode.

Reaction of the I/O

Type of I/O	One-sided I/O of previous master CPU	One-sided I/O of new master CPU	Switched I/O
I/O modules to be removed[1)]	are no longer addressed by the CPU.		
I/O modules still present	are no longer addressed by the CPU. Output modules output the configured substitute or holding values.	Are assigned new parameters[2)] and updated by the CPU.	continue operation without interruption.
DP stations to be removed	as for I/O modules to be removed (see above)		
1) No longer included in the hardware configuration, but still plugged in 2) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 109).

14.6.6 STEP 7, step 6: Transition to redundant system mode

Starting situation

The fault-tolerant system is operating with the new (restricted) hardware configuration in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU connects and is updated. The fault-tolerant system is operating in redundant system mode.

Reaction of the I/O

Type of I/O	One-sided I/O of reserve CPU	One-sided I/O of master CPU	Switched I/O
I/O modules to be removed[1)]	are no longer addressed by the CPU.		
I/O modules still present	Are assigned new parameters[2)] and updated by the CPU.	continue operation without interruption.	
DP stations to be removed	as for I/O modules to be removed (see above)		
1) No longer included in the hardware configuration, but still plugged in 2) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the connect and update later. For additional information, refer to section Time monitoring (Page 109).

14.6.7 STEP 7, step 7: Modification of hardware

Starting situation

The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Procedure

1. Disconnect all the sensors and actuators from the components you want to remove.
2. Remove the relevant components from the system.
   - Remove the central modules from the rack.
   - Remove the modules from modular DP stations
   - Remove DP stations from DP master systems.

NOTICE
With switched I/O: Always complete all changes on **one** segment of the redundant DP master system before you modify the next segment.

Result

The removal of non-configured modules does not influence the user program. The same applies to removing DP stations.

The fault-tolerant system continues to operate in redundant system mode.

14.6.8 STEP 7, step 8: Editing and downloading organization blocks

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Make sure that the interrupt OBs 4x and 82 no longer contain any interrupts of the removed components.
2. Download the modified OBs and the corresponding program elements to the target system.

Result

The fault-tolerant system is operating in redundant system mode.

14.6.9 Removing interface modules in STEP 7

Always switch off the power before you remove the IM460 and IM461 interface modules, external CP 443-5 Extended DP master interface module, and their connecting cables.

Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

Procedure

1. Change the hardware configuration offline (see section STEP 7, step 1: Editing the hardware configuration offline (Page 243))
2. Modify and download the user program (see section STEP 7, step 2: Editing and downloading the user program (Page 244))
3. Stop the reserve CPU (see section STEP 7, step 3: Stopping the reserve CPU (Page 244))
4. Download the new hardware configuration to the reserve CPU (see section STEP 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 245))
5. Follow the steps below to remove an interface module from the subsystem of the reserve CPU:
   - Switch off the power supply of the reserve subsystem.
   - Remove an IM460 from the central unit.

     or
   - Remove an expansion unit from an existing chain.

     or
   - Remove an external DP master interface module.
   - Switch on the power supply of the reserve subsystem again.
6. Switch to CPU with altered configuration (see section STEP 7, step 5: Switching to CPU with modified configuration (Page 245))
7. Proceed as follows to remove an interface module from the subsystem of the original master CPU (currently in STOP mode):
   - Switch off the power supply of the reserve subsystem.
   - Remove an IM460 from the central unit.

     or
   - Remove an expansion unit from an existing chain.

     or
   - Remove an external DP master interface module.
   - Switch on the power supply of the reserve subsystem again.

8. Change to redundant system mode (see section STEP 7, step 6: Transition to redundant system mode (Page 246))
9. Modify and download the user organization blocks (see section STEP 7, step 8: Editing and downloading organization blocks (Page 248))

14.7 Editing CPU parameters

14.7.1 Editing CPU parameters

Only certain CPU parameters (object properties) can be edited in operation. These are highlighted in the screen forms by blue text. If you have set blue as the color for dialog box text on the Windows Control Panel, the editable parameters are indicated in black characters.

NOTICE
If you edit any protected parameters, the system will reject any attempt to changeover to the CPU containing those modified parameters. The event W#16#5966 is written to the diagnostic buffer. and you will then have to restore the wrongly changed parameters in the parameter configuration to their last valid values.

Table 14- 1 Modifiable CPU parameters

Tab	Editable parameter
Start-up	Monitoring time for signaling readiness by modules
	Monitoring time for transferring parameters to modules
Cycle/clock memory	Scan cycle monitoring time
	Cycle load due to communication
	Size of the process image of inputs *)
	Size of the process image of outputs *)
Memory	Local data for the various priority classes *)
	Communication resources: Maximum number of communication jobs.You may only increase the configured value of this parameter *).
Time-of-day interrupts (for each time-of-day interrupt OB)	"Active" checkbox
	"Execution" list box
	Starting date
	Time
Watchdog interrupt (for each watchdog interrupt OB)	Execution
	Phase offset
Diagnostics/clock	Correction factor
Security	Security level and password

Tab	Editable parameter
H parameter	Test cycle time
	Maximum cycle time extension
	Maximum communication delay
	Maximum inhibit time for priority classes > 15
	Minimum I/O retention time
*) Modifying these parameters also modifies the memory content.	

The selected new values should match both the currently loaded and the planned new user program.

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

To edit the CPU parameters of a fault-tolerant system, follow the steps outlined below. Details of each step are described in a subsection.

Step	What to do?	See section
1	Editing CPU parameters offline	Step 1: Editing CPU parameters offline (Page 252)
2	Stopping the reserve CPU	Step 2: Stopping the reserve CPU (Page 252)
3	Downloading modified CPU parameters to the reserve CPU	Step 3: Downloading a new hardware configuration to the reserve CPU (Page 253)
4	Switching to CPU with modified configuration	Step 4: Switching to CPU with modified configuration (Page 253)
5	Transition to redundant system mode	Step 5: Transition to redundant system mode (Page 254)

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections Step 2: Stopping the reserve CPU (Page 252) to Step 5: Transition to redundant system mode (Page 254). The system behavior remains as described.

You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode". You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode".

14.7.2 Step 1: Editing CPU parameters offline

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Edit the relevant CPU properties offline in HW Config.
2. Compile the new hardware configuration, but do **not** load it into the target system just yet.

Result

The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.

14.7.3 Step 2: Stopping the reserve CPU

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

14.7.4 Step 3: Downloading a new hardware configuration to the reserve CPU

Starting situation

The fault-tolerant system is operating in single mode.

Procedure

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

NOTICE
The user program and connection configuration cannot be downloaded in single mode.

Result

The modified CPU parameters in the new hardware configuration of the standby CPU do not yet have an effect on ongoing operation.

14.7.5 Step 4: Switching to CPU with modified configuration

Starting situation

The modified hardware configuration is downloaded to the reserve CPU.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result

The reserve CPU links up, is updated and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system continues operating in single mode.

Reaction of the I/O

Type of I/O	One-sided I/O of previous master CPU	One-sided I/O of new master CPU	Switched I/O
I/O modules	are no longer addressed by the CPU. Output modules output the configured substitute or holding values.	Are assigned new parameters[1)] and updated by the CPU.	continue operation without interruption.
1) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 109).

Where the values for the monitoring times in the CPUs differ, the higher values always apply.

14.7.6 Step 5: Transition to redundant system mode

Starting situation

The fault-tolerant system operates with the modified CPU parameters in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU connects and is updated. The fault-tolerant system is operating in redundant system mode.

Reaction of the I/O

Type of I/O	One-sided I/O of reserve CPU	One-sided I/O of master CPU	Switched I/O
I/O modules	Are assigned new parameters[1] and updated by the CPU.	continue operation without interruption.	
1) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the connect and update later. For additional information, refer to section Time monitoring (Page 109).

Where the values for the monitoring times in the CPUs differ, the higher values always apply.

14.8 Changing the CPU memory configuration

14.8.1 Changing the CPU memory configuration

The redundant system state is only possible if both CPUs have the same memory configuration. For this the following condition must be met:

- The size and type of load memory (RAM or FLASH) on both CPUs must match.

The memory configuration of the CPUs can be modified in operation. Possible modifications of S7-400H memory:

- Expanding load memory
- Changing the type of load memory

14.8.2 Expanding load memory

The following methods of memory expansion are possible:

- Upgrade the load memory by inserting a memory card with more memory space
- Upgrade the load memory by inserting a RAM card, if no memory card was previously inserted

If you change memory in this way, the entire user program is copied from the master CPU to the reserve CPU during the link-up process (see section Update sequence (Page 103)).

Restrictions

Memory should preferably be expanded using RAM cards, because this will ensure that the user program is copied to load memory of the reserve CPU in the link-up process.

In principle, it is also possible to use FLASH Cards to expand load memory. However, it is then your responsibility to download the entire user program and the hardware configuration to the new FLASH Card (see procedure in section Changing the type of load memory (Page 257)).

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

Proceed as follows in the specified sequence:

Step	What to do?	How does the system react?
1	Switch the reserve CPU to STOP using the programming device.	The system is now operating in single mode.
2	Replace the memory card in the CPU with a card which has the required (higher) capacity.	Reserve CPU requests memory reset.
3	Reset the reserve CPU using the programming device.	–
4	Start the reserve CPU with the menu command "PLC > Mode > Switch to CPU ... with expanded memory configuration".	• The reserve CPU links up, is updated and becomes the master. • Previous master CPU changes to STOP. • System operates in single mode.
5	Turn off power to the second CPU.	The subsystem is disabled.
6	Modify the memory configuration of the second CPU as you did in steps 2 to 3 for the first CPU.	–
7	Start the second CPU with the menu command "PLC > Mode > Switch to CPU ... with expanded memory configuration".	• The second CPU is linked up and updated. • The system is now operating again in redundant system mode.

14.8.3 Changing the type of load memory

The following types of memory cards are available for load memory:

- RAM card for the test and commissioning phase
- FLASH Card for permanent storage of the completed user program

The size of the new memory card is irrelevant here.

If you change your memory configuration in this way, the system does not transfer any program parts from the master CPU to the reserve CPU. Instead, it transfers only the contents of the unchanged blocks of the user program (see section Switch to CPU with modified configuration or expanded memory configuration (Page 106)).

It is your responsibility to download the entire user program to the new load memory.

Note

After reloading connections/gateways, it is no longer possible to change from a RAM card to a FLASH card.

Starting situation

The fault-tolerant system is operating in redundant system mode.

The current status of the user program is available on the PG/ES as a STEP 7 project in block format.

CAUTION

You cannot deploy a user program you uploaded from the target system here.

It is not permissible to recompile the user program from an STL source file, because this action would set a new time stamp at all blocks and so prevent the block contents from being copied when there is a master-reserve changeover.

Procedure

Proceed as follows in the specified sequence:

Step	What to do?	How does the system react?
1	Switch the reserve CPU to STOP using the programming device.	The system is now operating in single mode.
2	Replace the existing memory card in the reserve CPU with a new one of the required type.	Reserve CPU requests memory reset.
3	Reset the reserve CPU using the programming device.	–
4	Download the program data to the reserve CPU in STEP 7 by selecting the "Download User Program to Memory Card" command. **Notice**: Select the correct CPU from the selection dialog.	–
5	Start the reserve CPU with the menu command "PLC > Mode > Switching to CPU with modified configuration".	• The reserve CPU links up, is updated and becomes the master. • Previous master CPU changes to STOP. • System operates in single mode.
6	Modify the memory configuration of the second CPU as you did for the first CPU in step 2.	–
7	Download the user program and the hardware configuration to the second CPU.	–
8	Start the second CPU from the PG.	• The second CPU is linked up and updated. • The system is now operating again in redundant system mode.

NOTICE

If you want to change to FLASH Cards, you can load them with the user program and hardware configuration in advance without inserting them in the CPU. Steps 4 and 7 can then be omitted.

However, the memory cards in both CPUs must be loaded in the same sequence. Changing the order of blocks in the load memories will lead to termination of the link-up process.

Writing to a FLASH Card in the fault-tolerant system

You can always write to a FLASH Card while the fault-tolerant system is in RUN, without having to stop the fault-tolerant system. This is, however, only possible if the online data of the hardware configuration and the user program in both CPUs and the corresponding offline data in your engineering station match.

Inserting the Flash card

Proceed as follows:

1. Set the reserve CPU to STOP and insert the FLASH Card into the CPU.
2. Reset the CPU using STEP 7.
3. Download the program data with the STEP 7 "Download User Program to Memory Card" command. Note: Select the correct CPU from the selection dialog.
4. Switch to the CPU with the changed configuration using the "Operating Mode" dialog. This changes over the master/reserve roles; the CPU with the Flash Card is now the master CPU. The reserve CPU is now in STOP.
5. Next, insert the Flash Card in the CPU that is in STOP. Reset the CPU using STEP 7.
6. Carry out step 4: Download the program data with the STEP 7 "Download User Program to Memory Card" command. Note: Select the correct CPU from the selection dialog.
7. Execute a warm restart of the reserve CPU using the "Operating Mode" dialog. The system status now changes to "Redundant" mode.

Removing the FLASH card

The online and offline data consistency described earlier also applies when you remove FLASH Cards from a fault-tolerant system. In addition, the available RAM size must not be less than the actual size of the STEP 7 program (STEP 7 Program > Block Container > "Blocks" Properties).

1. Set the reserve CPU to STOP and remove the FLASH Card. Adapt the memory configuration as required.
2. Reset the CPU using STEP 7.
3. Download the block container using STEP 7.
4. Switch to the CPU with the changed configuration using the "Operating Mode" dialog.
5. Remove the FLASH Card from the CPU which is now in STOP. Adapt the RAM configuration as required, and then perform a CPU memory reset.
6. Execute a warm restart of the reserve CPU using the "Operating Mode" dialog. The system status now changes to "Redundant" mode.

14.9 Re-parameterization of a module

14.9.1 Re-parameterization of a module

Refer to the information text in the "Hardware Catalog" window to determine which modules (signal modules and function modules) can be reconfigured during ongoing operation. The specific reactions of individual modules are described in the respective technical documentation.

NOTICE
If you edit any protected parameters, the system will reject any attempt to changeover to the CPU containing those modified parameters. The event W#16#5966 is written to the diagnostic buffer. and you will then have to restore the wrongly changed parameters in the parameter configuration to their last valid values.

The selected new values must match the current and the planned user program.

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

To edit the parameters of modules in a fault-tolerant system, perform the steps outlined below. Details of each step are described in a subsection.

Step	What to do?	See section
1	Editing parameters offline	Step 1: Editing parameters offline (Page 261)
2	Stopping the reserve CPU	Step 2: Stopping the reserve CPU (Page 262)
3	Downloading modified CPU parameters to the reserve CPU	Step 3: Downloading a new hardware configuration to the reserve CPU (Page 262)
4	Switching to CPU with modified configuration	Step 4: Switching to CPU with modified configuration (Page 263)
5	Transition to redundant system mode	Step 5: Transition to redundant system mode (Page 264)

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections Step 2: Stopping the reserve CPU (Page 262) to Step 5: Transition to redundant system mode (Page 264). The system behavior remains as described.

You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode".

14.9.2 Step 1: Editing parameters offline

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Edit the module parameters offline in HW Config.
2. Compile the new hardware configuration, but do **not** load it into the target system just yet.

Result

The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.

14.9.3 Step 2: Stopping the reserve CPU

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

14.9.4 Step 3: Downloading a new hardware configuration to the reserve CPU

Starting situation

The fault-tolerant system is operating in single mode.

Procedure

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

NOTICE
The user program and connection configuration cannot be downloaded in single mode.

Result

The modified parameters in the new hardware configuration of the reserve CPU do not yet have an effect on ongoing operation.

14.9.5 Step 4: Switching to CPU with modified configuration

Starting situation

The modified hardware configuration is downloaded to the reserve CPU.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result

The reserve CPU links up, is updated and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system continues operating in single mode.

Reaction of the I/O

Type of I/O	One-sided I/O of previous master CPU	One-sided I/O of new master CPU	Switched I/O
I/O modules	are no longer addressed by the CPU. Output modules output the configured substitute or holding values.	are given new parameter settings[1)] and updated by the CPU.	continue operation without interruption.
1) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Auto-Hotspot.

Where the values for the monitoring times in the CPUs differ, the higher values always apply.

Calling OB 83

After transferring the parameter data records to the desired modules, OB 83 is called. The sequence is as follows:

1. After you have made the parameter changes to an module in STEP 7 and loaded them in RUN in the CPU, the OB 83 is started (trigger event W#16#3367). Relevant in the OB start information are the logical start address (OB83_MDL_ADDR) and the module type (OB83_MDL_TYPE). From now on, the input and/or output data of the module might no longer be correct, and no SFCs that send data records to this module may be active.

2. After termination of OB 83, the parameters of the module are reset.

3. After termination of the parameter reset operation, the OB 83 is started again (trigger event W#16#3267 if the parameterization was successful, or W#16#3968 if it was unsuccessful). The input and output data of the module is the same as after an insertion interrupt, meaning that under certain circumstances may not yet be correct. With immediate effect, you can again call SFCs that send data records to the module.

14.9.6 Step 5: Transition to redundant system mode

Starting situation

The fault-tolerant system operates with the modified parameters in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU connects and is updated. The fault-tolerant system is operating in redundant system mode.

Reaction of the I/O

Type of I/O	One-sided I/O of reserve CPU	One-sided I/O of master CPU	Switched I/O
I/O modules	Are assigned new parameters[1)] and updated by the CPU.	Continue operation without interruption.	
1) Central modules are also reset first. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).			

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the connect and update later. For additional information, refer to section Time monitoring (Page 109).

Where the values for the monitoring times in the CPUs differ, the higher values always apply.

Synchronization modules 15

15.1 Synchronization modules for S7–400H

Function of the synchronization modules

Synchronization modules are used for communication between two redundant S7-400H CPUs. You require two synchronization modules per CPU, connected in pairs by fiber-optic cable.

The system supports hot-swapping of synchronization modules, and so allows you to influence the repair response of the fault-tolerant systems and to control the failure of the redundant connection without stopping the plant.

If you remove a synchronization module in redundant system mode, there is a loss of synchronization. The reserve CPU changes to ERROR-SEARCH mode for some minutes. If the new synchronization module is inserted and the redundant link is reestablished during this time, the reserve CPU switches to redundant system mode, otherwise it switches to STOP.

Once you have inserted the new synchronization module and reestablished the redundant link, you must restart the reserve CPU.

Distance between the S7–400H CPUs

Two types of synchronization module are available:

Order number	Maximum distance between the CPUs
6ES7 960–1AA04–0XA0	10 m
6ES7 960–1AB04–0XA0	10 km

Long synchronization cables may increase cycle times by up to 10% per cable kilometer.

Note

A fault-tolerant system requires 4 synchronization modules of the same type.

Mechanical configuration

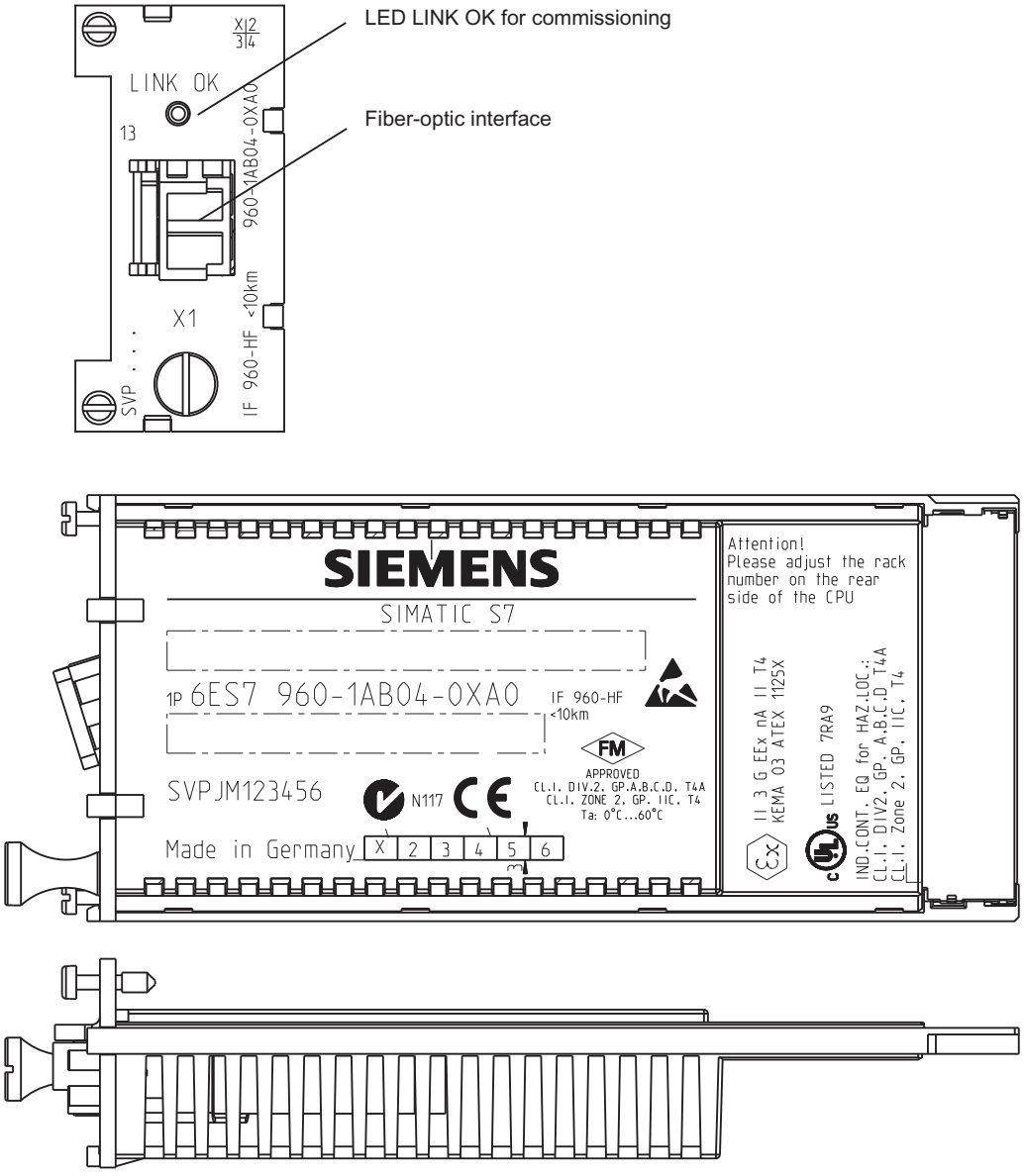


Figure 15-1 Synchronization module

⚠ CAUTION
Risk of injury. The synchronization module is equipped with a laser system and is classified as a "CLASS 1 LASER PRODUCT" according to IEC 60825–1. Avoid direct contact with the laser beam. Do not open the housing. Always observe the information provided in this manual, and keep the manual to hand as a reference.

LED LINK OK

During commissioning of the fault-tolerant system, you can use the "LINK OK" LED on the synchronization module to check the quality of the connection between the CPUs.

LED LINK OK	Meaning
Lit	The connection is OK
Flashing	The connection is not reliable, and the signal is disrupted Check the connectors and cables Check whether the fiber-optic cables are installed according to the guidelines in section Installation of fiber-optic cables (Page 270)
Unlit	The connection is interrupted, or there is insufficient light intensity Check the connectors and cables Check whether the fiber-optic cables are installed according to the guidelines in section Installation of fiber-optic cables (Page 270)

OB 84

When operating in redundant system mode, the CPU's operating system calls OB 84 if it detects a reduced performance in the redundant link between the two CPUs.

Fiber-optic interfaces of unused modules

Fiber-optic interfaces of unused modules must be blanked off during storage to protect the optical equipment. The plugs are in the synchronization module when shipped.

Technical data

Technical data	6ES7 960–1AA04–0XA0	6ES7 960–1AB04–0XA0
Maximum distance between the CPUs	10 m	10 km
Power supply	5.1 V, supplied by the CPU	5.1 V, supplied by the CPU
Current consumption	210 mA	250 mA
Power loss Wavelength of the optical transceiver	1.1 W 850 nm	1.3 W 1300 nm
Maximal permitted attenuation of the fiber-optic cable	7 dB	12 dB
Maximum permitted difference in cable lengths	9 m	50 m
Dimensions W x H x D (mm)	25 x 53 x 140	25 x 53 x 140
Weight	0.065 kg	0.065 kg

15.2 Installation of fiber-optic cables

Introduction

Fiber-optic cables may only be installed by trained and qualified personnel. Always observe the applicable rules and statutory regulations. The installation must be carried out with meticulous care, because faulty installations represent the most common source of error. Causes are:

- Kinking of the fiber-optic cable due to an insufficient bending radius.
- Crushing of the cable as a result of excess forces caused by persons treading on the cable, or by pinching, or by the load of other heavy cables.
- Overstretching due to high tensile forces.
- Damage on sharp edges etc.

Permitted bending radius for prefabricated cables

You may not go below the following bending radius when laying the cable:

- Next to connector: 55 mm
- During installation: 60 mm (repeated)
- After installation: 40 mm (one-time)

Points to observe when installing the fiber-optic cables for the S7-400H synchronization link

Always route the two fiber-optic cables separately. This increases availability and protects the fiber-optic cables from potential double errors caused, for example, by interrupting both cables at the same time.

Always make sure the fiber-optic cables are connected to both CPUs before switching on the power supply or the system, otherwise the CPUs may process the user program as the master CPU.

Local quality assurance

Check the points outlined below before you install the fiber-optic cables:

- Does the delivered package contain the correct fiber-optic cables?
- Any visible transport damage to the product?
- Have you organized a suitable intermediate on-site storage for the fiber-optic cables?
- Does the category of the cables match the connecting components?

Storage of the fiber-optic cables

if you do not install the fiber-optic cable immediately after you received the package, it is advisable to store it in a dry location where it is protected from mechanical and thermal influences. Observe the permitted storage temperatures specified in the data sheet of the fiber-optic cable. You should not remove the fiber-optic cables from the original packaging until you are going to install them.

Open installation, wall breakthroughs, cable ducts:

Note the points outlined below when you install fiber-optic cables:

- The fiber-optic cables may be installed in open locations, provided you can safely exclude any damage in those areas (vertical risers, connecting shafts, telecommunications switchboard rooms, etc.).
- Fiber-optic cables should be mounted on mounting rails (cable trays, wire mesh ducts) using cable ties. Take care not to crush the cable when you fasten it (see Pressure).
- Always deburr or round the edges of the breakthrough before you install the fiber-optic cable, in order to prevent damage to the sheathing when you pull in and fasten the cable.
- The bending radii must not be smaller than the value specified in the manufacturer's data sheet.
- The branching radii of the cable ducts must correspond to the specified bending radius of the fiber-optic cable.

Cable pull-in

Note the points below when pulling-in fiber-optic cables:

- Always observe the information on pull forces in the data sheet of the corresponding fiber-optic cable.
- Do not reel off any greater lengths when you pull in the cables.
- Install the fiber-optic cable directly from the cable drum wherever possible.
- Do not spool the fiber-optic cable sideways off the drum flange (risk of twisting).
- You should use a cable pulling sleeve to pull in the fiber-optic cable.
- Always observe the specified bending radii.
- Do not use any grease or oil-based lubricants.
  You may use the lubricants listed below to support the pulling-in of fiber-optic cables.
  - Yellow compound (Wire-Pulling, lubricant from Klein Tools; 51000)
  - Soft soap
  - Dishwashing liquid
  - Talcum powder
  - Detergent

Pressure

Do not exert any pressure on the cable, for example, by the inappropriate use of clamps (cable quick-mount) or cable ties. Your installation should also prevent anyone from stepping onto the cable.

Influence of heat

Fiber-optic cables are highly sensitive to direct heat, so the cables must not be worked on using hot-air guns or gas burners as used in heat-shrink tubing technology.

15.3 Selecting fiber-optic cables

Make allowance for the following conditions and situations when selecting a suitable fiber-optic cable:

- Required cable lengths
- Indoor or outdoor installation
- Any particular protection against mechanical stress required?
- Any particular protection against rodents required?
- Can an outside cable be laid straight underground?
- Does the fiber-optic cable have to be water-proof?
- Which temperatures influence the installed fiber-optic cable?

Cable length up to 10 m

The synchronization module 6ES7 960–1AA04–0XA0 can be operated in pairs with fiber-optic cables up to a length of 10 m.

Select cables with the following specification for lengths up to 10 m:

- Multimode fiber 50/125 µ or 62.5/125 µ
- Patch cable for indoor applications
- 2 x duplex cables per fault-tolerant system, crossed
- Connector type LC–LC

Such cables are available in the following length as accessories for fault-tolerant systems:

Table 15- 1 Accessory fiber-optic cable

Length	Order number
1 m	6ES7960–1AA04–5AA0
2 m	6ES7960–1AA04–5BA0
10 m	6ES7960–1AA04–5KA0

Cable length up to 10 km

The synchronization module 6ES7 960-1AB04-0XA0 can be operated in pairs with fiber-optic cables up to a length of 10 km.

The following rules apply:

- Make sure there is enough strain relief on the modules if you use fiber-optic cables longer than 10 m.
- Keep to the specified ambient operating conditions of the fiber-optic cables used (bending radii, pressure, temperature...)
- Observe the technical specifications of the fiber-optic cable (attenuation, bandwidth...)

Fiber-optic cables with lengths above 10 m usually have to be custom-made. In the first step, select the following specification:

- Single-mode fiber (mono-mode fiber) 9/125 µ

  For short lengths required for testing and commissioning you may also use the lengths up to 10 m available as accessories. For continuous use, only the specified cables with single-mode fibers are permitted.

The table below shows the further specifications, based on your application:

Table 15- 2 Specification of fiber-optic cables for indoor applications

Cabling	Components required	Specification
The entire cabling is routed within a building No cable junction is required between the indoor and outdoor area The necessary cable length is available in one piece. There is no need to connect several cable segments by means of distribution boxes. Complete installation using prefabricated patch cables	Patch cables	2 x duplex cables per system Connector type LC–LC Crossed cores Further specifications you may need to observe for your plant: UL approval Halogen-free materials
	Prefabricated cable	Multicore cables, 4 cores per system Connector type LC–LC Crossed cores Further specifications you may need to observe for your plant: UL approval Halogen-free materials
The entire cabling is routed within a building No cable junction is required between the indoor and outdoor area The necessary cable length is available in one piece. There is no need to connect several cable segments by means of distribution boxes. Complete installation using prefabricated patch cables	including patch cables for indoor applications as required	1 cable with 4 cores per fault-tolerant system Both interfaces in one cable 1 or 2 cables with several shared cores Separate installation of the interfaces in order to increase availability (reduction of common cause factor) Connector type ST or SC, for example, to match other components; see below Further specifications you may need to observe for your plant: UL certification Halogen-free materials Avoid splicing cables in the field. Use prefabricated cables with pulling protection/aids in whiplash or breakout design, including measuring log.
	Patch cable for indoor applications	Connector type LC on ST or SC, for example, to match other components
Installation using distribution boxes, see Fig. 15–2	One distribution/junction box per branch Installation and patch cables are connected via the distribution box. Either ST or SC plug-in connections can be used, for example. Check the cross-over installation when you wire the CPUs.	Connector type ST or SC, for example, to match other components

Table 15- 3 Specification of fiber-optic cables for outdoor applications

Cabling	Components required	Specification
A cable junction is required between the indoor and outdoor area see Fig. 15-2	• Installation cables for outdoor applications	Installation cables for outdoor applications • 1 cable with 4 cores per fault-tolerant system Both interfaces in one cable • 1 or 2 cables with several shared cores Separate installation of the interfaces in order to increase availability (reduction of common cause factor) • Connector type ST or SC, for example, to match other components; see below Further specifications you may need to observe for your plant: • UL approval • Halogen-free materials Observe further specifications as required for local conditions: • Protection against increased mechanical stress • Protection against rodents • Water-proofing • Suitable for direct underground installation • Suitable for the given temperature ranges Avoid splicing cables in the field. Use prefabricated cables with pulling protection/aids in whiplash design, including measuring log.
	• including patch cables for indoor applications as required	• 1 cable with 4 cores per fault-tolerant system Both interfaces in one cable • 1 or 2 cables with several shared cores Separate installation of the interfaces in order to increase availability (reduction of common cause factor) • Connector type ST or SC, for example, to match other components; see below Further specifications you may need to observe for your plant: • UL approval • Halogen-free materials Avoid splicing cables in the field. Use prefabricated cables with pulling protection/aids in whiplash or breakout design, including measuring log.
	• Patch cable for indoor applications	• Connector type LC on ST or SC, for example, to match other components

Cabling	Components required	Specification
A cable junction is required between the indoor and outdoor area see Fig. 15-2	• One distribution/junction box per branch Installation and patch cables are connected via the distribution box. Either ST or SC plug-in connections can be used, for example Check the cross-over installation when you wire the CPUs.	• Connector type ST or SC, for example, to match other components

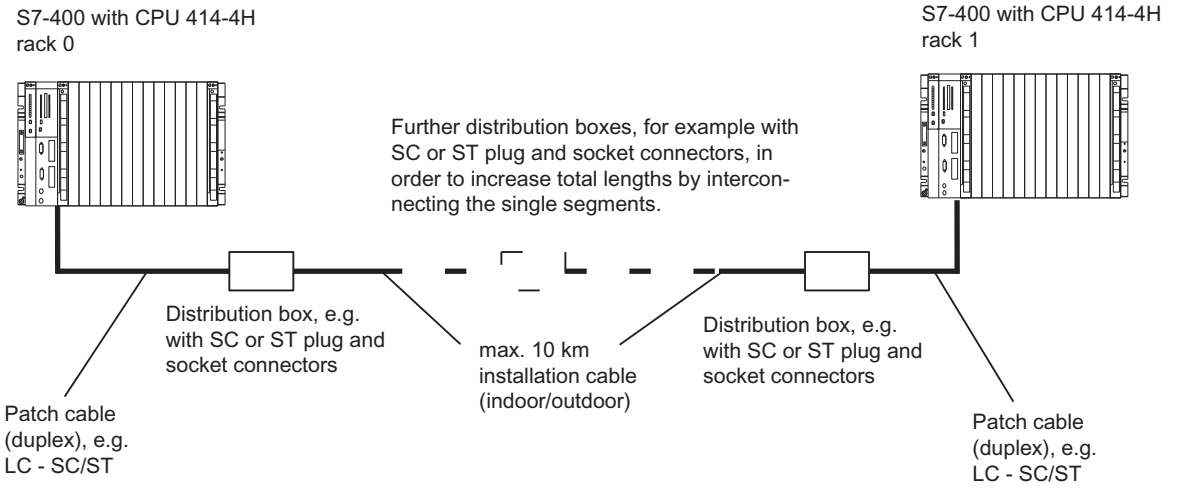


Figure 15-2 Fiber-optic cables, installation using distribution boxes

S7-400 cycle and response times

16

This section describes the decisive factors in the cycle and response times of your of S7-400 station.

You can read out the cycle time of the user program from the relevant CPU using the programming device (refer to the manual *Configuring Hardware and Connections with STEP 7*).

The examples included show you how to calculate the cycle time.

An important aspect of a process is its response time. How to calculate this factor is described in detail in this section. When operating a CPU 41x-H as master on the PROFIBUS DP network, you also need to include the additional DP cycle times in your calculation (see section Response time (Page 289)).

Additional information

For more detailed information on the following execution times, refer to the S7–400H instruction list. This lists all the *STEP 7* instructions that can be executed by the particular CPUs along with their execution times and all the SFCs/SFBs integrated in the CPUs and the IEC functions that can be called in *STEP 7* with their execution times.

16.1 Cycle time

This section describes the decisive factors in the cycle time, and how to calculate it.

Definition of cycle time

The cycle time is the time the operating system requires to execute a program, i.e. to execute OB 1, including all interrupt times required by program parts and for system activities.

This time is monitored.

Time slice model

Cyclic program processing, and therefore also user program processing, is based on time slices. To demonstrate the processes, let us presume a global time slice length of exactly 1 ms.

Process image

During cyclic program processing, the CPU requires a consistent image of the process signals. To ensure this, the process signals are read/written prior to program execution. Subsequently, during program processing the CPU does not access the signal modules directly when addressing the input (I) and output (O) address areas, but rather it accesses the CPU's internal memory area containing the I/O process image.

Sequence of cyclic program processing

The table below shows the various phases in cyclic program execution.

Table 16- 1 Cyclic program processing

Step	Sequence
1	The operating system initiates the scan cycle monitoring time.
2	The CPU copies the values from the process output images to the output modules.
3	The CPU reads the status of inputs of the input modules, and then updates the process image of the inputs.
4	The CPU processes the user program in time slices and executes the instructions specified in the program.
5	At the end of a cycle, the operating system executes pending tasks, e.g. loading and deleting of blocks.
6	Finally, on expiration of any given minimum cycle time, the CPU returns to the start of the cycle and restarts cycle monitoring.

Elements of the cycle time

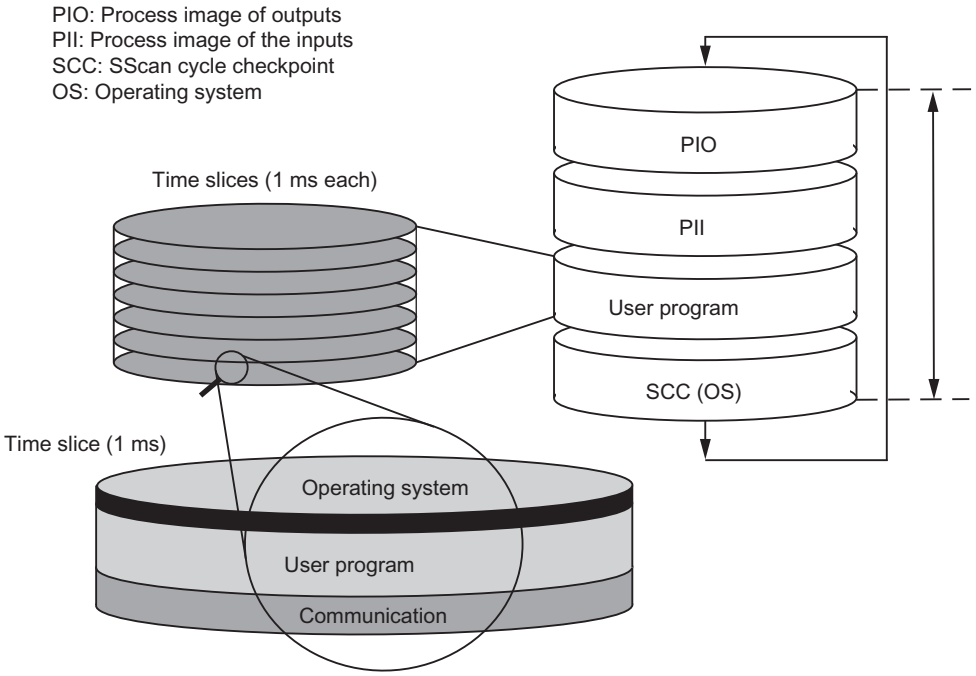


Figure 16-1 Elements and composition of the cycle time

16.2 Calculating the cycle time

Extending the cycle time

The cycle time of a user program is extended by the factors outlined below:

- Time-based interrupt processing
- Hardware interrupt processing (see also section Interrupt response time (Page 299))
- Diagnostics and error processing (see also section Example of calculation of the interrupt response time (Page 301))
- Communication via MPI and CPs connected to the communication bus (e.g.: Ethernet, Profibus, DP) as a factor in communication load
- Special functions such as operator control and monitoring of tags or the block status
- Transfer and deletion of blocks, compressing of the user program memory

Influencing factors

The table below shows the factors influencing the cycle time.

Table 16- 2 Factors influencing cycle time

Factors	Remark
Transfer time for the process output image (POI) and process input image (PII)	See tables from 16-3 onwards
User program execution time	This value is calculated based on the execution times of the various statements (see the *S7-400 statement list*).
Operating system execution time at the cycle control point	See Table 16-7
Extension of cycle time due to communication load	You configure the maximum permitted communication load on the cycle as a percentage in **STEP 7** (*Programming with STEP 7* manual). See section Communication load (Page 286).
Load on cycle times due to interrupts	Interrupt requests can always stop user program execution. See Table 16-8

Process image update

The table below shows the time a CPU requires to update the process image (process image transfer time). The specified times only represent "ideal values", and may be extended accordingly by any interrupts or communication of the CPU.

Calculation of the transfer time for process image update:

C+ portion in the central unit (taken from row A of the table below)
+ portion in the expansion unit with local link (from row B)
+ portion in the expansion unit with remote link (from row C)
+ portion via the integrated DP interface (from row D)
+ portion of consistent data via the integrated DP interface (from row E1)
+ portion of consistent data via external DP interface (from row E2)

= Transfer time for process image update

The tables below show the various portions of the transfer time for a process image update (process image transfer time). The specified times only represent "ideal values", and may be extended accordingly by any interrupts or communication of the CPU.

Table 16- 3 Portion of the process image transfer time, CPU 412-3H

	Portion n = number of bytes in the process image m = number of accesses to process image*)	CPU 412-3H stand-alone mode	CPU 412-3H redundant
K	Base load	13 µs	16 µs
A **)	In central unit Read/write byte/word/double word	m * 9.5 µs	m * 40 µs
B **)	In expansion unit with local link Read/write byte/word/double word	m * 24 µs	m * 52 µs
C **)***)	In expansion unit with remote link Read/write byte/word/double word	m * 48 µs	m * 76 µs
D	In the DP area for the integrated DP interface Read byte/word/double word	m * 2.0 µs	m * 35 µs
D	In the DP area for the external DP interfaces Read/write byte/word/double word	m * 6.0 µs	m * 40 µs
E1	Consistent data in the process image for the integrated DP interface Read/write data	n * 1.4 µs	n * 4.4 µs
E2	Consistent data in the process image for the external DP interface (CP 443–5 extended) Read/write data	n * 3.0 µs	n * 6.5 µs
*) The module data is updated with the minimum number of accesses. (e.g.: 8 bytes result in 2 double word accesses; 16 bytes in 4 double word accesses.)			
**) In the case of I/O inserted into the central unit or into an expansion unit, the specified value contains the execution time of the I/O module			
***) Measured with IM460-3 and IM461-3 at a link length of 100 m			

Table 16- 4 Portion of the process image transfer time, CPU 414-4H

	Portion n = number of bytes in the process image m = number of accesses to process image*)	CPU 414–4H stand-alone mode	CPU 414–4H redundant
K	Base load	8 µs	9 µs
A **)	In central unit Read/write byte/word/double word	m * 8.5 µs	m * 25.7 µs
B **)	In expansion unit with local link Read/write byte/word/double word	m * 23 µs	m * 40 µs
C **)***)	In expansion unit with remote link Read/write byte/word/double word	m * 58 µs	m * 64 µs
D	In the DP area for the integrated DP interface Read byte/word/double word	m * 1.3 µs	m * 21.5 µs
D	In the DP area for the external DP interfaces Read/write byte/word/double word	m * 5.2 µs	m * 24.6 µs
E1	Consistent data in the process image for the integrated DP interface Read/write data	n * 0.66 µs	n * 3.1 µs

	Portion n = number of bytes in the process image m = number of accesses to process image*)	CPU 414–4H stand-alone mode	CPU 414–4H redundant
E2	Consistent data in the process image for the external DP interface (CP 443–5 extended) Read/write data	n * 2.5 µs	n * 6.5 µs
*) The module data is updated with the minimum number of accesses. (e.g.: 8 bytes result in 2 double word accesses; 16 bytes in 4 double word accesses.)			
**) In the case of I/O inserted into the central unit or into an expansion unit, the specified value contains the execution time of the I/O module			
***) Measured with IM460-3 and IM461-3 at a link length of 100 m			

Table 16- 5 Portion of the process image transfer time, CPU 417-4H

	Portion n = number of bytes in the process image m = number of accesses to process image*)	CPU 417–4H stand-alone mode	CPU 417–4H redundant
K	Base load	3 µs	4 µs
A **)	In central unit Read/write byte/word/double word	m * 7.3 µs	m * 15.7 µs
B **)	In expansion unit with local link Read/write byte/word/double word	m * 20 µs	m * 26 µs
C **)***)	In expansion unit with remote link Read/write byte/word/double word	m * 45 µs	m * 50 µs
D	In the DP area for the integrated DP interface Read byte/word/double word	m * 1.2 µs	m * 13 µs
D	In the DP area for the external DP interface Read/write byte/word/double word	m * 5 µs	m * 15 µs
E1	Consistent data in the process image for the integrated DP interface Read/write data	n * 0.25 µs	n * 2.5 µs
E2	Consistent data in the process image for the external DP interface (CP 443–5 extended) Read/write data	n * 2.25 µs	n * 3.4 µs
*) The module data is updated with the minimum number of accesses. (e.g.: 8 bytes result in 2 double word accesses; 16 bytes in 4 double word accesses.)			
**) In the case of I/O inserted into the central unit or into an expansion unit, the specified value contains the execution time of the I/O module			
***) Measured with IM460-3 and IM461-3 at a link length of 100 m			

Extending the cycle time

The calculated cycle time of a S7-400H CPU must be multiplied by a CPU-specific factor. The table below lists these factors:

Table 16- 6 Extending the cycle time

Start-up	412–3H stand-alone mode	412–3H redundant	414–4H stand-alone mode	414–4H redundant	417–4H stand-alone mode	417–4H redundant
Factor	1,04	1,2	1,05	1,2	1,05	1,2

Long synchronization cables may further increase cycle times by up to 10% per cable kilometer.

Operating system execution time at the cycle control point

The table below shows the operating system execution time at the cycle checkpoint of the CPUs.

Table 16- 7 Operating system execution time at the cycle control point

Sequence	412-3H stand-alone mode	412-3H redundant	414-4H stand-alone mode	414-4H redundant	417-4H stand-alone mode	417-4H redundant
Cycle control at the SCCP	271-784 µs ∅ 284 µs	679-1890 µs ∅ 790 µs	198-553 µs ∅ 204 µs	548-1417 µs ∅ 609 µs	83 - 315 µs ∅ 85 µs	253 - 679 µs ∅ 270 µs

Extended cycle time due to nested interrupts

Table 16- 8 Extended cycle time due to nested interrupts

CPU	Hardware interrupt	Diagnostic interrupt	Time-of-day interrupt	Delay interrupt	Watchdog interrupt	Programming / I/O access error	Asynchronous error
CPU 412-3 stand-alone mode	481 µs	488 µs	526 µs	312 µs	333 µs	142 µs / 134 µs	301 µs
CPU 412-3 H redundant	997 µs	843 µs	834 µs	680 µs	674 µs	427 µs / 179 µs	832 µs
CPU 414–4 H stand-alone mode	315 µs	326 µs	329 µs	193 µs	189 µs	89 µs / 85 µs	176 µs
CPU 414–4 H redundant	637 µs	539 µs	588 µs	433 µs	428 µs	272 µs / 114 µs	252 µs

CPU	Hardware interrupt	Diagnostic interrupt	Time-of-day interrupt	Delay interrupt	Watchdog interrupt	Programming / I/O access error	Asynchronous error
CPU 417–4 H stand-alone mode	160 µs	184 µs	101 µs	82 µs	120 µs	36 µs / 35 µs	90 µs
CPU 417–4 H redundant	348 µs	317 µs	278 µs	270 µs	218 µs	121 µs / 49 µs	115 µs

The program runtime at interrupt level must be added to this time extension.

The corresponding times are added together if the program contains nested interrupts.

16.3 Different cycle times

The cycle time (T_{cyc}) length is not the same in every cycle. The figure below shows different cycle times T_{cyc1} and T_{cyc2}. T_{cyc2} is longer than T_{cyc1} because the cyclically executed OB 1 is interrupted by a TOD interrupt OB (here: OB 10).

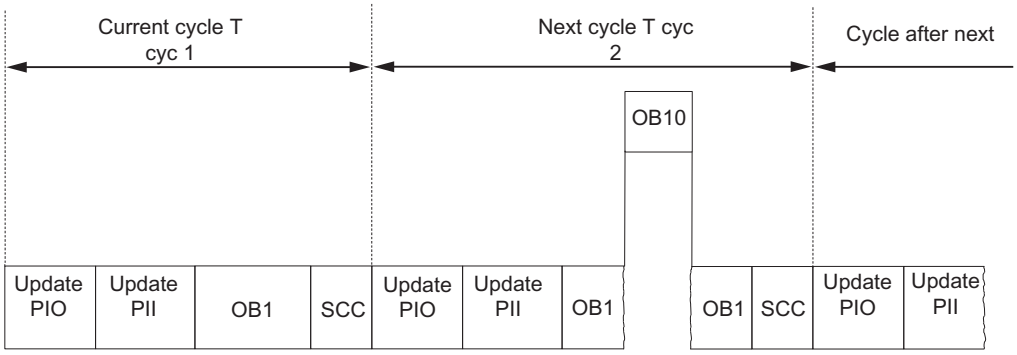


Figure 16-2 Different cycle times

Fluctuation of the block processing time (e.g. OB 1) may also be a factor causing cycle time fluctuation, due to:

- conditional instructions
- conditional block calls
- different program paths
- loops, etc.

Maximum cycle time

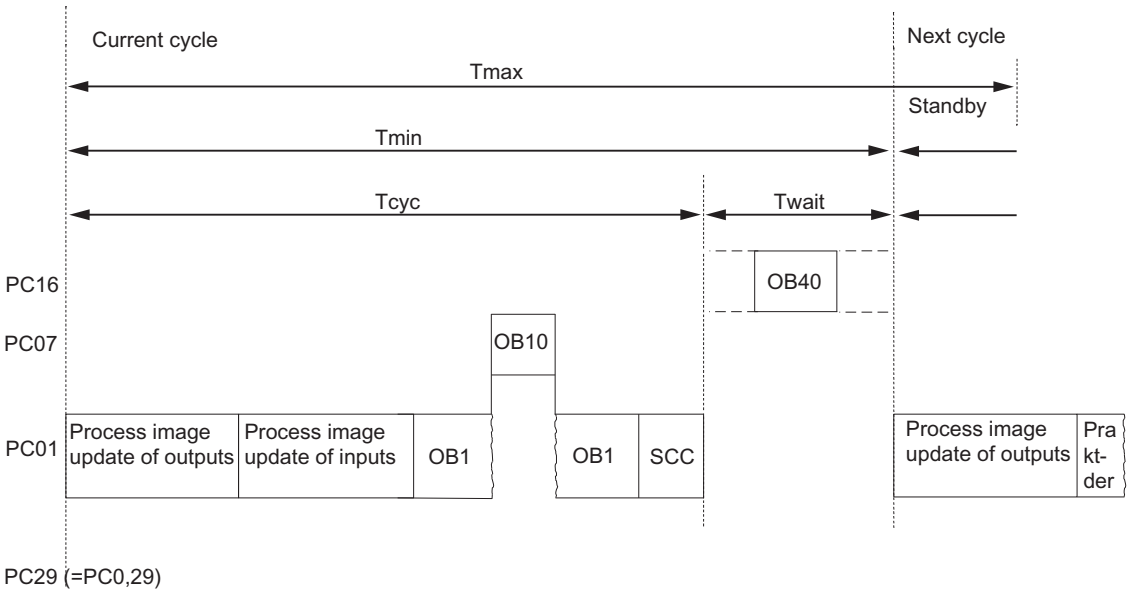
In STEP 7 you can modify the default maximum cycle time (scan cycle monitoring time). OB 80 is called when this time expires. In this block you can specify the CPUs response to this time error. If you do not retrigger the cycle time with SFC 43, OB 80 doubles the cycle time at the first call. In this case the CPU switches to STOP mode when OB 80 is called a second time.

The CPU switches to STOP mode if OB 80 does not exist in its memory.

Minimum cycle time

In STEP 7 you can set a minimum cycle time for a CPU. This is practical if

- the intervals between starting program execution of OB 1 (free cycle) are to be more or less of the same length, or
- the cycle time were too short, the process images would be updated more often than necessary



Tmin = configurable minimum cycle time
Tmax = configurable maximum cycle time
Tcyc = the cycle time
Twait = difference between Tmin and the actual cycle time. Within this time you can process interrupt events or SCC tasks
PC = Priority Class

Figure 16-3 Minimum cycle time

The actual cycle time is the sum of T_{cyc} and T_{wait}. It is thus always longer or equal to T_{min}.

16.4 Communication load

The operating system provides the CPU continuously with the configured time slices as a percentage of the overall CPU processing resources (time slice technique). Processing performance not required for communication is made available to other processes.

In the hardware configuration you can specify a communication load value between 5% and 50%. The default value is 20%.

This percentage is to be interpreted as mean value, i.e. communication resources may take significantly more than 20% of a time slice. The communication portion is then only a few % or 0% in the next time slice.

The formula below describes the influence of communication load on the cycle time:

$$\text{Actual cycle time} = \text{Cycle time} \times \frac{100}{100 - \text{"Configured communication load in \%"}}$$

Round the result up to the next highest integer !

Figure 16-4 Formula: Influence of communication load

Data consistency

The user program is interrupted to process communications. This interruption can be triggered after any statement. These communication jobs may lead to a change in user data. As a result, data consistency cannot be ensured over several accesses.
How to ensure data consistency in operations comprising more than one command is described in the "Consistent data" section.

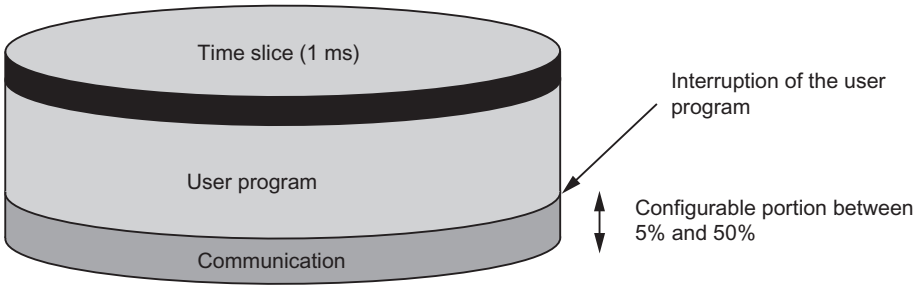


Figure 16-5 Distribution of a time slice

The operating system takes a certain portion of the remaining time slice for internal tasks. This portion is included in the factor defined in the tables starting at 16-3.

Example: 20% communication load

In the hardware configuration you have set a communication load of 20%.

The calculated cycle time is 10 ms.

This means that a setting of 20% communication load allocates an average of 200 µs to communication and 800 µs to the user program in each time slice. So the CPU requires 10 ms / 800 µs = 13 time slices to execute one cycle. This means the physical cycle time is equivalent to 13 times 1-ms time slice = 13 ms, if the CPU fully utilizes the configured communication load.

That is to say, 20% communication does not extend the cycle by a linear amount of 2 ms, but by 3 ms.

Example: 50% communication load

In the hardware configuration you have set a communication load of 50 %.

The calculated cycle time is 10 ms.

This means that 500 µs remain in each time slice for the cycle. So the CPU requires 10 ms / 500 µs = 20 time slices to execute one cycle. This means the physical cycle time is 20 ms if the CPU fully utilizes the configured communication load.

So a setting of 50% communication load allocates 500 µs to communication and 500 µs to the user program in each time slice. So the CPU requires 10 ms / 500 µs = 20 time slices to execute one cycle. This means the physical cycle time is equivalent to 20 times 1-ms time slice = 20 ms, if the CPU fully utilizes the configured communication load.

This means that 50% communication does not extend the cycle by a linear amount of 5 ms, but by 10 ms (= doubling the calculated cycle time).

Dependency of the actual cycle time on communication load

The figure below describes the non-linear dependency of the actual cycle time on communication load. In our example we have chosen a cycle time of 10 ms.

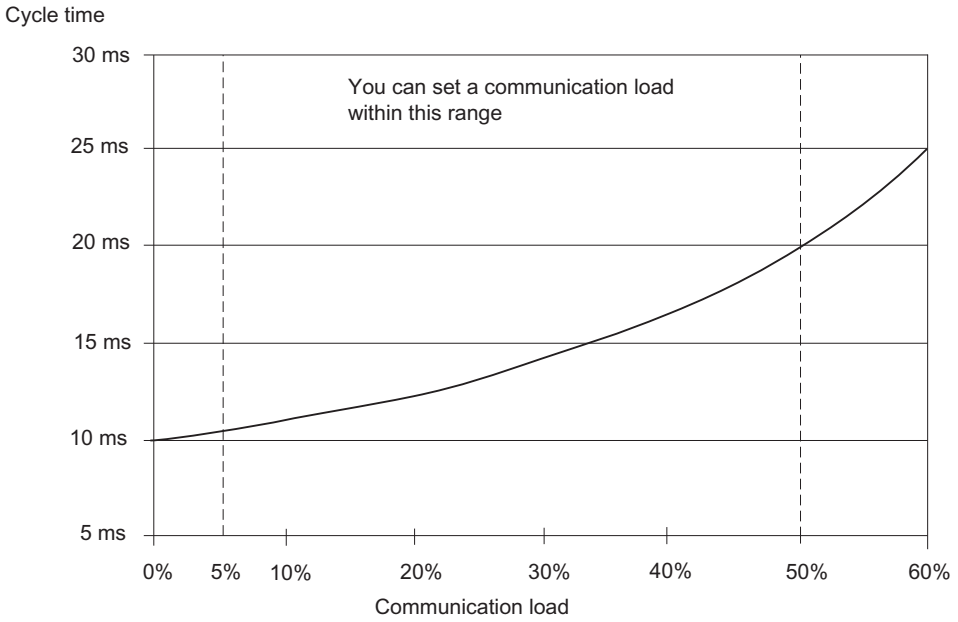


Figure 16-6 Dependency of the cycle time on communication load

Further effects on the actual cycle time

Seen statistically, the extension of cycle times due to communication load leads to more asynchronous events occurring within an OB 1 cycle, for example interrupts. This further extends the OB 1 cycle. How much it is extended depends on the number of events per OB 1 cycle and the time required for processing these events.

Remarks

- Change the value of the "communication load" parameter to check the effects on the cycle time during system runtime.
- Always take the communication load into account when you set the maximum cycle time, otherwise you risk timeouts.

Recommendations

- Use the default setting whenever possible.
- Increase this value only if the CPU is used primarily for communication, and if time is not a critical factor for the user program! In all other situations you should only reduce this value!

16.5 Response time

Definition of response time

The response time is the time from detecting an input signal to changing the output signal associated with it.

Fluctuation range

The actual response time lies between the shortest and the longest response time. You must always assume the longest response time when configuring your system.

The section below deals with the shortest and longest response times, in order to provide an overview of the fluctuation in the length of response times.

Factors

The response time depends on the cycle time and the following factors:

- Delay of the inputs and outputs
- Additional DP cycle times on the PROFIBUS DP network
- Execution in the user program

Delay of the I/Os

Make allowances for the following module-specific delay times:

- For digital inputs: the input delay time
- For digital inputs with interrupt function: the input delay time + internal preparation time
- For digital outputs: negligible delay times
- For relay outputs: typical delay times of 10 ms to 20 ms.
  The delay of relay outputs also depends on the temperature and voltage.
- For analog inputs: cycle time for analog input
- For analog outputs: response time at analog outputs

For information on delay times, refer to the technical specifications of the signal modules.

DP cycle times on the PROFIBUS DP network

If you configured your PROFIBUS DP network in **STEP 7**, **STEP 7** calculates the typical DP cycle time to be expected. You can then view the DP cycle time of your configuration on the PG in the bus parameters section.

The figure below provides an overview of the DP cycle time. In this example, we assume an average value for each DP slave of 4 bytes of data.

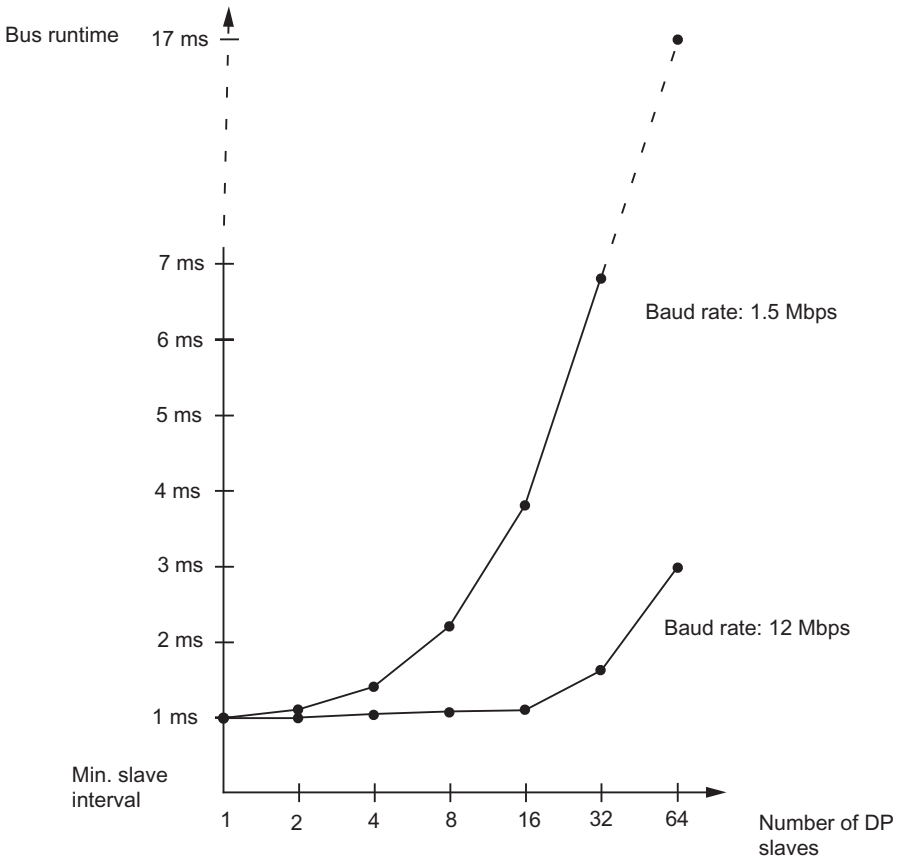


Figure 16-7 DP cycle times on the PROFIBUS DP network

If you are operating a PROFIBUS DP network with more than one master, you will need to take the DP cycle time into account for each master. In other words, perform a separate calculation for each master and add the results together.

Shortest response time

The figure below shows the conditions under which the shortest response time is achieved.

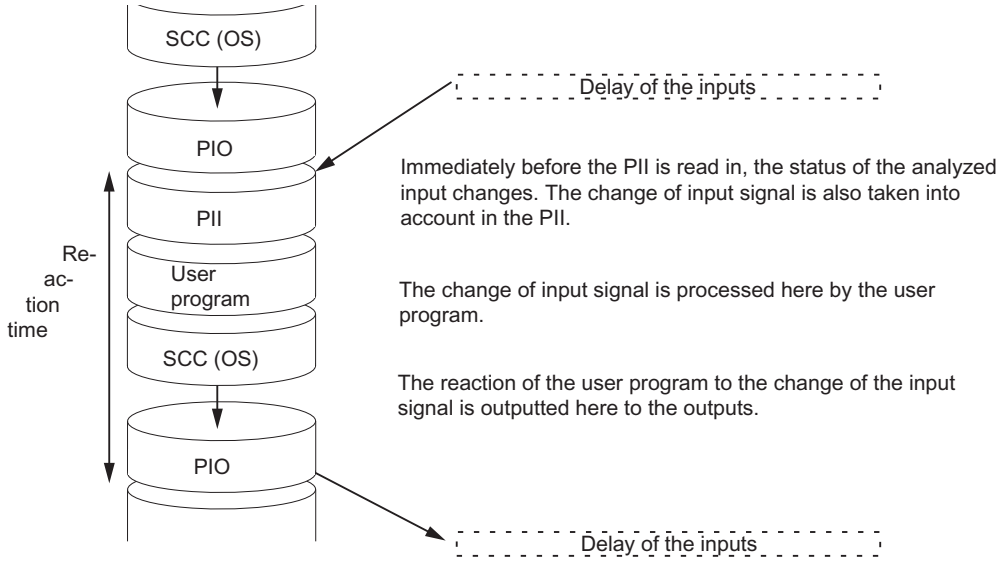


Figure 16-8 Shortest response time

Calculation

The (shortest) response time is calculated as follows:

- 1 x process image transfer time of the inputs +
- 1 x process image transfer time of the outputs +
- 1 x program processing time +
- 1 x operating system processing time at the SCCP +
- Delay of the inputs and outputs

The result is equivalent to the sum of the cycle time plus the I/O delay times.

Note

If the CPU and signal module are not in the central unit, you will have to add twice the delay time of the DP slave frame (including processing in the DP master).

Longest response time

The figure below shows the conditions under which the longest response time is achieved.

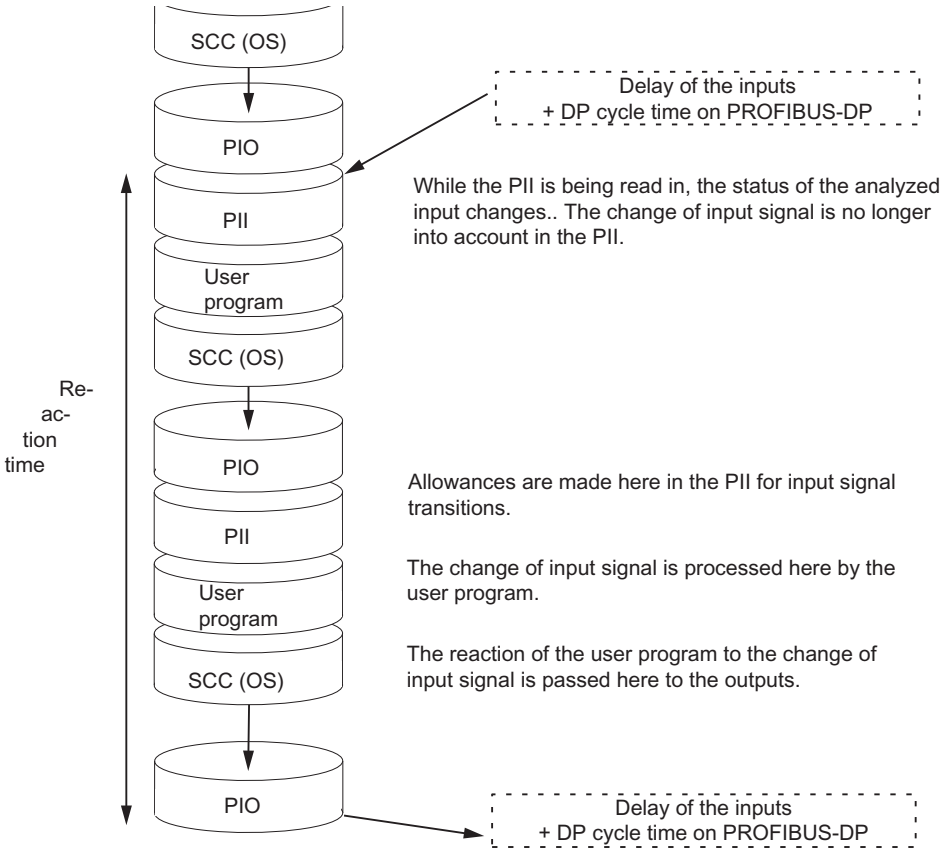


Figure 16-9 Longest response time

Calculation

The (longest) response time is calculated as follows:

- 2 x process image transfer time of the inputs +
- 2 x process image transfer time of the outputs +
- 2 x operating system processing time +
- 2 x program processing time +
- 2 x delay of the DP slave frame (including processing in the DP master) +
- Delay of the inputs and outputs

This is equivalent to the sum of twice the cycle time and the delay in the inputs and outputs plus twice the DP cycle time.

I/O direct access

You can achieve faster response times with direct access to the I/Os in your user program, e.g. with

- L PIB or
- T PQW

you can in part work around the response times as described above.

Reducing the response time

This reduces the maximum response time to

- Delay of the inputs and outputs
- User program execution time (can be interrupted by higher-priority interrupt handling)
- Runtime of direct access
- Twice the bus delay time of DP

The following table lists the execution times of direct access by the CPU to I/O modules. The times shown are "ideal values".

Table 16- 9 Direct access of the CPUs to I/O modules

Access mode	412-3H stand-alone mode	412-3H redundant	414-4H stand-alone mode	414-4H redundant	417-4H stand-alone mode	417-4H redundant
Read byte	3.5 µs	30.5 µs	3.0 µs	21.0 µs	2.2 µs	11.2 µs
Read word	5.2 µs	33.0 µs	4.5 µs	22.0 µs	3.9 µs	11.7 µs
Read double word	8.2 µs	33.0 µs	7.6 µs	23.5 µs	7.0 µs	14.7 µs
Write byte	3.5 µs	31.1 µs	2.8 µs	21.5 µs	2.3 µs	11.3 µs
Write word	5.2 µs	33.5 µs	4.5 µs	22.5 µs	3.9 µs	11.8 µs
Write double word	8.5 µs	33.5 µs	7.8 µs	24.0 µs	7.1 µs	15.0 µs

Table 16- 10 Direct access of the CPUs to I/O modules in the expansion unit with local link

Access mode	412-3H stand-alone mode	412-3H redundant	414-4H stand-alone mode	414-4H redundant	417-4H stand-alone mode	417-4H redundant
Read byte	6.9 µs	32.6 µs	6.3 µs	22.5 µs	5.7 µs	13.4 µs
Read word	12.1 µs	36.5 µs	11.5 µs	27.5 µs	10.8 µs	18.6 µs
Read double word	22.2 µs	46.5 µs	21.5 µs	37.5 µs	20.9 µs	28.7 µs
Write byte	6.6 µs	31.6 µs	5.9 µs	22.5 µs	5.5 µs	13.4 µs
Write word	11.7 µs	36.7 µs	11.0 µs	27.5 µs	10.4 µs	18.3 µs
Write double word	21.5 µs	46.4 µs	20.8 µs	37.0 µs	20.2 µs	28.0 µs

Table 16- 11 Direct access of the CPUs to I/O modules in the expansion unit with remote link

Access mode	412-3H stand-alone mode	412-3H redundant	414-4H stand-alone mode	414-4H redundant	417-4H stand-alone mode	417-4H redundant
Read byte	11.5 µs	35.0 µs	11.5 µs	26.0 µs	11.3 µs	17.0 µs
Read word	23.0 µs	47.0 µs	23.0 µs	37.5 µs	22.8 µs	28.6 µs
Read double word	46.0 µs	70.0 µs	46.0 µs	60.5 µs	45.9 µs	51.7 µs
Write byte	11.0 µs	35.0 µs	11.0 µs	26.0 µs	10.8 µs	16.8 µs
Write word	22.0 µs	46.0 µs	22.0 µs	37.0 µs	21.9 µs	27.8 µs
Write double word	44.5 µs	68.5 µs	44.5 µs	59.0 µs	44.0 µs	50.0 ms

The specified times are purely CPU processing times and apply, unless otherwise stated, to signal modules in the central unit.

Note

You can also achieve fast response times by using hardware interrupts; see section Interrupt response time (Page 299).

16.6 Calculating cycle and response times

Cycle time

1. Using the Instruction List, determine the runtime of the user program.
2. Calculate and add the process image transfer time. You will find guide values for this in the tables starting at 16-3.
3. Add the processing time at the scan cycle checkpoint. You will find guide values for this in Table 16–8.
4. Multiply the calculated value by the factor in Table 16–7.

The final result is the **cycle time**.

Extension of the cycle time due to communication and interrupts

1. Multiply the result by the following factor:

   100 / (100 – "configured communication load in %")

2. Using the instruction list, calculate the runtime of the program elements processing the interrupts. To do so, add the relevant value from Table 16-9.
   Multiply this value by the factor from step 4.
   Add this value to the theoretical cycle time as often as the interrupt is triggered or is expected to be triggered during the cycle time.

The result is an approximated **actual cycle time**. Note down the result.

Table 16- 12 Example of calculating the response time

Shortest response time	Longest response time
3. Next, calculate the delays in the inputs and outputs and, if applicable, the cycle times on the PROFIBUS DP network.	3. Multiply the actual cycle time by factor 2.
	4. Next, calculate the delays in the inputs and outputs and the DP cycle times on the PROFIBUS DP network.
4. The result you obtain is the **shortest response time**.	5. The result you obtain is the **longest response time**.

16.7 Examples of calculating the cycle and response times

Example I

You have installed an S7-400 with the following modules in the central unit:

- a 414-4H CPU in redundant system mode
- 2 digital input modules SM 421; DI 32xDC 24 V (each with 4 bytes in the PI)
- 2 digital output modules SM 422; DO 32xDC 24 V/0.5 (each with 4 bytes in the PI)

User program

According to the instruction list, the user program runtime is 15 ms.

Calculating the cycle time

The cycle time for the example results from the following times:

- As the CPU-specific factor is 1.2, the user program execution time is:
  approx. 18.0 ms
- Process image transfer time (4 double-word accesses)

  Process image: 9 µs + 4 ×25.7 µs = approx. 0.112 ms
- OS execution time at the scan cycle checkpoint:
  approx. 0.609 ms

The sum of the listed times is equivalent to the cycle time:

Cycle time = 18.0 ms + 0.112 ms + 0.609 ms **= 18.721 ms**.

Calculation of the actual cycle time

- Allowance for communication load (default value: 20%):
  18.721 ms * 100 / (100–20) **= 23.401 ms**.
- There is no interrupt processing.

So the actual, rounded up cycle time is **23.5 ms**.

Calculating the longest response time

- Longest response time
  23.5 ms * 2 **= 47.0 ms**.
- The delay of the inputs and outputs is negligible.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- There is no interrupt processing.

So the longest, rounded up response time is **= 47 ms**.

Example II

You have installed an S7-400 with the following modules:

- a 414–4H CPU in redundant system mode
- 4 digital input modules SM 421; DI 32×DC 24 V (each with 4 bytes in the PI)
- 3 digital output modules SM 422; DO 16xDC 24 V /2 (each with 2 bytes in the PI)
- 2 analog input modules SM 431; AI 8x13 bit (not in the PI)
- 2 analog output modules SM 432; AO 8x13 bit (not in the PI)

CPU parameters

The CPU was parameterized as follows:

- Cycle load due to communication: 40%

User program

According to the instruction list, the user program runtime is 10.0 ms.

Calculating the cycle time

The theoretical cycle time for the example is derived from the following times:

- As the CPU-specific factor is 1.2, the user program execution time is:
  approx. 12.0 ms
- Process image transfer time (4 x double-word access and 3 x word access)

  Process image: 9 µs + 7 ×25.7 µs = approx. 0.189 ms
- Operating system runtime at scan cycle checkpoint:
  approx. 0.609 ms

The sum of the listed times is equivalent to the cycle time:

Cycle time = 12.0 ms + 0.189 ms + 0.609 ms **= 12.789 ms**.

Calculation of the actual cycle time

- Allowance for communication load:
  12.789 ms * 100 / (100–40) **= 21.33 ms**.
- A time-of-day interrupt with a runtime of 0.5 ms is triggered every 100 ms.
  The interrupt can be triggered a maximum of one time during a cycle:
  0.5 ms + 0.588 ms (from table 16-9) **= 1.088 ms.**
  Allowing for communication load:
  1.088 ms * 100 / (100–40) **= 1.813 ms**.
- 21.33 ms + 1.813 ms **= 23.143 ms**.

Taking into account the time slices, the actual rounde up cycle time is **23.2 ms**.

Calculating the longest response time

- Longest response time
  23.2 ms * 2 **= 46.4 ms**.
- Delay of inputs and outputs
  - The maximum input delay of the digital input module SM 421; DI 32×DC 24 V is 4.8 ms per channel
  - The output delay of the digital output module SM 422; DO 16×DC 24 V/2A is negligible.
  - Analog input module SM 431; AI 8×13Bit was parameterized for 50 Hz interference frequency suppression. The result is a conversion time of 25 ms per channel. As 8 channels are active, a cycle time of the analog input module of 200 ms results.
  - Analog output module SM 432; AO 8×13Bit was parameterized for operation in the measuring range 0 ... 10 V. This results in a conversion time of 0.3 ms per channel. Since 8 channels are active, the result is a cycle time of 2.4 ms. The transient time of a resistive load of 0.1 ms must be added to this. The result is an analog output response time of 2.5 ms.
- All components are installed in the central unit, so DP cycle times can be ignored.
- Case 1: The system sets an output channel of the digital output module after a digital input signal is read in. The result is as follows:

  Response time = 46.4 ms + 4.8 ms = 51.2 ms.
- Case 2: The system reads in and outputs an analog value. The result is as follows:

  Response time = 46.4 ms + 200 ms + 2.5 ms = 248.9 ms.

16.8 Interrupt response time

Definition of interrupt response time

The interrupt response time is the time from the first occurrence of an interrupt signal to the call of the first instruction in the interrupt OB.

General rule: Higher priority interrupts are handled first. This means the interrupt response time is increased by the program execution time of the higher-priority interrupt OBs, and by previous interrupt OBs of the same priority which have not yet been processed (queue).

Calculating the interrupt response time

Minimum interrupt response time of the CPU
+ minimum interrupt response time of the signal modules
+ DP cycle time on PROFIBUS DP

= Shortest interrupt response time

Maximum interrupt response time of the CPU
+ maximum interrupt response time of the signal modules
+ 2 * DP cycle time on PROFIBUS DP

= Longest interrupt response time

Process and diagnostic interrupt response times of the CPUs

Table 16- 13 Process and interrupt response times; maximum interrupt response time without communication

CPU	Hardware interrupt response times		Diagnostic interrupt response times	
	min.	max.	min.	max.
412-3H stand-alone mode	366 µs	572 µs	354 µs	563 µs
412-3H redundant	370 µs	1143 µs	620 µs	982 µs
414-4H stand-alone mode	231 µs	361 µs	225 µs	356 µs
414-4H redundant	464 µs	726 µs	366 µs	592 µs
417-4H stand-alone mode	106 µs	158 µs	104 µs	167 µs
417-4H redundant	234 µs	336 µs	185 µs	294 µs

Increasing the maximum interrupt response time with communication

The maximum interrupt response time is extended when the communication functions are active. The additional time is calculated using the following formula:

CPU 41x–4H t_v = 100 µs + 1000 µs × n%, significant extension possible

where n = cycle load due to communication

Signal modules

The hardware interrupt response time of signal modules is made up as follows:

- Digital input modules

  Hardware interrupt response time = internal interrupt processing time + input delay

  You will find these times in the data sheet for the respective digital input module.

- Analog input modules

  Hardware interrupt response time = internal interrupt processing time + conversion time

  The internal interrupt processing time for analog input modules can be neglected. The conversion times can be found in the data sheet for the individual analog input modules.

The diagnostic interrupt response time of the signal modules is the time from detection of a diagnostic event by the signal module to the triggering of the diagnostic interrupt by the signal module. This short time can be neglected.

Hardware interrupt processing

Hardware interrupt processing begins when the hardware interrupt OB4x is called. Higher-priority interrupts stop hardware interrupt processing. Direct access to I/O modules is executed during the execution time of the operation. After the hardware interrupt has been processed, the system either resumes cyclic program processing, or calls and processes interrupt OBs of the same or lower priority.

16.9 Example of calculation of the interrupt response time

Elements of the interrupt response time

As a reminder: The hardware interrupt response time is made up of:

- The hardware interrupt response time of the CPU
- The hardware interrupt response time of the signal module
- Twice the DP cycle time on PROFIBUS DP

Example: You have installed a 417-4H CPU and four digital modules in the central unit. One digital input module is the SM 421; DI 16×UC 24/60 V; with process and diagnostic interrupts. You have enabled only the hardware interrupt in your CPU and SM parameterization. You decided not to use time-driven processing, diagnostics or error handling. You have parameterized an input delay of 0.5 ms for the digital input modules. No activities are required at the scan cycle checkpoint. You have set a cycle load of 20% due to communication.

Calculation

In this example, the hardware interrupt response time is based on following time factors:

- Hardware interrupt response time of CPU 417-4H: Approx. 0.6 ms (mean value in redundant system mode)
- Extension due to communication according to the description in section Interrupt response time (Page 299):

100 µs + 1000 µs × 20% = 300 µs = 0.3 ms

- Hardware interrupt response time of SM 421; DI 16×UC 24/60 V:
  - Internal interrupt processing time: 0.5 ms
  - Input delay: 0.5 ms
- The DP cycle time on the PROFIBUS DP is irrelevant, because the signal modules are installed in the central unit.

The hardware interrupt response time is equivalent to the sum of the listed time factors:

Hardware interrupt response time = 0.6 ms + 0.3 ms + 0.5 ms + 0.5 ms = **approx. 1.9 ms**.

This calculated hardware interrupt response time is the time between detection of a signal at the digital input and the call of the first instruction in OB 4x.

16.10 Reproducibility of delay and watchdog interrupts

Definition of "reproducibility"

Time-delay interrupt:

The period that expires between the call of the first operation in the interrupt OB and the programmed time of interrupt.

Watchdog interrupt:

The fluctuation range of the interval between two successive calls, measured between the respective initial operations of the interrupt OB.

Reproducibility

The following table contains the reproducibility of time-delay and watchdog interrupts of the CPUs.

Table 16- 14 Reproducibility of time-delay and watchdog interrupts of the CPUs

Module	Reproducibility	
	Time-delay interrupt	Watchdog interrupt
CPU 412-3H stand-alone mode	-499 µs / +469 µs	-315 µs / +305 µs
CPU 412-3H redundant	-557 µs / +722 µs	-710 µs / +655 µs
CPU 414-4H stand-alone mode	-342 µs / +386 µs	-242 µs / +233 µs
CPU 414-4H redundant	-545 µs / +440 µs	-793 µs / +620 µs
CPU 417-4H stand-alone mode	-311 µs / +277 µs	-208 µs / +210 µs
CPU 417-4H redundant	-453 µs / +514 µs	-229 µs / +289 µs

These times only apply if the interrupt can actually be executed at this time and if it is not delayed, for example, by higher-priority interrupts or queued interrupts of equal priority.

Technical data

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17.1 Technical data of the CPU 412–3H; (6ES7 412–3HJ14–0AB0)

CPU and version	
MLFB	6ES7 412–3HJ14–0AB0
• Firmware version	V 4.5
Associated programming package	STEP 7 V 5.3 SP2 or higher with hardware update

Memory	
Work memory	
• integrated	512 KB for code 256 KB for data
Load memory	
• integrated	256 KB of RAM
• Expandable FEPROM	With memory card (FLASH) 1 MB up to 64 MB
• Expandable RAM	With memory card (RAM) 256 KB up to 64 MB
Backup with battery	Yes, all data

Execution times	
Execution times of	
• Bit instructions	75 ns
• Word instructions	75 ns
• Fixed-point arithmetic	75 ns
• Floating-point arithmetic	225 ns

Timers/counters and their retentivity	
S7 counters	2048
• Retentivity, configurable	From C 0 to C 2047
• Default	From C 0 to C 7
• Counting range	0 to 999
IEC counters	Yes

Timers/counters and their retentivity	
• Type	SFB
S7 timers	2048
• Retentivity, configurable	From T 0 to T 2047
• Default	No retentive timers
• Time setting range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data areas and their retentivity	
Total retentive data area (incl. bit memories, timers, counters)	Total work and load memory (with backup battery)
Bit memory	8 KB
• Retentivity, configurable	From MB 0 to MB 8191
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Maximum 4095 (DB 0 reserved) Number range 1 - 4095
• Size	Maximum 64 KB
Local data (selectable)	Maximum 16 KB
• Default	8 KB

Blocks	
OBs	See instruction list
• Size	Maximum 64 KB
Nesting depth	
• Per priority class	24
• Additional ones in an error OB	1
SDBs	Maximum 512
FBs	Maximum 2048 Number range 0 - 2047
• Size	Maximum 64 KB
FCs	Maximum 2048 Number range 0 - 2047
• Size	Maximum 64 KB

Address areas (inputs/outputs)	
Total I/O address area	8 KB/8 KB
• Distributed	Including diagnostic addresses, addresses for I/O interface modules, etc.
MPI/DP interface	2 KB/2 KB
Process image	8 KB / 8 KB (selectable)
• Default	256 bytes/256 bytes
• Number of process image partitions	Maximum 15
• Consistent data	Max. 244 bytes
Access to consistent data in the process image	Yes
Digital channels	Maximum 65536/ Maximum 65536
• Central	Maximum 65536/ Maximum 65536
Analog channels	Maximum 4096/ Maximum 4096
• Central	Maximum 4096/ Maximum 4096

Construction	
Central units/expansion units	Maximum 1/21
Multicomputing	No
Number of plug-in IMs (total)	Maximum 6
• IM 460	Maximum 6
• IM 463–2	Maximum 4, in stand-alone mode only
Number of DP masters	
• integrated	1
• Via CP 443–5 Ext.	Maximum 10
Operable FMs and CPs	
• FM, CP (point-to-point) see Appendix Function modules and communication processors supported by the S7-400H (Page 355)	Limited by the number of slots and the number of connections
• CP 441	Limited by the number of connections, maximum of 30
• PROFIBUS and Ethernet CPs including CP 443–5 Extended	Maximum 14, of which max. 10 CPs as DP masters
Connectable OPs	15, 8 of these with message processing

Time	
Clock (real-time clock)	Yes
• Buffered	Yes
• Resolution	1 ms
Maximum deviation per day	
• Power off (backed up)	1.7 s
• Power on (not backed up)	8.6 s
Runtime meter	8
• Number/number range	0 to 7
• Value range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Clock synchronization	Yes
• In AS, on MPI and DP	As master or slave
Time difference in the system with synchronization via MPI	Max. 200 ms

S7 message functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Maximum 8
Block-related messages	Yes
• Simultaneously active Alarm_S/SQ blocks or Alarm_D/DQ blocks	Maximum 100
Alarm_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (selectable)	Maximum 600
• Default	300
Process control messages	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16

Test and commissioning functions	
Status/modify variable	Yes
• Variable	Inputs/outputs, bit memories, DB, distributed inputs/outputs, timers, counters
• Number of variables	Maximum 70
Forcing	Yes
• Variable	Inputs/outputs, bit memories, distributed inputs/outputs
• Number of variables	Maximum 256
Status LED	Yes, FRCE-LED
Status block	Yes
Single step	Yes
Number of breakpoints	4
Diagnostic buffer	Yes
• Number of entries	Maximum 3200 (selectable)
• Default	120

Communication	
PG/OP communication	Yes
Routing	Yes
S7 communication	Yes
• User data per job	Maximum 64 KB
• Of which consistent	1 variable (462 bytes)
S7 basic communication	No
Global data communication	No
S5-compatible communication	Using FC AG_SEND and AG_RECV, max. via 10 CPs 443–1 or 443–5
• User data per job	Maximum 8 KB
• Of which consistent	240 bytes
Number of simultaneous AG_SEND/AG_RECV jobs	Maximum 24/24, see CP manual
Standard communication (FMS)	Yes, via CP and loadable FB
Number of connection resources for S7 connections via all interfaces and CPs	16, incl. one each reserved for programming device and OP

Interfaces
Do not configure the CPU as a DP slave.

1. interface	
Designation of the interface	X1
Type of interface	integrated
Physics	RS 485/PROFIBUS and MPI
Isolated	Yes
Interface power supply (15 to 30 V DC)	Max. 150 mA
Number of connection resources	MPI: 16, DP: 16

Functionality	
• MPI	Yes
• PROFIBUS DP	DP master

1. interface in MPI mode	
Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Transmission rates	Maximum 12 Mbit/s

1. interface in DP master mode	
Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Constant bus cycle time	No
• SYNC/FREEZE	No
• Enable/disable DP slaves	No
• Direct data exchange (slave-to-slave communication)	No
Transmission rates	Maximum 12 Mbit/s

1. interface in DP master mode	
Number of DP slaves	Maximum 32
Number of slots per interface	Maximum 544
Address range	Maximum 2 KB inputs / 2 KB outputs
User data per DP slave	Maximum 244 Maximum 244 bytes inputs Maximum 244 bytes outputs Maximum 244 slots Maximum 128 bytes per slot
Note: • The total sum of the input bytes across all slots may not exceed 244. • The total sum of the output bytes across all slots may not exceed 244. • The address range of the interface (maximum 2 KB inputs / 2 KB outputs) must not be exceeded in total across all 32 slaves.	

2. and 3rd interface	
Designation of the interfaces	IF1, IF2
Type of interface	Plug-in synchronization module (fiber-optic cable)
Usable interface module	Synchronization module IF 960 (only in redundant system mode; in stand-alone mode the interface remains free/covered)
Length of the synchronization cable	Max. 10 m, can only be operated with synchronization module 6ES7 960-1AA04-0XA0

Programming	
Programming language	LAD, FBD, STL, SCL, CFC, Graph, HiGraph®
Instruction set	See instruction list
Nesting levels	8
System functions (SFC)	See instruction list
Number of simultaneously active SFCs per chain	
• SFC 59 "RD_REC"	8
• SFC 58 "WR_REC"	8
• SFC 55 "WR_PARM"	8
• SFC 57 "PARM_MOD"	1
• SFC 56 "WR_DPARM"	2
• SFC 13 "DPNRM_DG"	8
• SFC 51 "RDSYSST"	8
• SFC 103 "DP_TOPOL"	1

Programming	
The total number of active SFCs on all external chains may be four times more than on one single chain.	
System function blocks (SFB)	See instruction list
Number of simultaneously active SFBs per chain	
• SFB 52 "RDREC"	8
• SFB 53 "WRREC"	8
The total number of active SFBs on all external chains may be four times more than on one single chain.	
User program protection	Password protection
Access to consistent data in the process image	Yes

CiR synchronization time (in stand-alone mode)	
Base load	150 ms
Time per I/O byte	40 µs

Dimensions	
Mounting dimensions W x H x D (mm)	50 x 290 x 219
Slots required	2
Weight	Approx. 0.990 kg

Voltages and currents	
Current consumption from the S7-400 bus (5 V DC)	Typ. 1.2 A Max. 1.5 A
Current consumption from S7-400 bus (24 V DC) The CPU does not consume any current at 24 V, it only makes this voltage available on the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, however with a maximum of 150 mA per interface
Current output to DP interface (5 V DC)	Max. 90 mA
Backup current	Average 190 µA (up to 40 °C) Maximum 660 µA
Maximum backup time	See *Module Specifications* Reference Manual, Section 3.3.
Feed of external backup voltage to the CPU	5 V to 15 V DC
Power loss	Typ. 6.0 W

17.2 Technical data of the CPU 414–4H; (6ES7 414–4HM14–0AB0)

CPU and version	
MLFB	6ES7 414–4HM14–0AB0
• Firmware version	V 4.5
Associated programming package	STEP 7 V 5.3 SP2 or higher with hardware update

Memory	
Work memory	
• integrated	1400 KB for code 1400 KB for data
Load memory	
• integrated	256 KB of RAM
• Expandable FEPROM	With memory card (FLASH) 1 MB up to 64 MB
• Expandable RAM	With memory card (RAM) 256 KB up to 64 MB
Backup with battery	Yes, all data

Execution times	
Execution times of	
• Bit instructions	45 ns
• Word instructions	45 ns
• Fixed-point arithmetic	45 ns
• Floating-point arithmetic	135 ns

Timers/counters and their retentivity	
S7 counters	2048
• Retentivity, configurable	From C 0 to C 2047
• Default	From C 0 to C 7
• Counting range	0 to 999
IEC counters	Yes
• Type	SFB
S7 timers	2048
• Retentivity, configurable	From T 0 to T 2047
• Default	No retentive timers

Timers/counters and their retentivity	
• Time setting range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data areas and their retentivity	
Total retentive data area (incl. bit memories, timers, counters)	Total work and load memory (with backup battery)
Bit memory	8 KB
• Retentivity, configurable	From MB 0 to MB 8191
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Maximum 4095 (DB 0 reserved) Number range 1 - 4095
• Size	Maximum 64 KB
Local data (selectable)	Maximum 16 KB
• Default	8 KB

Blocks	
OBs	See instruction list
• Size	Maximum 64 KB
Nesting depth	
• Per priority class	24
• Additional ones in an error OB	1
SDBs	Maximum 512
FBs	Maximum 2048 Number range 0 - 2047
• Size	Maximum 64 KB
FCs	Maximum 2048 Number range 0 - 2047
• Size	Maximum 64 KB

Address areas (inputs/outputs)	
Total I/O address area	8 KB/8 KB
• Distributed	Including diagnostic addresses, addresses for I/O interface modules, etc.
MPI/DP interface	2 KB/2 KB
DP interface	6 KB/6 KB
Process image	8 KB / 8 KB (selectable)
• Default	256 bytes/256 bytes
• Number of process image partitions	Maximum 15
• Consistent data	Max. 244 bytes
Access to consistent data in the process image	Yes
Digital channels	Maximum 65536/ Maximum 65536
• Central	Maximum 65536/ Maximum 65536
Analog channels	Maximum 4096/ Maximum 4096
• Central	Maximum 4096/ Maximum 4096

Construction	
Central units/expansion units	Maximum 1/21
Multicomputing	No
Number of plug-in IMs (total)	Maximum 6
• IM 460	Maximum 6
• IM 463–2	Maximum 4, in stand-alone mode only
Number of DP masters	
• integrated	2
• Via CP 443–5 Ext.	Maximum 10
Operable FMs and CPs	
• FM, CP (point-to-point) see Appendix Function modules and communication processors supported by the S7-400H (Page 355)	Limited by the number of slots and the number of connections
• CP 441	Limited by the number of connections, maximum of 30
• PROFIBUS and Ethernet CPs including CP 443–5 Extended	Maximum 14, of which max. 10 CPs as DP masters
Connectable OPs	31, 8 of these with message processing

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
Maximum deviation per day	
• Power off (backed up)	1.7 s
• Power on (not backed up)	8.6 s
Runtime meter	8
• Number	0 to 7
• Value range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Clock synchronization	Yes
• In AS, on MPI and DP	As master or slave
Time difference in the system with synchronization via MPI	Max. 200 ms

S7 message functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Maximum 8
Block-related messages	Yes
• Simultaneously active Alarm_S/SQ blocks or Alarm_D/DQ blocks	Maximum 100
Alarm_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (selectable)	Maximum 1200
• Default	900
Process control messages	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16

Test and commissioning functions	
Status/modify variable	Yes
• Variable	Inputs/outputs, bit memories, DB, distributed inputs/outputs, timers, counters
• Number of variables	Maximum 70
Forcing	Yes
• Variable	Inputs/outputs, bit memories, distributed inputs/outputs
• Number of variables	Maximum 256
Status LED	Yes, FRCE-LED
Status block	Yes
Single step	Yes
Number of breakpoints	4
Diagnostic buffer	Yes
• Number of entries	Maximum 3200 (configurable)
• Default	120

Communication	
PG/OP communication	Yes
Routing	Yes
S7 communication	Yes
• User data per job	Maximum 64 KB
• Of which consistent	1 variable (462 bytes)
S7 basic communication	No
Global data communication	No
S5-compatible communication	Using FC AG_SEND and AG_RECV, max. via 10 CPs 443–1 or 443–5
• User data per job	Maximum 8 KB
• Of which consistent	240 bytes
Number of simultaneous AG_SEND/AG_RECV jobs	Maximum 24/24, see CP manual
Standard communication (FMS)	Yes (via CP and loadable FB)
Number of connection resources for S7 connections via all interfaces and CPs	32, incl. one each reserved for programming device and OP

Interfaces
Do not configure the CPU as a DP slave.

1. interface	
Designation of the interface	X1
Type of interface	integrated
Physics	RS 485/Profibus
Isolated	Yes
Interface power supply (15 to 30 V DC)	Maximum 150 mA
Number of connection resources	MPI: 32, DP: 32

Functionality	
• MPI	Yes
• PROFIBUS DP	DP master

1. interface in MPI mode	
Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Transmission rates	Maximum 12 Mbit/s

1. interface in DP master mode	
• Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Constant bus cycle time	No
• SYNC/FREEZE	No
• Enable/disable DP slaves	No
• Direct data exchange (slave-to-slave communication)	No

1. interface in DP master mode	
• Transmission rates	Maximum 12 Mbit/s
• Number of DP slaves	Maximum 32
• Number of slots per interface	Maximum 544
• Address range	Maximum 2 KB inputs / 2 KB outputs
• User data per DP slave	Maximum 244 bytes Maximum 244 bytes inputs, Maximum 244 bytes outputs, Maximum 244 slots Maximum 128 bytes per slot
Note: • The total sum of the input bytes across all slots may not exceed 244. • The total sum of the output bytes across all slots may not exceed 244. • The address range of the interface (maximum 2 KB inputs / 2 KB outputs) must not be exceeded in total across all 32 slaves.	

2. interface	
Designation of the interface	X2
Type of interface	integrated
Physics	RS 485/Profibus
Isolated	Yes
Interface power supply (15 to 30 V DC)	Maximum 150 mA
Number of connection resources	16

Functionality	
• PROFIBUS DP	DP master

2. interface in DP master mode	
Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Constant bus cycle time	No
• SYNC/FREEZE	No

2. interface in DP master mode	
• Enable/disable DP slaves	No
• Direct data exchange (slave-to-slave communication)	No
• Transmission rates	Up to 12 Mbit/s
• Number of DP slaves	Maximum 96
• Number of slots per interface	Maximum 1632
• Address range	Maximum 6 KB inputs / 6 KB outputs
• User data per DP slave	Maximum 244 bytes Maximum 244 bytes inputs, Maximum 244 bytes outputs, Maximum 244 slots Maximum 128 bytes per slot
Note: • The total sum of the input bytes across all slots may not exceed 244. • The total sum of the output bytes across all slots may not exceed 244. • The address range of the interface (maximum 6 KB inputs/6 KB outputs) must not be exceeded in total across all 96 slaves.	

3. and 4th interface	
Designation of the interfaces	IF1, IF2
Type of interface	Plug-in synchronization module (fiber-optic cable)
Usable interface module	Synchronization module IF 960 (only in redundant system mode; in stand-alone mode the interface remains free/covered)
Length of the synchronization cable	Maximum 10 km

Programming	
Programming language	LAD, FBD, STL, SCL, CFC, Graph, HiGraph®
Instruction set	See instruction list
Nesting levels	8
System functions (SFC)	See instruction list
Number of simultaneously active SFCs per chain	
• SFC 59 "RD_REC"	8
• SFC 58 "WR_REC"	8
• SFC 55 "WR_PARM"	8
• SFC 57 "PARM_MOD"	1
• SFC 56 "WR_DPARM"	2
• SFC 13 "DPNRM_DG"	8

Programming	
• SFC 51 "RDSYSST"	8
• SFC 103 "DP_TOPOL"	1
The total number of active SFCs on all external chains may be four times more than on one single chain.	
System function blocks (SFB)	See instruction list
Number of simultaneously active SFBs per chain	
• SFB 52 "RDREC"	8
• SFB 53 "WRREC"	8
The total number of active SFBs on all external chains may be four times more than on one single chain.	
User program protection	Password protection
Access to consistent data in the process image	Yes

CiR synchronization time (in stand-alone mode)	
Base load	100 ms
Time per I/O byte	25 µs

Dimensions	
Mounting dimensions W x H x D (mm)	50 x 290 x 219
Slots required	2
Weight	Approx. 0.995 kg

Voltages and currents	
Current consumption from S7–400 bus (5 V DC)	Typ. 1.4 A Max. 1.7 A
Current consumption from S7-400 bus (24 V DC) The CPU does not consume any current at 24 V, it only makes this voltage available on the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, however, a maximum of 150 mA per interface
Current output to DP interface (5 V DC)	Max. 90 mA
Backup current	Average 190 µA (up to 40 °C) Maximum 660 µA
Maximum backup time	See *Module Specifications* Reference Manual, Section 3.3.
Feed of external backup voltage to the CPU	5 V to 15 V DC
Power loss	Typ. 7.0 W

17.3 Technical data of the CPU 417–4H; (6ES7 417–4HT14–0AB0)

CPU and version	
MLFB	6ES7 417–4HT14–0AB0
• Firmware version	V 4.5
Associated programming package	STEP 7 V 5.3 SP2 or higher with hardware update

Memory	
Work memory	
• integrated	15 MB for code 15 MB for data
Load memory	
• integrated	256 KB of RAM
• Expandable FEPROM	With memory card (FLASH) 1 MB up to 64 MB
• Expandable RAM	With memory card (RAM) 256 KB up to 64 MB
Backup with battery	Yes, all data

Execution times	
Execution times of	
• Bit instructions	18 ns
• Word instructions	18 ns
• Fixed-point arithmetic	18 ns
• Floating-point arithmetic	54 ns

Timers/counters and their retentivity	
S7 counters	2048
• Retentivity, configurable	From C 0 to C 2047
• Default	From C 0 to C 7
• Counting range	0 to 999
IEC counters	Yes
• Type	SFB
S7 timers	2048
• Retentivity, configurable	From T 0 to T 2047
• Default	No retentive timers

Timers/counters and their retentivity	
• Time setting range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data areas and their retentivity	
Total retentive data area (incl. bit memories, timers, counters)	Total work and load memory (with backup battery)
Bit memory	16 KB
• Retentivity, configurable	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Maximum 8191 (DB 0 reserved) Number range 1 to 8191
• Size	Maximum 64 KB
Local data (selectable)	Maximum 64 KB
• Default	32 KB

Blocks	
OBs	See instruction list
• Size	Maximum 64 KB
Nesting depth	
• Per priority class	24
• Additional ones in an error OB	2
SDBs	Maximum 512
FBs	Maximum 6144 Number range 0 - 6143
• Size	Maximum 64 KB
FCs	Maximum 6144 Number range 0 - 6143
• Size	Maximum 64 KB

Address areas (inputs/outputs)	
Total I/O address area	16 KB/16 KB
• Distributed	incl. diagnostics addresses, addresses for I/O interface modules, etc
MPI/DP interface	2 KB/2 KB
DP interface	8 KB/8 KB
Process image	16 KB/16 KB (programmable)
• Default	1024 bytes/1024 bytes
• Number of process image partitions	Maximum 15
• Consistent data	Max. 244 bytes
Access to consistent data in the process image	Yes
Digital channels	Maximum 131072/ Maximum 131072
• Central	Maximum 131072/ Maximum 131072
Analog channels	Maximum 8192/ Maximum 8192
• Central	Maximum 8192/ Maximum 8192

Construction	
Central units/expansion units	Maximum 1/21
Multicomputing	No
Number of plug-in IMs (total)	Maximum 6
• IM 460	Maximum 6
• IM 463–2	Maximum 4, in stand-alone mode only
Number of DP masters	
• integrated	2
• Via CP 443–5 Ext.	Maximum 10
Number of plug-in S5 modules via adapter casing (in the central unit)	None
Operable function modules and communications processors	
• FM, CP (point-to-point) see Appendix Function modules and communication processors supported by the S7-400H (Page 355)	Limited by the number of slots and the number of connections
• CP 441	Limited by the number of connections, maximum of 30
• PROFIBUS and Ethernet CPs including CP 443–5 Extended	Maximum 14, of which max. 10 CPs as DP masters
Connectable OPs	63, 16 of these with message processing

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
Maximum deviation per day	
• Power off (backed up)	1.7 s
• Power on (not backed up)	8.6 s
Runtime meter	8
• Number	0 to 7
• Value range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Clock synchronization	Yes
• In AS, on MPI and DP	As master or slave
Time difference in the system with synchronization via MPI	Max. 200 ms

S7 message functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Maximum 16
Block-related messages	Yes
• Simultaneously active Alarm_S/SQ blocks or Alarm_D/DQ blocks	Maximum 200
Alarm_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (selectable)	Maximum 10000
• Default	1200
Process control messages	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	64

Test and commissioning functions	
Status/modify variable	Yes
• Variable	Inputs/outputs, bit memories, DB, distributed inputs/outputs, timers, counters
• Number of variables	Maximum 70
Forcing	Yes
• Variable	Inputs/outputs, bit memories, distributed inputs/outputs
• Number of variables	Maximum 512
Status LED	Yes, FRCE-LED
Status block	Yes
Single step	Yes
Number of breakpoints	4
Diagnostic buffer	Yes
• Number of entries	Maximum 3200 (configurable)
• Default	120

Communication	
PG/OP communication	Yes
Routing	Yes
Number of connection resources for S7 connections via all interfaces and CPs	64, incl. one each reserved for programming device and OP
S7 communication	Yes
• User data per job	64 bytes
• Of which consistent	1 variable (462 bytes)
Global data communication	No
S7 basic communication	No
S5-compatible communication	Using FC AG_SEND and AG_RECV, max. via 10 CPs 443–1 or 443–5
• User data per job	Maximum 8 KB
• Of which consistent	240 bytes
Number of simultaneous AG_SEND/AG_RECV jobs	Maximum 64/64, see CP manual
Standard communication (FMS)	Yes (by means of CP and loadable FC)
Number of connection resources for S7 connections via all interfaces and CPs	64, incl. one each reserved for programming device and OP

Interfaces
Do not configure the CPU as a DP slave.

1. interface	
Designation of the interface	X1
Type of interface	integrated
Physics	RS 485/Profibus
Isolated	Yes
Interface power supply (15 to 30 V DC)	Maximum 150 mA
Number of connection resources	MPI: 44, DP: 32 a diagnostic repeater in the chain reduces the number of connection resources by 1

Functionality	
• MPI	Yes
• PROFIBUS DP	DP master

1. interface in MPI mode	
• Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Transmission rates	Maximum 12 Mbit/s

1. interface in DP master mode	
Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Constant bus cycle time	No
• SYNC/FREEZE	No
• Enable/disable DP slaves	No

1. interface in DP master mode	
• Direct data exchange (slave-to-slave communication)	No
Transmission rates	Maximum 12 Mbit/s
Number of DP slaves	Maximum 32
Number of slots per interface	Maximum 544
Address range	Maximum 2 KB inputs / 2 KB outputs
User data per DP slave	Maximum 244 bytes Maximum 244 bytes inputs, Maximum 244 bytes outputs, Maximum 244 slots Maximum 128 bytes per slot
Note: • The total sum of the input bytes across all slots may not exceed 244. • The total sum of the output bytes across all slots may not exceed 244. • The address range of the interface (maximum 2 KB inputs / 2 KB outputs) must not be exceeded in total across all 32 slaves.	

2. interface	
Designation of the interface	X2
Type of interface	integrated
Physics	RS 485/Profibus
Isolated	Yes
Interface power supply (15 to 30 V DC)	Maximum 150 mA
Number of connection resources	32, a diagnostic repeater in the chain reduces the number of connection resources by 1

Functionality	
• PROFIBUS DP	DP master

2. interface in DP master mode	
Services	
• PG/OP communication	Yes
• Routing	Yes
• S7 communication	Yes
• Global data communication	No
• S7 basic communication	No
• Constant bus cycle time	No
• SYNC/FREEZE	No
• Enable/disable DP slaves	No
• Direct data exchange (slave-to-slave communication)	No
Transmission rates	Maximum 12 Mbit/s
Number of DP slaves	Maximum 125
Number of slots per interface	Maximum 2173
Address range	Maximum 8 KB inputs / 8 KB outputs
User data per DP slave	Maximum 244 bytes Maximum 244 bytes inputs, Maximum 244 bytes outputs, Maximum 244 slots Maximum 128 bytes per slot
Note: • The total sum of the input bytes across all slots may not exceed 244. • The total sum of the output bytes across all slots may not exceed 244. • The address range of the interface (maximum 8 KB inputs / 8 KB outputs) must not be exceeded in total across all 125 slaves.	

3. and 4th interface	
Designation of the interfaces	IF1, IF2
Type of interface	Plug-in synchronization module (fiber-optic cable)
Usable interface module	Synchronization module IF 960 (only in redundant system mode; in stand-alone mode the interface remains free/covered)
Length of the synchronization cable	Maximum 10 km

Programming	
Programming language	LAD, FBD, STL, SCL, CFC, Graph, HiGraph®
Instruction set	See instruction list
Nesting levels	8
System functions (SFC)	See instruction list
Number of simultaneously active SFCs per chain	
• SFC 59 "RD_REC"	8
• SFC 58 "WR_REC"	8
• SFC 55 "WR_PARM"	8
• SFC 57 "PARM_MOD"	1
• SFC 56 "WR_DPARM"	2
• SFC 13 "DPNRM_DG"	8
• SFC 51 "RDSYSST"	8
• SFC 103 "DP_TOPOL"	1
The total number of active SFCs on all external chains may be four times more than on one single chain.	
System function blocks (SFB)	See instruction list
Number of simultaneously active SFBs per chain	
• SFB 52 "RDREC"	8
• SFB 53 "WRREC"	8
The total number of active SFBs on all external chains may be four times more than on one single chain.	
User program protection	Password protection
Access to consistent data in the process image	Yes

CiR synchronization time (in stand-alone mode)	
Base load	60 ms
Time per I/O byte	10 µs

Dimensions	
Mounting dimensions W x H x D (mm)	50 x 290 x 219
Slots required	2
Weight	Approx. 0.995 kg

Voltages and currents	
Current consumption from S7–400 bus (5 V DC)	Typ. 1.5 A Max. 1.8 A
Current consumption from S7-400 bus (24 V DC) The CPU does not consume any current at 24 V, it only makes this voltage available on the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, however, a maximum of 150 mA per interface
Current output to DP interface (5 V DC)	Max. 90 mA
Backup current	Average 970 µA (up to 40 °C) Maximum 1980 µA
Maximum backup time	See Module Data Reference Manual, section 3.3
Feed of external backup voltage to the CPU	5 V to 15 V DC
Power loss	Typ. 7.5 W

17.4 Technical data of memory cards

Data

Name	Order number	Current consumption at 5 V	Backup currents
MC 952 / 256 KB / RAM	6ES7952-1AH00-0AA0	typ. 35 mA max. 80 mA	typ. 1 µA max. 40 µA
MC 952 / 1 MB / RAM	6ES7952-1AK00-0AA0	typ. 40 mA max. 90 mA	typ. 3 µA max. 50 µA
MC 952 / 2 MB / RAM	6ES7952-1AL00-0AA0	typ. 45 mA max. 100 mA	typ. 5 µA max. 60 µA
MC 952 / 4 MB / RAM	6ES7952-1AM00-0AA0	typ. 45 mA max. 100 mA	typ. 5 µA max. 60 µA
MC 952 / 8 MB / RAM	6ES7952-1AP00-0AA0	typ. 45 mA max. 100 mA	typ. 5 µA max. 60 µA
MC 952 / 16 MB / RAM	6ES7952-1AS00-0AA0	typ. 100 mA max. 150 mA	typ. 50 µA max. 125 µA
MC 952 / 64 MB / RAM	6ES7952-1AY00-0AA0	typ. 100 mA max. 150 mA	typ. 100 µA max. 500 µA
MC 952 / 1 MB / 5 V FLASH	6ES7952-1KK00-0AA0	typ. 40 mA max. 90 mA	–
MC 952 / 2 MB / 5 V FLASH	6ES7952-1KL00-0AA0	typ. 50 mA max. 100 mA	–
MC 952 / 4 MB / 5 V FLASH	6ES7952-1KM00-0AA0	typ. 40 mA max. 90 mA	–
MC 952 / 8 MB / 5 V FLASH	6ES7952-1KP00-0AA0	typ. 50 mA max. 100 mA	–
MC 952 / 16 MB / 5 V FLASH	6ES7952-1KS00-0AA0	typ. 55 mA max. 110 mA	–
MC 952 / 32 MB / 5 V FLASH	6ES7952-1KT00-0AA0	typ. 55 mA max. 110 mA	–
MC 952 / 64 MB / 5 V FLASH	6ES7952-1KY00-0AA0	typ. 55 mA max. 110 mA	–
Dimensions WxHxD (in mm)		7.5 x 57 x 87	
Weight		Max. 35 g	
EMC protection		Provided by construction	

17.5 Runtimes of the FCs and FBs for redundant I/Os

Table 17- 1 Runtimes of the blocks for redundant I/Os

Block	Runtime in stand-alone/single mode	Runtime in redundant mode
FC 450 RED_INIT Specifications are based on the startup	2 ms + 300 µs / configured module pairs The specification for a module pair is a mean value. The runtime may be < 300 µs for a few modules. For a large number of redundant modules the value may be > 300 µs.	-
FC 451 RED_DEPA	160 µs	360 µs
FB 450 RED_IN Called from the corresponding sequence level.	750 µs + 60 µs / module pair of the current TPA The specification for a module pair is a mean value. The runtime may be additionally increased if discrepancies occur resulting in passivation and logging to the diagnostic buffer. The runtime may also be increased by a depassivation carried out at the individual sequence levels of FB RED_IN. Depending on the number of modules in the sequence level, the depassivation may increase the runtime of the FB RED_IN by 0.4 ... 8 ms. An 8 ms increase can be expected in redundant operation of modules totaling more than 370 pairs of modules at a sequence level.	1000 µs + 70 µs / module pair of the current TPA The specification for a module pair is a mean value. The runtime may be additionally increased if discrepancies occur resulting in passivation and logging to the diagnostic buffer. The runtime may also be increased by a depassivation carried out at the individual sequence levels of FB RED_IN. Depending on the number of modules in the sequence level, the depassivation may increase the runtime of the FB RED_IN by 0.4 ... 8 ms. An 8 ms increase can be expected in redundant operation of modules totaling more than 370 pairs of modules at a sequence level.
FB 451 RED_OUT Called from the corresponding sequence level.	650 µs + 2 µs / module pair of the current TPA The specification for a module pair is a mean value. The runtime may be < 2 µs for a few modules. For a large number of redundant modules the value may be > 2 µs.	860 µs + 2 µs / module pair of the current TPA The specification for a module pair is a mean value. The runtime may be < 2 µs for a few modules. For a large number of redundant modules the value may be > 2 µs.

Block	Runtime in stand-alone/single mode	Runtime in redundant mode
FB 452 RED_DIAG	Called in OB 72: 160 µs Called in OB 82, 83, 85: 250 µs + 5 µs / configured module pairs Under extreme conditions the runtime of FB RED_DIAG is increased up to 1.5 ms. . This is the case when the working DB is 60 KB or larger and if there are interrupt trigger addresses that do not belong to the redundant I/O.	Called in OB 72: 360 µs Called in OB 82, 83, 85: 430 µs (basic load) + 6 µs / configured module pairs Under extreme conditions the runtime of FB RED_DIAG is increased up to 1.5 ms. . This is the case when the working DB is 60 KB or larger and if there are interrupt trigger addresses that do not belong to the redundant I/O.
FB 453 RED_STATUS	160 µs 4 µs/ configured module pairs * number of module pairs) The runtime depends on the random position of the module being searched for in the working DB. When a module address is not redundant, the entire working DB is searched. This results in the longest runtime of FB RED_STATUS. The number of module pairs is based either on all inputs (DI/AI) or all outputs (DO/AO).	350 µs + 5 µs / configured module pairs * number of module pairs) The runtime depends on the random position of the module being searched for in the working DB. When a module address is not redundant, the entire working DB is searched. This results in the longest runtime of FB RED_STATUS. The number of module pairs is based either on all inputs (DI/AI) or all outputs (DO/AO).

NOTICE

These are guide values, not absolute values. The actual value may deviate from these specifications in some cases. This overview is intended as a guide and should help you estimate how use of the RED_IO library may change the cycle time.

Characteristic values of redundant automation systems

A

This appendix provides a brief introduction to the characteristic values of redundant automation systems, and shows the practical effects of redundant configurations, based on a selection of configurations.

You will find an overview of the MTBF of various SIMATIC products in the SIMATIC FAQ at:

http://support.automation.siemens.com

under entry ID 16818490

A.1 Basic concepts

The quantitative assessment of redundant automation systems is usually based on their reliability and availability parameters. These are described in detail below.

Reliability

Reliability refers to the capability of technical equipment to fulfill its function during its operating period. This is usually no longer the case if any of its components fails.

So a commonly used measure for reliability is the **MTBF** (**M**ean **T**ime **B**etween **F**ailure). This can be analyzed statistically based on the parameters of running systems, or by calculating the failure rates of the components used.

Reliability of modules

The reliability of SIMATIC components is extremely high as a consequence of extensive quality assurance measures in design and production.

Reliability of automation systems

The use of redundant modules considerably prolongs the MTBF of a system. The combination of integrated high-quality self-tests and error detection mechanisms of the S7-400H CPUs allows the detection and localization of virtually all errors.

The MTBF of an S7-400H is determined by the **MDT** (**M**ean **D**own **T**ime) of a system unit. This time is derived in essence from the error detection time plus the time required to repair or replace defective modules.

In addition to other measures, a CPU provides a self-test function with an adjustable test cycle time. The default test cycle time is 90 minutes. This time has an influence on the error detection time. The repair time usually required for a modular system such as the S7-400H is 4 hours.

Mean Down Time (MDT)

The MDT of a system is determined by the times outlined below:

- Time required to detect an error
- Time required to find the cause of an error
- Time required for troubleshooting and to restart the system

The system MDT is calculated based on the MDT of the individual system components. The structure in which the components make up the system also forms part of the calculation.

Correlation between MDT and MTBF: MDT << MTBF

The MDT value is of the highest significance for the quality of system maintenance. The most important factors are:

- Qualified personnel
- Efficient logistics
- High-performance tools for diagnostics and error recognition
- A sound repair strategy

The figure below shows the dependency of the MDT on the times and factors mentioned above.

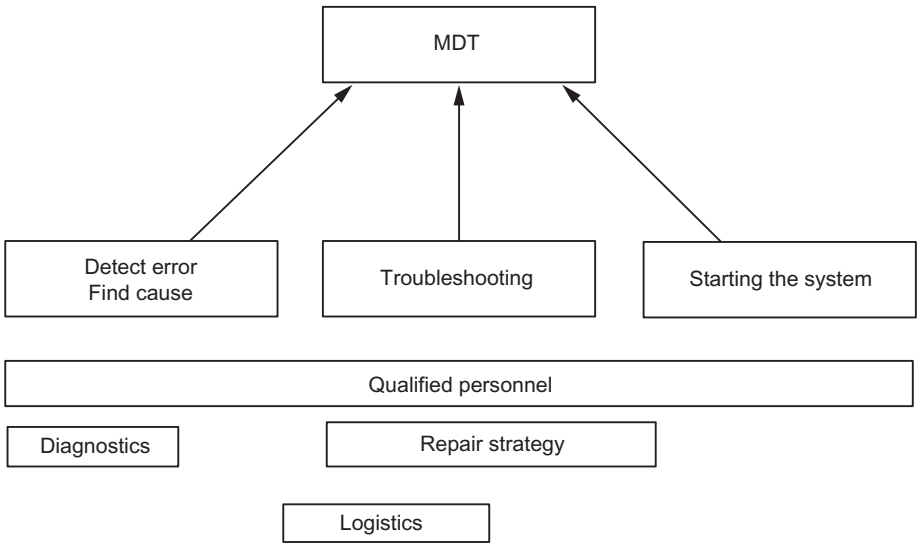


Figure A-1 MDT

The figure below shows the parameters included in the calculation of the MTBF of a system.

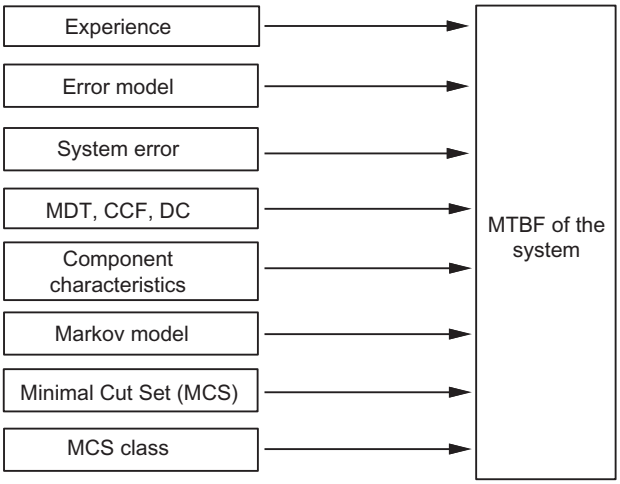


Figure A-2 MTBF

Requirements

This analysis assumes the following conditions:

- The failure rate of all components and all calculations is based on an average temperature of 40 °C.
- The system installation and configuration is free of errors.
- All replacement parts are available locally, in order to prevent extended repair times due to missing spare parts. This keeps the component MDT down to a minimum.
- The MDT of individual components is 4 h. The system's MDT is calculated based on the MDT of the individual components plus the system structure.
- The MTBF of the components conforms to the SN 29500 standard, which corresponds to MIL–HDBK 217–F.
- The calculations are made using the diagnostic coverage of each component.
- A CCF factor between 0.2% and 2% is assumed, depending on the system configuration.

Common Cause Failure (CCF)

The Common Cause Failure (CCF) is an error which is caused by one or more events which also lead to an error state on two or more separate channels or components in a system. A CCF leads to a system failure.

The CCF may be caused by one of the following factors:

- Temperature
- Humidity
- Corrosion
- Vibration and shock
- Electromagnetic interference
- Electrostatic discharge
- RF interference
- Unexpected sequence of events
- Operating errors

The CCF factor defines the ratio between the probability of the occurrence of a CCF and the probability of the occurrence of any other error.

Typical CCF factors range from 2% to 0.2% in a system with identical components, and between 1% and 0.1% in a system containing different components.

Within the range stipulated in IEC 61508, a CCF factor between 0.02% and 5% is used to calculate the MTBF.

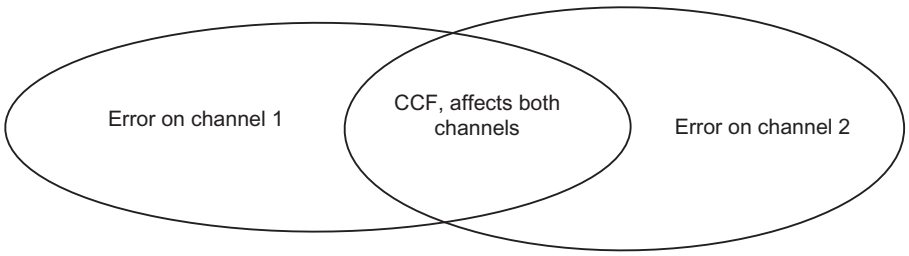


Figure A-3 Common Cause Failure (CCF)

Reliability of an S7-400H

The use of redundant modules prolongs the system MTBF by a large factor. The integrated high-grade self-test and the test/message functions of the S7-400H CPUs enable the detection and localization of virtually all errors. The calculated diagnostic coverage is around 90%.

The reliability in stand-alone mode is described by the corresponding failure rate. The failure rate for all S7 components is calculated according to the SN29500 standard.

The reliability in redundant mode is described by the failure rate of the components involved. This is termed "MTBF" below. Those combinations of failed components which cause a system failure are described and calculated using Markov models. Calculations of the system MTBF take account of the diagnostic coverage and the common cause factor.

Availability

Availability is the probability that a system is operable at a given point of time. This can be enhanced by means of redundancy, for example by using redundant I/O modules or multiple encoders at the same sampling point. Redundant components are arranged such that system operability is not affected by the failure of a single component. Here, again, an important element of availability is a detailed diagnostics display.

The availability of a system is expressed as a percentage. It is defined by the mean time between failure (MTBF) and the mean time to repair MTTR (MDT). The availability of a two-channel (1-out-of-2) fault-tolerant system can be calculated using the following formula:

$$V = \frac{MTBF_{1v2}}{MTBF_{1v2} + MDT} 100\%$$

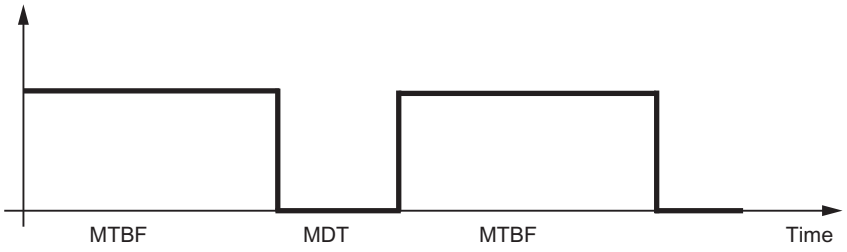


Figure A-4 Availability

A.2 Comparison of MTBF for selected configurations

The following sections compare systems with a centralized and distributed I/Os.

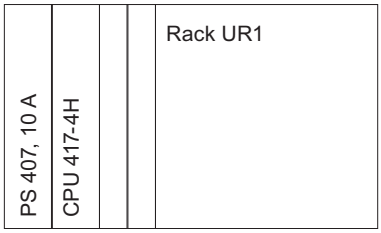
The following framework conditions are set for the calculation.

- MDT (Mean Down Time) 4 hours
- Ambient temperature 40 degrees
- Buffer voltage is safeguarded

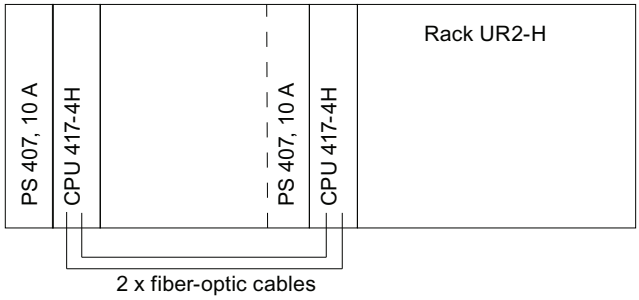
A.2.1 System configurations with redundant CPU 417-4H

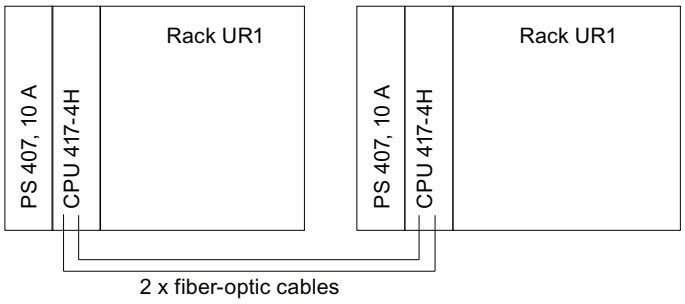
The following system with one CPU (e.g. 417-4H) operating in stand-alone mode forms the basis for the calculation of a reference factor, which defines the multiple of the system MTBF of other systems with centralized I/Os compared to the base line.

Fault-tolerant CPU in stand-alone mode

Fault-tolerant CPU in stand-alone mode (e.g. CPU 417-4H)	Factor
	1

Redundant CPUs in different racks

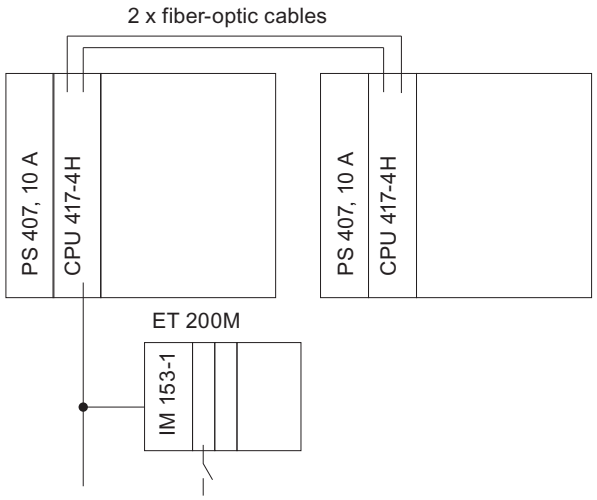
Redundant CPU 417–4H in divided rack, CCF = 2%	Factor
	20

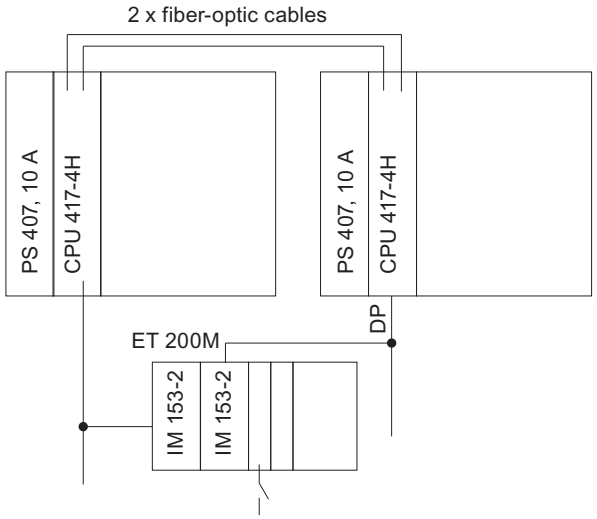
Redundant CPU 417–4H in two separated racks, CCF = 1 %	Factor
	38

A.2.2 System configurations with distributed I/Os

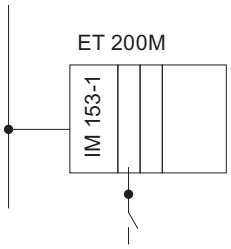
The following system with two fault-tolerant CPUs 417-4 H and one-sided I/Os described below is taken as a basis for calculating a reference factor, which specifies the multiple of the availability of the other systems with distributed I/Os compared with the base line.

Redundant CPUs with single-channel, one-sided or switched I/Os

One-sided distributed I/Os	Base line
	1

Switched distributed I/O, CCF = 2%	Factor
	15

Redundant CPUs with redundant I/Os

Single-channel, one-sided I/O	MTBF factor
	1

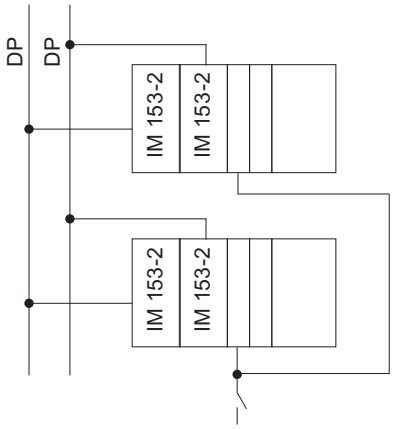
Redundant I/O	MTBF factor
	See following table

Table A-1 MTBF factors of the redundant I/Os

Module	MLFB	MTBF factor CCF = 1%
Digital input modules, distributed		
DI 24xDC24V	6ES7 326–1BK0x–0AB0	> 5
DI 8xNAMUR [EEx ib]	6ES7 326–1RF0x–0AB0	> 5
DI16xDC24V, Alarm	6ES7 321–7BH00–0AB0	4
Analog input modules, distributed		
AI 6x13Bit	6ES7 336–1HE0x–0AB0	> 5
AI8x12Bit	6ES7 331–7KF02–0AB0	5
Digital output modules, distributed		
DO 10xDC24V/2A	6ES7 326–2BF0x–0AB0	> 5
DO8xDC24V/2A	6ES7 322–1BF01–0AA0	3
DO32xDC24V/0.5A	6ES7 322–1BL00–0AA0	3

Summary

There are now several thousand applications of redundant automation systems in the field, in various configurations. To calculate the MTBF, we assumed an average configuration.

Based on experience in the field, an assumption of a MTBF of 3000 years is 95% reliable.

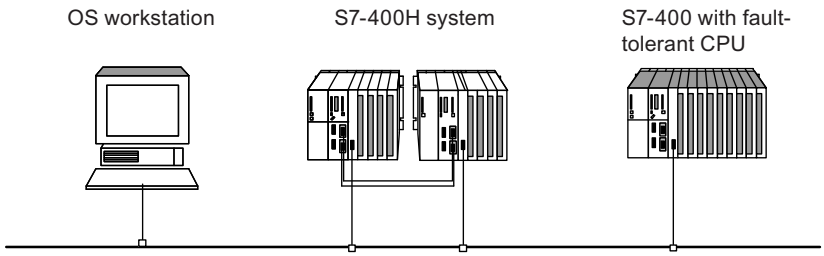
The system MTBF value calculated is about 230 years for a system configuration with redundant CPU 417-4H.

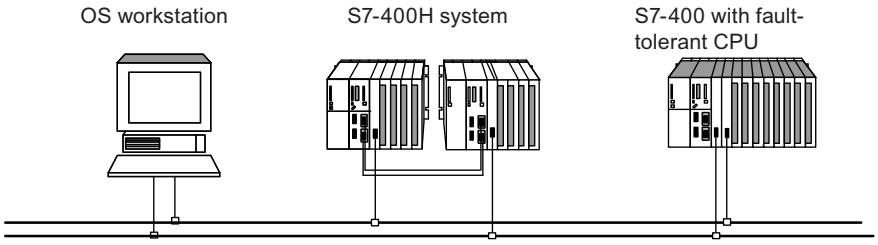
A.2.3 Comparison of system configurations with standard and fault-tolerant communication

The next section shows a comparison between standard and fault-tolerant communication for a configuration consisting of a fault-tolerant system, a fault-tolerant CPU operating in stand-alone mode, and a single-channel OS.

The comparison only took account of the CP and cable communication components.

Systems with standard and fault-tolerant communication

Standard communication	Base line
	1

Fault-tolerant communication	Factor
	Approx. 80

Stand-alone operation

B

Overview

This appendix provides the necessary information for you to operate a fault-tolerant CPU (414-4H or 417-4H) in stand-alone mode. You will learn:

- how stand-alone mode is defined
- when stand-alone mode is required
- what you have to take into account for stand-alone operation
- how the fault tolerance-specific LEDs react
- how to configure stand-alone operation of a fault-tolerant CPU
- how you can expand it to form a fault-tolerant system

The differences from a standard S7-400 CPU that you have to take into account when configuring and programming the fault-tolerant CPU are given in appendix Differences between fault-tolerant systems and standard systems (Page 351).

Definition

By stand-alone operation, we mean the use of a fault-tolerant CPU in a standard SIMATIC-400 station.

Reasons for stand-alone operation

The applications outlined below are only possible when using a fault-tolerant CPU, so they are not possible with standard S7-400 CPUs.

- Use of fault-tolerant connections
- Configuration of the S7-400F fail-safe automation system

  A fail-safe user program can only be compiled for execution on a fault-tolerant CPU with a F-runtime license (for more details refer to the *S7-400F and S7-400FH Automation Systems* manuals).

Note

The self-test of the fault-tolerant CPU is also performed in stand-alone mode.

What you have to take into account for stand-alone operation of a fault-tolerant CPU

NOTICE
When operating a fault-tolerant CPU in stand-alone mode, no synchronization modules may be connected. The rack number must be set to "0".

Although a fault-tolerant CPU has additional functions compared to a standard S7-400 CPU, it does not support specific functions. So particularly when programming your automation system, you need to know the CPU on which you are going to run the user program. A user program written for a standard S7-400 CPU usually will not run on a fault-tolerant CPU in stand-alone mode without adaptations.

The table below lists the differences between the operation of a fault-tolerant CPU in stand-alone mode and in redundant mode.

Table B-1 Differences between stand-alone mode and redundant mode

Function	Fault-tolerant CPU in stand-alone mode	Fault-tolerant CPU in redundant system mode
Connection of S5 modules via IM or adapter casing	via IM 463–2	No
Redundancy error OBs (OB 70, OB 72)	Yes, but no calls	Yes
CPU hardware fault (OB 84)	after the detection and elimination of memory errors	after the detection and elimination of memory errors with reduced performance of the redundant link between the two CPUs
SSL ID W#16#0232 index W#16#0004 byte 0 of the "index" word in the data record	W#16#F8	Single mode: W#16#F8 or W#16#F9 Redundant: W#16#F8 and W#16#F1 or W#16#F9 and W#16#F0
Multi-DP master mode	Yes	No
System modifications during operation	Yes, as described in the "System Modification during Operation Using CIR" manual.	Yes, as described in chapter Failure and replacement of components during operation (Page 197) for redundant operation.

Fault tolerance-specific LEDs

The REDF, IFM1F, IFM2F, MSTR, RACK0 and RACK1 LEDs show the reaction specified in the table below in stand-alone mode.

LED	Behavior
REDF	Unlit
IFM1F	Unlit
IFM2F	Unlit
MSTR	Lit
RACK0	Lit
RACK1	Unlit

Configuring stand-alone mode

Precondition: No synchronization module may be inserted in the fault-tolerant CPU.

Procedure:

1. Insert a **SIMATIC-400** station in your project.
2. Configure the station with the fault-tolerant CPU according to your hardware configuration. For stand-alone operation, insert the fault-tolerant CPU in a standard rack (Insert > Station > S7–400 station in SIMATIC Manager).
3. Parameterize the fault-tolerant CPU. Use the default values, or customize the necessary parameters.
4. Configure the necessary networks and connections. For stand-alone operation you can configure "fault-tolerant S7 connections".

For help on procedure refer to the Help topics in SIMATIC Manager.

Expansion to a fault-tolerant system

WARNING

You can only expand your system to a fault-tolerant system if you have not assigned any odd numbers to expansion units in stand-alone mode.

To expand the fault-tolerant CPU later to form a fault-tolerant system:

1. Open a new project and insert a fault-tolerant station.
2. Copy the entire rack from the standard SIMATIC-400 station and insert it twice into the fault-tolerant station.
3. Insert the subnets as required.
4. Copy the DP slaves from the old stand-alone project to the fault-tolerant station as required.
5. Reconfigure the communication connections.
6. Carry out all changes required, such as the insertion of one-sided I/Os.

For information on how to configure the project refer to the Online Help.

Changing the operating mode of a fault-tolerant CPU

The procedure for changing the operating mode of a fault-tolerant CPU differs depending on the operating mode you want to switch to and the rack number configured for the CPU:

Changing from redundant to stand-alone mode

1. Remove the synchronization modules.
2. Remove the CPU.
3. Set rack number 0 on the CPU.
4. Install the CPU.
5. Download a project with the stand-alone configuration to the CPU.

Changing from stand-alone mode to redundant mode, rack number 0

1. Insert the synchronization modules into the CPU.
2. Run an unbuffered power cycle, for example, by removing and inserting the CPU, or download a project to the CPU in which it is configured for redundant mode.

Changing from stand-alone mode to redundant mode, rack number 1

1. Set rack number 1 on the CPU.
2. Install the CPU.
3. Insert the synchronization modules into the CPU.

System modification during operation in stand-alone mode

With a system modification during operation, it is also possible to make certain configuration changes in RUN on fault-tolerant CPUs. The procedure corresponds to that for standard CPUs. Processing is halted during this, but for no more than 2.5 seconds (parameterizable). During this time, the process outputs retain their current values. In process control systems in particular, this has virtually no effect on the process. See also the *"Modifying the System during Operation via CiR"* manual.

System modifications during operation are only supported with distributed I/O. They require a configuration as shown in the figure below. To give you a clear overview, this shows only one DP master system and one PA master system.

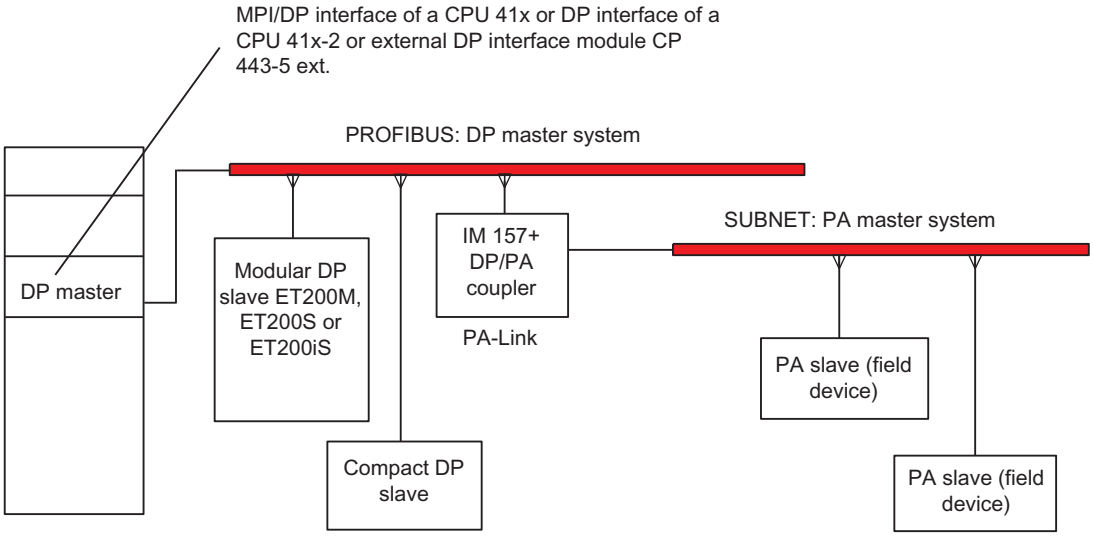


Figure B-1 Overview: System structure for system modifications during operation

Hardware requirements for system modifications during operation

To modify a system during operation, the following hardware requirements must be met at the commissioning stage:

- Use of an S7-400 CPU
- S7-400 H-CPU only in stand-alone mode
- If you use a CP 443-5 Extended, this must have a firmware V5.0 or higher.
- To add modules to an ET 200M: Use an IM 153-2, MLFB 6ES7 153-2BA00-0XB0 or higher, or an IM 153-2FO, MLFB 6ES7 153-2BB00-0XB0 or higher. The installed ET 200M also requires an active backplane bus with sufficient free space for the planned expansion. Include the ET 200M so that it complies with IEC 61158.
- If you want to add entire stations: Make sure that you have the required connectors, repeaters, etc.
- If you want to add PA slaves (field devices): Use IM 157, MLFB 6ES7 157-0AA82-0XA00 or higher, in the corresponding DP/PA link.

Note

You can freely combine components which support system modifications during operation with those that do not. Depending on your selected configuration, there may be restrictions affecting the components on which you can make system modifications during operation.

Software requirements for system modifications during operation

To make modifications during operation, the user program must be written so that station failures or module faults, for example, do not lead to a CPU STOP.

Permitted system modifications: Overview

During operation, you can make the following system modifications:

- Add components or modules with modular DP slaves ET 200M, ET 200S and ET 200iS, provided they are compliant with IEC 61158
- Use of previously unused channels in a module or submodule of the modular slaves ET 200M, ET 200S, and ET 200iS
- Add DP slaves to an existing DP master system
- Add PA slaves (field devices) to an existing PA master system
- Add DP/PA couplers downstream of an IM 157
- Add PA Links (including PA master systems) to an existing DP master system
- Assign added modules to a process image partition
- Change parameter settings for I/O modules, for example selecting different interrupt limits
- Undo changes: Modules, submodules, DP slaves and PA slaves (field devices) you added earlier can be removed again

Migrating from S5-H to S7-400H

C

This appendix will help you to migrate to fault-tolerant S7 systems if you are already familiar with the fault-tolerant systems of the S5 family.

Basic knowledge of the STEP 7 configuration software is required for converting from the S5-H to the S7-400H.

C.1 General aspects

Documentation

The following manuals are available to familiarize you with the STEP 7 basic software:

- *Configuring hardware and connections in STEP 7*
- *Programming with STEP 7*

Information on the various programming languages is available in the reference manuals listed below.

- *System and standard functions*
- STL, LAD, FBD for S7-300/400

The *From S5 to S7* manual supports you with details on migration.

C.2 Configuration, programming, and diagnostics

Configuration

Configuration was performed in STEP 5 using a dedicated configuration package, such as COM 155H.

In STEP 7, the fault-tolerant CPUs are configured using the base software. In SIMATIC Manager, you can create a fault-tolerant station and configure it in HW Config. The special features of the redundant CPUs are grouped on a small number of tabs. Integration into networks and configuration of connections is handled with NetPro.

Diagnostics and programming

In S5, error diagnostics are implemented with the help of the error data block to which the system writes all error data. Error OB 37 is started automatically when any entries are made. Additional information has been stored in the H memory word.

The H memory word consists of a status byte and a control byte. Control information can be set bit-by-bit in the STEP 5 user program.

In STEP 7, system diagnostics is accomplished by means of the diagnostic buffer or by readout of "partial lists" from the system status list (specific information for fault-tolerant systems, for example, is located in SSL71). This query can be performed with the help of the programming device or in the user program with SFC 51 "RDSYSST".

OB 70 is available for I/O redundancy loss, and OB 72 for CPU redundancy loss.

The function of the control byte is implemented in STEP 7 by means of SFC 90 "H_CTRL".

Topic in S5	Equivalent in S7
Error OB 37	Error OBs OB 70 and OB 72
Memory control word	SFC 90 "H_CTRL"
Memory status word	SSL71
Error block	Diagnostic buffer

Differences between fault-tolerant systems and standard systems

D

When configuring and programming a fault-tolerant automation system with fault-tolerant CPUs, you must make allowances for a number of differences from the standard S7-400 CPUs. A fault-tolerant CPU has additional functions compared to a standard S7-400 CPU, on the other hand it does not support specific functions. This has to be taken in account particularly if you wish to run a program that was created for a standard S7-400 CPU on a fault-tolerant CPU.

The ways in which the programming of fault-tolerant systems differs from that for standard systems are summarized below. You will find further differences in appendix Stand-alone operation (Page 343).

If you use any of the affected calls (OBs and SFCs) in your user program, you will need to adapt your program accordingly.

Additional functions of fault-tolerant systems

Function	Additional programming
Redundancy error OBs	• I/O redundancy error OB (OB 70) • CPU redundancy error OB (OB 72) For detailed information, refer to the *System and Standard Functions* Reference Manual.
CPU hardware fault	OB 84 is also called if the performance of the redundant link between the two CPUs is reduced.
Additional information in OB start information and in diagnostic buffer entries	The rack number and the CPU (master/reserve) are specified. You can evaluate this additional information in the program.
SFC for fault-tolerant systems	You can control processes in fault-tolerant systems using SFC 90 "H_CTRL".
Fault-tolerant communication connections	Fault-tolerant connections are configured and do not require further programming. You can use the SFBs for configured connections when using fault-tolerant connections.
Self-test	The self-test is performed automatically, no further programming is required,
High-quality RAM test	The CPU performs a high-quality RAM test after an unbuffered POWER ON.
Switched I/O	No additional programming required, see section Using single-channel switched I/O (Page 127).

Function	Additional programming
Information in the system status list	• You can also obtain data records for the fault tolerance-specific LEDs from the partial list with SSL ID W#16#0019. • You can also obtain data records for the redundancy error OBs from the partial list with SSL ID W#16#0222. • You can obtain information on the current status of the fault-tolerant system from the partial list with SSL ID W#16#xy71. • You can also obtain data records for the fault tolerance-specific LEDs from the partial list with SSL ID W#16#0174. • The partial list with the SSL ID W#16#xy75 provides information on the status of the communication between the fault-tolerant system and switched DP slaves.
Update monitoring	The operating system monitors the following four configurable timers: • Maximum cycle time extension • Maximum communication delay • Maximum inhibit time for priority classes > 15 • Minimum I/O retention time No additional programming is required for this. For more detailed information, refer to chapter Link-up and update (Page 95).
SSL ID W#16#0232 index W#16#0004 byte 0 of the "index" word in the data record	Fault-tolerant CPU in stand-alone mode: W#16#F8 Fault-tolerant CPU in single mode: W#16#F8 or W#16#F9 Fault-tolerant CPU in redundant mode: W#16#F8 and W#16#F1 or W#16#F9 and W#16#F0

Restrictions of the fault-tolerant CPU compared to a standard CPU

Function	Restriction of the fault-tolerant CPU
Hot restart	A hot restart is not possible. OB 101 is not possible
Multicomputing	Multicomputing is not possible. OB 60 and SFC 35 are not supported
Startup without configuration loaded	Startup without loaded configuration is not possible.
Background OB	OB 90 is not supported.
Multi-DP master mode	The fault-tolerant CPUs do not support multi-DP master mode in REDUNDANT mode.
Direct communication between DP slaves	Cannot be configured in STEP 7
Constant bus cycle time for DP slaves	No constant bus cycle time for DP slaves in the fault-tolerant system
Synchronization of DP slaves	Synchronization of DP slave groups is not supported. SFC 11 "DPSYC_FR" is not supported.
Disabling and enabling DP slaves	Disabling and enabling DP slaves is not possible. SFC 12 "D_ACT_DP" is not supported.

Function	Restriction of the fault-tolerant CPU
Insertion of DP modules in the module slots for interface modules	Not possible. The module slots are designed only for use by synchronization modules.
Runtime response	The command execution time for a CPU 41x–4H is slightly higher than for a corresponding standard CPU (see *S7–400 Instruction List* and *S7-400H Instruction List*). This must be taken into account for all time-critical applications. You may need to increase the scan cycle monitoring time.
DP cycle time	A CPU 41x-4H has a slightly longer DP cycle time than the corresponding standard CPU.
Delays and inhibits	During update: • The asynchronous SFCs for data records are acknowledged negatively • Messages are delayed • All priority classes up to 15 are initially delayed • Communication jobs are rejected or delayed • Finally, all priority classes are disabled For more detailed information, refer to chapter 7.
Use of symbol-oriented messages (SCAN)	The use of symbol-oriented messages is not possible.
Global data communication	GD communication is not possible (neither cyclically, nor by calling system functions SFC 60 "GD_SND" and SFC 61 "GD_RCV")
S7 basic communication	Communication functions (SFCs) for basic communication are not supported.
Open block communication	Open block communication is not supported by the S7-400H.
S5 connection	The connection of S5 modules by means of an adapter casing is not possible. The connection of S5 modules via IM 463-2 is only supported in stand-alone mode.
CPU as DP slave	Not possible
Use of SFC 49 "LGC_GADR"	You are operating an S7-400H automation system in redundant mode. If you declare the logical address of module of the switched DP slave at the LADDR parameter and call SFC 49, the high byte of the RACK parameter returns the DP master system ID of the active channel. If there is no active channel, the function outputs the ID of the DP master system belonging to the master CPU.
Call of SFC 51 "RDSYSST" with SSL_ID=W#16#xy91	The data records of the SSL partial lists shown below cannot be read with SFC 51 "RDSYSST": • SSL_ID=W#16#0091 • SSL_ID=W#16#0191 • SSL_ID=W#16#0291 • SSL_ID=W#16#0391 • SSL_ID=W#16#0991 • SSL_ID=W#16#0E91
SFC 70/71 call	Not possible

Function	Restriction of the fault-tolerant CPU
Reading our the serial number of the memory card	Not possible
Resetting the CPU to the factory state	Not possible
Data set routing	Not possible via integrated DP interface, possible via CP 443-5

Function modules and communication processors supported by the S7-400H

E

You can use the following function modules (FMs) and communication processors (CPs) on an S7-400H automation system:

Note

There may be further restrictions for individual modules. Refer to the information in the corresponding product information and FAQ, or in SIMATIC NET News.

FMs and CPs which can be used centrally

Module	Order No.	Release	One-sided	Redundant
Counter module FM 450	6ES7 450–1AP00–0AE0	As of product version 2	Yes	No
Function module FM 458-1 DP	6DD 1607-0AA1	As of firmware 1.1.0	Yes	No
	6DD 1607-0AA2	As of firmware version 2.0.0	Yes	No
Communication processor CP 441-1 (point-to-point link)	6ES7 441–1AA02–0AE0	As of product version 2	Yes	No
	6ES7 441–1AA03–0AE0	As of product version 1 with firmware V1.0.0		
	6ES7 441–1AA04–0AE0	As of product version 1 with firmware V1.0.0		
	6ES7 441–2AA02–0AE0	As of product version 2		
	6ES7 441–2AA03–0AE0	As of product version 1 with firmware V1.0.0		
	6ES7 441–2AA04–0AE0	As of product version 1 with firmware V1.0.0		
Communication processor CP 441-2 (point-to-point link)	6ES7 441–2AA03–0AE0	As of product version 1 with firmware V1.0.0	Yes	No
Communication processor CP 443-1 Multi (Industrial Ethernet, TCP / ISO transport)	6GK7 443–1EX10–0XE0	As of product version 1 with firmware V2.6.7	Yes	Yes
	6GK7 443–1EX11–0XE0	As of product version 1 with firmware V2.6.7	Yes	Yes
Communication processor CP 443-1 Multi (Industrial Ethernet ISO and TCP/IP 2-port switch) Without PROFINET IO and PROFINET CBA	6GK7 443–1EX20–0XE0	As of product version 1 with firmware V1.0.26	Yes	Yes

Module	Order No.	Release	One-sided	Redundant
	6GK7 443–1GX20–0XE0 S7 connections via Gbit port are not permissible	As of product version 3 with firmware V2.0	Yes	Yes
Communication processor CP 443-5 Basic (PROFIBUS; S7 communication)	6GK7 443–5FX01–0XE0	As of product version 1 with firmware V3.1	Yes	Yes
Communication processor CP 443-5 Basic (PROFIBUS; S7 communication)	6GK7 443–5FX02–0XE0	As of product version 2 with firmware V3.2	Yes	Yes
Communication processor CP 443-5 Extended (PROFIBUS; master on PROFIBUS DP) [1]	6GK7 443–5DX02–0XE0	As of product version 2 with firmware V3.2.3	Yes	Yes
Communication processor CP 443-5 Extended (PROFIBUS DPV1) [1] [2]	6GK7 443–5DX03–0XE0	As of product version 1 with firmware V5.1.4	Yes	Yes
Communication processor CP 443-5 Extended (PROFIBUS DPV1) [1] [2]	6GK7 443–5DX04–0XE0	As of product version 1 with firmware V6.0	Yes	Yes

[1] Only these modules should be used as external master interfaces on the PROFIBUS DP.

[2] These modules support DPV1 as external DP master interface module (complying with IEC 61158/EN 50170).

FMs and CPs usable for distributed one-sided use

Note

You can use all the FMs and CPs released for the ET 200M with the S7-400H in distributed and one-sided mode.

FMs and CPs usable for distributed switched use

Module	Order No.	Release
Communication processor CP 341–1 (point-to-point link)	6ES7 341–1AH00–0AE0 6ES7 341–1BH00–0AE0 6ES7 341–1CH00–0AE0	As of product version 3
	6ES7 341–1AH01–0AE0 6ES7 341–1BH01–0AE0 6ES7 341–1CH01–0AE0	As of product version 1 with firmware V1.0.0
	6ES7 341–1AH02–0AE0 6ES7 341–1BH02–0AE0 6ES7 341–1CH02–0AE0	As of product version 1 with firmware V2.0.0
Communication processor CP 342–2 (ASI bus interface module)	6GK7 342–2AH01–0XA0	As of product version 1 with firmware V1.10
Communication processor CP 343–2 (ASI bus interface module)	6GK7 343–2AH00–0XA0	As of product version 2 with firmware V2.03

Module	Order No.	Release
Counter module FM 350–1	6ES7 350–1AH01–0AE0 6ES7 350–1AH02–0AE0	As of product version 1
Counter module FM 350–2	6ES7 350–2AH00–0AE0	As of product version 2
Control module FM 355 C	6ES7 355–0VH10–0AE0	As of product version 4
Control module FM 355 S	6ES7 355–1VH10–0AE0	As of product version 3
High-speed Boolean processor FM 352–5	6ES7352–5AH00–0AE0	As of product version 1 with firmware V1.0.0
Control module FM 355–2 C	6ES7 355–0CH00–0AE0	As of product version 1 with firmware V1.0.0
Control module FM 355–2 S	6ES7 355–0SH00–0AE0	As of product version 1 with firmware V1.0.0

NOTICE

One-sided or switched function and communication modules are

not synchronized in the fault-tolerant system if they are in pairs, e.g. two identical FM 450 modules operating in one-sided mode do **not** synchronize their counter states.

Connection examples for redundant I/Os

F

F.1 SM 321; DI 16 x DC 24 V, 6ES7 321–1BH02–0AA0

The diagram below shows the connection of two redundant encoders to two SM 321; DI 16 x DC 24 V. The encoders are connected to channel 0.

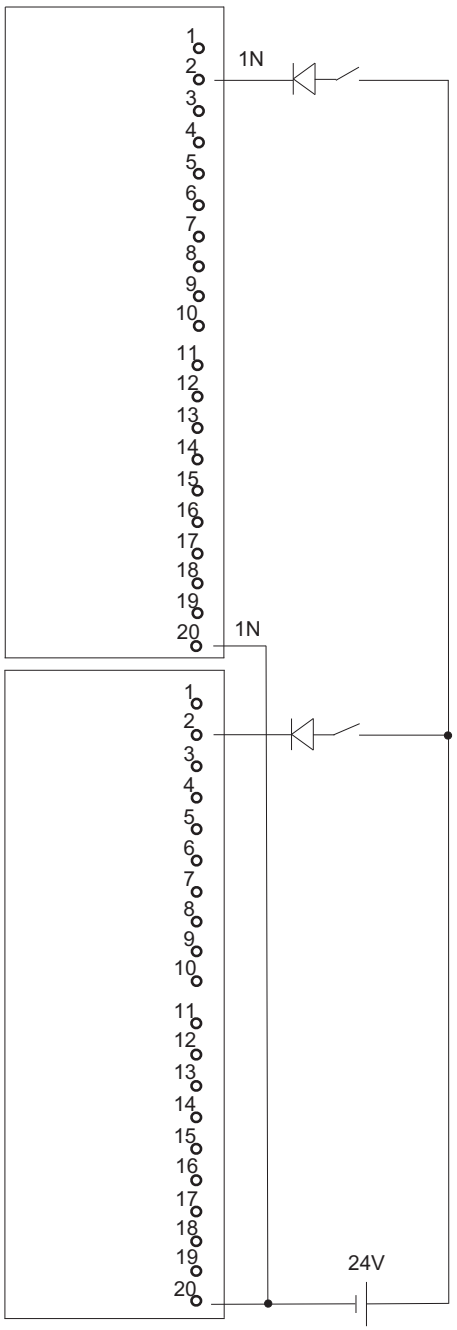


Figure F-1 Example of an interconnection with SM 321; DI 16 x DC 24 V

F.2 SM 321; DI 32 x DC 24 V, 6ES7 321–1BL00–0AA0

The diagram below shows the connection of two redundant encoder pairs to two redundant SM 321; DI 32 x DC 24 V. The encoders are connected to channel 0 and channel 16 respectively.

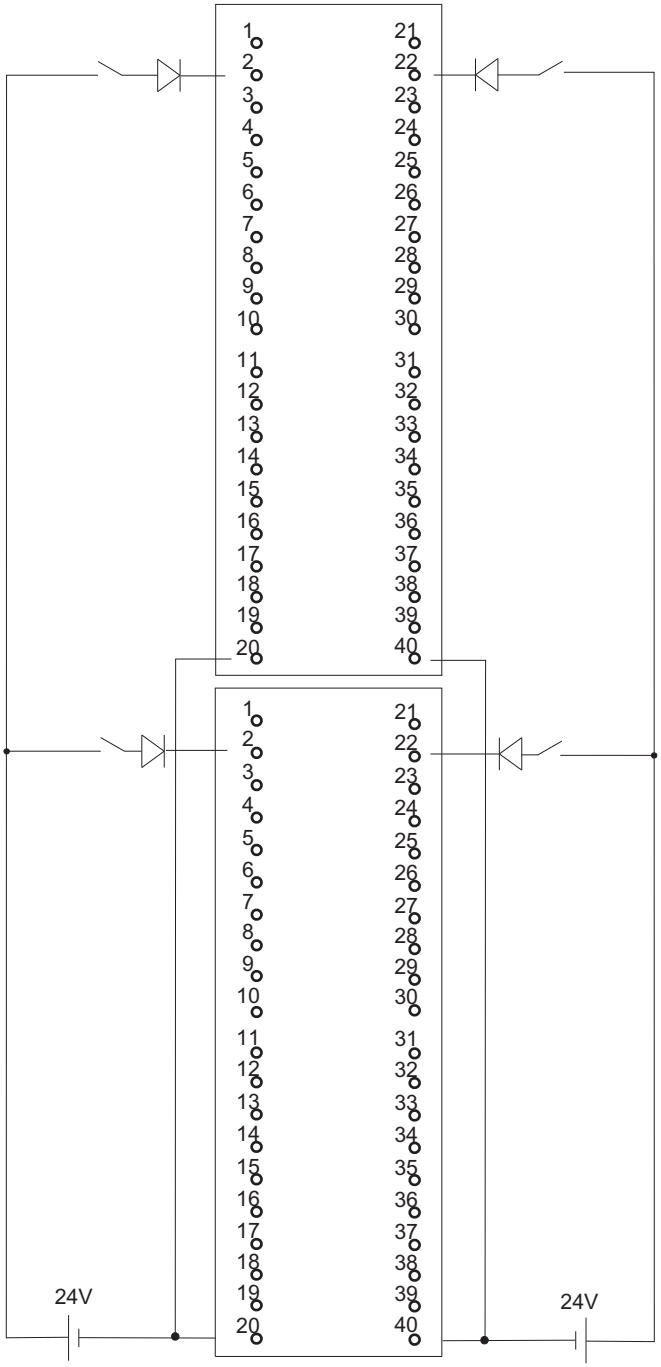


Figure F-2 Example of an interconnection with SM 321; DI 32 x DC 24 V

F.3 SM 321; DI 16 x AC 120/230V, 6ES7 321–1FH00–0AA0

The diagram below shows the connection of two redundant encoders to two SM 321; DI 16 x AC 120/230 V. The encoders are connected to channel 0.

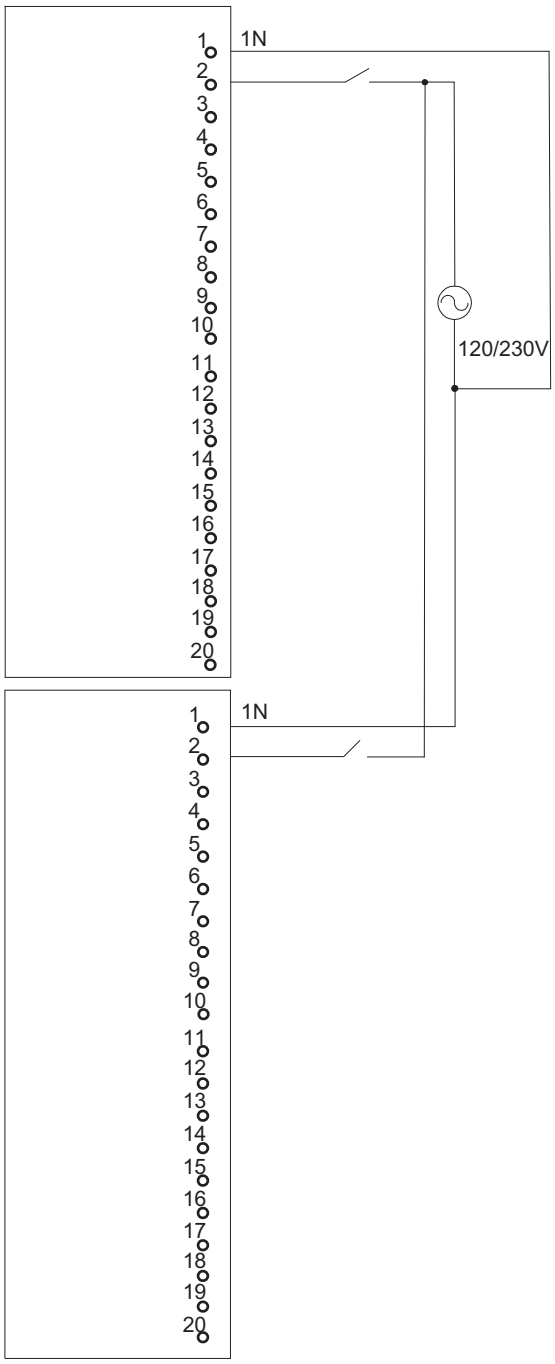


Figure F-3 Example of an interconnection with SM 321; DI 16 x AC 120/230 V

F.4 SM 321; DI 8 x AC 120/230 V, 6ES7 321–1FF01–0AA0

The diagram below shows the connection of two redundant encoders to two SM 321; DI 8 AC 120/230 V. The encoders are connected to channel 0.

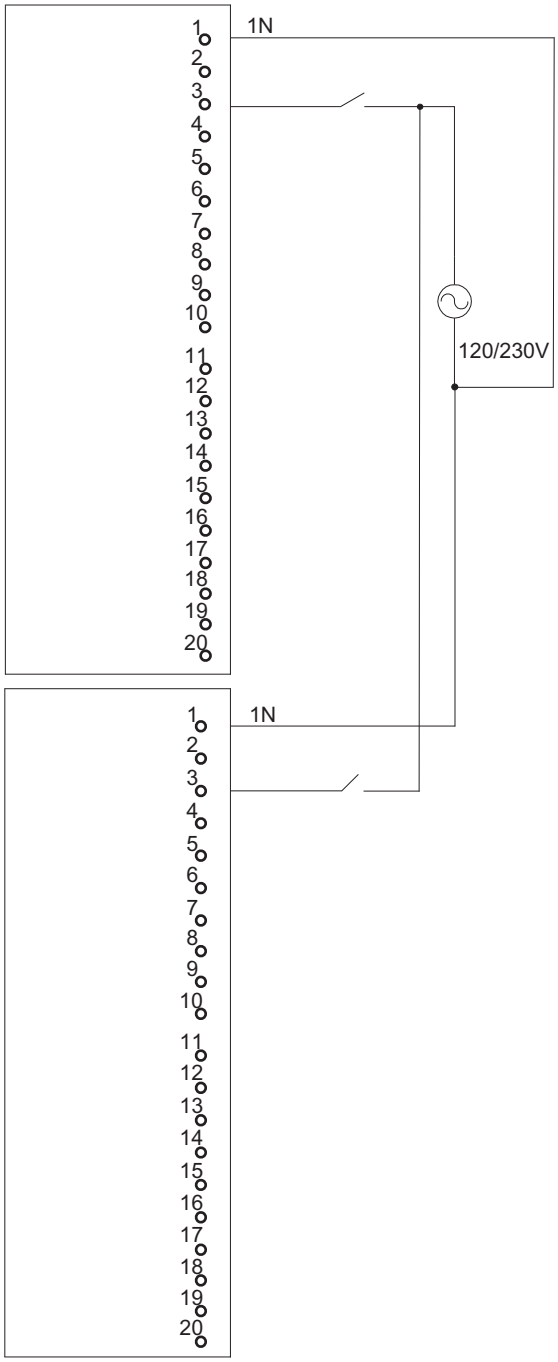


Figure F-4 Example of an interconnection with SM 321; DI 8 x AC 120/230 V

F.5 SM 321; DI 16 x DC 24V, 6ES7 321–7BH00–0AB0

The diagram below shows the connection of two redundant encoder pairs to two SM 321; DI 16 x DC 24V. The encoders are connected to channels 0 and 8.

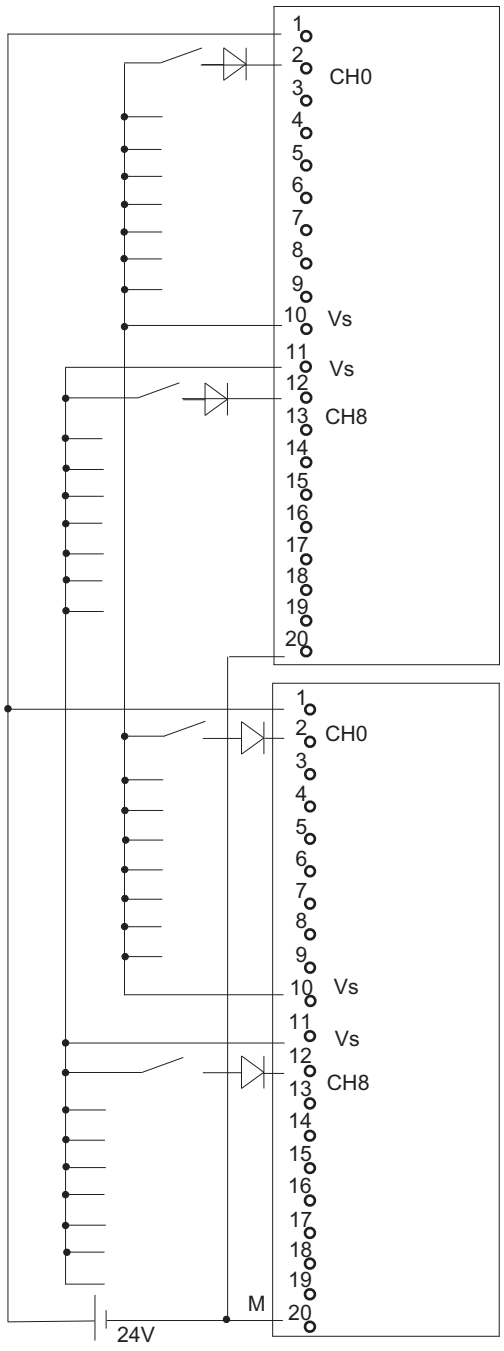


Figure F-5 Example of an interconnection with SM 321; DI 16 x DC 24V

F.6 SM 321; DI 16 x DC 24V, 6ES7 321–7BH01–0AB0

The diagram below shows the connection of two redundant encoder pairs to two SM 321; DI 16 x DC 24V. The encoders are connected to channels 0 and 8.

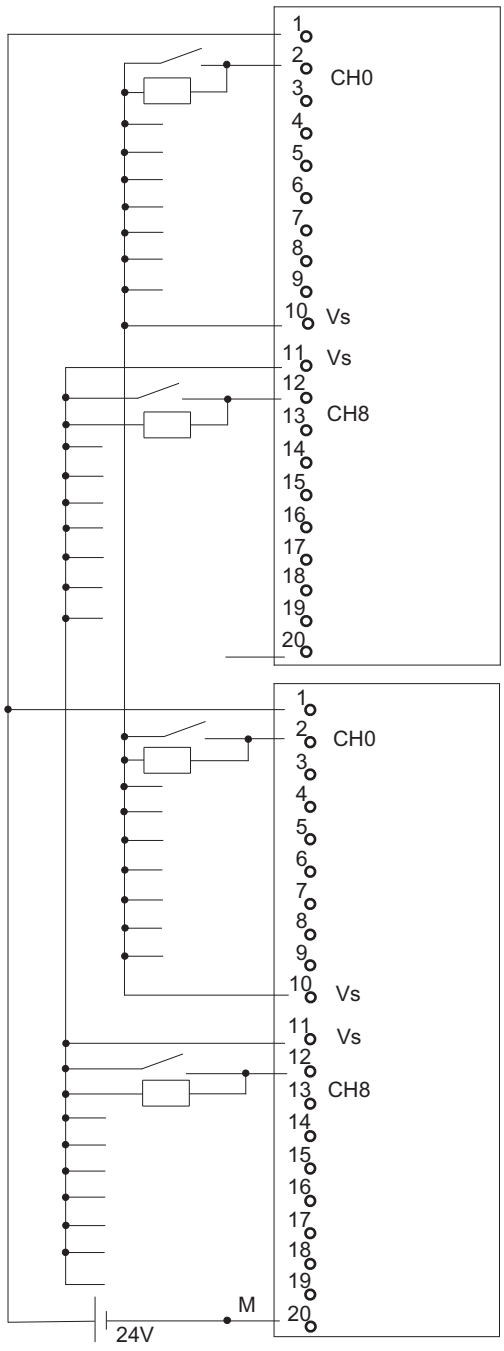


Figure F-6 Example of an interconnection with SM 321; DI 16 x DC 24V

F.7 SM 326; DO 10 x DC 24V/2A, 6ES7 326–2BF01–0AB0

The diagram below shows the connection of an actuator to two redundant SM 326; DO 10 x DC 24V/2A. The actuator is connected to channel 1.

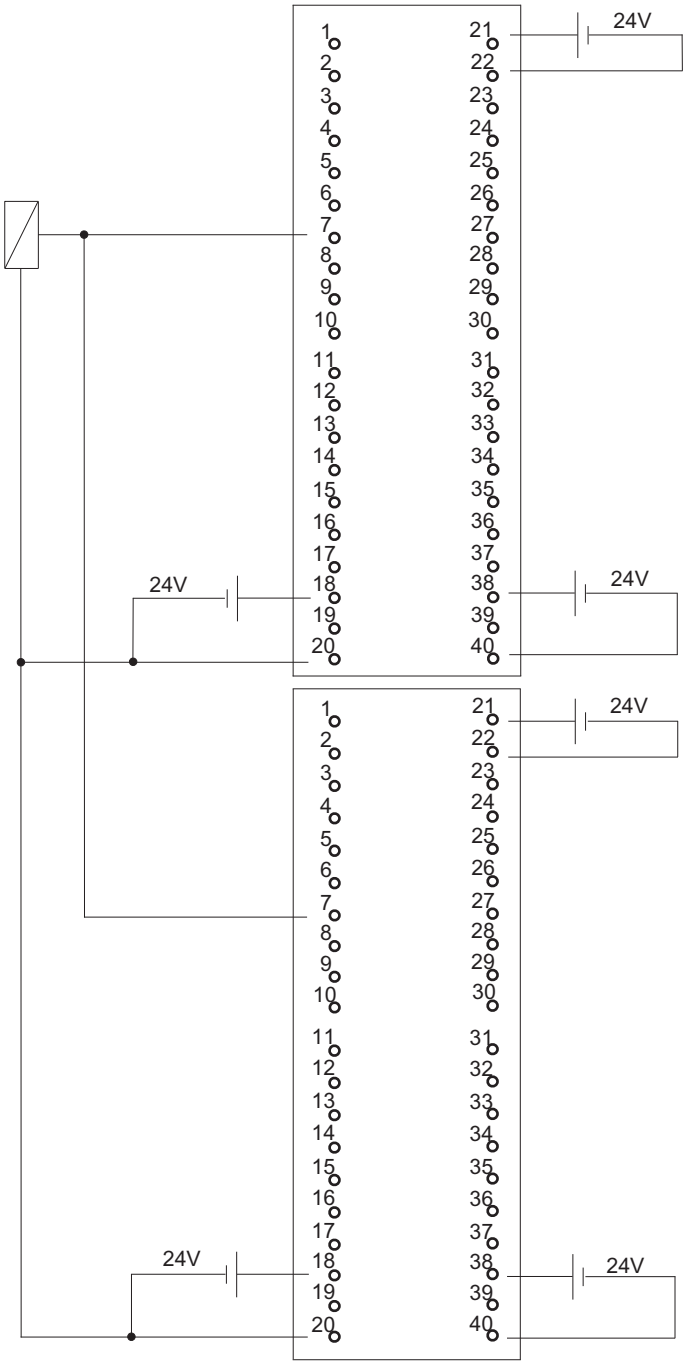


Figure F-7 Example of an interconnection with SM 326; DO 10 x DC 24V/2A

F.8 SM 326; DI 8 x NAMUR, 6ES7 326–1RF00–0AB0

The diagram below shows the connection of two redundant encoders to two redundant SM 326; DI 8 x NAMUR . The encoders are connected to channel 4.

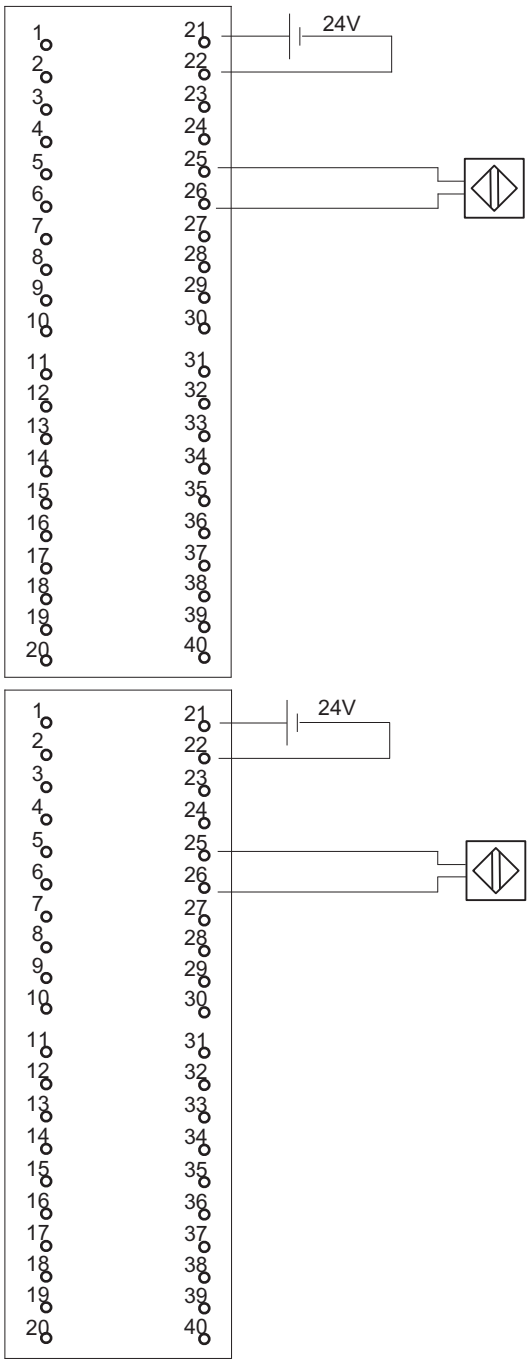


Figure F-8 Example of an interconnection with SM 326; DI 8 x NAMUR

F.9 SM 326; DI 24 x DC 24 V, 6ES7 326–1BK00–0AB0

The diagram below shows the connection of one encoder to two redundant SM 326; DI 24 x DC 24 V. The encoder is connected to channel 13.

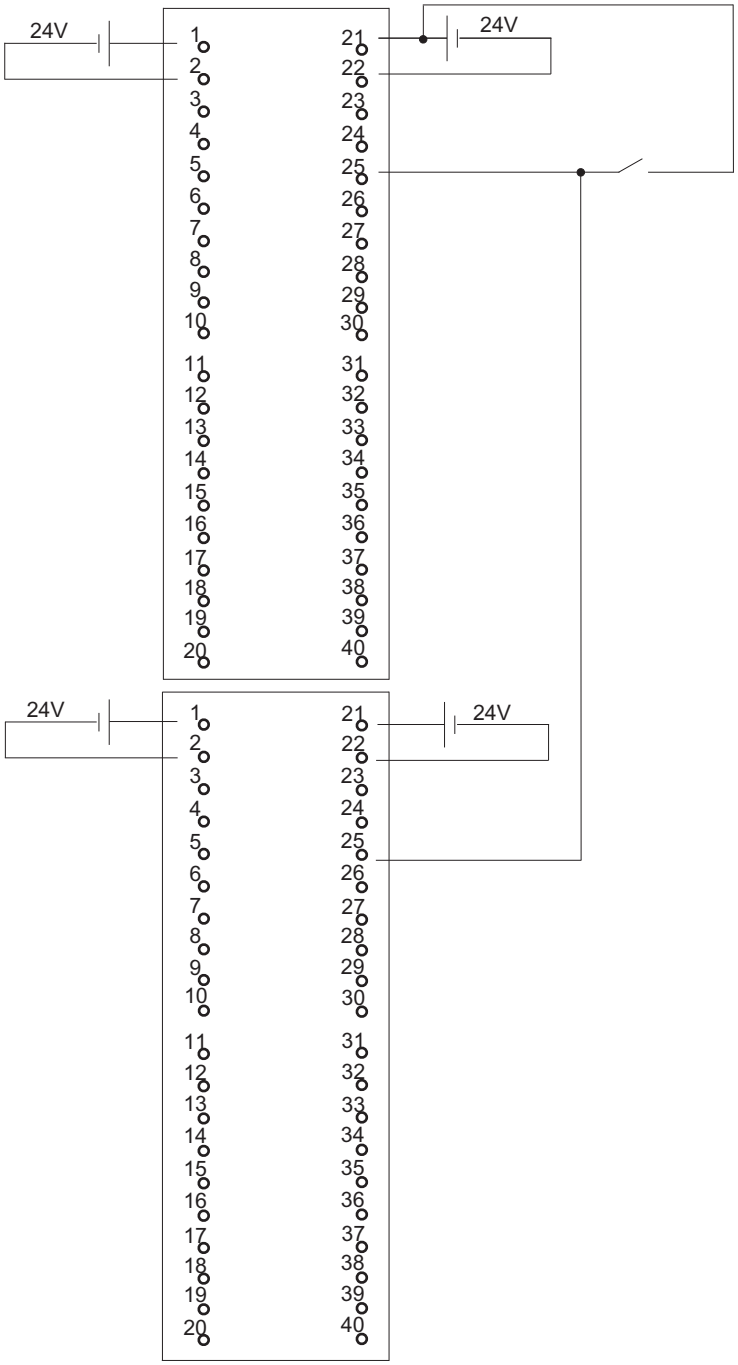


Figure F-9 Example of an interconnection with SM 326; DI 24 x DC 24 V

F.10 SM 421; DI 32 x UC 120 V, 6ES7 421–1EL00–0AA0

The diagram below shows the connection of a redundant encoder to two SM 421; DI 32 x UC 120 V. The encoder is connected to channel 0.

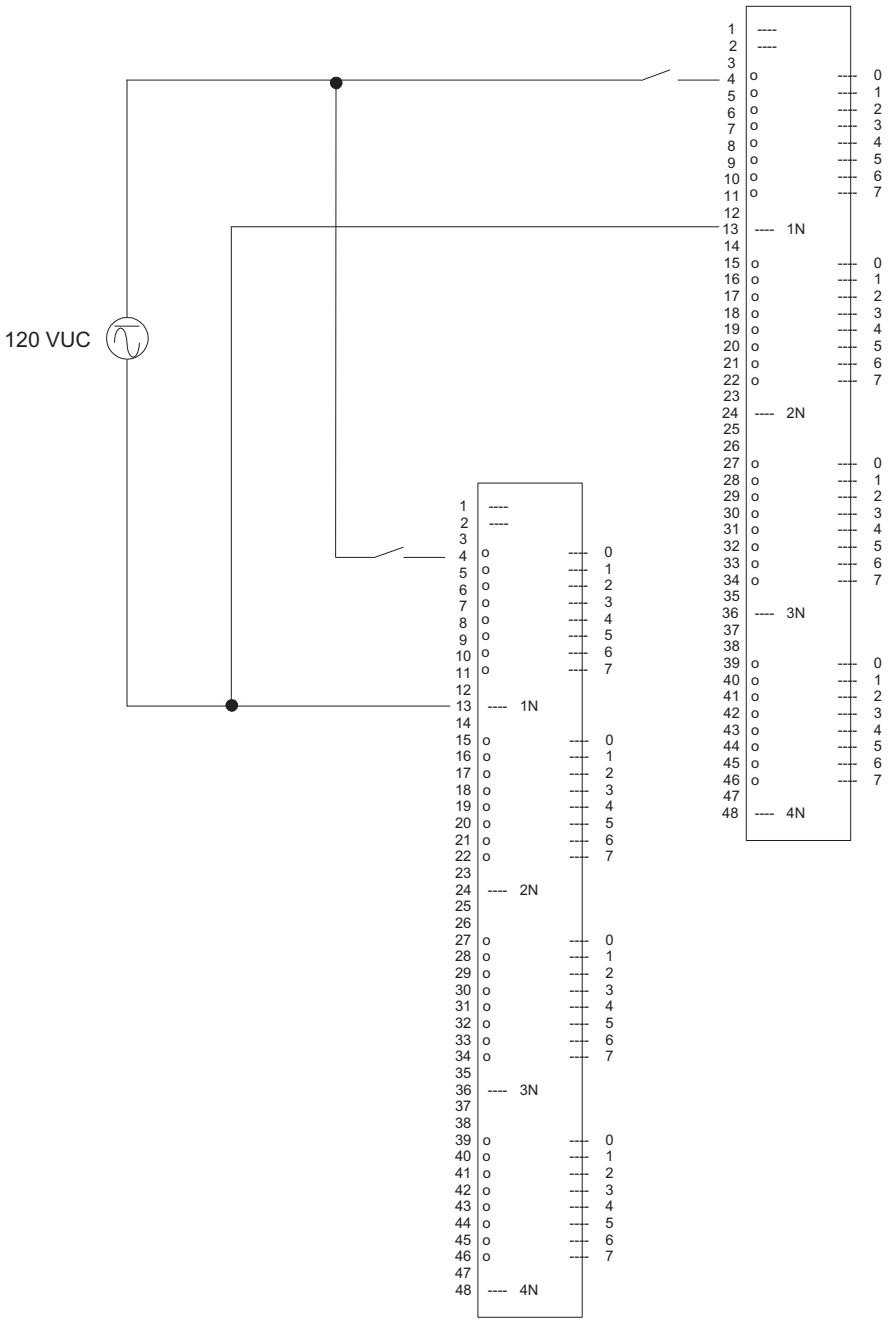


Figure F-10 Example of an interconnection with SM 421; DI 32 x UC 120 V

F.11 SM 421; DI 16 x DC 24 V, 6ES7 421–7BH01–0AB0

The diagram below shows the connection of two redundant encoders pairs to two SM 421; D1 16 x 24 V. The encoders are connected to channel 0 and 8.

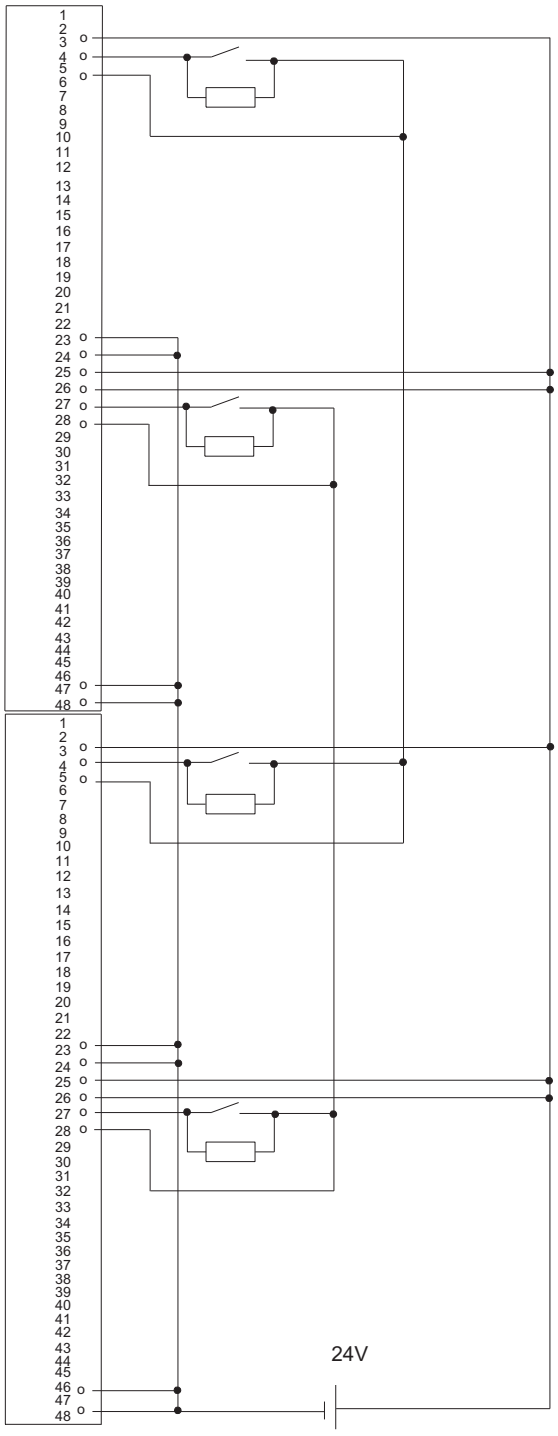


Figure F-11 Example of an interconnection with SM 421; DI 16 x 24 V

F.12 SM 421; DI 32 x DC 24 V, 6ES7 421–1BL00–0AB0

The diagram below shows the connection of two redundant encoders to two SM 421; D1 32 x 24 V. The encoders are connected to channel 0.

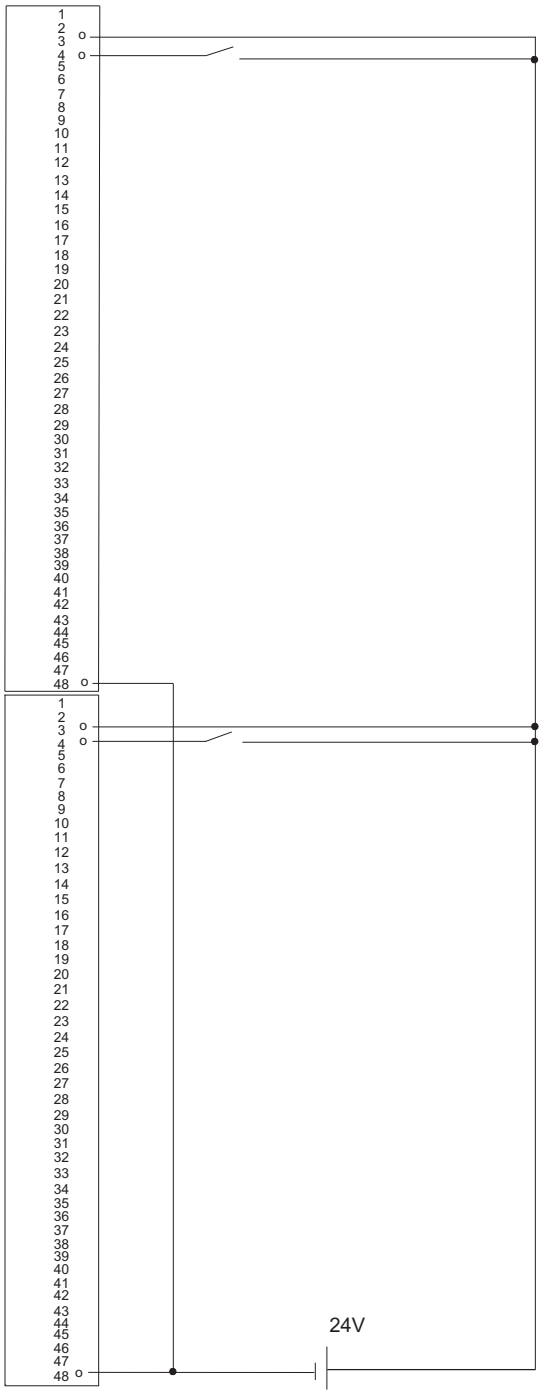


Figure F-12 Example of an interconnection with SM 421; DI 32 x 24 V

F.13 SM 421; DI 32 x DC 24 V, 6ES7 421–1BL01–0AB0

The diagram below shows the connection of two redundant encoders to two SM 421; D1 32 x 24 V. The encoders are connected to channel 0.

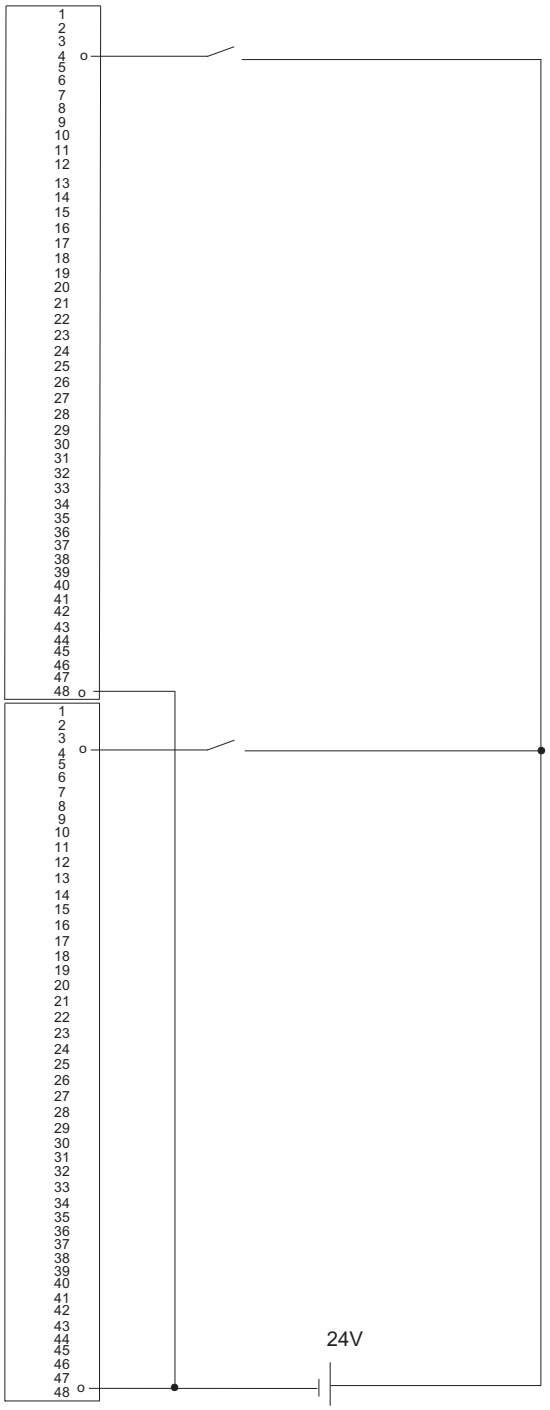


Figure F-13 Example of an interconnection with SM 421; DI 32 x 24 V

F.14 SM 322; DO 8 x DC 24 V/2 A, 6ES7 322–1BF01–0AA0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 8 x DC 24 V. The actuator is connected to channel 0.

Types with U_r >=200 V and I_F >= 2 A are suitable as diodes

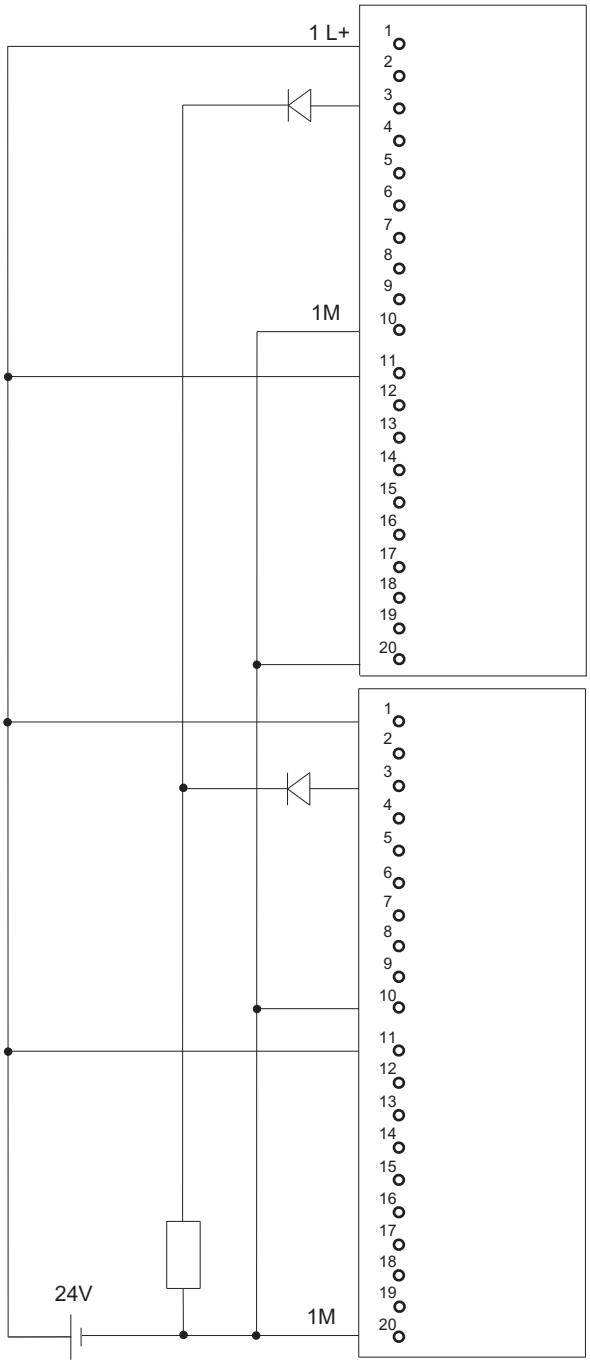


Figure F-14 Example of an interconnection with SM 322; DO 8 x DC 24 V/2 A

F.15 SM 322; DO 32 x DC 24 V/0,5 A, 6ES7 322–1BL00–0AA0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 32 x DC 24 V. The actuator is connected to channel 1.

Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with U_r >=200 V and I_F >= 1 A

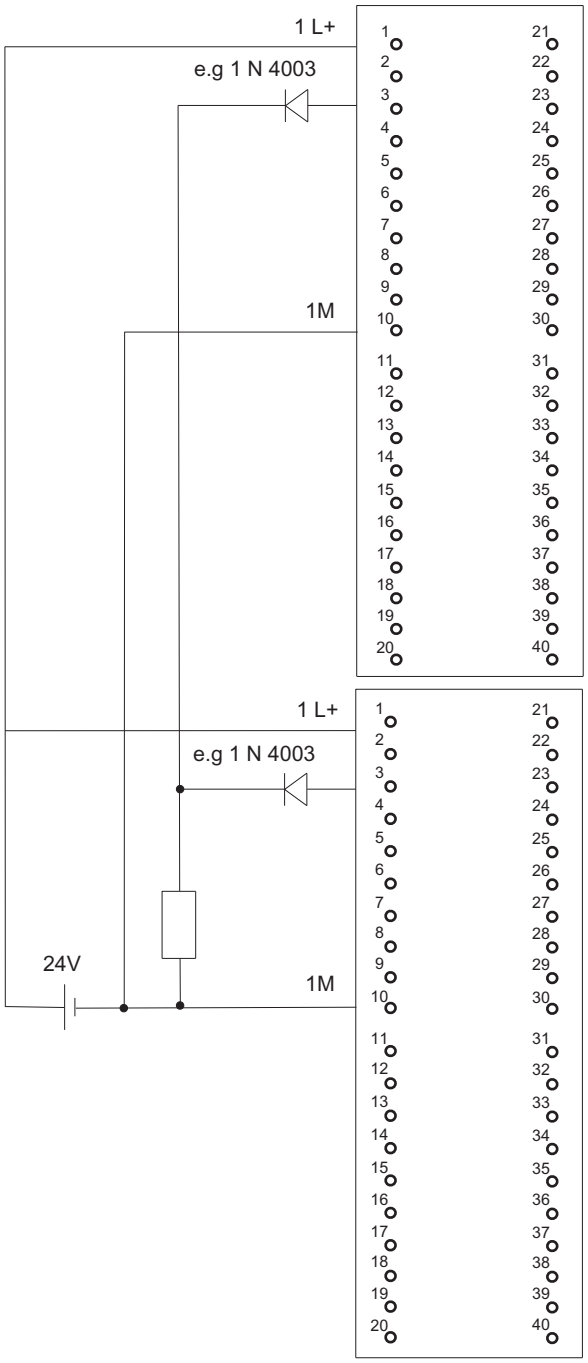


Figure F-15 Example of an interconnection with SM 322; DO 32 x DC 24 V/0.5 A

F.16 SM 322; DO 8 x AC 230 V/2 A, 6ES7 322–1FF01–0AA0

The diagram below shows the connection of an actuator to two SM 322; DO 8 x AC 230 V/2 A. The actuator is connected to channel 0.

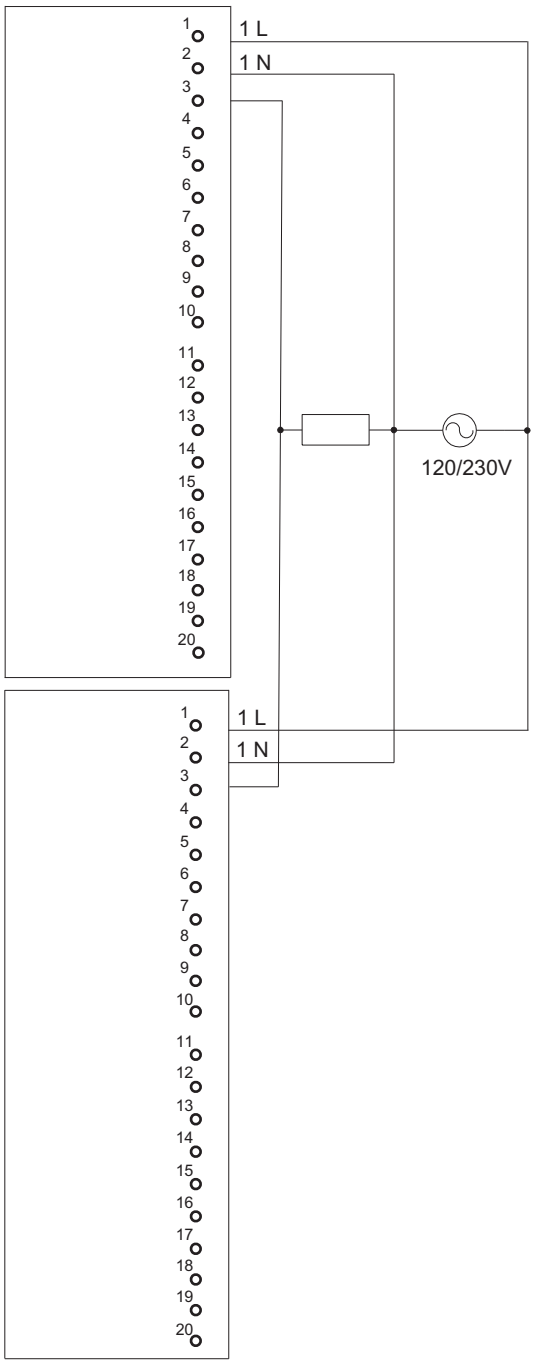


Figure F-16 Example of an interconnection with SM 322; DO 8 x AC 230 V/2 A

F.17 SM 322; DO 4 x DC 24 V/10 mA [EEx ib], 6ES7 322–5SD00–0AB0

The diagram below shows the connection of an actuator to two SM 322; DO 16 x DC 24 V/10 mA [EEx ib]. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with $U_{\_r}$ >=200 V and $I_{\_F}$ >= 1 A

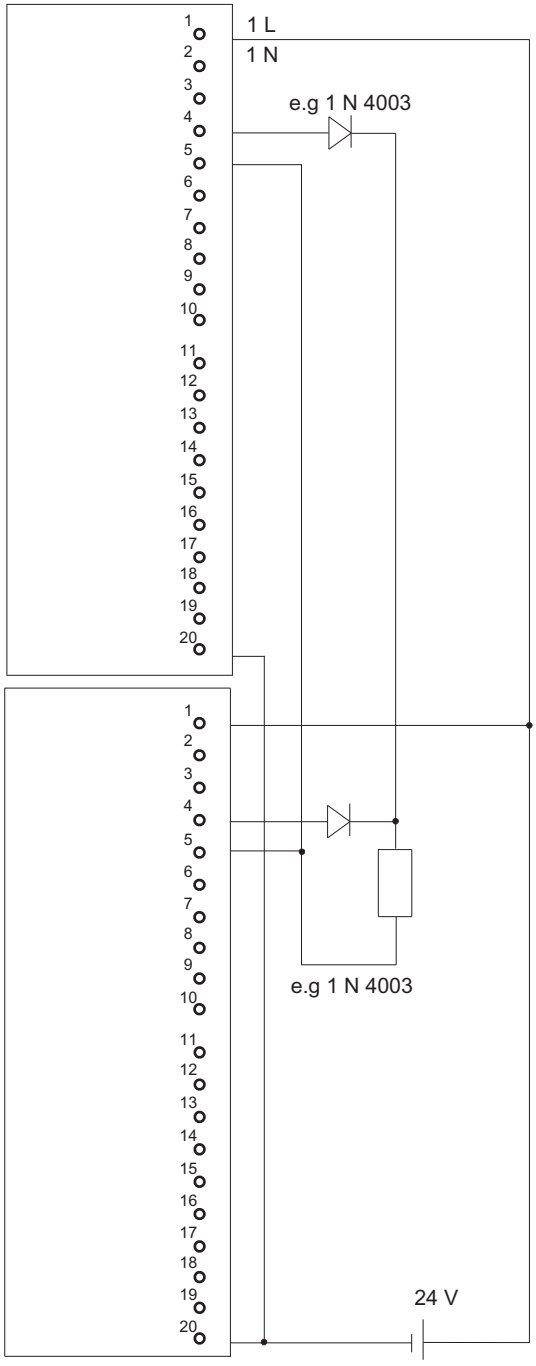


Figure F-17 Example of an interconnection with SM 322; DO 16 x DC 24 V/10 mA [EEx ib]

F.18 SM 322; DO 4 x DC 15 V/20 mA [EEx ib], 6ES7 322–5RD00–0AB0

The diagram below shows the connection of an actuator to two SM 322; DO 16 x DC 15 V/20 mA [EEx ib]. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with U_r >=200 V and I_F >= 1 A

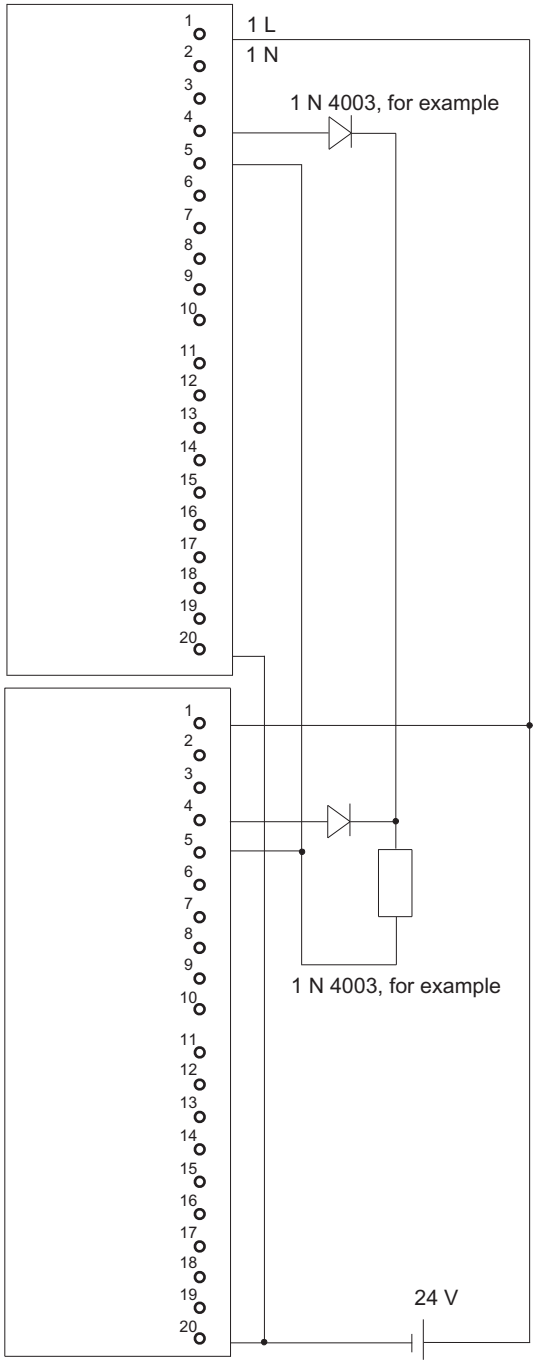


Figure F-18 Example of an interconnection with SM 322; DO 16 x DC 15 V/20 mA [EEx ib]

F.19 SM 322; DO 8 x DC 24 V/0.5 A, 6ES7 322–8BF00–0AB0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 8 x DC 24 V/0.5 A. The actuator is connected to channel 0.

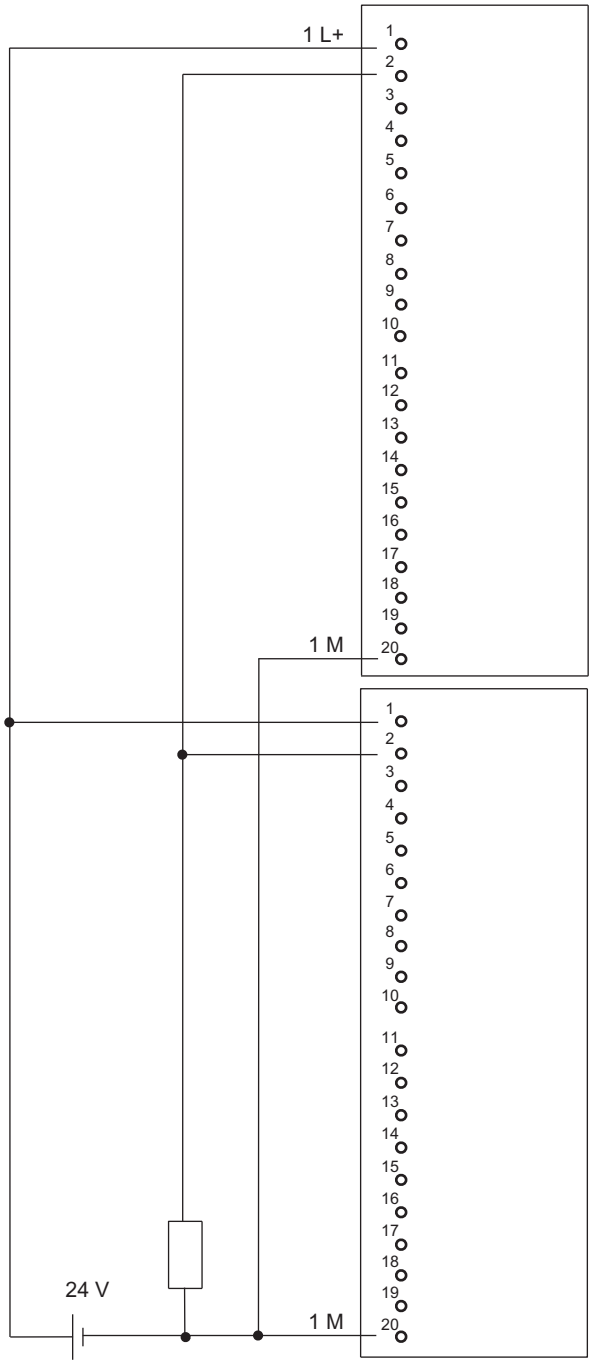


Figure F-19 Example of an interconnection with SM 322; DO 8 x DC 24 V/0.5 A

F.20 SM 322; DO 16 x DC 24 V/0.5 A, 6ES7 322–8BH01–0AB0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 16 x DC 24 V/0.5 A. The actuator is connected to channel 8.

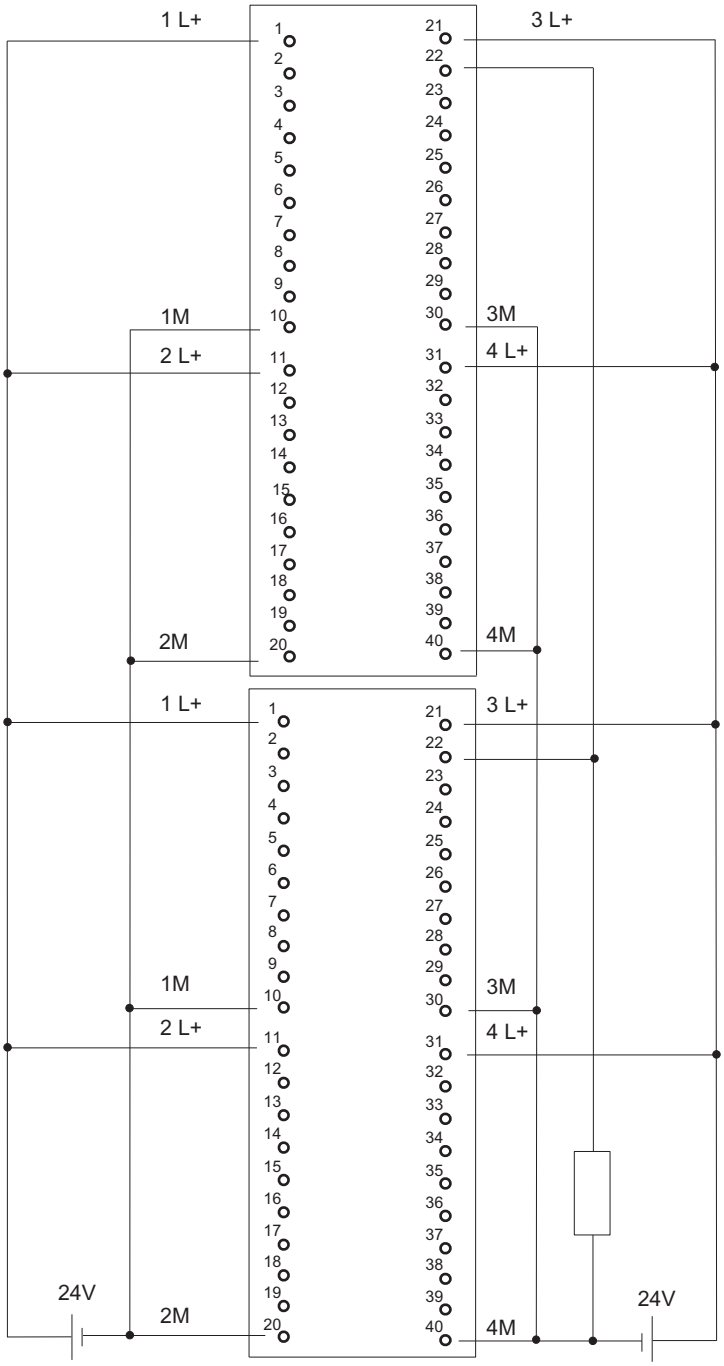


Figure F-20 Example of an interconnection with SM 322; DO 16 x DC 24 V/0.5 A

F.21 SM 332; AO 8 x 12 Bit, 6ES7 332–5HF00–0AB0

The diagram below shows the connection of two actuators to two redundant SM 332; AO 8 x 12 Bit. The actuators are connected to channels 0 and 4. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with U_{rr} >=200 V and I_F >= 1 A

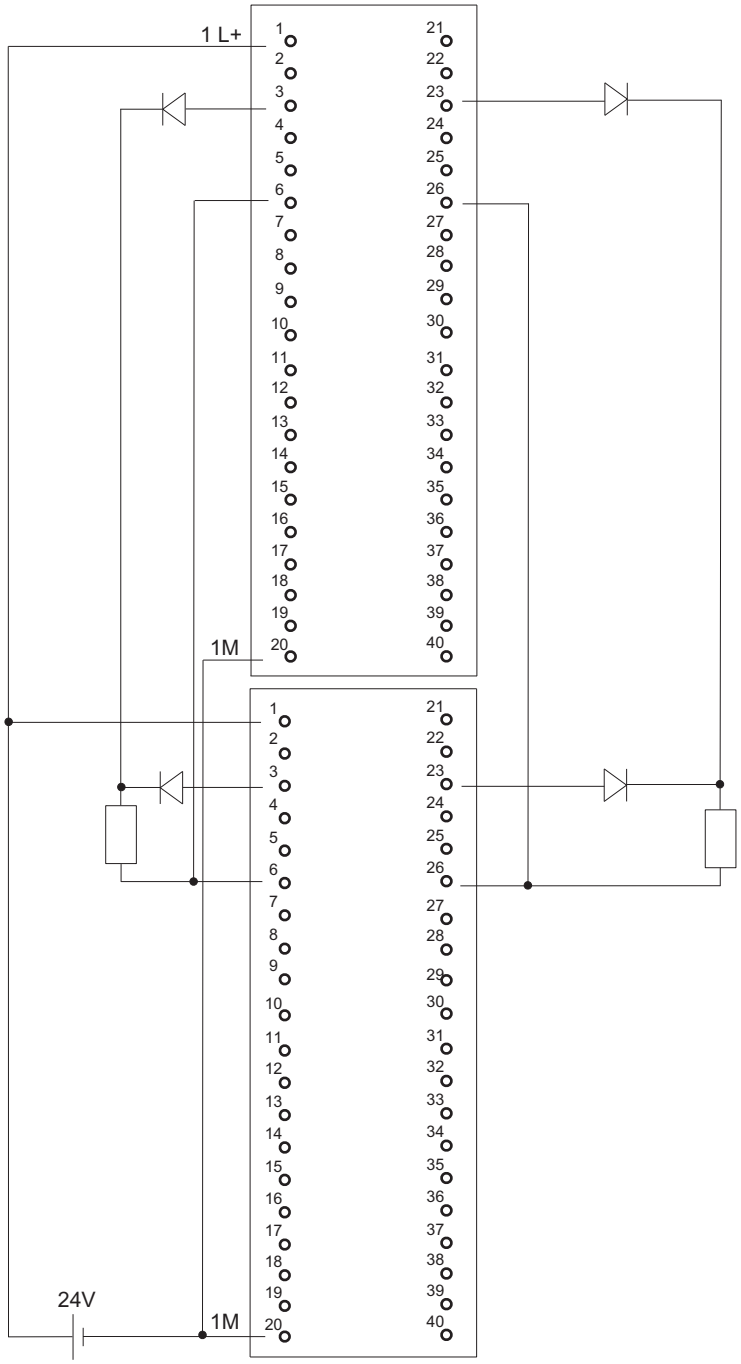


Figure F-21 Example of an interconnection with SM 332, AO 8 x 12 Bit

F.22 SM 332; AO 4 x 0/4...20 mA [EEx ib], 6ES7 332–5RD00–0AB0

The diagram below shows the connection of an actuator to two SM 332; AO 4 x 0/4...20 mA [EEx ib]. The actuator is connected to channel 0.
Suitable diodes are, for example, types from the series 1N4003 ... 1N4007 or any other diode with U_r >=200 V and I_F >= 1 A

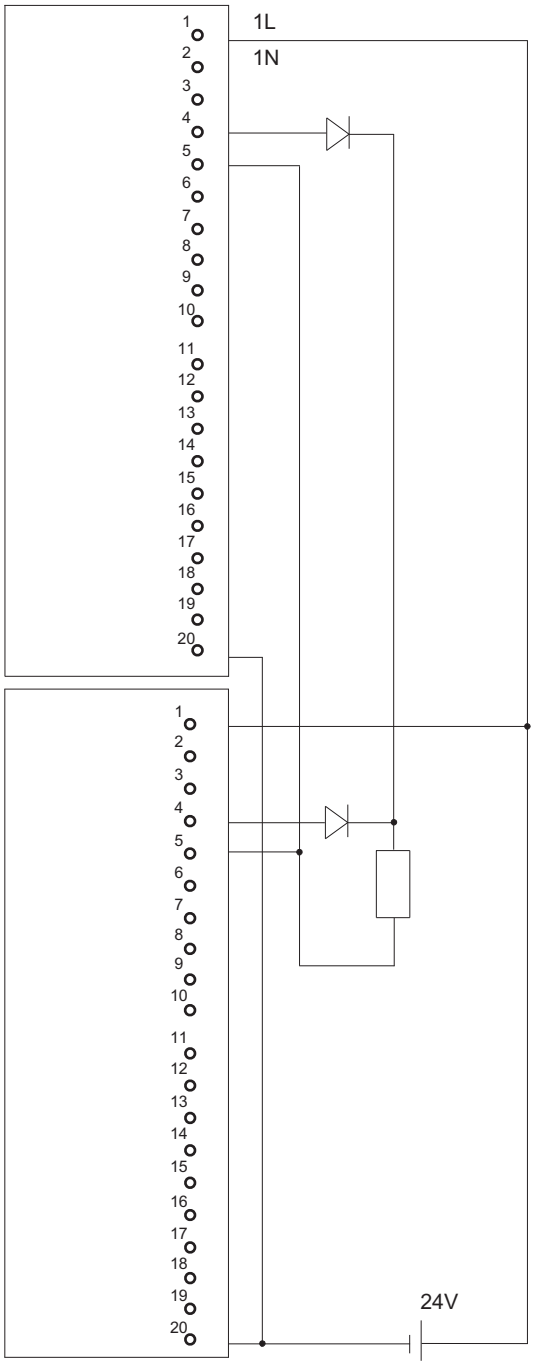


Figure F-22 Example of an interconnection with SM 332; AO 4 x 0/4...20 mA [EEx ib]

F.23 SM 422; DO 16 x AC 120/230 V/2 A, 6ES7 422–1FH00–0AA0

The diagram below shows the connection of an actuator to two SM 422; DO 16 x 120/230 V/2 A. The actuator is connected to channel 0.

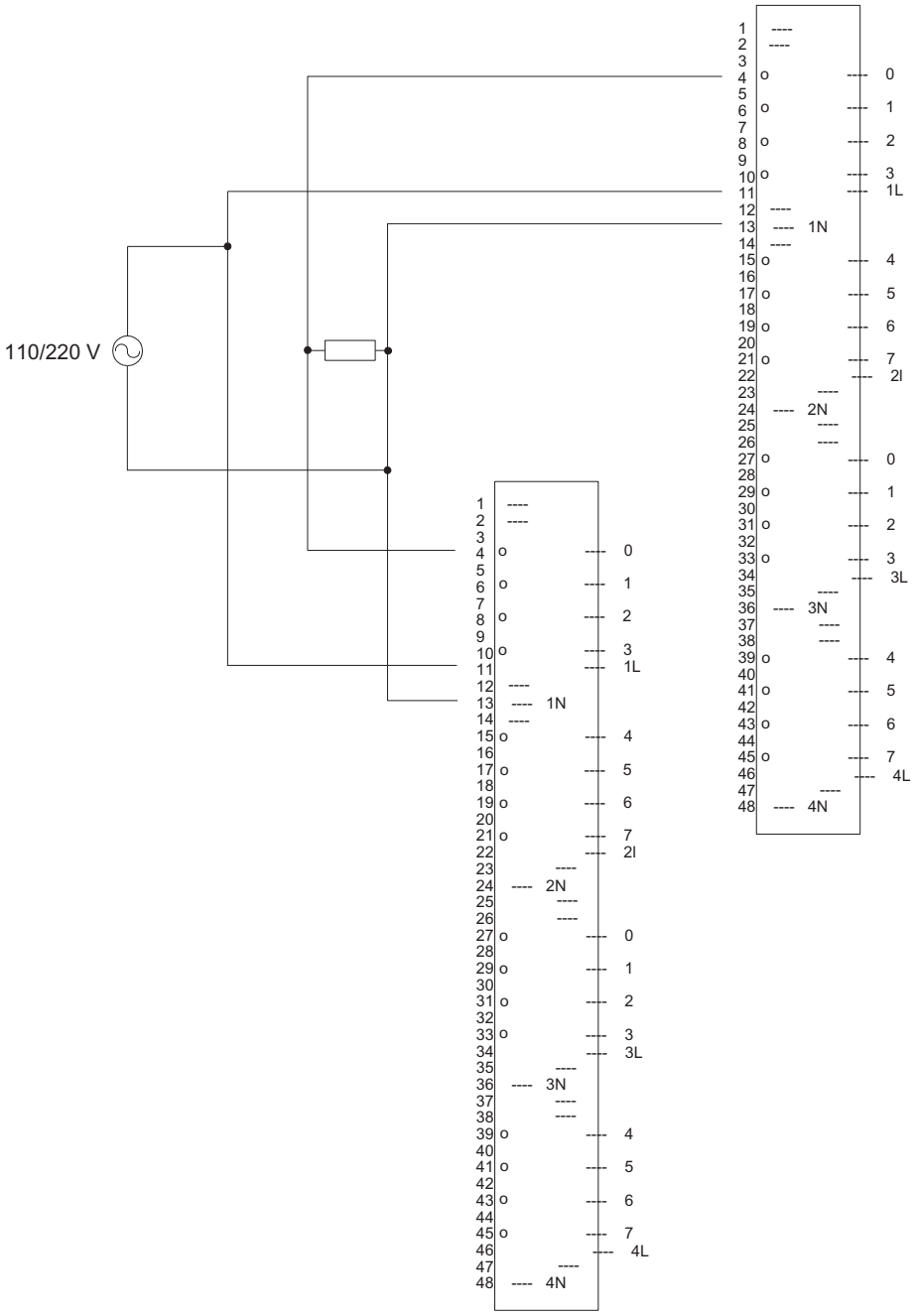


Figure F-23 Example of an interconnection with SM 422; DO 16 x 120/230 V/2 A

F.24 SM 422; DO 32 x DC 24 V/0.5 A, 6ES7 422–7BL00–0AB0

The diagram below shows the connection of an actuator to two SM 422; DO 32 x 24 V/0.5 A. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with U_r >=200 V and I_F >= 1 A

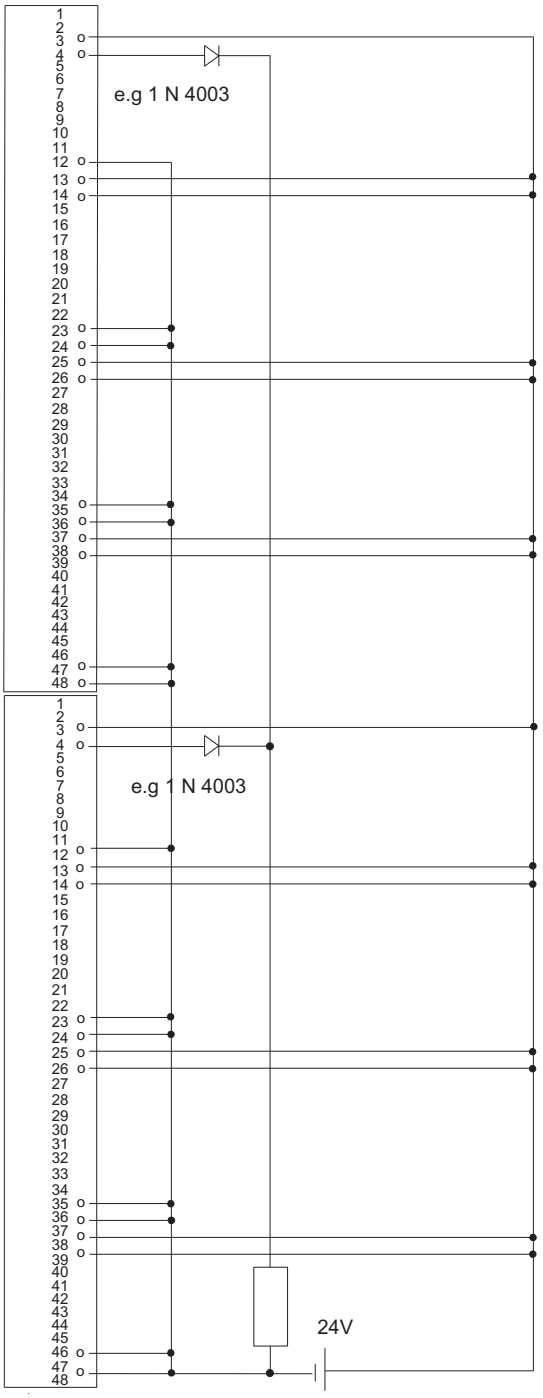


Figure F-24 Example of an interconnection with SM 422; DO 32 x DC 24 V/0.5 A

F.25 SM 331; AI 4 x 15 Bit [EEx ib]; 6ES7 331–7RD00–0AB0

The diagram below shows the connection of a 2-wire transmitter to two SM 331; AI 4 x 15 Bit [EEx ib]. The transmitter is connected to channel 1. Suitable Zener diode: BZX85C6v2.

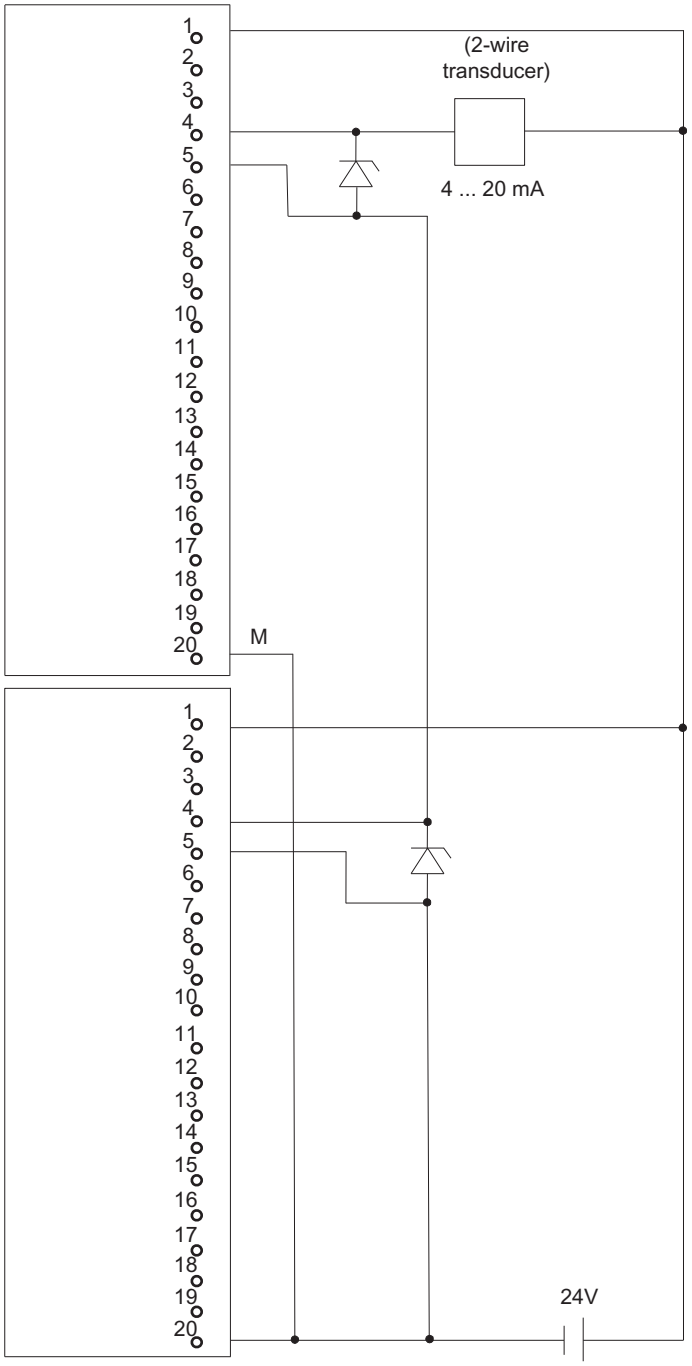


Figure F-25 Example of an interconnection with SM 331, AI 4 x 15 Bit [EEx ib]

F.26 SM 331; AI 8 x 12 Bit, 6ES7 331–7KF02–0AB0

The diagram below shows the connection of a transmitter to two SM 331; AI 8 x 12 Bit. The transmitter is connected to channel 0.

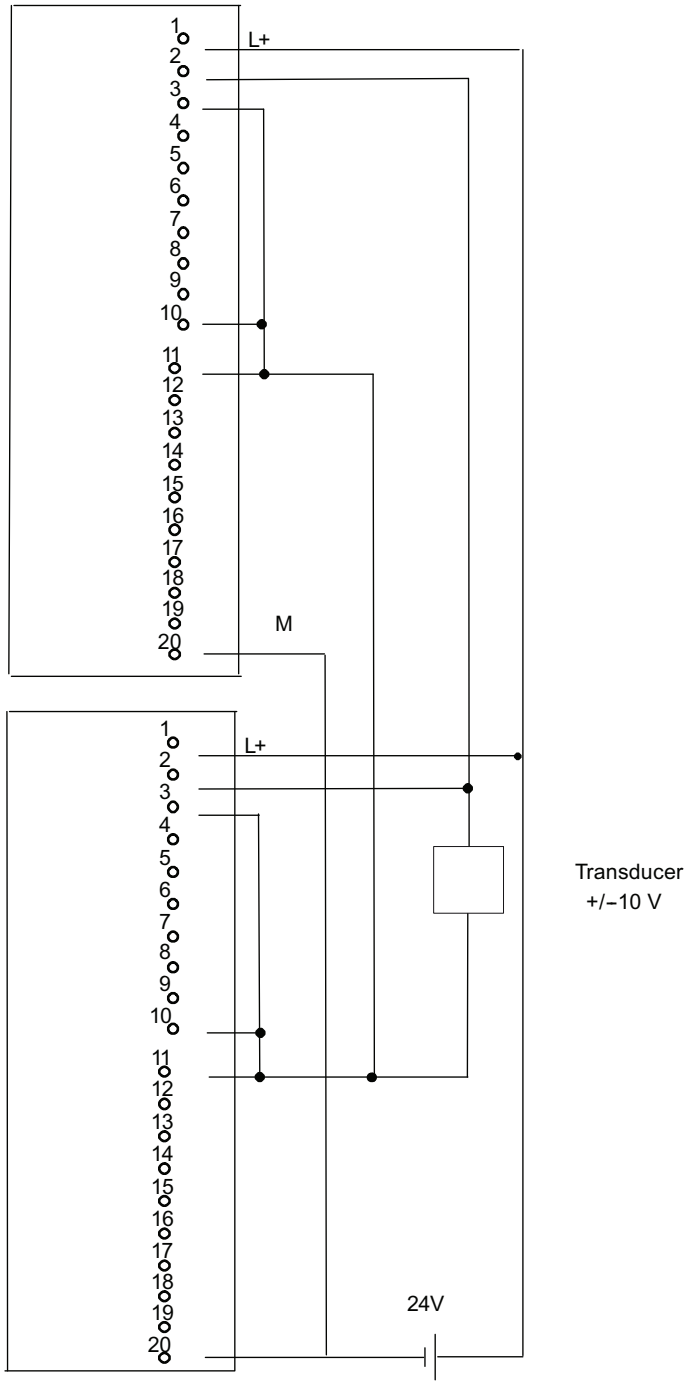


Figure F-26 Example of an interconnection with SM 331; AI 8 x 12 Bit

F.27 SM 331; AI 8 x 16 Bit; 6ES7 331–7NF00–0AB0

The figure below shows the connection of a transmitter to two redundant SM 331; AI 8 x 16 Bit. The transmitter is connected to channel 0 and 7 respectively.

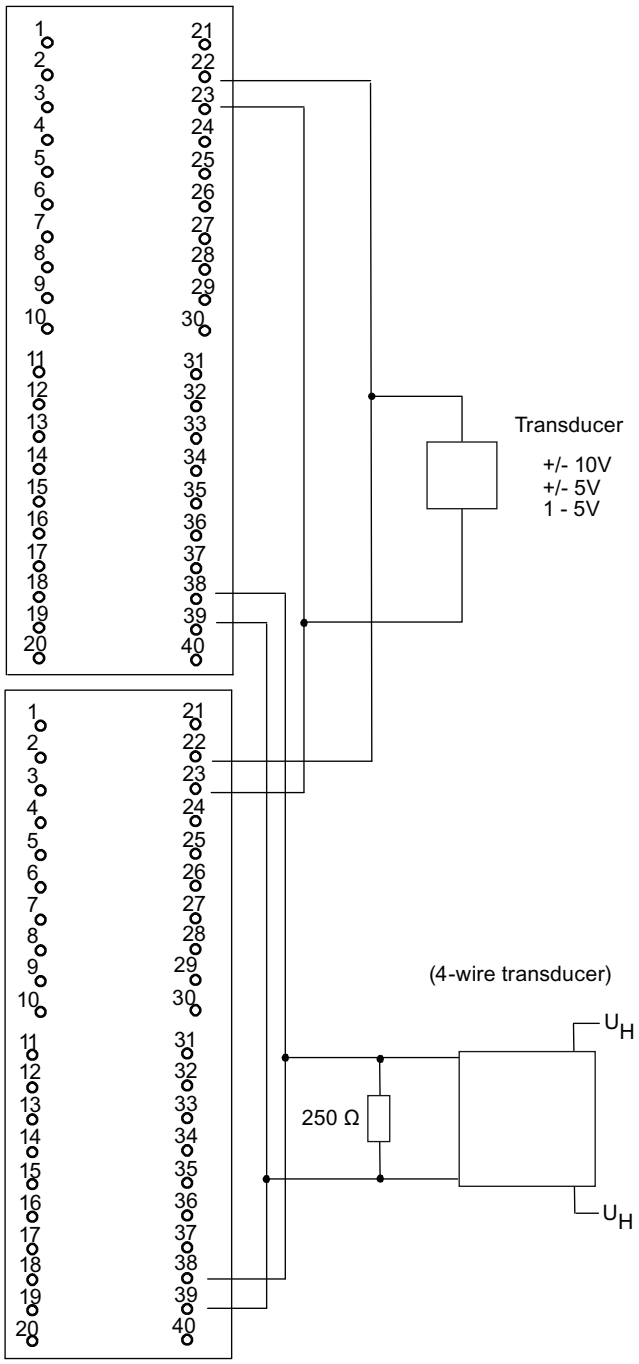


Figure F-27 Example of an interconnection with SM 331; AI 8 x 16 Bit

F.28 SM 331; AI 8 x 16 Bit; 6ES7 331–7NF10–0AB0

The figure below shows the connection of a transmitter to two redundant SM 331; AI 8 x 16 Bit. The transmitter is connected to channel 0 and 3 respectively.

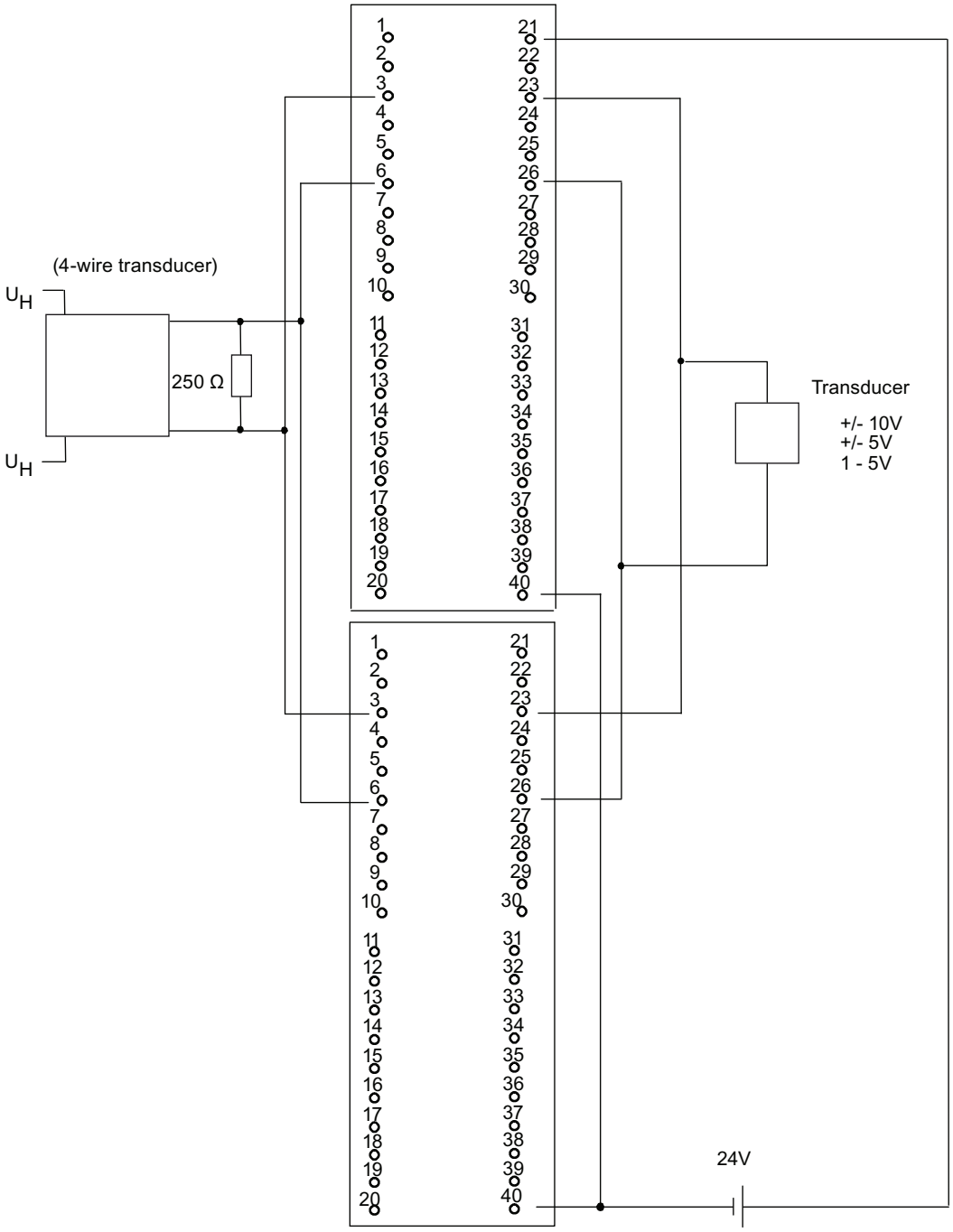


Figure F-28 Example of an interconnection with SM 331; AI 8 x 16 Bit

F.29 AI 6xTC 16Bit iso, 6ES7331-7PE10-0AB0

The figure below shows the connection of a thermocouple to two redundant SM 331 AI 6xTC 16Bit iso.

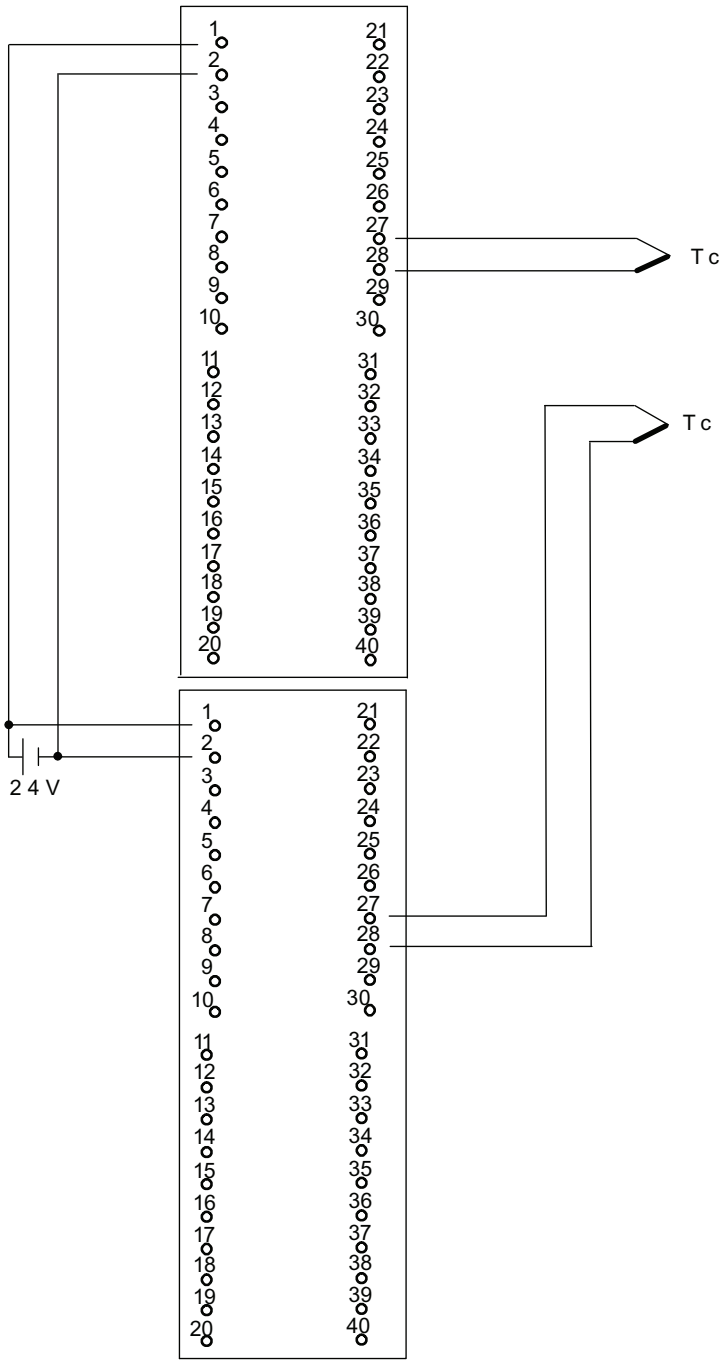


Figure F-29 Example of an interconnection AI 6xTC 16Bit iso

F.30 SM331; AI 8 x 0/4...20mA HART, 6ES7 331-7TF01-0AB0

The diagram below shows the connection of a 4-wire transmitter to two redundant SM 331; AI 8 x 0/4...20mA HART.

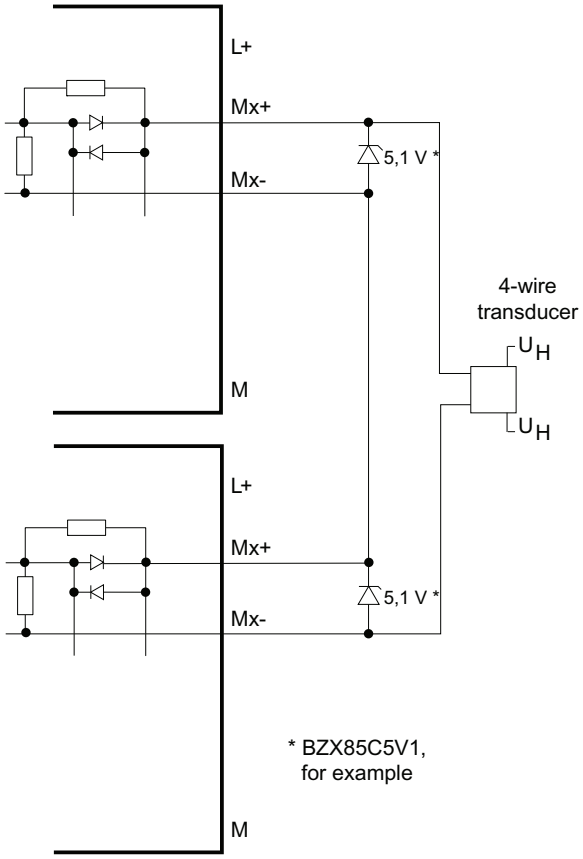


Figure F-30 Interconnection example 1 SM 331; AI 8 x 0/4...20mA HART

The diagram below shows the connection of a 2-wire transmitter to two redundant SM 331; AI 8 x 0/4...20mA HART.

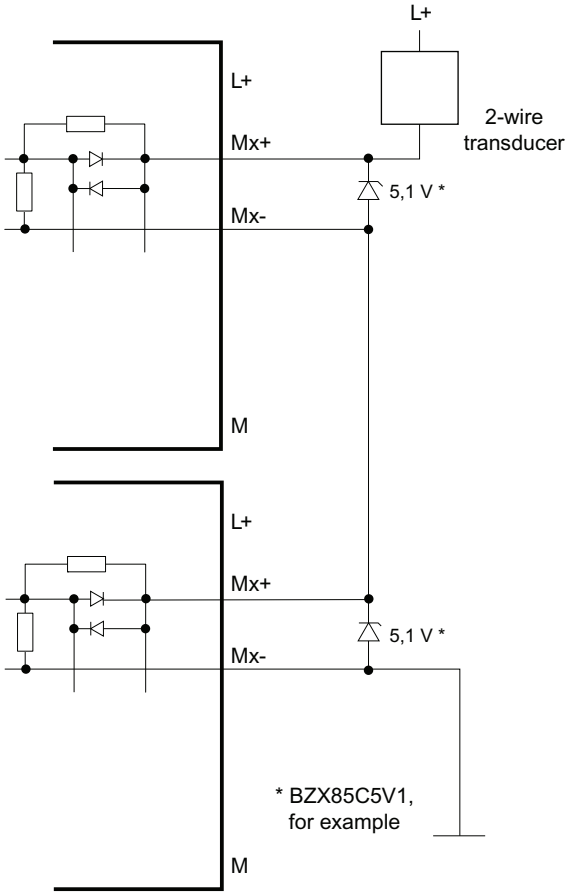


Figure F-31 Interconnection example 2 SM 331; AI 8 x 0/4...20mA HART

F.31 SM 332; AO 4 x 12 Bit; 6ES7 332–5HD01–0AB0

The diagram below shows the connection of an actuator to two SM 332; AO 4 x 12 Bit. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with $U_{\_r}$ >=200 V and $I_{\_F}$ >= 1 A

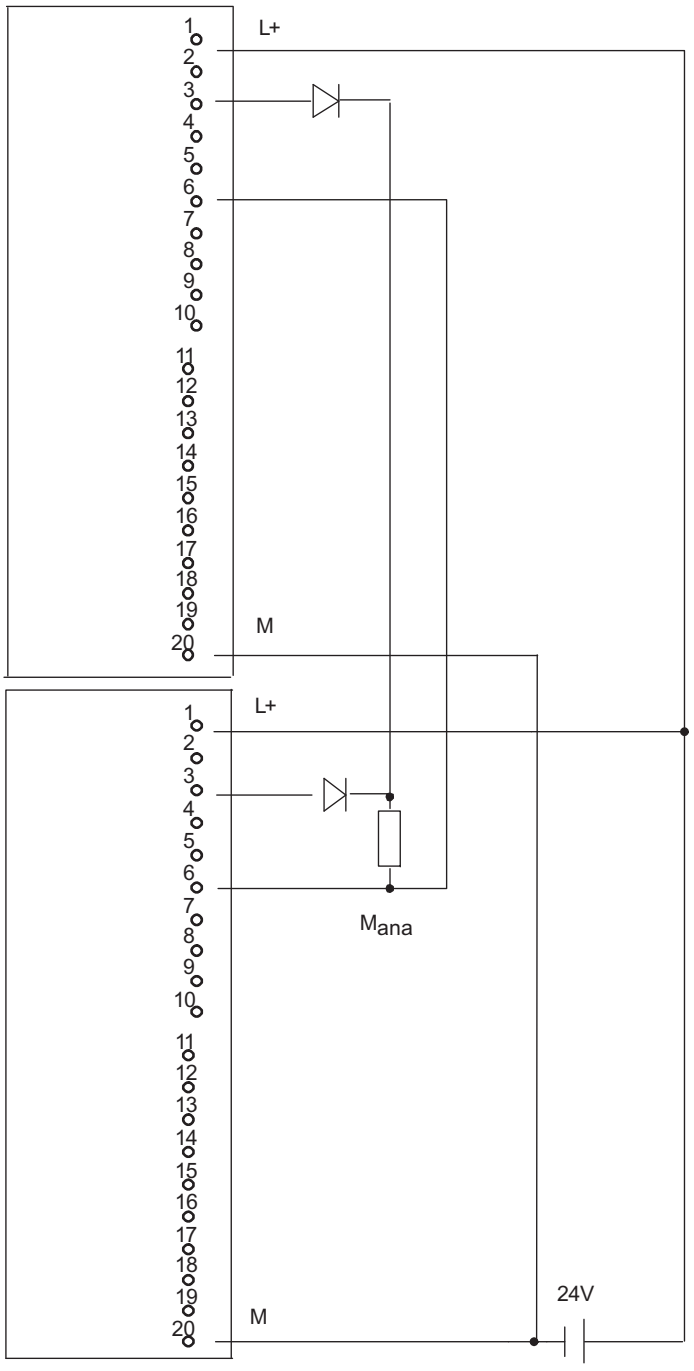


Figure F-32 Example of an interconnection with SM 332, AO 4 x 12 Bit

F.32 SM332; AO 8 x 0/4...20mA HART, 6ES7 332-8TF01-0AB0

The diagram below shows the connection of an actuator to two SM 332; AO 8 x 0/4...20 mA HART.

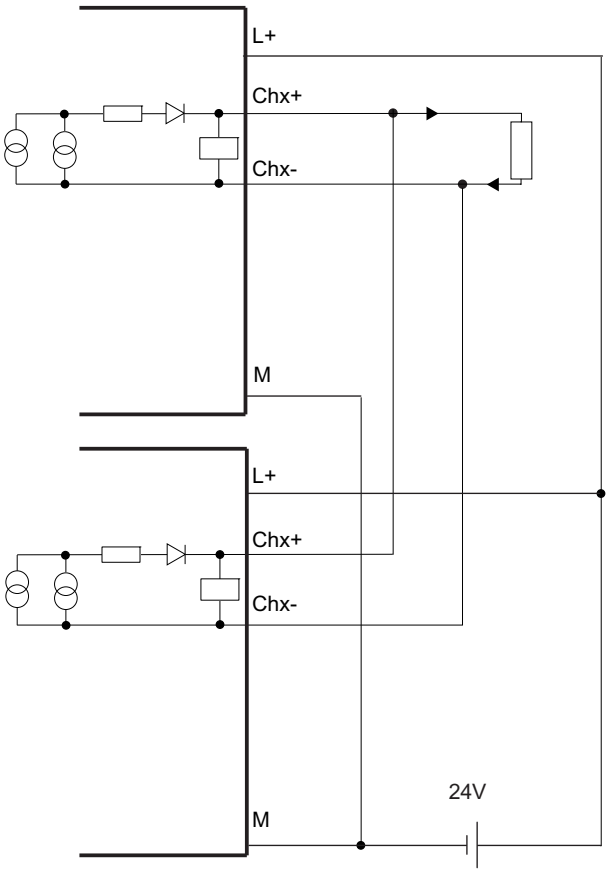


Figure F-33 Interconnection example 3 SM 332; AO 8 x 0/4...20mA HART

F.33 SM 431; AI 16 x 16 Bit, 6ES7 431–7QH00–0AB0

The diagram below shows the connection of a sensor to two SM 431; AI 16 x 16 Bit. Suitable Zener diode: BZX85C6v2.

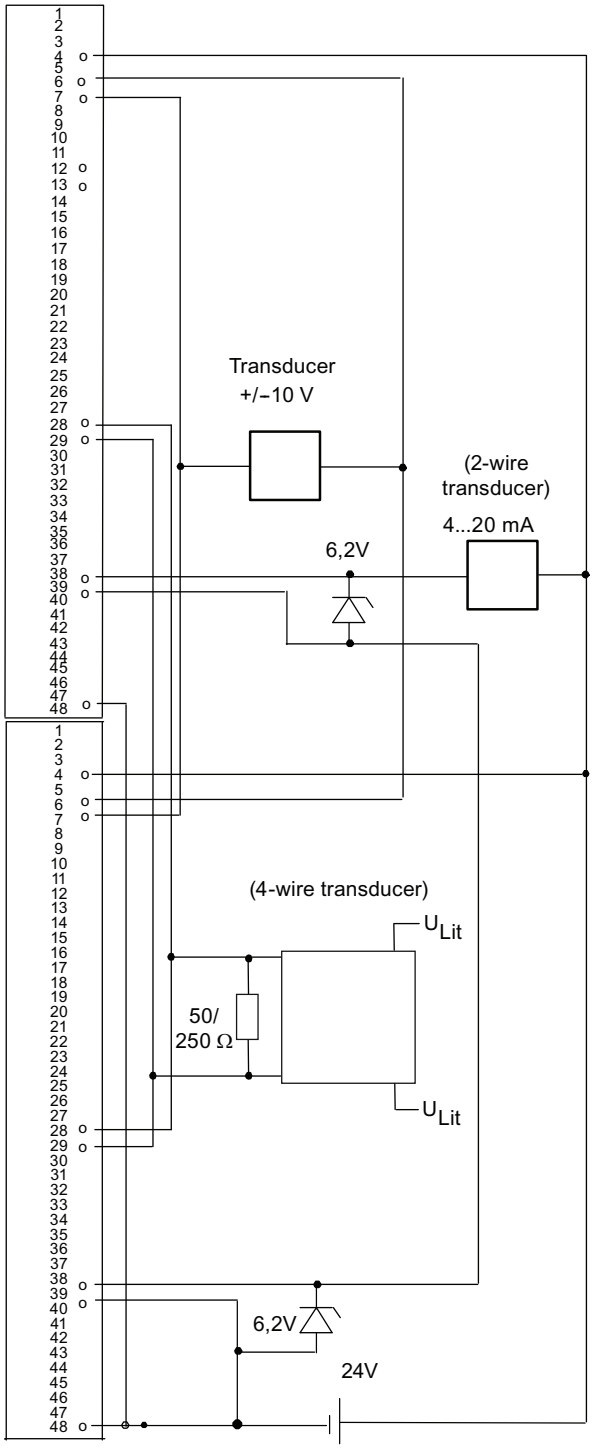


Figure F-34 Example of an interconnection with SM 431; AI 16 x 16 Bit

Glossary

1-out-of-2 system

See dual-channel fault-tolerant system

Comparison error

An error that may occur while memories are being compared on a fault-tolerant system.

Dual-channel fault-tolerant system

Fault-tolerant system with two central processing units

ERROR-SEARCH

An operating mode of the reserve CPU of a fault-tolerant system in which the CPU performs a complete self-test.

Fail-safe systems

Fail-safe systems are characterized by the fact that, when certain failures occur, they remain in a safe state or go directly to another safe state.

Fault-tolerant station

A fault-tolerant station containing two central processing units (master and reserve).

Fault-tolerant system

A fault-tolerant system consists of at least two central processing units (master and reserve). The user program is processed identically in both the master and reserve CPUs.

Fault-tolerant systems

Fault-tolerant systems are designed to reduce production downtime. Availability can be enhanced, for example, by means of component redundancy .

I/O, one-sided

We speak of a one-sided I/O when an input/output module can be accessed by only one of the redundant central processing units. It may be single-channel or multi-channel (redundant) module.

I/O, redundant

We speak of a redundant I/O when there is more than one input/output module available for a process signal. It may be connected as one-sided or switched module. Terminology: "Redundant one-sided I/O" or "Redundant switched I/O"

I/O, single-channel

When there is only one input/output module for a process signal, in contrast to a redundant I/O, this is known as a single-channel I/O. It may be connected as one-sided or switched module.

I/O, switched

We speak of a switched I/O when an input/output module can be accessed by all of the redundant central processing units of a fault-tolerant system. It may be single-channel or multi-channel (redundant) module.

Link-up

In the link-up system mode of a fault-tolerant system, the master CPU and the reserve CPU compare the memory configuration and the contents of the load memory. If they establish differences in the user program, the master CPU updates the user program of the reserve CPU.

Master CPU

The central processing unit that is the first redundant central processing unit to start up . It continues to operate as the master when the redundancy connection is lost . The user program is processed identically in both the master and reserve CPUs.

Mean Down Time (MDT)

The mean down time MDT essentially consists of the time until error detection and the time required to repair or replace defective modules.

Mean Time Between Failures (MTBF)

The average time between two failures and, consequently, a criterion for the reliability of a module or a system.

Mean Time to Repair (MTTR)

The mean time to repair MTTR denotes the average repair time of a module or a system, in other words, the time between the occurrence of an error and the time when the error has been rectified .

Redundancy, functional

Redundancy with which the additional technical means are not only constantly in operation but also involved in the scheduled function. Synonym: active redundancy.

Redundant

In redundant system mode of a fault-tolerant system the central processing units are in RUN mode and are synchronized over the redundant link.

Redundant link

A link between the central processing units of a fault-tolerant system for synchronization and the exchange of data .

Redundant systems

Redundant systems are characterized by the fact that important automation system components are available more than once (redundant). When a redundant component fails, processing of the program is not interrupted.

Reserve CPU

The redundant central processing unit of a fault-tolerant system that is linked to the master CPU. It goes to STOP mode when the redundancy connection is lost. The user program is processed identically in both the master and reserve CPUs.

Self-test

In the case of fault-tolerant CPUs defined self-tests are executed during startup, cyclical processing and when comparison errors occur. They check the contents and the state of the CPUs and the I/Os.

Single mode

An H system changes to single mode, when it was configured to be redundant and only one CPU is in RUN. This CPU is then automatically the master CPU.

Stand-alone operation

Stand-alone mode is the use of a fault-tolerant CPU in a standard SIMATIC-400 station.

Stop

With fault-tolerant systems: In the stop system mode of a fault-tolerant system, the central processing units of the fault-tolerant system are in STOP mode.

Synchronization module

An interface module for the redundant link in a fault-tolerant system.

Update

In the update system mode of a fault-tolerant system, the master CPU updates the dynamic data of the reserve CPU.

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