SIEMENS

Programmable Controller S5-010W

E811 — STANDEXEMPLAR

Manual   Order No.: 6ES5 998-0CA21

Issue   1

Contents	Order No.:
Instructions	GWA 4NEB 807 1021-02
Programming Instructions	GWA 4NEB 807 1071-02

SIEMENS AKTIENGESELLSCHAFT

SIMATIC S5

SIMATIC S5-010W
Programmable Controller

Operating Instructions

SIEMENS

SIMATIC S5–010W Programmable Controller

6ES5 010

Operating Instructions
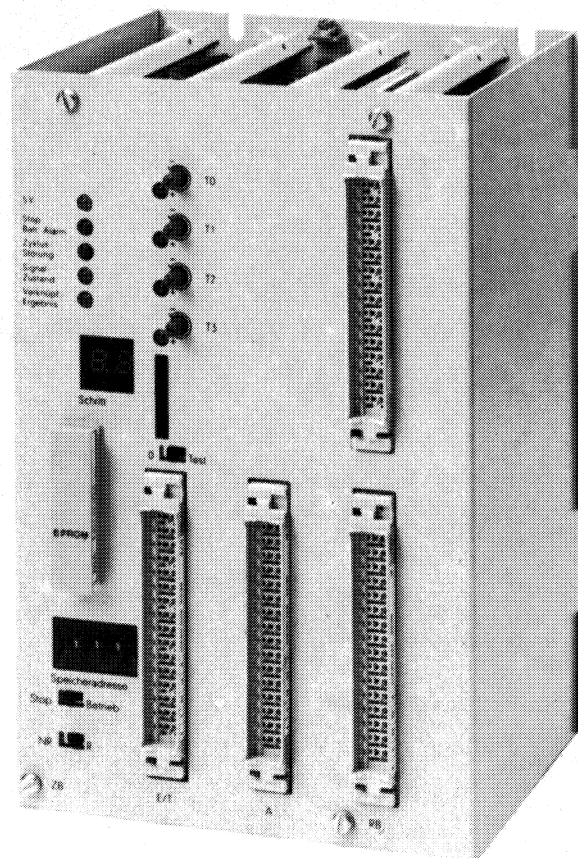
Fig. 1   S5–010W programmable controller with three I/O modules

1

1. Description

1.1 Application
1.2 Construction

1.1 Application

The S5–010W programmable controller belongs to the SIMATIC S5 family of programmable controllers and has been designed for use with small machine tools and adaptive control systems. It is suitable for automation tasks for which contactors, relays or simple hard-wired electronic systems have been used in the past. The range of functions available permits the assembly of binary logic control systems with memory and time functions.
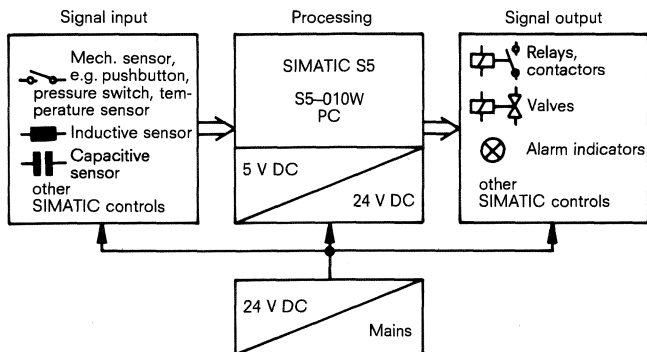

Fig. 2   Application of S5–010W programmable controllers

1.2 Construction

The S5–010W programmable controller comprises a housing containing plug-in printed-circuit boards measuring 160 × 250 mm. Each PCB represents a functional unit.

The modules are housed in an open frame and are interconnected through a 20-way bus which is secured to the rear of the housing. The housing frame permits easy mounting in electronic equipment cabinets and machine tools; no fan is needed.

There are three types of housing available, on with four, one with six and one with eight module locations.

Central processing unit 900

The CPU contains the following:

Bit processor
Power supply unit, 24 V primary/5 V secondary
Memory for flag operations
Backup battery for retentive flags
Service panel
Receptacle for memory submodule 910

Memory submodule 910

Erasable read-only memory (EPROM) for 1K, 2K or 4K statements, depending on the version.

Input/timer module 400

Digital output module 410 (solid-state)

Interface module 772

For interfacing S5–010W programmable controllers to higher-level control systems.

Programming unit interface module 500

For on-line operation of the S5–010W with the 630, 631 and 670 programming units.
Mechanical design as for S5–110 A modules.
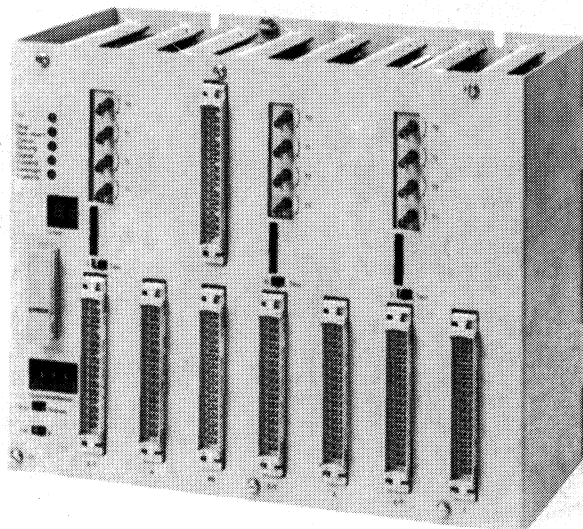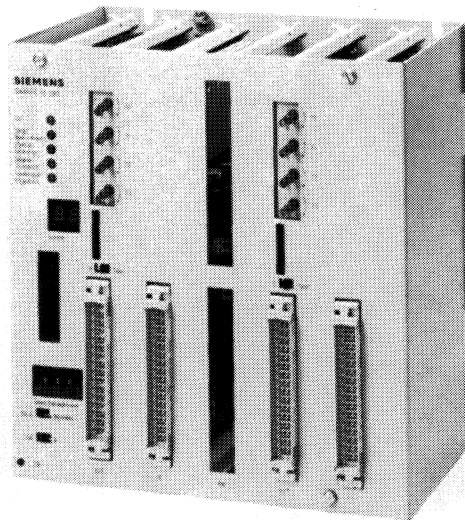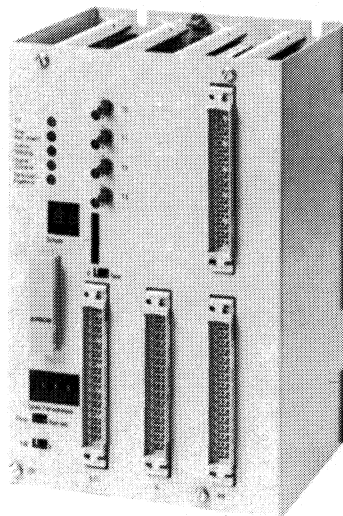
Fig. 3   S5–010W programmable controllers with 4, 6 and 8 module locations

S5–010W module configurations

The CPU, interface module and input/timer modules are assigned to definite locations. One of the two output modules can be used in place of the interface module.

The maximum configuration is then as follows:

PC with four module locations:

Analog timers: 4
Inputs: 40
Outputs: 56

PC with six module locations:

Analog timers: 8
Inputs: 80
Outputs: 84

PC with eight module locations:

Analog timers: 12
Inputs: 120
Outputs: 112

Fig. 4   Maximum module configuration of the S5–010W programmable controllers

1. Description

1.3 Principle of operation

The program memory contains the STEP 5 program written by the user. The memory is organized bytewise, one byte comprising 8 bits and 2 bytes constituting a complete statement, e.g. AI 5.1. This statement implies the following:
– Examine input I 5.1 to see whether it is "1" and AND this signal with the result of the previous scanning operation.
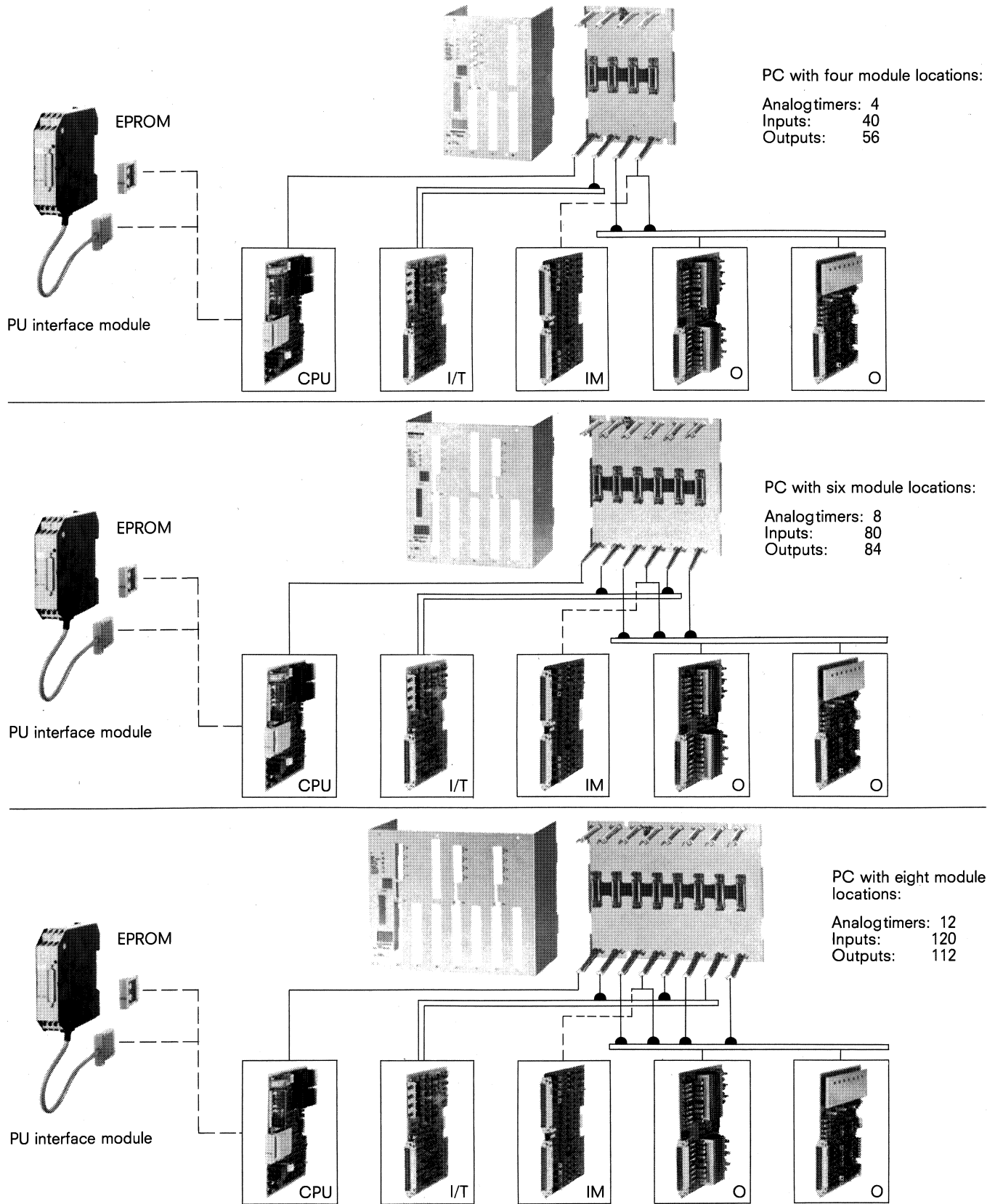
The statements contained in the program memory are executed consecutively and cyclically by the processor. The individual memory locations are referenced by an address counter. By incrementing the address counter by +1, it is possible to read out the next two bytes (a complete statement).

The following is a description of the principle of operation of the PC by way of example of the AI 5.1 and = Q 5.3 statements (see Fig. 5).

When the address counter of the processor reaches the appropriate memory location, the "AI 5.1" statement stored there is read out.

The parameter 5.1 is output via the address bus to all I/O modules, where it is decoded by the address decoders.

The operation decoder of the CPU evaluates the operand "I" and holds all output modules disabled via the enabling bus.

In conjunction with the full parameter, therefore, input 5.1 is specified and can be examined. Depending on the signal status at the input of this element, either "1" or "0" is transmitted on the input data bus (D_{IN}) to the sequence logic unit of the processor for further processing.

From the bit pattern for the letter "A" in the operation "AI" (A = AND), the decoder recognizes that the result of the scan has to be ANDed with the result of the previous scanning operation in the logic unit.

The new RLO (result of logic operation) is stored in the logic unit.

The next statement, in this case "= Q 5.3", is read out by incrementing the address counter again. The address 5.3 is output via the address bus to all I/O modules, where it is decoded.

The decoder evaluates the operand "= Q" and places the result of the logic operation (RLO) stored in the logic on the output data bus (D_{OUT}). After enabling of the I/O modules, the RLO is available at output Q 5.3. Due to the cyclic execution of the statements, the output statuses must be stored on the output module.
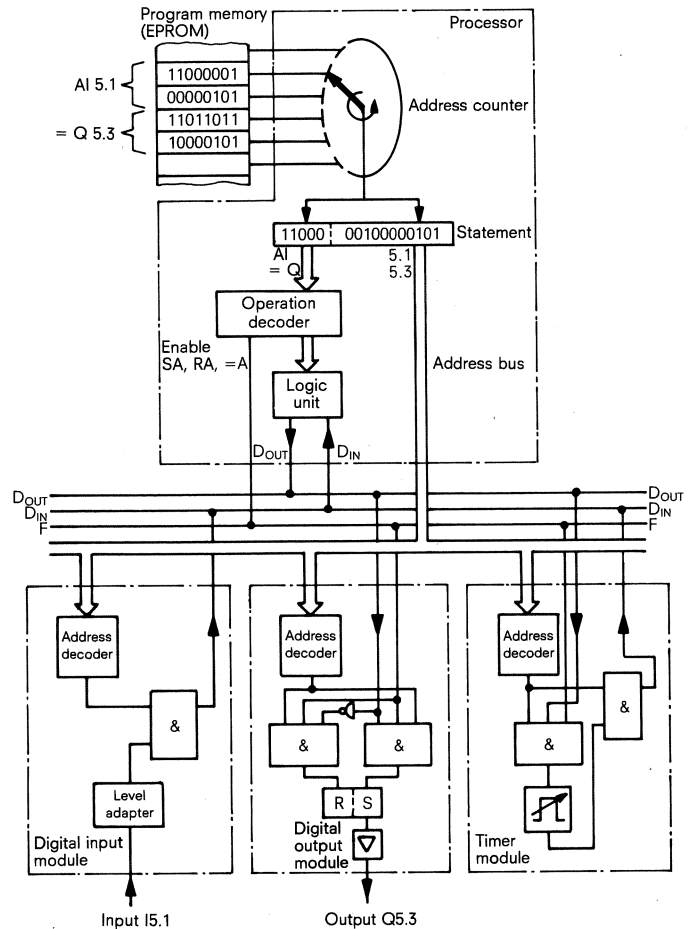

Fig. 5 Principle of operation of the S5–010W programmable controller

4

Central processing unit 6ES5900–OAA12

The CPU incorporates the following functional units:

– Power supply
– Processor with cycle time monitor
– Memory for flag operations
– Receptacle for EPROM submodule

Power supply

The 24 V DC power supply is provided by a non-stabilized power supply.

The operating voltage of + 5 V required for internal signal processing is produced from the 24 V supply.

Processor

The processor decodes the programmed statements and executes the relevant operations (see STEP 5 operation set for the S5-010 PC). The execution time for a statement corresponds to the period of the system clocking and is approximately 20 μs. For 1 K statements, therefore, this gives a cycle time of 20 ms.
For cycle time monitoring, the program controller contains a 200 ms timer which is continuously reset by the "BE"/"BEC" (block end) and AF0.0 (interrupt) operations. If no resetting of the timer takes place during a 200 ms period, the control system is in an undefined state. The "Cycle fault" display lights up and the link between pins X3 and X4 via the "Watchdog monitor" relay contact is interrupted. To prevent the indefinite state of the control system from being transferred to the machine being controlled it is advisable to run the +24 V supply for all output modules through a contactor driven by the watchdog monitor relay (see Connection diagram, page 11). This will ensure that all outputs assume the logic state "0" during a scan fault.

Memory for flag operations

A 1024 × 1 bit static RAM is used for flag operations. The memory is subdivided into three areas (see Fig. 7).

Retentive flags:

These flags are addressed by the operations SF, RF, = F, etc. The flag area has battery backup, i. e. the flags retain their signal statuses in the event of power failure. The battery backup can be disabled by a switch on the CPU (see "Service panel").

Non-retentive flags:

These flags are addressed by the operations SF, RF, = F, etc. In the event of a power failure, this flag area is erased.

Output flags:

Output flags are addressed by output operations (SQ, RQ, = Q), i. e. they are set and reset in parallel with the outputs. When scanning the outputs (AQ, ANQ, OQ, ONQ), only these flags are examined; the actual outputs of output and timer modules cannot be scanned. Output flags are erased in the event of power failure.

Output flag Q00.0 cannot be used; flag F00.0 is only needed for interrupt processing.

EPROM submodule 910

EPROMs mounted on a plug-in submodule are used to store the STEP5 program. Submodules are available for 1K, 2K and 4K statements.
The memory submodule is plugged into the appropriate receptacle on the programming unit for programming. After programming, the module is plugged into the receptacle provided for it on the CPU.
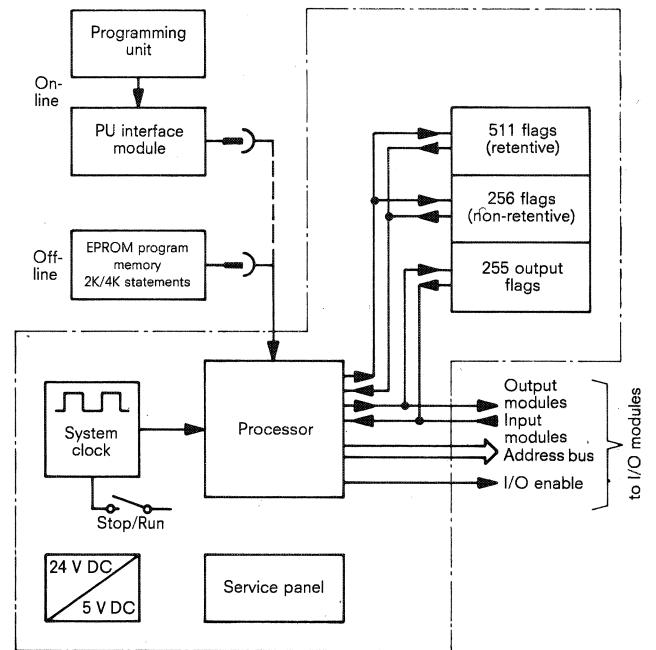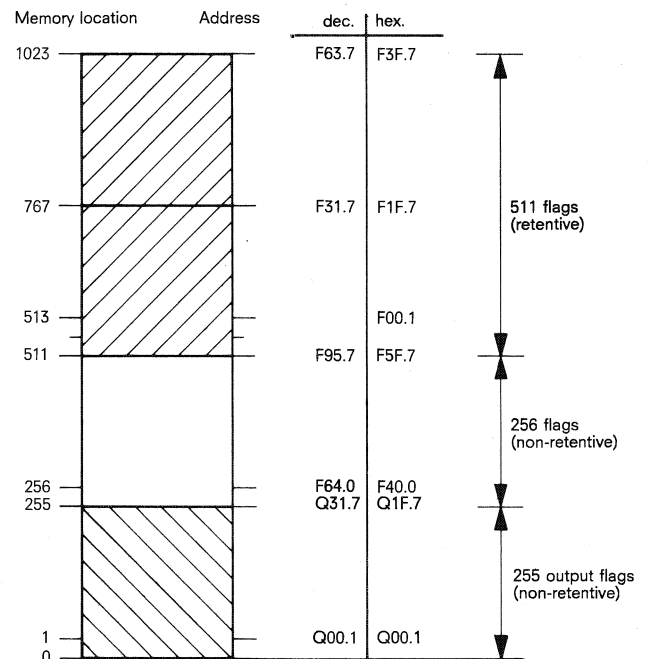

Fig. 6 Block diagram of the CPU

Fig. 7 Memory organization, address assignment

1. Description

1.3 Principle of operation

Input/timer module 6ES5400–OAA11

The module contains the following:

40 inputs for 24 V DC
Four of these can be used as interrupt inputs. Interrupts can be initiated by either the leading edge or trailing edge of the input signal and can be disabled by removing a jumper.

Four analog timers:
Time ranges: 10 ms – 100 ms
100 ms – 1 s
1 s – 10 s
10 s – 100 s

Time setting:
Coarse setting by thumbwheel switch
Fine adjustment by built-in potentiometers

Displays:
LEDs light up while the timer is running.
Accuracy of the timers:
Due to the cyclic execution of the statements, the PC does not detect until some time later that a time has elapsed. The relative error of a timer in relation to its delay time t_{ZS} and the cycle time t_{CYCLE} of the STEP 5 program is shown in Fig. 8.
Analog timers cannot be used for times that are shorter than the cycle time.
The maximum relative error is $\frac{\Delta t}{t_{ZS}}$ max. $= 100 \frac{t_{CYCLE}}{t_{ZS}}$ [%].

The maximum absolute error is always equal to the cycle time.
In the case of programs with interrupt processing and when using the "BEC" (block end conditionally) statements, it must be remembered that the cycle time t_{CYCLE} is not constant. The maximum relative error can always be estimated from
$\frac{\Delta t}{t_{ZS}}$ max. $= 100 \frac{t_{CYCLE}}{t_{ZS}}$ [%].
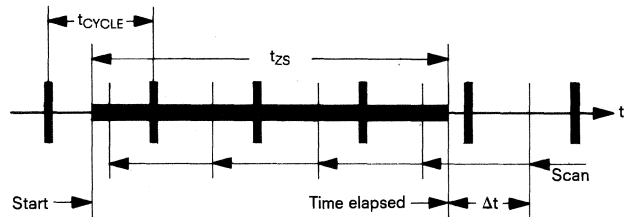
Relative error: $\frac{\Delta t}{t_{ZS}}$ 0 … 100 $\frac{t_{CYCLE}}{t_{ZS}}$ [%] when $t_{ZS} > t_{CYCLE}$.

Fig. 8   Relative error of timer

Digital output module 6ES5410-0AA12

The module contains the following:

– 24 outputs, 24 V DC/0.8 A; simultaneity factor 50 %
– 4 outputs, 24 V DC/2 A

Each of the 0.8 A outputs is electronically protected against short-circuit.
Extra-fast fuses (FF 2.5/250 G) are fitted for protecting the 2 A outputs.
The voltage induced when disconnecting inductive loads is limited to −15 V by internal suppression elements. With inductive loading and rated current, the maximum switching frequency is 1 Hz. Higher switching frequencies are permissible with partial loading of the outputs or if the load is predominantly resistive.

Digital output module 6ES5410-0AA41

The module contains the following:

– 16 outputs, 24 V DC/2 A; simultaneity factor 50 %

Each of the outputs is protected by an integral extra-fast fuse (FF 2.5/250 G). The voltage induced when interrupting inductive loads is limited to −15 V by internal suppression elements. To special order, each output can also be fitted with a freewheeling diode which can be cut out if it is not needed. The circuit-breaking characteristics (qualitative) with and without a freewheeling diode are shown in Fig. 9.

It must be pointed out that the use of freewheeling diodes can cause the current in the inductive load to increase again due to the extended disconnection time. This will cause pumping of the contactor contacts and therefore increased wear.
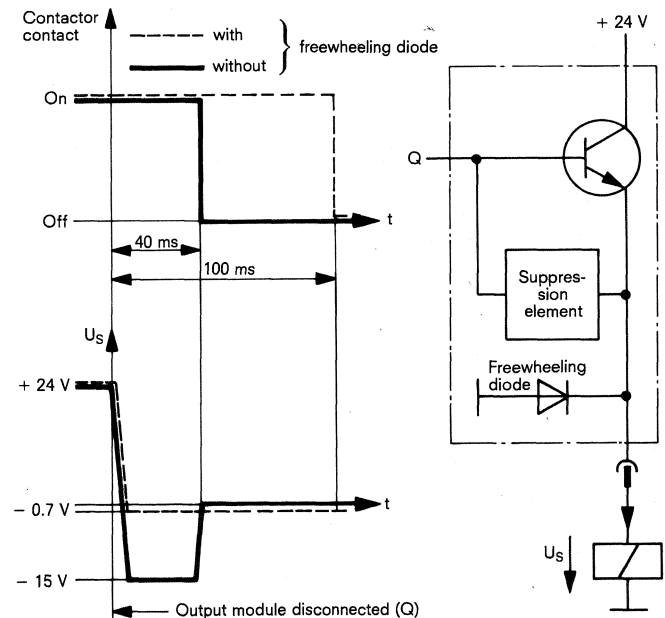

Fig. 9   Interrupting inductive loads (qualitative characteristics)

Interface module 6ES5772-0AA12

General:

The 6ES5772-0AA12 modules enable up to 15 individual S5-010 programmable controllers to be interfaced to a higher-ranking PC (e.g. S5-150), one such module being needed for each PC. This arrangement is particularly meaningful when the PCs of several autonomous individual machines of, for example, a production line are to operate under a higher-ranking control system.

Signal interchange takes place on a peripheral bus which is looped through all the interface modules, starting from the master PC.

It should be pointed out that a radial arrangement of the peripheral bus is possible and may be the better solution for many applications. It avoids, for example, having to shut down all the S5-010 PCs when changing modules in only one of them.

The master PC must have eight inputs and 13 outputs for 24 V. The peripheral bus carries the following signals:

- 8 bits for 8 binary signals from the S5-010 W PC (inputs of the master PC)
- 8 bits for 8 binary signals to the S5-010 W PC (outputs of the master PC)
- 4 bits for addressing the interface modules
- 1 bit for low/high byte selection

In addition to these 21 signal lines a further two are needed for the 24 V supply so that a 24-core SIMATIC cable can be used.
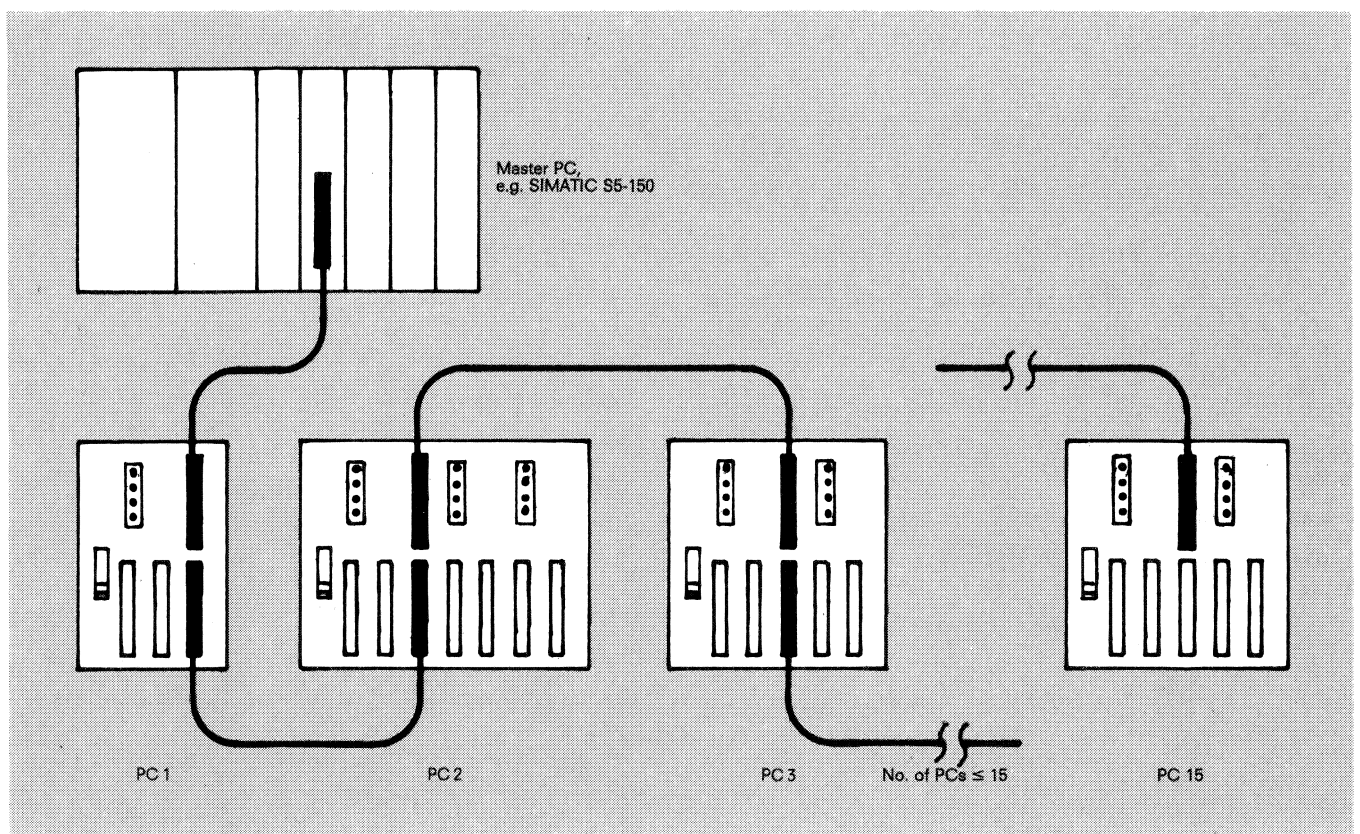
Fig. 10   Interfacing up to 15 S5-010 W programmable controllers to a master PC

All inputs and outputs, including the address bits, are galvanically isolated from the S5-010 PCs, which means that the individual PCs can have different reference potentials. The +24 V and M (reference potential) connections to the interface module must be taken from the power source supplying the input/output modules of the master PC.

The outputs have an output load capability of 30 mA and are current-limited. Since the peripheral bus runs through n ≦ 15 interface modules, all the eight outputs of an interface module are connected in parallel with n − 1 outputs of the other interface modules. The mutual loading of the outputs due to the paralleling is n × 1 mA. The load capability of each output is reduced by this amount.

1. Description

1.3 Principle of operation

Principle of operation

All aspects of data exchange are initiated by the master PC.
The interface modules are addressed sequentially by the master PC for T = 24 ms each. When the address is placed on the bus, the first eight signals (low byte) are transferred immediately, and the second eight signals (high byte) after T/2 = 12 ms, and buffered on the interface module or recalled from the buffer.
Seen from the S5-010 PC, the interface module is a module with 16 inputs and 16 outputs. Fig. 11 shows the interaction between the master PC and an S5-010 PC by means of a block diagram.

Minimum times must be adhered to for the transmission mode (see Fig. 12). Since the signals are transmitted through normal I/O modules as 24 V signals, allowance must be made for the delay times of the input module (S5-150) and interface module, which are necessary for reasons of noise immunity.
A minimum time of 12 ms is necessary for transmitting eight signal statuses in both directions. This gives a minimum time of 360 ms for 16 signal statuses (low and high bytes) to each of 15 PCs.

Interrupt processing

The interface module has been equipped with an interrupt circuit in order to improve the data throughput. The interrupt is generated when the S5-010 receives the output data from the master PC.
Cyclic execution of the STEP 5 program of the S5-010 controller is interrupted and the processor returns to the beginning of the program.
The first statements of the STEP 5 program are used for interrupt processing, which needs a time of $T_B = n \times 20\ \mu s$. After time $T_B + t_K + t_{CV}$ (t_K: input delay of interface module; t_{CV}: delay due to bus cable), the S5-010 PC has processed the input data (low byte address 6.0–6.7) of the master PC and updated its output data affecting interrupt processing (see Fig. 13).

Certain output data (address 7.0..7.7) are enabled for the master PC after the change from low to high byte and can be processed once the data are received by the master PC (T_E: input delay of master PC).

Interrupt processing therefore ensures that the transmission of data from the master PC to the S5-010 and from the S5-010 to the master PC takes place within the low byte and high byte, respectively, of the same addressing interval T.

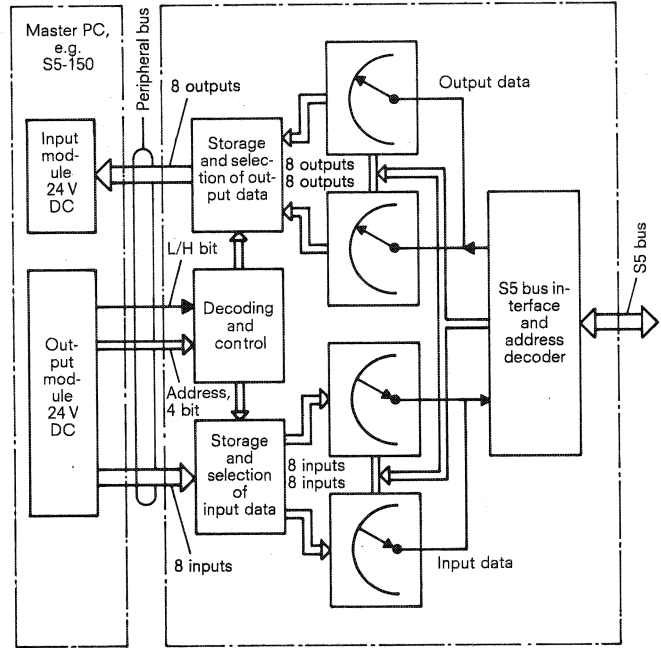Interrupt processing is activated by closing two DIPFIX switches.
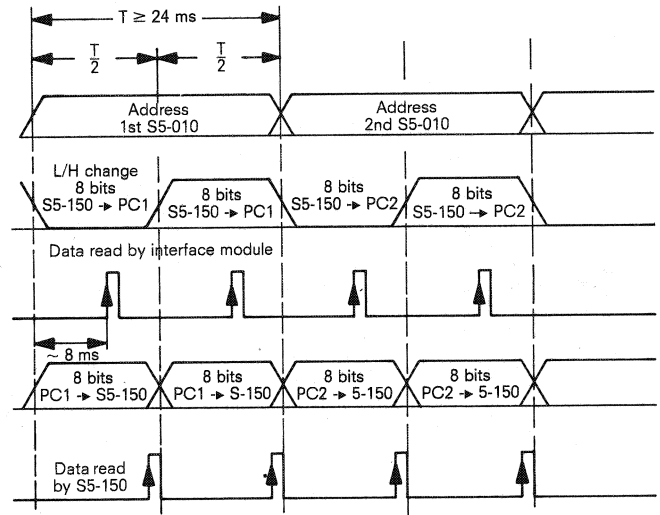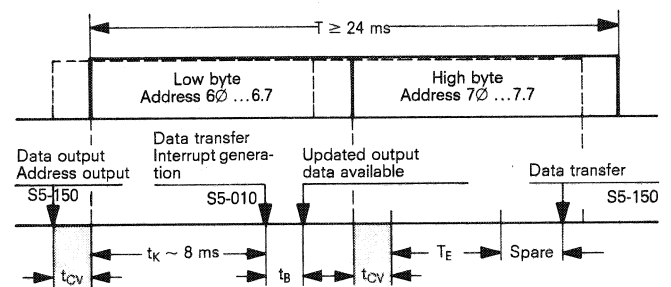

Fig. 11   Block diagram of the interface module

Fig. 12   Timing of the transfer mode

General technical specification

Construction	Open frame with plug-in modules	Memory capacity	1K, 2K, 4K		
		Memory type	EPROM		
Housing with	4 module locations 6 module locations 8 module locations	Addressing range	Hex.	Dec.	No.
		Timers	0.1...1F.7	(0.1...31.7)	255
		Inputs	0.1...1F.7	(0.1...31.7)	255
Power supply connections Watchdog contactor monitor	Tab connectors for quick-connect terminals 6.3 mm or 2 × 2.8 mm	Outputs	0.1...1F.7	(0.1...31.7)	255
		Output flags	0.1...1F.7	(0.1...31.7)	255
		Retentive flags	0.1...3F.7	(0.1...63.7)	511
Connections for inputs and outputs	48-way plug connector, range 2	Non-retentive flags	40.1...5F.7	(640.1...95.7)	256
Installation	in control cabinets (e.g. 19″) or on a vertical mounting surface	Battery backup for flags	Lithium battery, approx. 5 year life		
Ambient temperature range	0...+55°C	Execution time per statement	20 μs		
Storage temperature	−40...+85°C	Cycle monitoring time	200 ms		
Humidity rating	F to DIN 40040	Supply voltage	24 V DC (20...30 V)		
Altitude rating	S to DIN 40040	Current consumption of CPU	max. 800 mA		
Mechanical stressing		Test voltage	VDE 0160		
Vibration	10–58 Hz, constant deflection 0.15 mm	Clearances in air and creepage distances	VDE 0110		
Shock	30 g, 18 ms semi-sinusoidal				
Drop	VDE 0160	Degree of protection	IP 00		

Dimensions, weights, heat losses

Module	w × h × d (mm)	Weight (kg)	Heat loss (W)
CPU with 2K EPROM submodule with PU interface module		0.42	7 10
Input/timer module	35 × 250 × 160	0.3	8.5
Digital output module 4 × 2 A/24 × 0.8 A		0.5	30*
Digital output module 16 × 2 A		0.75	35*
Interface module		0.3	3
PU interface module 500	40 × 166 × 150	0.4	2

Empty housing with 4 module locations
    6 module locations
    8 module locations
	180 × 270 × 177
	260 × 270 × 177
	340 × 270 × 177
		2.7
		3.2
		4.3
			* Simultaneity
			factor 50 %

1. Description

1.4 Technical specification

INPUT/ TIMER MODULE 6ES5400-0AA11	No. of timers	Time adjustment coarse by thumb-wheel switch	fine by potentiometer	Reproducibility of time setting	Drift due to temperature	Long-term error	Recovery time	Fine adjustment by potentiometer (500 kΩ)	
	4	0.01.. 0.1 s 0.1 ... 1.0 s 1.0 ... 10 s 10.0 ...100 s	0.008... 0.160 s 0.050... 1.500 s 0.750... 25 s 7.0 ...230 s	± 3 % with constant scan time	+ 1 %/10°C	< 5 % per 1000 h	none	internal on frontplate	external, max. length of connecting lead 10 m (screened)

	No. of inputs	Rated input voltage	Input voltage for		Input rated current at "1" signal	Delay time		Max. lead length in live cable[5]) at				Insulation[6])	
			"0" signal	"1" signal		On	Off	24/48 V AC/DC	110 V AC	220 V AC	run sep-arately[4])	for rated value	tested at
	40	24 V DC	− 2 V...+ 6 V or open input	+ 15 V... + 35 V	9 mA	1.5–6.5 ms		1000 m	100 m	50 m	600 m	36 V DC	500 VAC

OUTPUT MODULE 6ES5410-	No. of outputs	Rated output voltage	Voltage ranges		Max. output current at "1" signal	Max. residual current at "0" signal	Signal level of "1" outputs	Limiting of volt. ind. on interrupt. ind. load	Switching frequency			Simultane-ity factor (see Fig. 13)	Insulation[6]) tested at
			Min.	Max.					Resistive	Lamp load	Inductive load		
0AA41	16	24 V DC	20 V DC	30 V DC	2 A	1 mA	U −2 V	−15 V	100 Hz	11 Hz	2 Hz	50 %	500 V DC
0AA12	4	24 V DC	20 V DC	30 V DC	2 A	1 mA	U −2 V	−15 V	100 Hz	11 Hz	2 Hz	100 %	500 V AC
	24				0.8 A	1 mA	U −1 V					50 %	

INTERFACE MODULE 6ES5772-0AA12	No. of inputs	Rated input voltage	Input voltage for		Input rated current at "1" signal	Delay time		Max. lead length in live cable[5]) at				Insulation[6])	
			"0" signal	"1" signal		On	Off	24/48 V AC/DC	110 V AC	220 V AC	run sep-arately[4])	for rated value	tested at
	8 + 8[1])	24 V	as for INPUT/ TIMER MODULE		6.5 mA	1.5–5.5 ms		1000 m	100 m	50 m	600 m	36 V DC	500 V AC
	5[2])					≦ 0.5 ms							
	floating												

	No. of outputs	Rated output voltage	Voltage ranges		Max. output current at "1" signal	Max. residual current at "0" signal	Signal level of "1" outputs
			Min.	Max.			
	8 + 8[1])	24 V DC	20 V DC	30 V DC	(30−n × 1)mA[3])	5 mA	U−1 V
	floating						

[1]) Data inputs and outputs changed over by low/high byte
[2]) Address inputs and low/high byte
[3]) n: No. of interface modules driven by a master PC
[4]) Various live unshielded cables run without spacing (referred to 220 V AC in adjacent cable)
[5]) Various live unshielded cables in a common sheath
[6]) Internal 5 V voltage to external supply voltage, inputs/outputs of a module to each other

2.1 Mechanical design

The lower part of the housing frame is secured to a vertical mounting surface by four screws (M6). Sufficient free space must be left above and below the unit so that all the heat losses can be dissipated by natural convection or cabinet ventilation.
When the modules have been plugged in the housing cover can be screwed into place.
The module locations are identified for the following standard configurations.

CPU: Central processing unit
I/T: Input/timer module
RB: Suitable for interfacing module
O: Output module

2.2 Connecting the power supplies

CPU:

The power supply and watchdog monitor are connected by tab connectors for quick-connect terminals (6.3 mm or 2 × 2.8 mm).

Terminal identification:

$$\left. \begin{array}{l} + 24\text{ V} \\ 0\text{ V} \end{array} \right\} \text{Power supply}$$

$$\left. \begin{array}{l} X3 \\ X4 \end{array} \right\} \begin{array}{l} \text{Floating contact (opens when PC at} \\ \text{"Stop" and for "Cycle fault")} \end{array}$$

I/O modules:

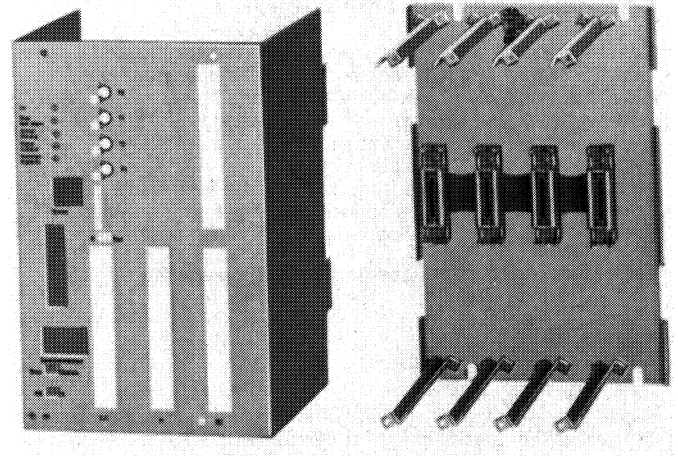For all I/O modules, the power supply is connected via the front connectors used for connecting the signal leads.
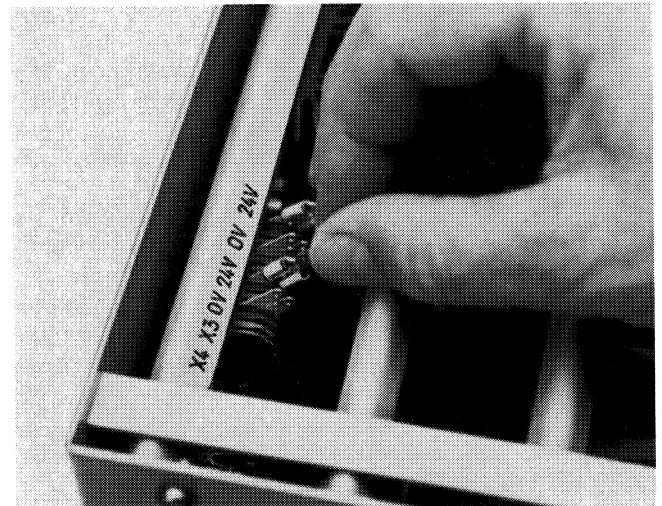

Fig. 14 Installing the housing
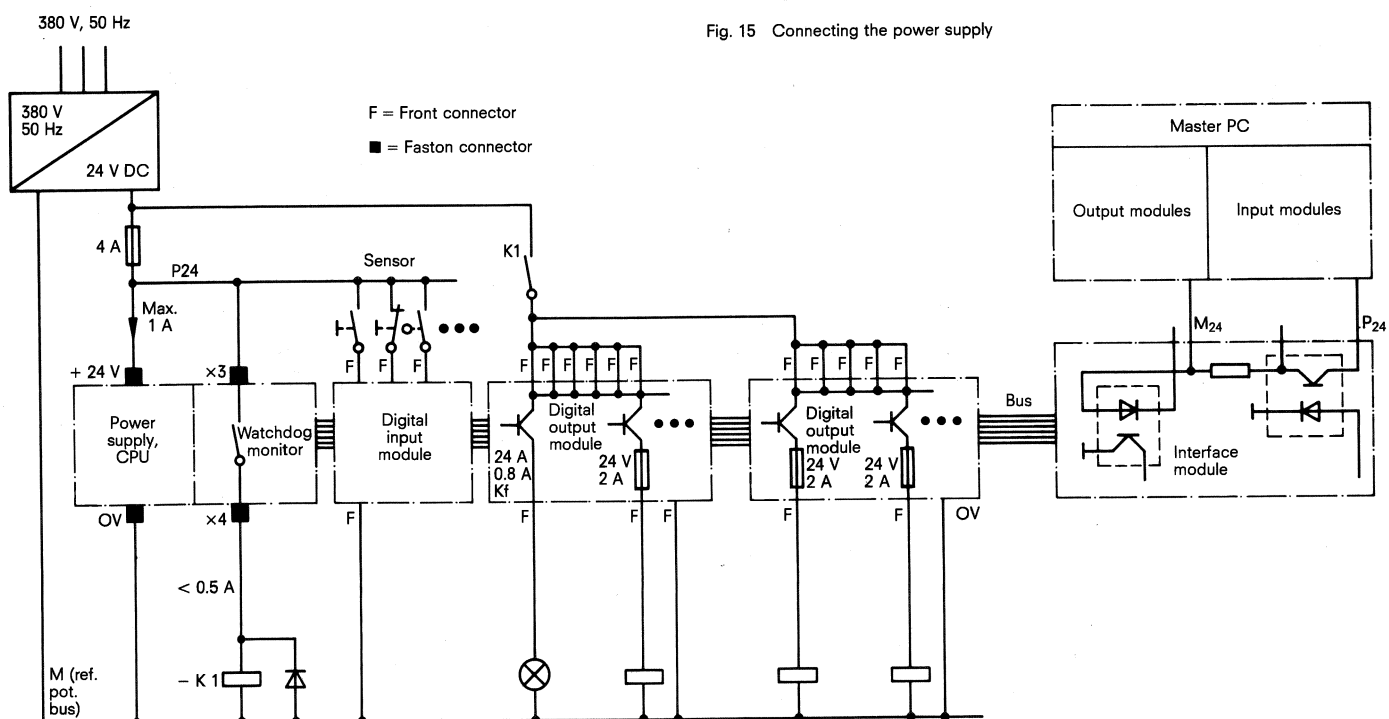

Fig. 15 Connecting the power supply

Fig. 16 Connecting diagram for the S5–010W

2.3 Connecting the signal leads

Each I/O module has a 48-way plug connector for the signal leads. The associated front connector comprises the shell with cable strain relief clamp and one of the following:
– 48-way socket connector with solder posts
– 48-way socket connector with 1 mm × 1 mm pins
– Insulator for 48 crimped connections
Reliable attachment of the front connector is assured by means of an extra locking bar on the connector body. Further details will be found in the section on "Spare parts".

For front connector pin assignments see page 21.

2.4 Electrical design

The power supply must be equipped with smoothing capacitors (approx. 200 μF per Amp load current).

The M-potential bus for the 24 V supply must be as close as possible to the S5-010. All M-potential leads which run to the S5-010 via connectors must have a conductor cross-section of at least 1 mm^2. The connecting lead between the M-potential bus and the protective earth conductor (PE) must have a conductor cross-section of at least 10 mm^2.

The housing of the S5-010 is attached to the mounting plate by means of serrated washers which eliminate the need for a ground wire connection.

24 V and 220 V leads should be run separately if possible or be bundled separately.

If contactors are housed in the same cabinet as the S5-010, or in the immediate vicinity of the cabinet, it is advisable to fit an RC circuit to the contactor coils (R = 220 Ω, C = 0.25 μF).

The following measures are recommended if there is a high noise level:

Fit a capacitor of 0.68 μF between the 0 V terminal of the CPU and the earthing terminal of the subhousing frame.

Connect the connector shell of the cable between the programming unit and its interface module to the M-potential bus of the 24 V supply (on-line operation).

2.5 General

The modules of the S5-010 programmable controller must not be plugged in or unplugged with the system live. The modules employ CMOS technology.

Notes on components and modules sensitive to electrical charge:

– **Printed circuits and components must not be touched with bare hands;** handle modules by means of the edge connector only.
– Persons intending to handle the modules must discharge themselves to frame potential before touching the modules.

Before unplugging the EPROM submodule the mode selector switch must be set to the "STOP" position.
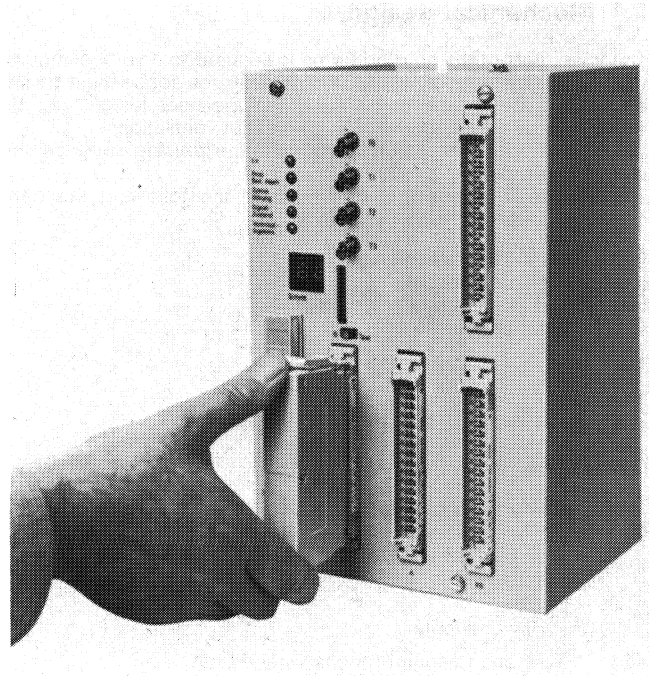

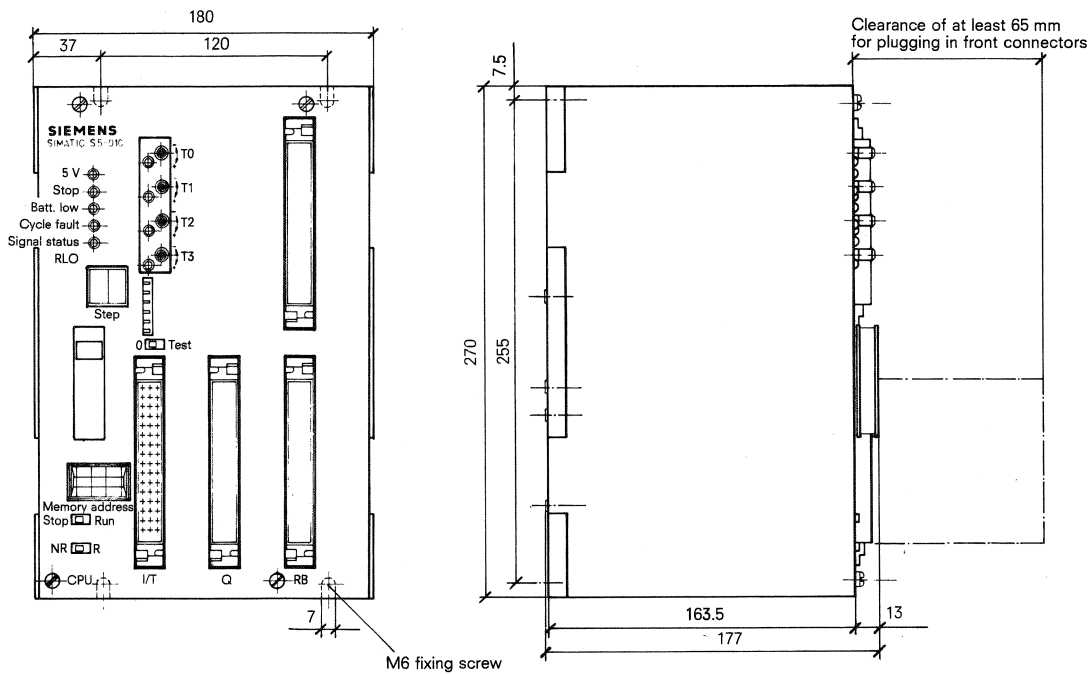Fig. 17 Inserting a front connector

Fig. 18   S5-010W programmable controller for four modules
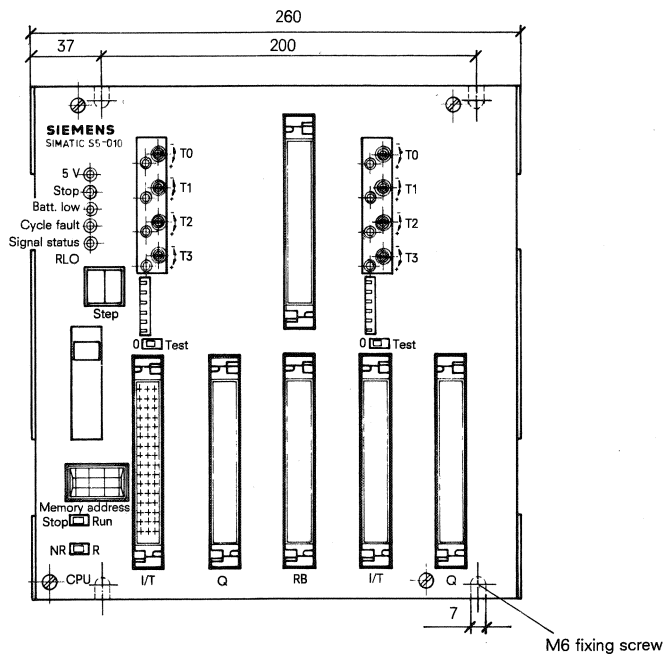

Fig. 19   S5-010W programmable controller for six modules
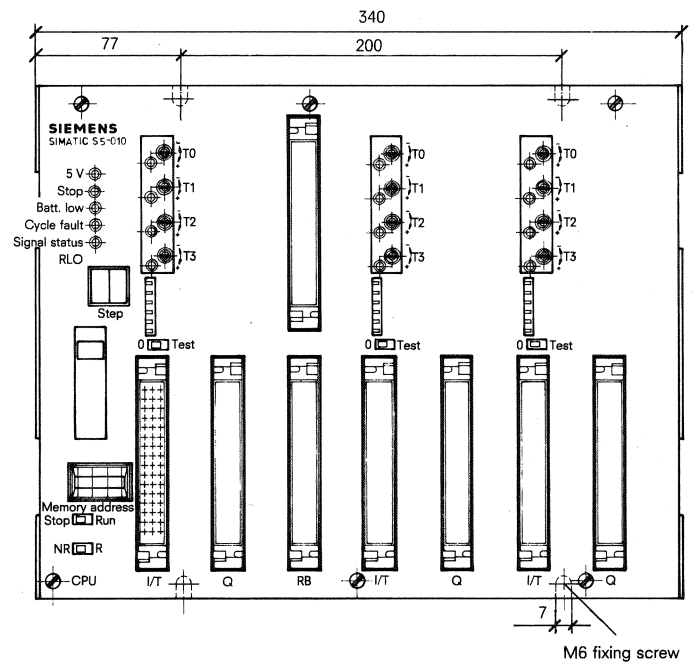

Fig. 20   S5-010W programmable controller for eight modules

3. Operation

3.1 Controls and displays

"5 V" LED:

The LED lights up green as soon as the 5 V supply obtained from the 24 V input supply is available.

"Stop/Batt. alarm" LED:

The orange LED lights up when the "Stop/Run" switch is in the "Stop" position or when the same switch is in the "Run" position and, when the 24 V input supply is switched on, the backup battery has insufficient charge to ensure the retention of the flags. The PC can be made ready for operation by moving the switch in the sequence "Run – Stop – Run". The LED will go out. Change the lithium battery.

"Cycle fault" LED:

The orange LED lights up if the program cycle is not proceeding satisfactorily (see description of processor, p. 5).

"Signal status" LED:

"Result of logic operation" (RLO) LED:

see "Memory address" thumbwheel switch

"Stop/Run" switch:

When this switch is moved from "Stop" to "Run", the user program is executed cyclically, starting at the first statement. Moving the switch from "Run" to "Stop" produces an initializing pulse which inhibits the output of commands. All outputs of the I/O modules are reset.

"R (retentive)/NR (non-retentive)" switch:

In the event of a power failure, the flag area F00.1–F3F.7 (F63.7) either has battery backup (position R) or not (position NR).

"Memory address" thumbwheel switch:

When an address is selected in the program memory by means of the thumbwheel switch, the signal status and the result of the logic operation (RLO) of the corresponding STEP 5 statement are displayed on the two LEDs, "Signal status" and "RLO" (result of logic operation). Display of the signal status has no meaning for setting commands (= Q, SQ, RQ).

"Step" 7-segment LED display:

When programming sequence controls, it is possible to identify each step by setting a flag (area 0.1...F.7). When programming step flags, make sure only **one flag** in the area 0.1...F.7 is set (see example in the programming instructions). The step flags may only be addressed by the SF and RF operations, not with = F. The "Step" display then shows the flag of the current step reached in the program and, in the event of a fault, the step at which the PC has stopped can quickly be ascertained.
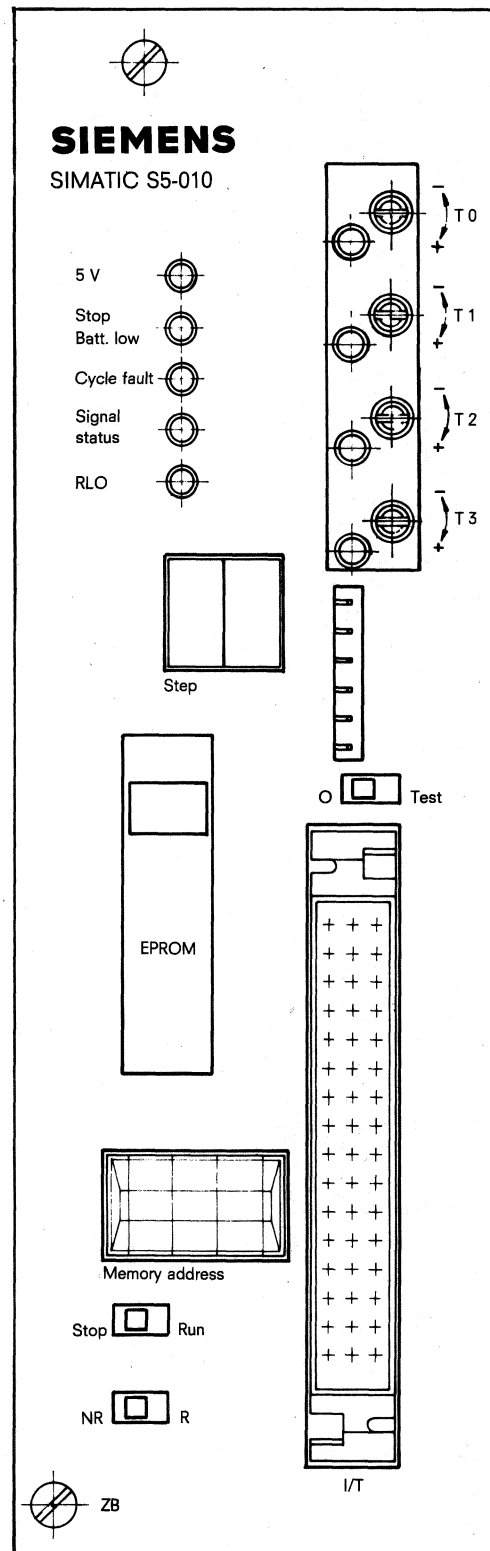

Fig. 21   Controls and displays on the S5-010 W programmable controller

3.2 Time setting

Sliding switch (4 positions):
Coarse setting of the time ranges **before** fitting the housing cover.

Potentiometers "T0...T3":
Fine setting of the timers.

LEDs "T0...T3":
The LEDs light up while the relevant timers are running.

"0/Test" switch:
With the PC at "Stop", the four timers can be started independently of the program by moving the switch from "0" to "Test".
The delay time can then be measured by means of a stopwatch from the length of time that the LED remains on. For setting short times with an oscilloscope or similar instrument, the following measuring points are provided above the switch:

X5...X8: Time T0...T3
   X9: Trigger signal   Output level 5 V (CMOS)
   X10: Frame

Screw terminals are provided for connecting external potentiometers for fine setting of the times.
Remove wire jumper.
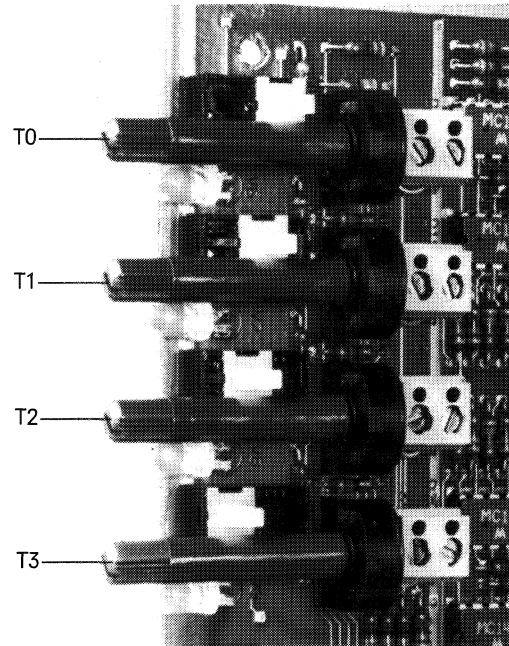Set internal potentiometer to "-" (series connection).

Fig. 22   Controls for time setting

3.3 Programming

The S5-010W programmable controller is programmed in the STEP 5 language (see Programming Instructions for the S5-010).
When using the 610 programming unit, the first four memory locations must be left free if there is to be subsequent documentation or amendment of the program by means of a 630, 631 or 670 programming unit (starting address AD004).
Also, when programming a memory submodule (EPROM) with a 630, 631 or 670 programming unit, make sure that the appropriate jumpers shown in Fig. 23 are fitted.

A 500 interface module is needed for on-line programming with the 630, 631 and 670 programming units.

Note: Avoid touching the printed circuits and components with bare hands.

Memory capacity (statements)	Submodule complement EPROM I	EPROM II	Jumper assignment K1	K2	K3	K4	K5
1K	2716 (2516)	–			X	X	
2K	2716 (2516)	2716 (2516)	X		X	X	
4K	2532	2532	X		X		X
Empty module with two IC sockets			X		X	X	
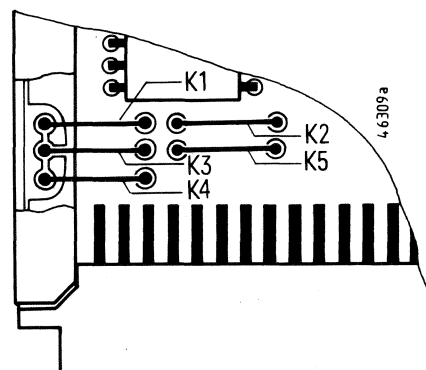
Fig. 23   Jumper assignment of the memory submodule to suit the various EPROMs

15

3.4 Start-up

Checking the wiring

Check the wiring of the external circuits before switching the PC on (see Connection diagram, p. 11).
Check the relevant instructions for installation.
Read the general instructions.

Checking the power supplies

Permitted tolerance of +24 V supply: 20...30 V DC
Maximum ripple content: 5 %
Note: Check carefully that there are no connections to circuits of higher voltages.

3.5 Jumper settings on the modules

The coding jumpers for the specified addressing range must be fitted on all I/O modules and checked (for assignment see "Address decoding").

Central processing unit:

Switch on the backup battery by closing the DIPFIX switch S4.
When using a memory submodule with
$\leq$ 2K statements: DIPFIX S5 closed/S6 open
  4K statements: DIPFIX S6 closed/S5 open
Switch off the "Step" LED display: remove the soldered jumper FG (service panel).

Input/timer module:

The pulse edge for interrupt initiation can be adjusted for all four interrupt inputs together.

Soldered jumper EF: pulse edge

Soldered jumper FG: pluse edge

Interrupt generation can be displayed by removing soldered jumper HK.

When using the internal potentiometer for fine setting of the time, wire jumpers must be fitted to the screw terminals.

Interface module:

Interrupt generation is activated with the DIPFIX switches X1/7 and X1/8. The assignment is as follows:

X1/7	X1/8	Interrupt initiation
● ●	● ●	None
●—●	● ●	Pulse edge
● ●	●—●	of L/H byte
●—●	●—●	
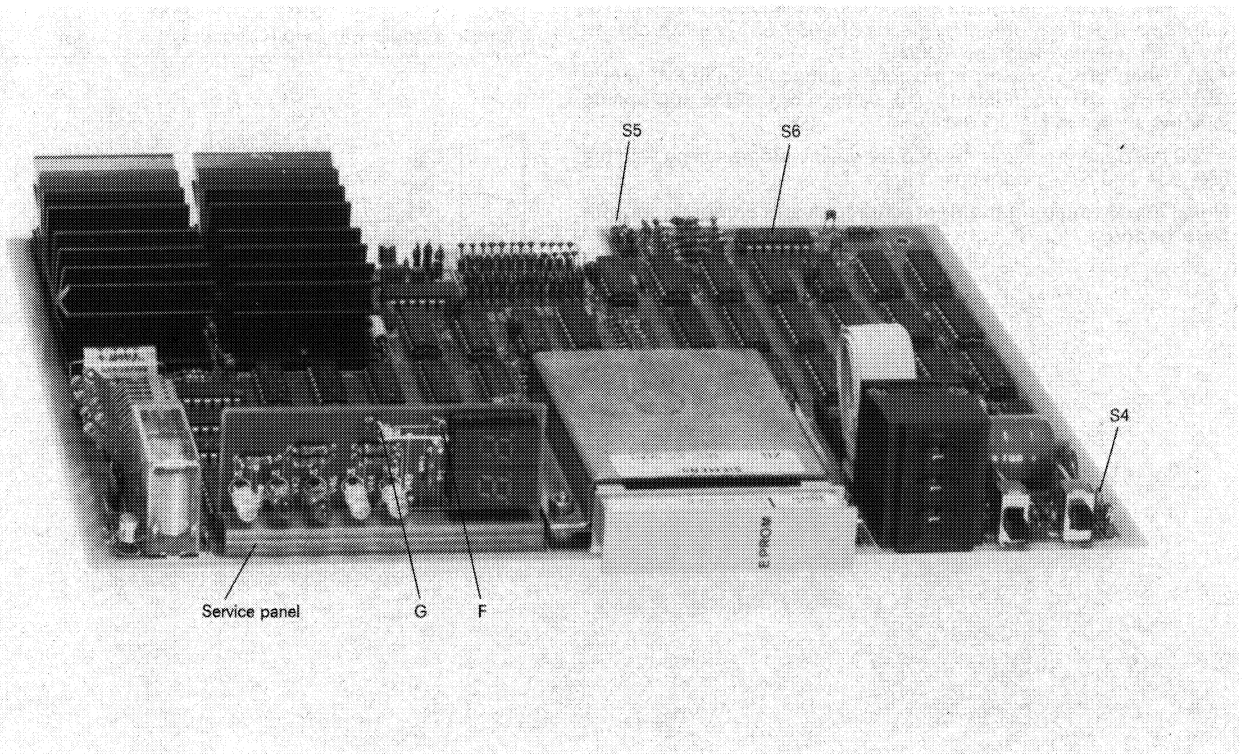
Fig. 24 Jumper assignment and positions of the DIL switches on the CPU
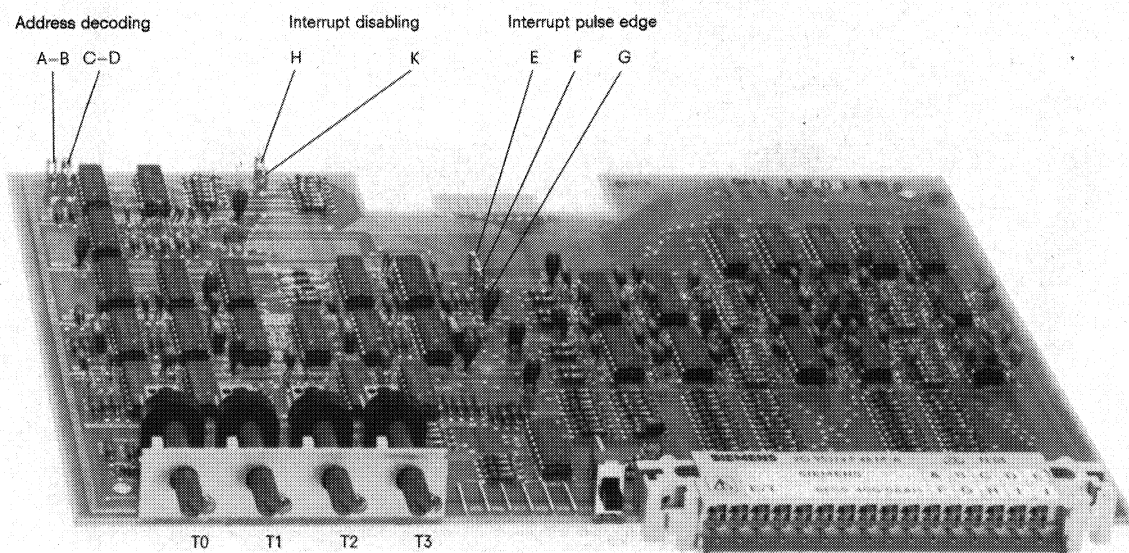
Fig. 25   Jumper assignment and positions of the DIL switches on the input/timer module
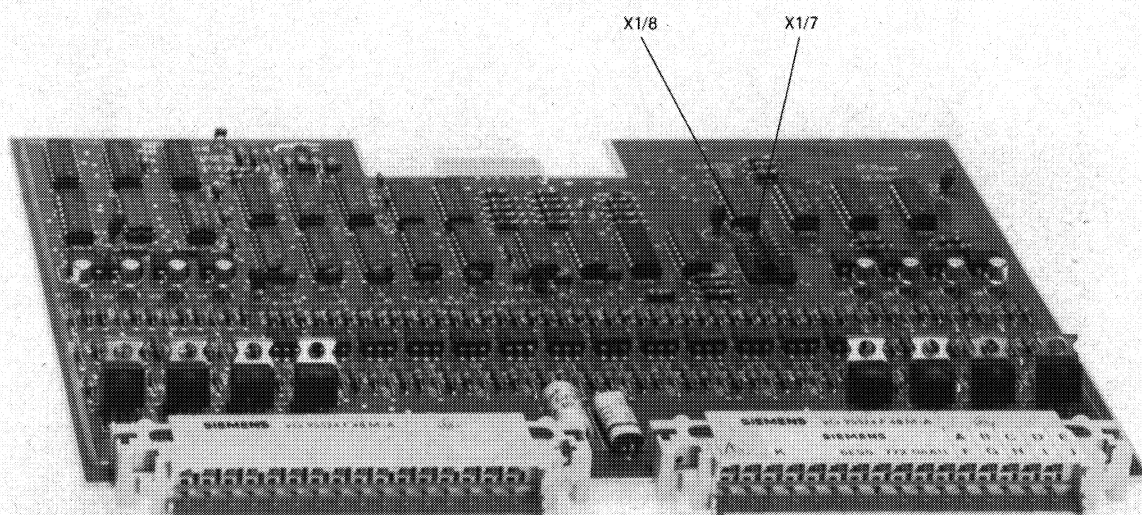
Fig. 26   Jumper assignment on the interface module

3. Operation

3.5 Jumper settings on the modules
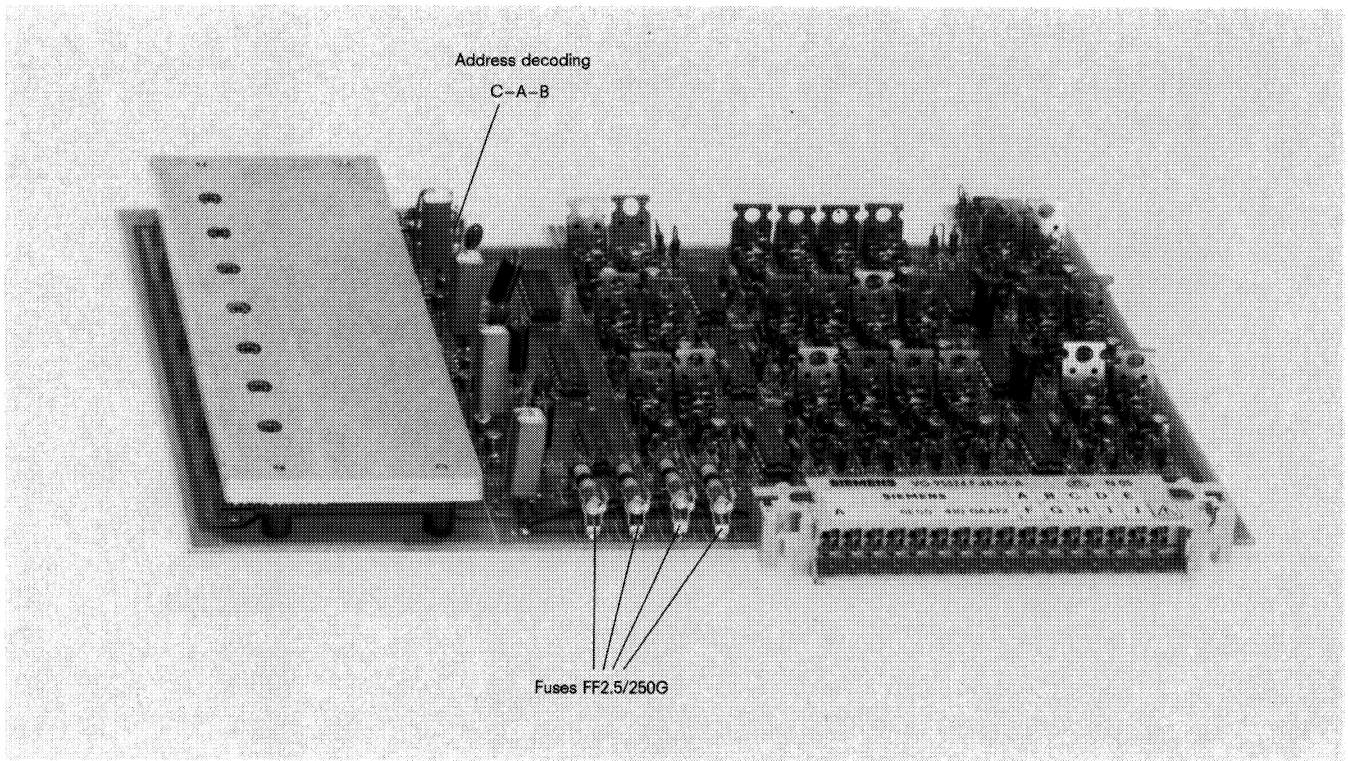
Fig. 27   Jumper assignment and fuses on the output module 0AA12
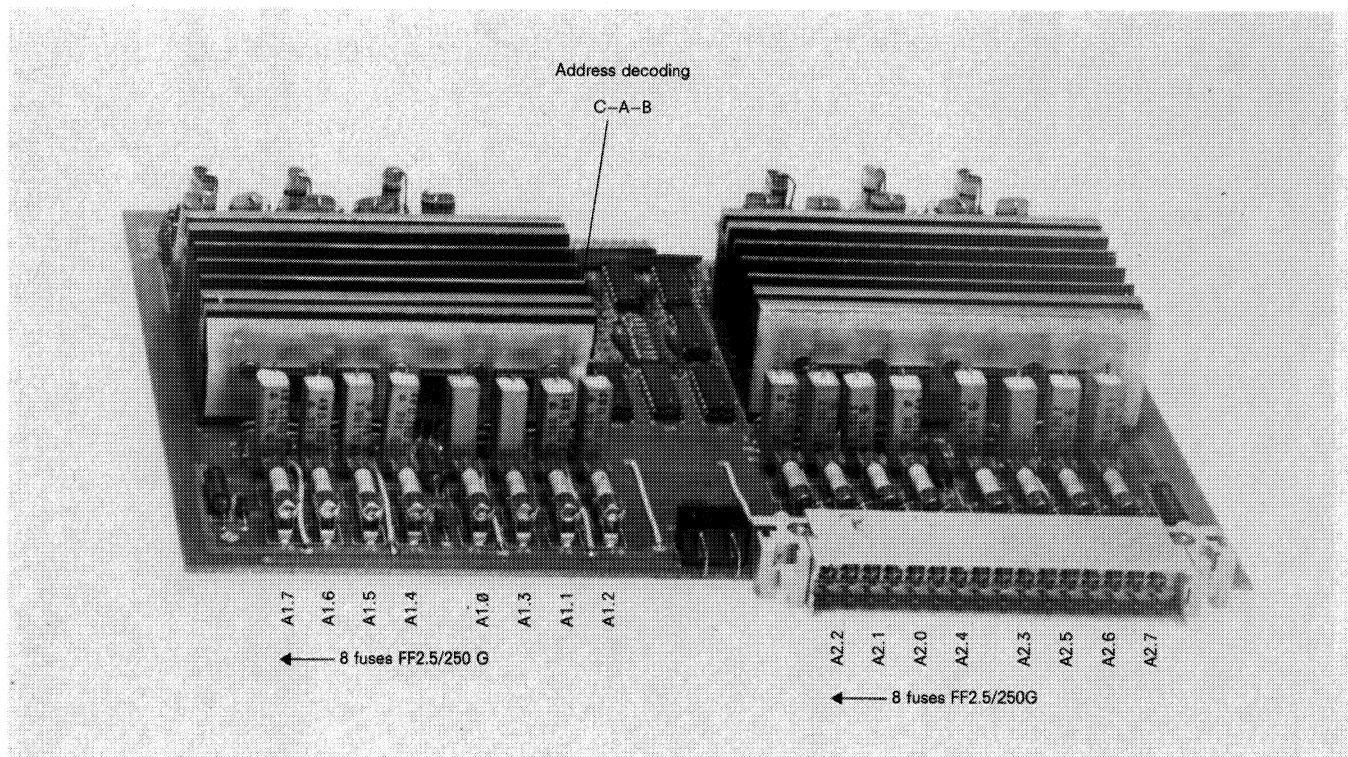
Fig. 28   Jumper assignment and fuses on the output module O AA41

18

3.6 Address decoding

On the I/0 modules there are coding jumpers (soldered jumpers or DIPFIX switches) whose function is to define the addressing range within which the I/0 modules are addressed by the CPU.

S5-010W: Setting the addressing range of the I/0 modules with coding jumpers

Address (decimal)		0	4	8	12	16	20	24	28	32
Input/timer module 6ES5400–0AA11	Z E									
Digital output module 6ES5410–0AA12	A A	2 08		2 08		2 08		2 08		
Digital output module 6ES5410–0AA41	A	2		2		2		2		
Interface module 6ES5772–0AA12	E A									

    2 2 A output   08 0.8 A output

3.7 Assignment of address coding jumpers

Input/timer module 6ES5400–0AA11

Coding jumpers A B C D	Timers	Interrupt inputs	Inputs	
● ● ● ●	00.1...00.4 00.1...00.4	01.0...01.3 01.0...01.3	01.4...05.7 01.4...05.7	hex. dec.
●—● ● ●	08.1...08.4 08.1...08.4	09.0...09.3 09.0...09.3	09.4...0D.7 09.4...13.7	hex. dec.
● ● ●—●	10.1...10.4 16.1...16.4	11.0...11.3 17.0...17.3	11.4...15.7 17.4...21.7	hex. dec.
●—● ●—●	18.1...18.4 24.1...24.4	19.0...19.3 25.0...25.3	19.4...1D.7 25.4...31.7	hex. dec.

Digital output module 6ES5410-0AA11/12

Coding jumpers B A C	2 A outputs	0.8 A outputs	
● ● ●	01.0...01.3 01.0...01.3	02.0...04.7 02.0...04.7	hex. dec.
●—● ●	09.0...09.3 09.0...09.3	0A.0...0C.7 10.0...12.7	hex. dec.
● ●—●	11.0...11.3 17.0...17.3	12.0...14.7 18.0...20.7	hex. dec.
●—●—●	19.0...19.3 25.0...25.3	1A.0...1C.7 26.0...28.7	hex. dec.

Digital output module 6ES5410-0AA41

| Coding jumpers B A C	2 A outputs	
● ● ●	01.0...02.7 01.0...02.7	hex. dec.
●—● ●	09.0...0A.7 09.0...10.7	hex. dec.
● ●—●	11.0...12.7 17.0...18.7	hex. dec.
●—●—●	19.0...1A.7 25.0...26.7	hex. dec.

Interface module 6ES4772-0AA12

DIPFIX switches X1/1 | X1/2 | X1/3 | X1/4				Consecutive No. of S5-010 controller
●⁄● | ●⁄● | ●⁄● | ●⁄●				–
●⁄● | ●⁄● | ●⁄● | ●—●				1
●⁄● | ●⁄● | ●—● | ●⁄●				2
●⁄● | ●⁄● | ●—● | ●—●				3
●—● | ●—● | ●—● | ●—●				15

DIPFIX switches X1/6 | X1/5		Inputs and outputs	
●⁄● | ●⁄●		06.0...07.7 06.0...07.7	hex. dec.
●⁄● | ●—●		0E.0...0F.7 14.0...15.7	hex. dec.
●—● | ●⁄●		16.0...17.7 22.0...23.7	hex. dec.
●—● | ●—●		1E.0...1F.7 30.0...31.7	hex. dec.

4. Maintenance

4.1 Changing the lithium battery
4.2 Testing and troubleshooting

The modules are almost entirely maintenance-free.

4.1 Changing the lithium battery (CPU)

The lithium battery has a life of about 5 years. When the battery needs replacing, the work should always be carried out by a trained person employing the following procedure:

1. Set the mode selector switch to "Stop"
2. Switch off the 24 V power supply
3. Take out the EPROM submodule
4. Disconnect the leads to the CPU
5. Remove the housing cover
6. Take out the CPU
7. Detach the terminal connectors, remove the old battery, fit the new battery, replace the connectors
8. Replace the CPU
9. Replace the housing cover and screw tight
10. Plug in the power supply cable
11. Insert the EPROM submodule
12. Switch on the 24 V power supply
13. Set the mode selector switch to "Run"

It is essential to use the correct type of battery specified.

4.2 Testing and troubleshooting
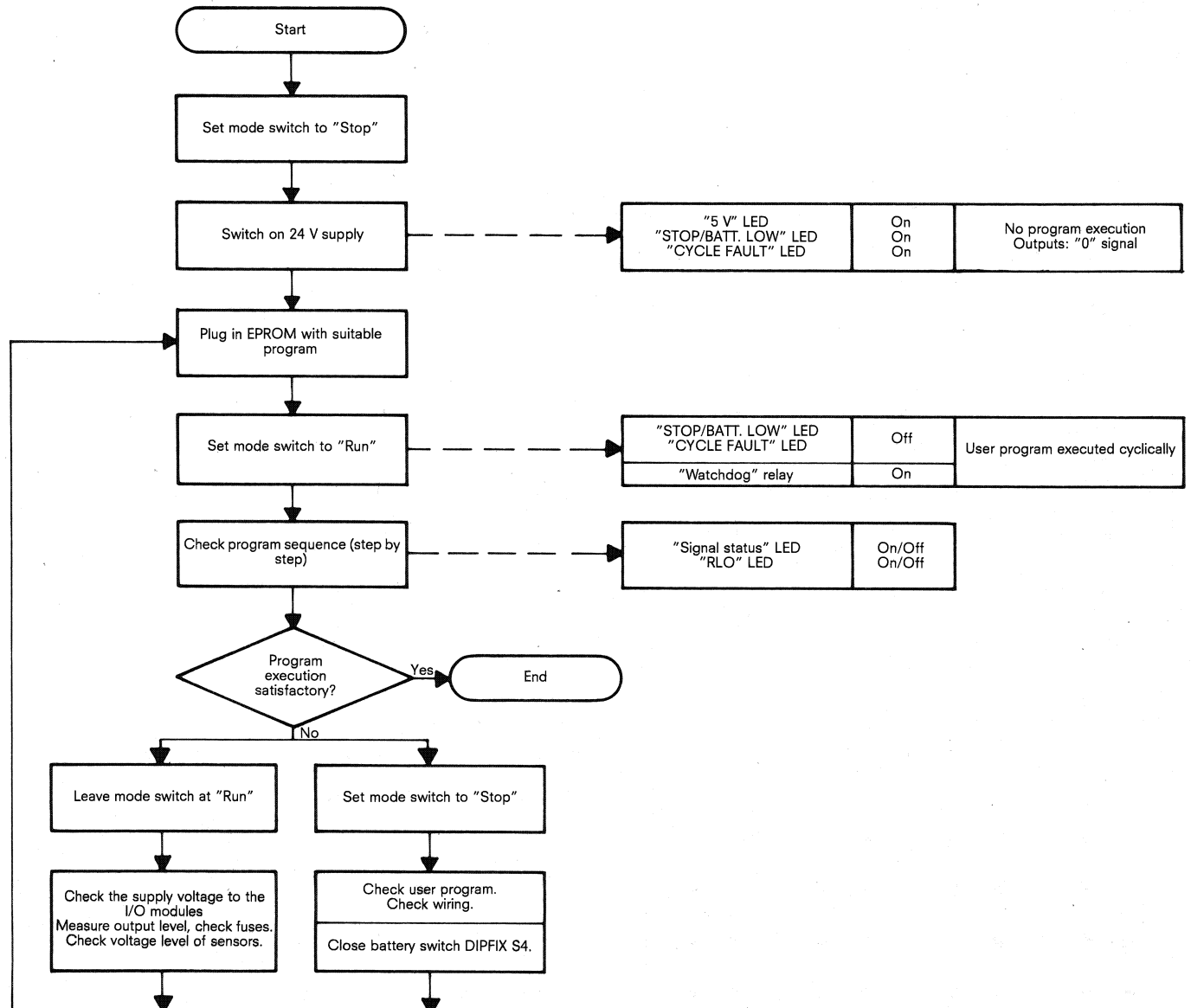
The initial power-up sequence of the PC is as follows:

Fig. 29 Testing and troubleshooting

20

5.1 Pin assignments

S5-010 bus signal assignments

B0...B4	Addressing of blocks
K0...K2	Addressing of inputs and outputs in the selected block
F_P	Enabling of I/0 module outputs
D_{IN}	Signal status of inputs
D_{OUT}	Signal status for setting the outputs
RI	Initializing pulse
IR	Interrupt request, group interrupt signal of relevant input/timer module
M	0 V DC (GND)

Socket connectors

2	unassigned	unassigned	1
4	+5 V	M	3
6	unassigned	unassigned	5
8	IR	RI	7
10	D_{IN}	D_{OUT}	9
12	F_P	B4	11
14	K2	B3	13
16	K1	B2	15
18	K0	B1	17
20	M	B0	19

The pin numbers are marked on the socket connectors.

Front connector pin assignments

The identification of the pins and their geometrical arrangement are shown in Fig. 30.
The correlation between connector pins and input/output addresses (without coding jumpers) is shown in the following tables.

Pin	d	b	z
2	I01.0	I02.0	I03.0
4	I01.1	I02.1	I03.1
6	I01.2	I02.2	I03.2
8	I01.3	I02.3	I03.3
10	I01.4	I02.4	I03.4
12	I01.5	I02.5	I03.5
14	I01.6	I02.6	I03.6
16	I01.7	I02.7	I03.7
18	I04.0	M	I05.0
20	I04.1	———	I05.1
22	I04.2	———	I05.2
24	I04.3	———	I05.3
26	I04.4	———	I05.4
28	I04.5	———	I05.5
30	I04.6	———	I05.6
32	I04.7	M	I05.7

Input/timer module 6ES5 400–0AA11

Pin	d	b	z
2	———	Pext.	Q02.7
4	———	Pext.	Q02.6
6	———	Mext.	Q02.5
8	———	Mext.	Q02.4
10	———	Pext.	Q02.3
12	———	Pext.	Q02.2
14	———	Mext.	Q02.1
16	———	Mext.	Q02.0
18	———	Pext.	Q01.7
20	———	Pext.	Q01.6
22	———	Mext.	Q01.5
24	———	Mext.	Q01.4
26	———	Pext.	Q01.3
28	———	Pext.	Q01.2
30	———	Mext.	Q01.1
32	———	Mext.	Q01.0

Digital output module 6ES5 410–0AA41

z	b	d	
+	+	+	32
+	+	+	30
+	+	+	28
+	+	+	26
+	+	+	24
+	+	+	22
+	+	+	20
+	+	+	18
+	+	+	16
+	+	+	14
+	+	+	12
+	+	+	10
+	+	+	8
+	+	+	6
+	+	+	4
+	+	+	2

Fig. 30 Front connector pin assignments (looking at plug connector)

Pin	d	b	z
2	Q01.0	Q02.0	Q03.0
4	Q01.1	Q02.1	Q03.1
6	Q01.2	Q02.2	Q03.2
8	Q01.3	Q02.3	Q03.3
10	———	Q02.4	Q03.4
12	———	Q02.5	Q03.5
14	———	Q02.6	Q03.6
16	———	Q02.7	Q03.7
18	Q04.0	M	———
20	Q04.1	P24	———
22	Q04.2	P24	———
24	Q04.3	P24	———
26	Q04.4	P24	———
28	Q04.5	P24	———
30	Q04.6	P24	———
32	Q04.7	M	———

Digital output module 6ES5 410–0AA12
0AA22

Pin	d	b	z
2	I0		Q0
4	I1		Q1
6	I2		Q2
8	I3		Q3
10	I4		Q4
12	I5		Q5
14	I6		Q6
16	I7		Q7
18	Bit 0		———
20	Bit 1		———
22	Bit 2		———
24	Bit 3		———
26	H/L byte		———
28			———
30	+24 V		———
32	M_{24}		———

Interface module 6ES5 772–0AA12

5. Appendix

5.2 Memory interface
5.3 Timing

5.2 Memory interface

shown on the plug connector of the memory submodule (looking at the pin side)

		c	b	a
1		$\overline{RI_0}$	0 V	+5 V (V_{cc})
2		A_0	A_1	A_2
3		A_3	A_4	A_5
4		A_6	A_7	A_8
5		A_9	A_{10}	A_{11}
6		PD1	PD2	$\overline{BE}$
7		NOP	VKE	STAT.
8		ZS	$\overline{T_1}$	K6
9		$\overline{FP}$	$\overline{FR}$	STOP
10		0_0	0_1	0_2
11		0_3	0_4	0_5
12		0_6	0_7	K1
13		$\overline{CS1}$	$\overline{RIA}$	K2
14		$\overline{CS2}$	$\overline{TS}$	K3
15		$\overline{T_{ext}}$	unas-signed	K4
16		Vpp	0 V	K5

A_0 to A_{11}	Address bus, bit 0 to 11
0_0 to 0_7	Data bus, bit 0 to 7
$\overline{CS\ 1,\ 2}$	CHIP SELECT. Enabling of first/second EPROM of user memory
PD 1, 2	Programming input of first/second EPROM ("Read" enable)
K1 to K5	Identification for memory capacity (0.5K, 1K or 2K statements)
K6	Battery test pin
VKE	Result of logic operation (RLO)
STAT	Signal status of I/0 modules
$\overline{BE}$	Block end
$\overline{RIA}$	Initializing pulse request
$\overline{TS}$	Stop clock
T_{ext}	External clock
$\overline{T_1}$	Basic clocking of CPU
NOP	No operation (test module: "1" $\triangleq$ NOP)
ZS	Stop address counter
$\overline{FP}$, $\overline{FR}$	Enable I/0 or RAM
$\overline{RI_0}$	Internal initializing pulse
STOP	Scan/Stop ("1" $\triangleq$ Stop)
Vpp	Power supply for readout (+ 5 V) and programming (+25 V) of the EPROMs

---

5.3 Timing

$t_1 \geq 2.5\ \mu s$
$t_2 \leq 19\ \mu s$
$t_3 \geq 4.0\ \mu s$
$t_4 \leq 6.0\ \mu s$
$\Delta \leq 2.0\ \mu s$

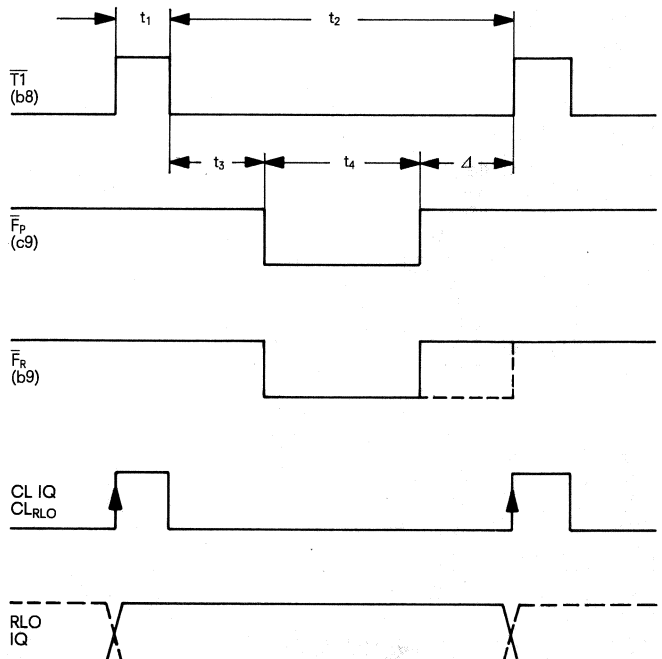|	
$\overline{T1}$	: Basic clock of CPU
F_P	: I/0 enable
F_R	: RAM enable
VKE	: Result of logic operation (RLO)
IQ	: First scan (IQ)
CL_{RLO}	: Clock pulse for RLO
CL_{EA}	: Clock pulse for first scan

Fig. 31 Timing

5.4 S5–010 machine code

| | S5-010 machine code | | | | | | | | | | | | | | | | Control signals | | | | | |
Oper-ation	Type C7	IQ/F C6	NEG. C5	C4	C3	K2 C2	K1 C1	K0 C0	I/Q B7	B6	B5	B4	B3	B2	B1	B0	Enable I/O FP	RAM FR	Clock First scan CL IQ	RLO CL RLO	First scan (IQ)	RLO
AI	1	1	0	0	0				0												0	
OI	1	1	0	0	1				0												0	
ANI	1	1	1	0	0				0												0	
ONI	1	1	1	0	1				0												0	
AQ	1	1	0	0	0	Pin address within a block			1	Block address 1st character			Block address 2nd character								0	
OQ	1	1	0	0	1				1												0	Program-dependent
ANQ	1	1	1	0	0				1												0	
ONQ	1	1	1	0	1				1												0	
AF	1	0	0	0	0				0												0	
OF	1	0	0	0	1				0												0	
ANF	1	0	1	0	0				0												0	
ONF	1	0	1	0	1				0												0	
SQ	1	1	0	1	0				1												1	
RQ	1	1	1	1	0				1												1	
= Q	1	1	0	1	1				1												1	
SF	1	0	0	1	0				0												1	
RF	1	0	1	1	0				0												1	
=F	1	0	0	1	1				0												1	
AF 0.0	1	0	0	0	0	0	0	0	0												No effect	No effect
NOP1	1	1	1	1	1	1	1	1	1													
NOP0	0	0	0	0	0	0	0	0	0													
BE	0	1	1	0	0	1	0	1	0												1	
BEC	0	0	0	0	0	1	0	1	0												1	

6. Spare parts

	Order No.	Weight approx. kg
Empty housing with 4 module locations	6ES5710-0AB11	2.7
Empty housing with 6 module locations	6ES5710-0AB21	3.2
Empty housing with 8 module locations	6ES5710-0AB31	4.3
Central processing unit with service panel and receptacle for EPROM submodule	6ES5900-0AA12	0.42
Memory submodule with sockets for 2K EPROM (without EPROM)	6ES5910-0AA01	
Memory submodule with EPROM for 1K statements	6ES5910-0AA21	0.04
Memory submodule with EPROM for 2K statements	6ES5910-0AA31	
Memory submodule with EPROM for 4K statements	6ES5910-0AA41	
Input/timer module 40 inputs, 24 V and 4 analog timers	6ES5400-0AA11	0.3
Digital output module, 24 V DC 24 outputs 0.8 A (current-limited) 4 outputs 2.0 A	6ES5410-0AA12	0.5
12 outputs 0.8 A (current-limited) 4 outputs 2.0 A	6ES5410-0AA22	
Digital output module, 24 V DC 16 outputs 2.0 A	6ES5410-0AA41	0.75
Interfacing module, 24 V DC 16 inputs 16 outputs	6ES5772-0AA12	0.3
Programming unit 610	6ES5610-8CA11	
Programming unit 630	6ES5630-0CA21	
Programming unit 631	6ES5631-0AA21	15
Programming unit 670	6ES5670-0CA21	27
Programming unit interface module 500 for on-line operation	6ES5500-7AA11	0.4
Lithium battery	6ES5980-0AD41	

	Order No.	Weight approx. kg
Fuses for output modules 0AA41 0AA12 FF2.5/250G	261 131	
SIEMENS connectors for I/0 modules		
Connector A with locking latches for round cables flat ribbon cables	6XX3 014 6XX3 015	
Connector B with locking latches Width 15 mm Width 20 mm	6XX3 010 6XX3 012	
Insert for round cables dia. 11.5 mm dia. 16 mm	6XX3 048 6XX3 050	
Insert for flat ribbon cables	6XX3 051	
Socket connector model F for crimped connections, 48-way	6XX3 016	
Crimp snap-in contacts for wire cross-sections of 0.09–0.15 mm^2 0.14–0.5 mm^2 0.75–1.5 mm^2	6XX3 031 6XX3 032 6XX3 033	
Socket connector model F for manually soldered connections, 48-way	6XX3 103	
HARTING connectors for I/0 modules		
Connector shell (wide)	09060480504	
Latching bar left right	09060009913 09060009919	
Latching element left right	09060009907 9908	
Insulator for crimped connections	0483201	
Socket contacts for crimping Round wire 0.14–0.5 mm^2 Round wire 0.75–1.5 mm^2	0006421 0006431	
Operator's Manual for S5-010W programmable controllers		
in German	6ES5998-0CA11	
in English	6ES5998-0CA21	
in French	6ES5998-0CA31	

SIEMENS-Bauteile-Service
Postfach 146, 8510 Fürth
Tel. (09 11) 30 01-1

Fa. Harting
Postfach 104
4992 Espelkamp