SIEMENS

TELEPERM M

AS 235 H
Automation System

ES 100 K
Extension System

Manual

Bestell-Nr. C79000-G8076-C293-07

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

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Order No. C79000–G8076–C293
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Register Contents

"Important Notes, Information, Suggestions/Corrections"

CE Labeling	"Notes on the CE Symbol for TELEPERM M AS" C79000-Q8076-C001-03
Guidelines	"Instructions and Guidelines for Planning, Installation and Operation of TELEPERM M Systems" Reference to the Guidelines Manual (with brief summary) for the TELEPERM M range C79000-D8076-C411-01
Safety-Related Guidelines	"Safety-Related Guidelines for the User" Summary of the safety-related aspects during operation of TELEPERM M systems C79000-D8076-C402-04
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Suggestions/ Corrections	"Suggestions/Corrections for Document/Manual" A return sheet for suggestions of improvement is enclosed. C79000-D8075-C404-08

Notes on the CE Symbol for TELEPERM M AS

EC Directive EMC

The following applies to the TELEPERM M products described in this manual:

89/336/EEC

Products which carry the CE symbol fulfil the requirements for the EC Directive 89/336/EEC.

The EC declaration of conformity and the documentation relating to this are available to the authorities concerned, according to the above–mentioned EC Directive, Article 10 (2), from:

CE

Siemens AG
Automation & Drives Group
A&D SE S21 S
Siemensallee 84
D–76187 Karlsruhe

Products which do not have the CE symbol meet the requirements and standards given in the System Manuals under ”General Technical Data”.

Fields of Application

For the TELEPERM M System, the following field of application apply according to this CE symbol:

Field of Application	**Requirement for**	
	Emitted interference	**Noise immunity**
Industry	EN 50081–2:1993	EN 50082–2:1995

Observing the Setup Guidelines

The setup guidelines and notes on safety given in the System Manuals must be observed during startup and when operating the TELEPERM M System.

Working on Cabinets

To protect the modules from the static electricity, the user must discharge his body’s electrostatic charge before opening cabinets.
Observe the general ESD Guidelines.

Notes on the CE Symbol for TELEPERM M AS

Notes on Manual–Auto Stations

A filter must be inserted in the power supply lines (SIFI C, B84113–C–B30 or similar).

Updated Technical Data

In addition to the specifications in the ”General Technical Data” of the System Manuals, the specifications on noise immunity and electromagnetic compatibility given below apply to modules carrying the CE symbol.

The specifications are valid for systems which are assembled according to the above–mentioned setup guidelines.

Electromagnetic Compatibility (EMC)

Radio interference suppression to EN 55011	
Limit value class	A [1]
Interference by conduction on AC and DC supply lines to EN 61000–4–4 / IEC 1000–4–4 (Burst)	2 kV
Interference by conduction on signal lines to EN 61000–4–4 / IEC 1000–4–4 (Burst)	2 kV
Interference by conduction on process lines to EN 61000–4–4 / IEC 1000–4–4 (Burst)	2 kV
Noise immunity to discharges of static electricity to EN 61000–4–2 / IEC 1000–4–2 (ESD)	4 kV [2]
Noise immunity to electromagnetic HF field [1] amplitude modulated to ENV 50140 / IEC 1000–4–3	80 to 1000 MHz 10 V/m 80 % AM (1 kHz)
Noise immunity to electromagnetic HF field [1] pulse modulated to ENV 50204	900 MHz 10 V/m 50 % c.d.f.
Noise immunity to high frequency (sinusoidal) to ENV 50141	0.15 to 80 MHz 10 V 80 % AM

1) With closed doors for AS 235 and AS 235 H, open for AS 235 K and ES 100 K

2) With AS 235 K and ES 100 K: 6 kV

Instructions and Guidelines for Planning, Installation and Operation of TELEPERM M Systems

Installation/operation

A summary of the basic requirements, ambient conditions and instructions for installing and operating TELEPERM M systems is contained in a separate Manual for the entire TELEPERM M range.
Title of the manual
"TELEPERM M
"Instructions and Guidelines for Planning, Installation, and Operation"

Manual contents

The manual deals with the following topics:

- Safety-related guidelines
- ESD guidelines
- Room planning and furnishing
- Installation instructions
- Mains and environmental requirements
- Data carriers
- Operation licenses
- Configuration instructions
- Mounting instructions
- Thermal load of the cabinet
- CS 275 bus system
- Surge protection
- Standards, directives, regulations

Manual directives

The manual is intended to be used by planning and configuring engineers, installation personnel and users of TELEPERM M systems.
It has to be taken into account during planning and commissioning.

Order No.

C79000-G8076-C417

TELEPERM M/ME
Safety-Related Guidelines for the User

1 General

This manual provides the information required for the intended use of the particular product. The documentation is written for technically qualified personnel such as engineers, programmers or maintenance specialists who have been specially trained and who have the specialized knowledge required in the field of instrumentation and control., called automation in the following.

A knowledge of the safety instructions and warnings contained in this manual and their appropriate application are prerequisites for safe installation, commissioning and maintenance as well as safe and proper operation of the product described. Only qualified personnel as defined in section 2 have the specialized knowledge that is necessary to correctly interpret the general danger notices and warnings contained in this documentation and implement them in each particular case.

This manual is an inherent part of the scope of supply even if, for logistic reasons, it has to be ordered separately. For the sake of clarity, not all details of all versions of the product are described in the documentation, nor can it cover all conceivable cases regarding installation, operation and maintenance. Should you require further information or face special problems that have not been dealt with in sufficient detail in this documentation, please contact your local Siemens office.

We would also point out that the contents of this product documentation shall not become a part of or modify any prior or existing agreement, commitment or legal relationship. The Purchase Agreement contains the complete and exclusive obligations of Siemens. Any statements contained in this documentation do not create new warranties or restrict the existing warranty.

2 Qualified Personnel

Persons who are **not qualified** should not be allowed to handle the equipment/system. Non-compliance with the warnings contained in this manual or appearing on the equipment itself can result in severe personal injury or damage to property. Only **qualified personnel** should be allowed to work on this equipment/system.

Qualified persons as referred to in the safety guidelines in this manual as well as on the product itself are defined as follows:

- System planning and design engineers who are familiar with the safety concepts of automation equipment;
- Operating personnel who have been trained to work with automation equipment and are conversant with the contents of the manual in as far as it is connected with the actual operation of the plant;
- Commissioning and service personnel who are trained to repair such automation equipment and who are authorized to energize, deenergize, clear, ground and tag circuits, equipment and systems in accordance with established safety practices.

3 Danger Notices

The notices and guidelines that follow are intended to ensure personal safety, as well as protecting the product and connected equipment against damage.

The safety notices and warnings for protection against loss of life (the users or service personnel) or for protection against damage to property are highlighted in this manual by the terms and pictograms defined here. The terms used in this manual and marked on the equipment itself have the following significance:

Danger

indicates that death, severe personal injury or substantial property damage **will** result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage **can** result if proper precautions are not taken.

Caution

indicates that minor personal injury or property damage **can** result if proper precautions are not taken.

Note

is an important information about the product, its operation or a part of the manual to which special attention is drawn.

Important

If in this manual "Important" should appear in bold type, drawing attention to any particularly information, the definition corresponds to that of "Warning", "Caution" or "Note".

4 Proper Usage

- The equipment/system or the system components may only be used for the applications described in the catalog or the manual, and only in combination with the equipment, components and devices of other manufacturers as far as this is recommended or permitted by Siemens.
- The product described has been developed, manufactured, tested and the documentation compiled in keeping with the relevant safety standards. Consequently, if the described handling instructions and safety guidelines described for planning, installation, proper operation and maintenance are adhered to, the product, under normal conditions, will not be a source of danger to property or life.

Warning

- After opening the housing or the protective cover or after opening the system cabinet, certain parts of this equipment/system will be accessible, which could have a dangerously high voltage level.
- Only suitably qualified personnel should be allowed access to this equipment/system.
- These persons must be fully conversant with any potential sources of danger and maintenance measures as set out in the instructions contained in this manual.
- It is assumed that this product be transported, stored and installed as intended, and maintained and operated with care to ensure that the product functions correctly and safely.

5 Guidelines for the Planning and Installation of the Product

The product generally forms a part of larger systems or plants. These guidelines are intended to help integrate the product into its environment without it constituting a source of danger.
The following facts require particular attention:

Note

Even when a high degree of safety-related reliability has been designed into an item of automation equipment by means of multichannel configuration, it is still imperative that the instructions contained in this manual be exactly adhered to. Incorrect handling can render ineffective the preventive measures incorporated into the system to protect it against dangerous process states, and even create new sources of danger.

The following advice regarding installation and commissioning of the product should - in specific cases - also be noted.

Warning

- Follow strictly the safety and accident prevention rules that apply in each particular case.
- Units which are designed as built-in units may only be operated as such, and table-mounted or portable equipment only with its casing closed.
- In the case of equipment with a permanent power connection which is not provided with an isolating switch and/or fuses which disconnect all poles, a suitable isolating switch or fuses must be provided in the building wiring system (distribution board). Furthermore, the equipment must be connected to a protective ground (PE) conductor.
- For equipment or systems with a fixed connecting cable but no isolating switch which disconnects all poles, the power socket with the grounding pin must be installed close to the unit and must be easily accessible.
- Before switching on the equipment, make sure that the voltage range setting on the equipment corresponds to the local power system voltage.
- In the case of equipment operating on 24 V DC, use an extra-low voltage with a protective separation with the mains supply. The protective separation has to comply with the following requirements:
  - VDE 0100 Part 410 ≙ HD 384-4-41 ≙ IEC 364-4-41 (as function extra-low voltage with protective separation) or
  - VDE 0805 ≙ EN 60950 ≙ IEC 950 (as a safety extra-low voltage SELV) or
  - VDE 0106 Part 101.
- The I/O modules are designed for operation with safety extra-low voltage acc. to IEC 950 / EN 60950/VDE 0805. Therefore only components whose connection points are separated in a safe manner (by means of the protective measure "Protective separation") from voltages (e.g. mains) may be connected to the inputs/outputs of these modules.
- Fluctuations or deviations of the power supply voltage from the rated value should not exceed the tolerances specified in the technical specifications. Otherwise, functional failures or dangerous conditions can occur in the electronic modules/equipment.
- Suitable measures must be taken to make sure that programs that are interrupted by a voltage dip or power supply failure resume proper operation when the power supply is restored. Care must be taken to ensure that dangerous operating conditions do not occur even momentarily. If necessary, the equipment must be forced into the "emergency off" state.
- Emergency tripping devices in accordance with EN 60204/IEC 204 (VDE 0113) must be effective in all operating modes of the automation equipment. Resetting the emergency off device must not result in any uncontrolled or undefined restart of the equipment.

Caution

- Install the power supply and signal cables in such a manner as to prevent inductive and capacitive interference voltages from affecting the automation functions.
- Automation equipment and its operating elements must be installed in such a manner as to prevent unintentional operation.
- Automation equipment can assume an undefined state in the case of a wire break in the signal lines. To prevent this, suitable hardware and software measures must be taken when interfacing the inputs and outputs of the automation equipment.

6 Active and Passive Faults in Automation Equipment

- Depending on the particular task for which the electronic automation equipment is used, both **active** as well as **passive** faults can result in a **dangerous** situation. For example, in actuator control (e.g. press control), an active fault is generally dangerous because it can result in an unauthorized startup of the actuator. On the other hand, a passive fault in a signalling function (alarm signalling system) can result in a dangerous, command-blocking operating state not being reported to the operator.
- This differentiation of the possible faults and their classification into dangerous and non-dangerous faults, depending on the particular task, is important for all safety considerations in respect of the product supplied and the its interaction with the process to be controlled.

Warning

In all cases where a fault in an automation equipment can result in severe personal injury or substantial damage to property, ie. where a dangerous fault can occur, safety-related and fail-safe systems (in general prototype-tested by the German Technical Inspectorate (TÜV)) must be used or additional external measures be taken or equipment provided to ensure or force safe operating conditions even in the event of a fault (e.g. by means of independent limit monitors, mechanical interlocks etc.).

7 Procedures for Maintenance and Repair

If measurement or testing work is to be carried out on an active unit, the rules and regulations contained in the "VBG 4.0 Accident prevention regulations" of the German employers liability assurance association (Berufsgenossenschaften) must be observed. Particular attention is drawn to paragraph 8 "Permissible exceptions when working on live parts". Use only suitable electrical tools.

Warning

- Repairs to an item of automation equipment may only be carried out by **Siemens service personnel** or **an authorized Siemens repair center.** For replacement purposes, use only parts or components that are contained in the spare parts list or listed in the "Spare parts" section of this manual. Unauthorized opening of equipment and improper repairs can result in loss of life or severe personal injury as well as substantial property damage
- Before opening the equipment, always remove the power plug or open the disconnecting switch.
- Only use the fuse types specified in the technical specifications or the maintenance instructions of this manual.
- Do not throw batteries into an open fire and do not carry out any soldering work on batteries (danger of explosion). Maximum ambient temperature 100°C. Lithium batteries or batteries containing mercury should not be opened or recharged. Make sure that the same type is used when replacing batteries.
- Batteries and accumulators must be disposed of as classified waste.
- The following points require attention when using monitors:
  Improper handling, especially the readjustment of the high voltage or fitting of another tube type can result in excessive X-ray radiation from the unit. The license to operate such a modified unit automatically lapses and the unit must not be operated at all.

Guidelines for Handling Electrostatically Sensitive Devices (ESD)

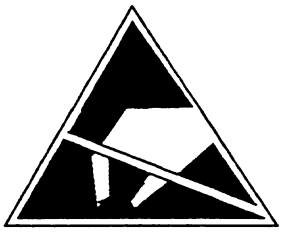
1 What is ESD?

VSLI chips (MOS technology) are used in practically all SIMATIC S5 and TELEPERM M modules. These VLSI components are, by their nature, very sensitive to overvoltages and thus to electrostatic discharge:

They are therefore defined as
"Electrostatically Sensitive Devices"

"ESD" is the abbreviation used internationally.

The following warning label on the cabinets, subracks and packing indicates that electrostatically sensitive components have been used and that the modules concerned are susceptible to touch:



ESDs can be destroyed by voltage and energy levels which are far below the level perceptible to human beings. Such voltages already occur when a component or a module is touched by a person who has not been electrostatically discharged. Components which have been subjected to such overvoltages cannot, in most cases, be immediately detected as faulty; the fault occurs only after a long period in operation.

An electrostatic discharge
- of 3500 V can be felt
- of 4500 V can be heard
- must take place at a minimum of 5000 V to be seen.

But just a fraction of this voltage can already damage or destroy an electronic component.

The typical data of a component can suffer due to damage, overstressing or weakening caused by electrostatic discharge; this can result in temporary fault behavior, e.g. in the case of
- temperature variations,
- mechanical shocks,
- vibrations,
- change of load.

Only the consequent use of protective equipment and careful observance of the precautions for handling such components can effectively prevent functional disturbances and failures of ESD modules.

2 When is a Static Charge Formed?

One can never be sure whether the human body or the material and tools which one is using are not electrostatically charged.

Small charges of 100 V are very common; these can, however, very quickly rise up to 35 000 V.

Examples of static charge:

– Walking on a carpet	up to 35 000 V
– Walking on a PVC flooring	up to 12 000 V
– Sitting on a cushioned chair	up to 18 000 V
– Plastic desoldering unit	up to 8 000 V
– Plastic coffee cup	up to 5 000 V
– Plastic bags	up to 5 000 V
– Books, etc. with a plastic binding	up to 8 000 V

3 Important Protective Measures against Static Charge

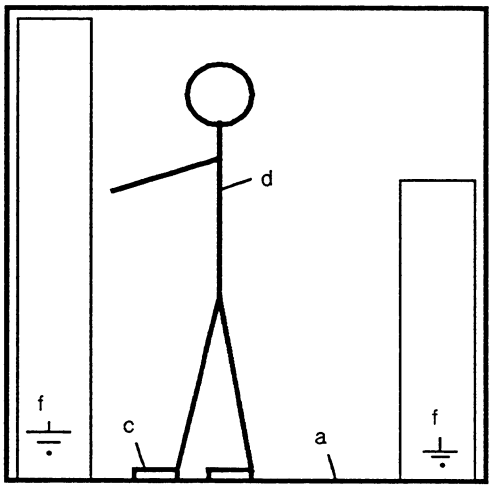
- Most plastic materials are highly susceptible to static charge and must therefore be kept as far away as possible from ESDs.
- Personnel who handle ESDs, the work table and the packing must all be carefully grounded.

4 Handling of ESD Modules

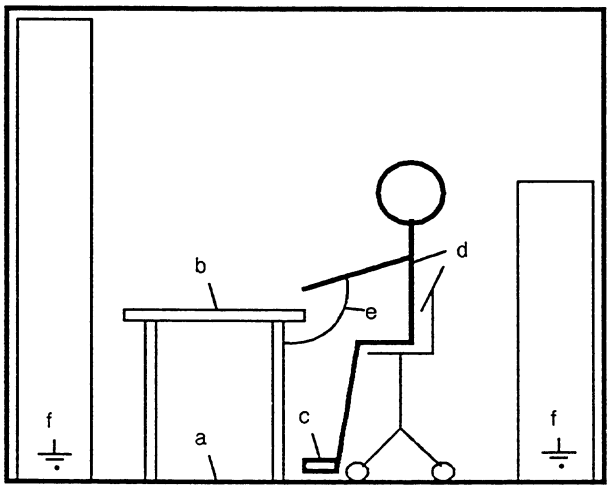
- One basic rule to be observed is that electronic modules should be touched by hand only if this is necessary for any work required to be done on them. Do not touch the component pins or the conductors.
- Touch components only if
  - the person is grounded at all times by means of a wrist strap

  or
  - the person is wearing special anti-static shoes or shoes with a grounding strip.
- Before touching an electronic module, the person concerned must ensure that (s)he is not carrying any static charge. The simplest way is to touch a conductive, grounded item of equipment (e.g. a blank metallic cabinet part, water pipe, etc.) before touching the module.
- Modules should not be brought into contact with insulating materials or materials which take up a static charge, e.g. plastic foil, insulating table tops, synthetic clothing, etc.
- Modules should only be placed on conductive surfaces (table with anti-static table top, conductive foam material, anti-static plastic bag, anti-static transport container).
- Modules should not be placed in the vicinity of monitors, TV sets (minimum distance from screen > 10 cm).

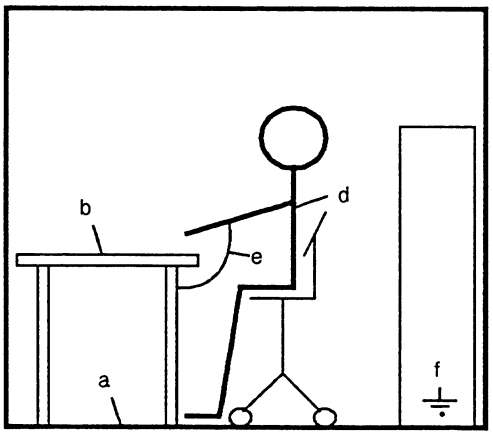
The diagram below shows the required protective measures against electrostatic discharge.



Standing position



Standing/sitting position



Sitting position

a Conductive flooring
b Anti-static table
c Anti-static shoes
d Anti-static coat
e Grounding wrist strap
f Grounding connection of the cabinets

5 Measurements and Modification to ESD Modules

- Measurements on modules may only be carried out under the following conditions:
  - The measuring equipment is grounded (e.g. via the PE conductor of the power supply system) or
  - when electrically isolated measuring equipment is used, the probe must be discharged (e.g. by touching the metallic casing of the equipment) before beginning measurements.
- Only grounded soldering irons may be used.

6 Shipping of ESD Modules

Anti-static packing material must always be used for modules and components, e.g. metalized plastic boxes, metal boxes, etc. for storing and dispatch of modules and components.

If the container itself is not conductive, the modules must be wrapped in a conductive material such as conductive foam, anti-static plastic bag, aluminium foil or paper. Normal plastic bags or foils should not be used under any circumstances.

For modules with built-in batteries ensure that the conductive packing does not touch or short-circuit the battery connections; if necessary cover the connections with insulating tape or material.

Vorschläge Korrekturen
Suggestions Corrections
Propositions Corrections
Propuestas Correcciones

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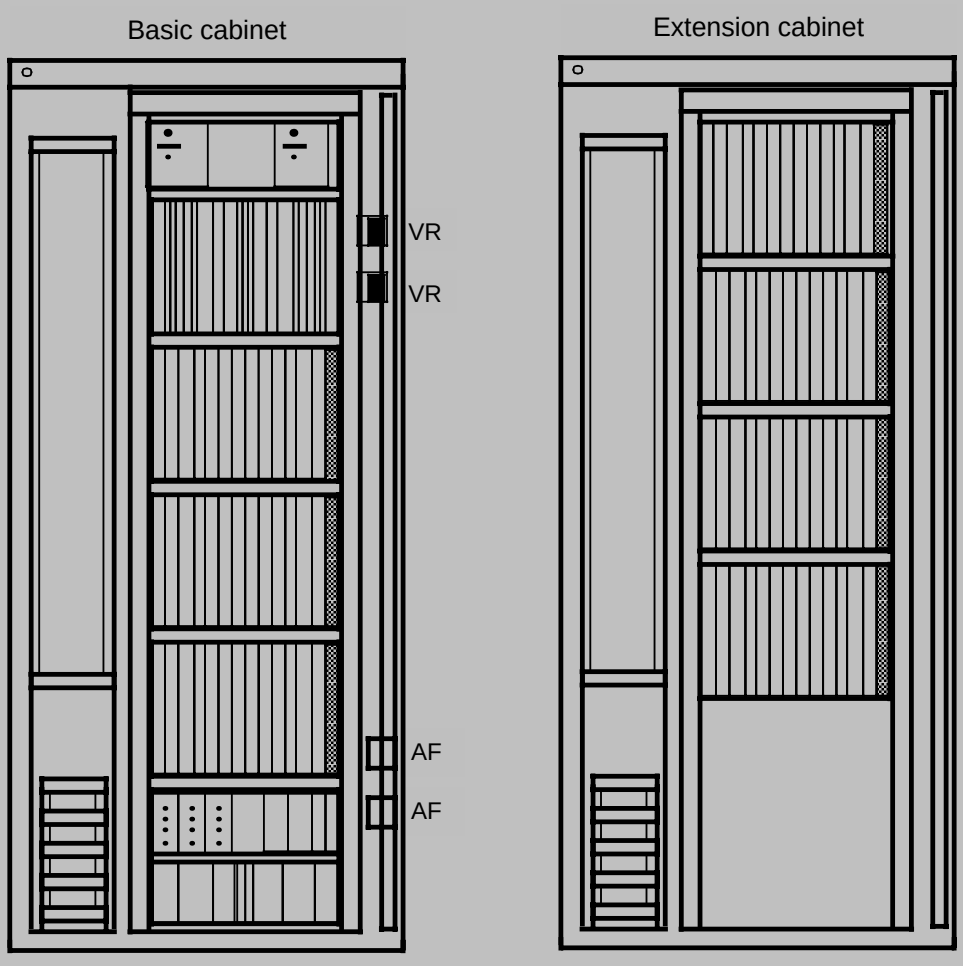
SIEMENS

TELEPERM M

AS 235 H Automation System

Instructions **C79000-B8076-C293-05**



Contents

Preface

The seven chapters of these Instructions provide the information required for safe and smooth operation of the **AS 235 H** automation system.

Chapter 1 shows possible **applications** and the features of the system.

Chapter 2 provides an overview of the **design** and possible system extensions.

Chapter 3 explains the **method of operation** and the system and its components.

Chapter 4 informs you about **installation** work and installation requirements to be met.

Chapter 5 specifies **commissioning**.

Chapter 6 deals with **maintenance**.

Chapter 7 summarizes the **technical data**.

First of all, read the **Safety-related Guidelines for the User**. You find these Instructions in this Manual in the Section before Register 1.

You also find the **Guidelines for Handling Electrostatically Sensitive Devices** in that Section. Reading these instructions carefully helps you to prevent personal injury and damages to the equipment before and during operation.

Abbreviations

I II	Identification numbers (Roman numerals) of the redundant subsystems (redundancies) within a multi-redundant system.
AA	Analog output module
ABE	Interrupt generating binary signal input module
AE	Analog input module
AF	Remote bus connector board
AS	Automation system
ASG	Interrupt generating signal transmitters
AZR	Flag register of the CPU 235 H
B	Backup (CPU status = synchronization and updating)
BA	Binary output module
B&B	Operator control and monitoring
BE	Binary input module
BGT	Subrack
BKA	Operator input channel interface module
BKU	Operator input channel switchover (video relay and adapter cable with AS 235 H)
BL	Blinking clock-pulse generator module
CS 275	LAN for linking TELEPERM M systems
CPU 235 H	Central processing unit 235 H
DG	Diagnostic unit
DGA	Diagnostic unit interface module
DMA	Direct memory access
DS	Data save (protective signal for memory modules)
E/A	Input and output (I/O)
EABA	I/O bus interface module
EE	Extension unit
EANK	One-out-of-n code; TELEPERM M procedure for detecting I/O addresses with no or multiple assignments
ES	Extension cabinet
EAVU	I/O comparator and switchover module
EPDL	Erasable programmable logic device
EPROM	Ultraviolet erasable programmable read-only memory
F	Failure (CPU mode)
F	Fail-safe (by redundancy)
FDC	Floppy-disk controller
FIFO	First in first out (queuing or handling hierarchy)
GE	Basic unit
GS	Basic cabinet
H	Fault-tolerant (by redundancy)
HF	H and F in compatible combination
LAN	Local area network; mid-range communications bus
L+	Positive supply voltage, 24 V rated value
LBG	Fan module
LED	Light emitting diode
LOES	Clearing the user memory by entering the keyboard command "LOES;"
LTM	I&C alarm

M	Earth, negative pole
M	Master (CPU mode)
MDA	Mini floppy disk interface module
MDE	Mini floppy disk unit
MDR	Event recorder
MDT	Mean downtime (mean time between the occurrence of a failure and operation restart)
ML	Alarm logic module
MTBF	Mean time between failures (mean time between two failure occurrences, i.e. faultless interval)
MtU	Technical document to be supplied with the system
MZ	Off-load earth, reference potential for analog inputs
N-AS	Local bus interface module for AS, new development, replaces N8-H
N8	TELEPERM M local bus interface, 8 bits on CS275 bus system
N8-H	N8 in a fault-tolerant 1-out-of-2 master/reserve configuration of a redundant automation system
NAU	Power failure
NV	Local bus distributor
OS	Operator control and monitoring system
P	Passive (asynchronous CPU status; no N8-H access etc.)
PBE	Testable binary input module
PBT	Process communication keyboard (TELEPERM M AS accessory)
PDR	Logging printer
PE	Protective earth, cabinet potential
PESP	Peripheral memory area
PUM	Buffer module
PRA	Testable relay output module
PROM	Programmable read-only memory
PM	L+ for alarm purposes
PS	L+ for logic "1" of 24-V inputs
PÜ	L+ for monitoring purposes
PU	Process interrupt
PU5	Standard: unassigned process interrupt No. 5 (PU5) which is exclusively used for redundancy-related purposes
QVZ	Time-out during memory or peripheral access
R	Standby (CPU mode)
RAM	Random access memory
RDY	Ready
ROM	Read-only memory
RSOF	Software reset
SAE	Cabinet connection element
SB	Synchronization module
SED31	Cabinet power supply diode
SEP	Standard slot in a subrack, 15.24 mm wide
SES	Cabinet power supply unit
SF	Signal interface module
SF61	Signal interface module in slot address 61 (mnemonic name for a group interrupt module in this slot; 48-bit binary input module)

SP	Memory module
STA	Starting block processing (keyboard input = STA)
STO	Halting block processing (keyboard input = STO)
SV	Power supply module
SVE	Power supply unit
SVME	Power supply unit for extension unit
SW	Software
TM	TELEPERM M
UI	Inductive bus converter unit for CS275
VD 11	Logic diode module for messages
VKB	Comparator coupler module
VR	Video relay
ZE	Central processing unit
ZEP	Central grounding point
ZRS	Central reset
ZT	Central unit (with AS 235 H containing two redundant CPUs)

1 Application

The new AS 235 H automation system is an enhancement of the 235 product family which satisfies particularly high requirements in the field of process control.

The AS 235 standard system is supplemented by a fault-tolerant and highly available variant.

H for "high availability"

The H in AS 235 H signals a higher availability than exists in a normal standard system.

This system has a redundant structure which enables the user to continue process manipulation and control tasks even after a tolerable fault has occurred.

The present system is a "1-out-of-2 system" whose availability is significantly increased by a redundant CPU configuration. Dedicated fault delimitation yields a high degree of non-interaction, this means that a solitary fault cannot be propagated from one subsystem to another. User-specific configuration enables a multiple redundant structure of the I/O system to be established which utilizes the given redundancy and permits easier execution of process tasks.

Warning:

The AS 235 H automation system (H system) is **not** a fail-safe system, despite its higher availability, its fault-tolerance and its non-interacting structure. It may **not** be used in plants where AS faults (e.g. the (unlikely) total failure of both CPUs) could cause hazardous conditions for persons, machinery or environment.
Such safety-relevant automation tasks require the use of either a fail-safe automation system (such as an F or HF system that has been prototype-tested by the German Technical Inspectorate) or an AS 235 H system equipped with suitable interlocking circuits and protective systems which safely prevent the occurrence of hazardous conditions.

Notes

 C79000-B8076-C293-05

2 Design

The AS 235 H standard configuration consists of the basic cabinet with one 1-tier and up to five 2-tier subracks. These subracks contain the power supply unit for the basic unit, both central processing units, up to three extension units, and the cabinet power supply unit.

One extension cabinet with up to four 2-tier subracks may be connected in addition. The subracks contain extension units.

Two operation units, each with color monitor, keyboards (process communication keyboard and**/**or configuring keyboard) and two printers (logging printer**/**event recorder), may be connected to the system.

The ES 100 K extension system provides further extension possibilities.
(Please refer to Chapter 4.7.6 for corresponding configuration suggestions.)

2.1 Cabinet

The AS 235 H automation system is installed in an AS 235 standard cabinet. Like the standard version, this cabinet is available with or without forced ventilation.

- Basic cabinet (GS)

The basic cabinet has the following structure (from top to bottom):

Power supply unit (SVE)

- one 24-V buffer module (internal 2-channel structure)
- two 5-V power supply modules (supply one CPU each)

Basic unit (fully equipped)

- one comparator coupler module (for both CPUs)
- two synchronization modules
- two diagnostic unit interface modules (option) [1)]
- two memory modules
- two central processor units (CPU 235 H)
- four I/O bus interface modules (2 as an option)
- four operator input channel interface modules (2 as an option)
- two mini floppy disk interface modules [2)]
- two N-AS or N8-H local bus interface modules (option) [3)]

Up to three extension units, each with

- one I/O comparator and switchover module
- up to 13 I/O modules [4)]

Cabinet power supply

- 24 circuit breakers
- three alarm logic modules (ML) (the third module is only required if an ES is connected)
- two VD11 diode modules (option)
- two SED31 power diode modules
- two UI bus converter units (option)
- one blinking clock-pulse generator
- two socket outlet tiers (connectors for up to four keyboards and two MDEs)

- Extension cabinet (ES)

Up to four extension units (EE), each with

- one I/O comparator and switchover module
- up to 13 I/O modules

Caution:

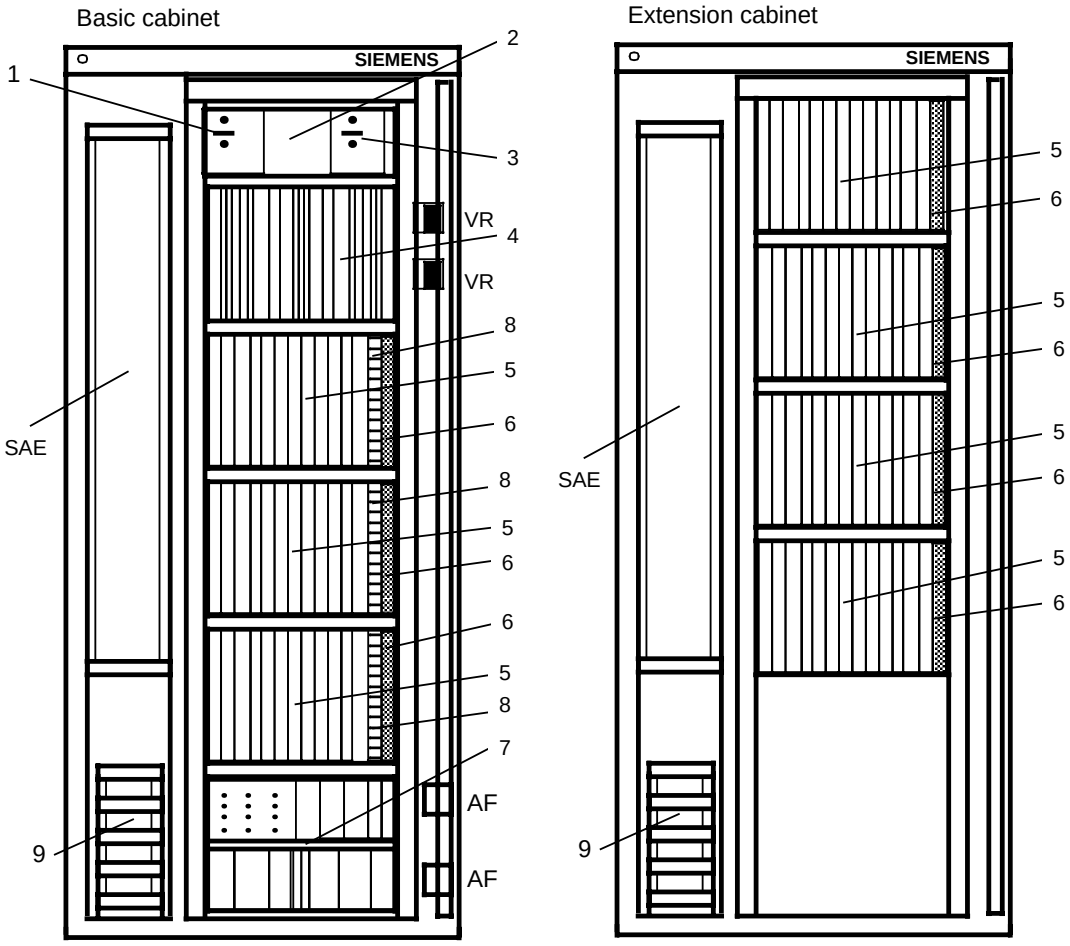
CPU 235 H (6DS1 141-8AA) may **not** be replaced by CPU 235 (6DS1140-8AA).

1) Only one module may be used in normal redundancy mode.
Caution: If there is no diagnostic interface module the module C74951-L445-B20 must be inserted.

2) Redundant installation of the mini floppy disk interface unit is necessary although only one drive is used.

3) Redundant installation is required if the CS275 bus system is used for communication.

4) One I/O module per extension unit in the basic cabinet may be replaced by a group interrupt module 6DS1 601-8BA (or 6DS1615-8AA).
Group interrupt modules in an AS 235 H system can be installed in up to triple-redundant mode in the EE slots 13, immediately next to the EAVU.



AF Remote bus connector board
SAE Cabinet connection elements
VR Video relay
1 Power supply unit I (5V)
2 Buffer module (24 V)
3 Power supply II (5V)
4 Basic unit (CPU I+II)
5 Extension unit (EE)
6 I/O comparator and switchover module (EAVU)
7 Cabinet power supply unit with:
Circuit breakers, socket outlets, alarm logic modules, logic diode modules, cabinet power supply diodes, inductive bus converter unit (option), blinking clock-pulse generator module
8 Group interrupt module (option) or I/O module
9 Process cable clamping bars

Fig 2.1 Cabinet layout

2.2 Power Supply Unit (SVE)

The power supply unit is installed in the topmost tier of the basic cabinet and provides the basic unit with both supply voltages.

Internally, the 24-V buffer module has a two-channel structure and buffers the DC 24-V voltage twice (for SV I and SV II).

The power supply modules at either side of the buffer module supply both CPUs independently with 5 V.

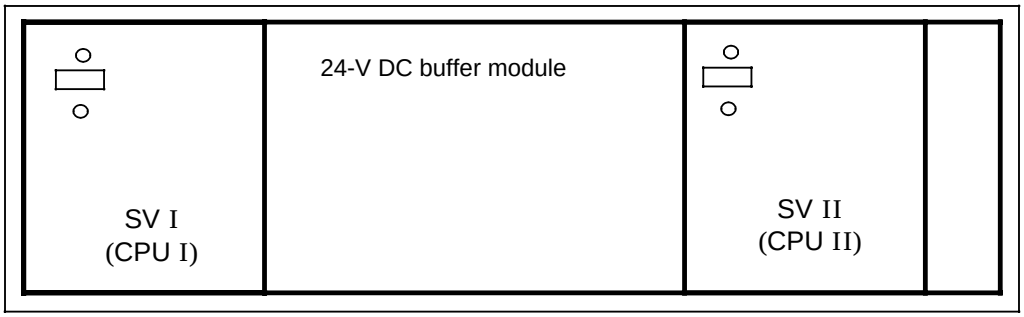
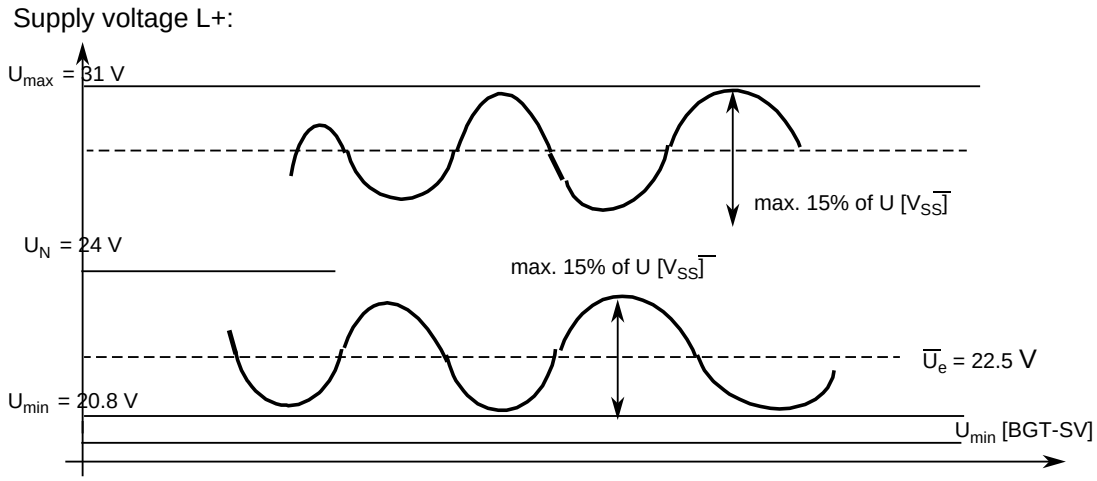
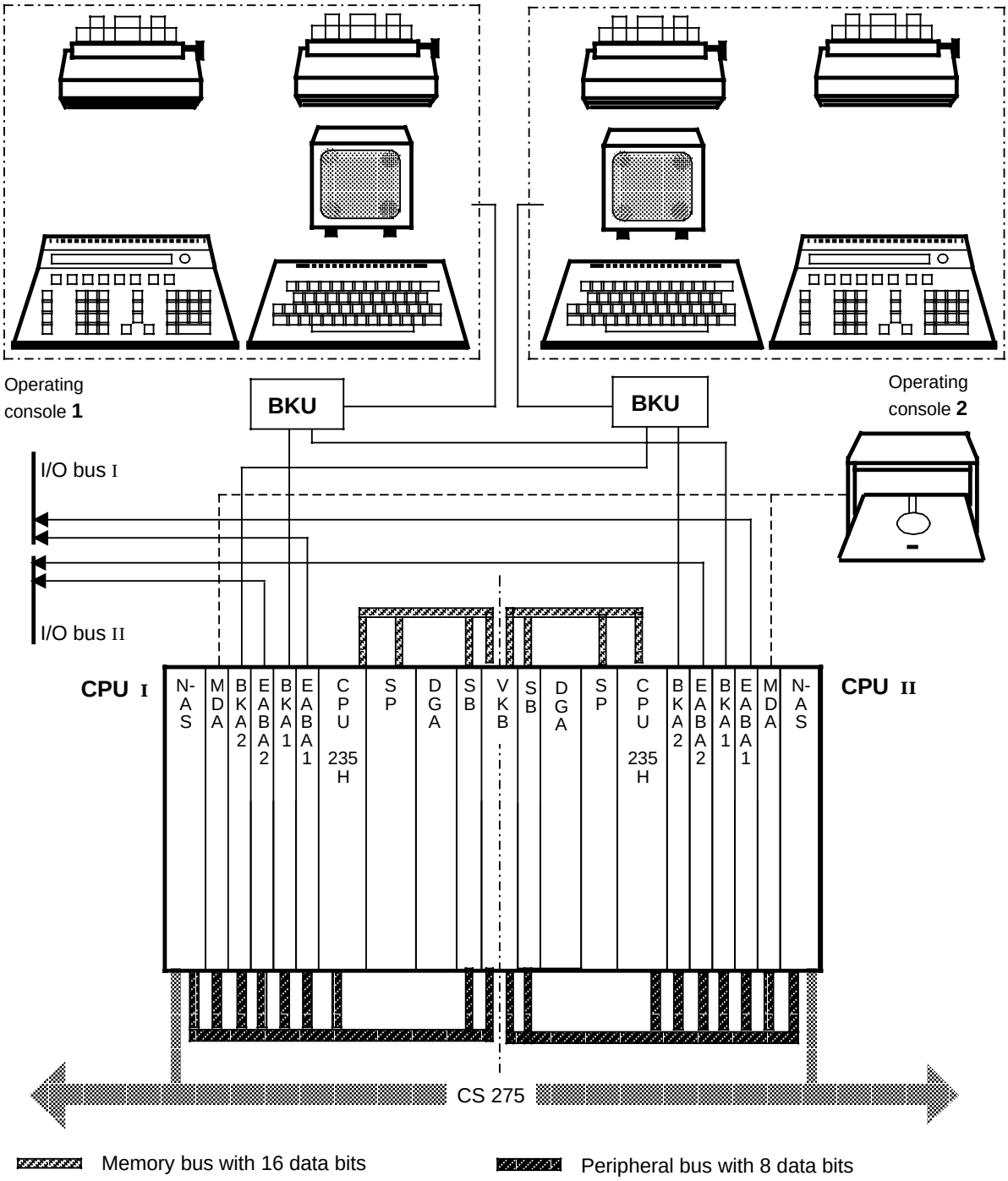


Fig. 2.2 AS 235 H power supply unit



2.3 Basic Unit (GE)

The basic unit consists of two central units (CPU I and CPU II) which are arranged in a mirrored structure in the subrack. The comparator coupler module (VKB), which is redundant in itself, forms the mirror axis of this system.
Seen from the front, the left-hand part is defined as CPU I, the right-hand part as CPU II.
Different to the AS 235 system, the backplane of the basic unit is completely structured as a supply and bus board. Yet, a detrimental connection of the two central units is not possible.
The supply voltages are fed to the central units via 2 x 1 cables (DC 24 V) and 2 x 3 cables (5 V).
The connection between operator input channel interface (BKA) and process communication keyboard*/*configuring keyboard*/*printer consists of standard cables *and* a special adapter cable.
A video relay is used for connecting a monitor to the two redundant BKA modules.
Ribbon cables which are plugged into the back of the basic unit interconnect the I/O bus interface modules and the I/O comparator and switchover modules (EAVU) in the extension units. The ribbon cables are plugged into the EAVU front panels.



KB Comparator coupler module
SB Synchronization module
DGA Diagnostic unit interface module [1])
SP Memory module
CPU Central processor unit module
BKU Operator input channel switchover unit, consisting of video relay and adapter cable
EABA 1 I/O bus interface module 1
BKA 1 Operator input channel interface 1
EABA 2 I/O bus interface module 2
BKA 2 Operator input channel interface 2
MDA Mini floppy disk interface module
N-AS Local bus interface module (N8-H permissible as well)

Fig. 2.3 System configuration

2.4 Extension Unit (EE)

An extension unit consists of a double-height subrack. Up to three extension units can be installed in a basic cabinet; an extension cabinet can accommodate up to four extension units.

Each extension unit features 14 slots. The I/O comparator and switchover module (EAVU) must always be installed in slot 14.

Any mix of I/O modules may be installed in the remaining 13 slots. A group interrupt module [1)] is to be installed in slot 13.

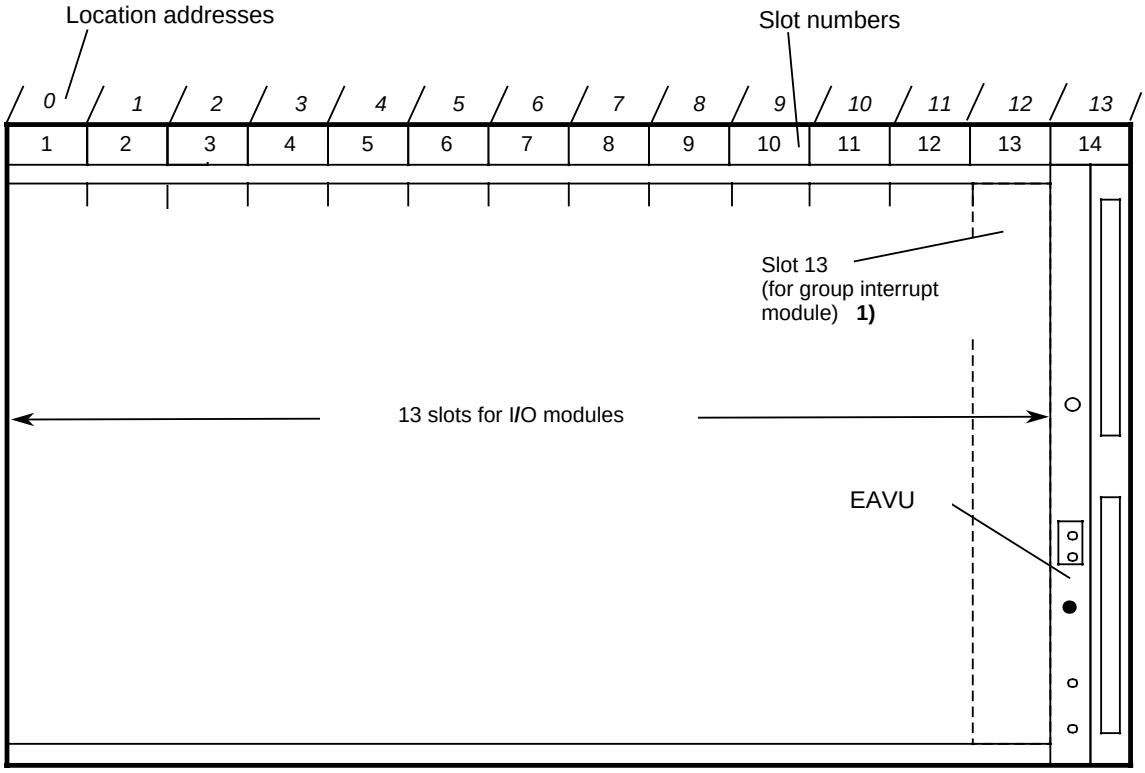


Fig. 2.4 Front of extension unit (EE)

1) Up to three group interrupt modules may be installed in the basic cabinet (one per extension unit).

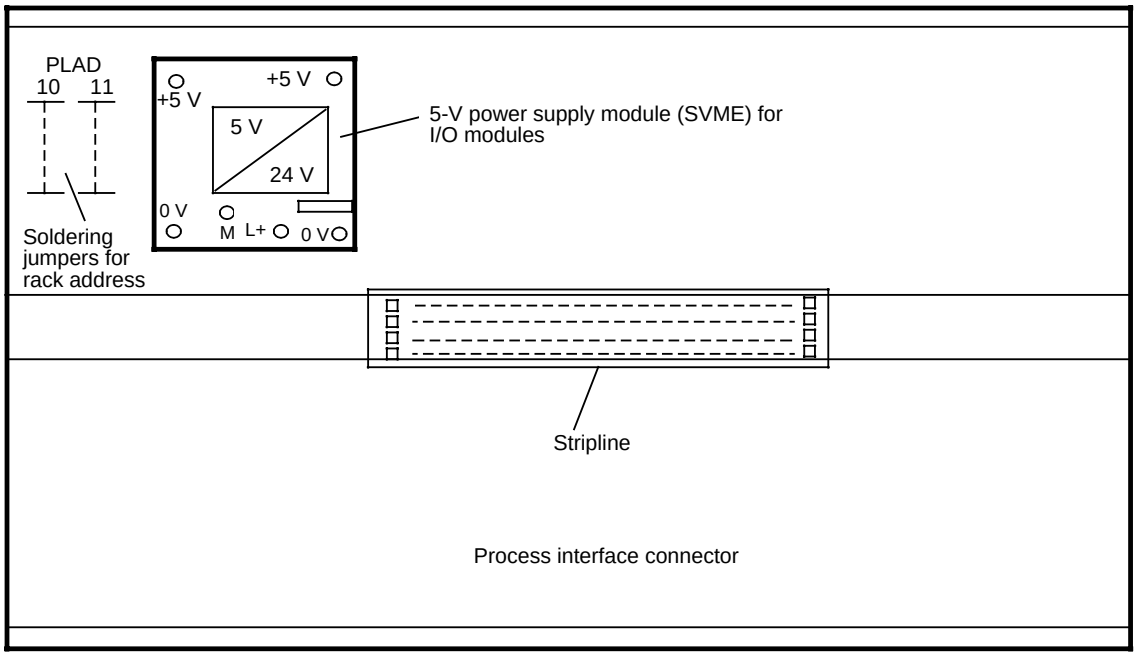
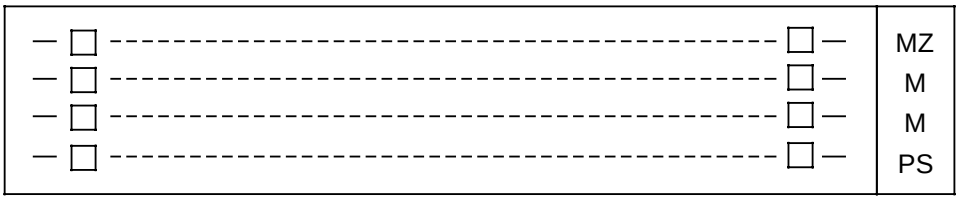


Fig. 2.5 Extension unit (rear)

Stripline:



The stripline may only be used for connecting the process interfaces of the I/O modules in the subrack (e.g. for I/O module input connections).
The stripline may not be used for feeding transducers, contacts etc.

The PS signal (24 V) is supplied by the EAVU. It is fused (1.6 A) on the EAVU module and routed via the X2 backplane connector to the stripline.

Caution:

Signal lines **may not** be routed from pins f32 and d32 (the process interface at the bottom connector of the I/O modules). The fuse ratings of the L+ potentials there are too high.

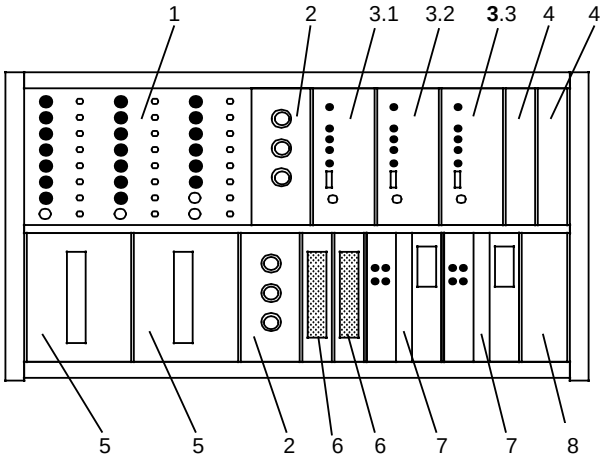
2.5 Cabinet Power Supply Unit (SES)

The cabinet power supply unit is a 2-tier subrack that is installed in the lower part of the main rack (location W) inside the basic cabinet.

The front section of the cabinet power supply unit contains the circuit breakers for the individual system components, the socket outlets for keyboard and mini floppy disk unit connections and the connectors for the cabinet power supply diodes, the cabinet monitoring modules and the remote bus.

The rear part of the cabinet power supply unit accommodates the terminal blocks for distributing the M potential and the individually fused 24-V voltages, and isolating terminals for connecting zener diode blocks (surge diverters) for the 24-V voltages.

A fully equipped cabinet power supply unit has the following structure:



1 Circuit breakers (F) for:

F1	CPU I	F9	EE 1	F17	PÜ 1
F2	CPU II	F10	EE 2	F18	PÜ 2
F3	Process communication keyboard 1	F11	EE 3	F19	Fan 1 for GS
F4	Process communication keyboard 2	F12	EE 4	F20	Fan 2 for ES
F5	Mini floppy disk unit 1	F13	EE 5	F21	Fan 1 for ES
F6	Mini floppy disk unit 2	F14	EE 6	F22	Fan 2 for ES
F7	UI	F15	EE7	F23	Heat exchanger for GS
F8	Reserve	F16	Reserve	F24	Heat exchanger for ES

2 Socket outlets for keyboard and mini floppy disk unit
3.1 ML alarm logic module for CPU I
3.2 ML alarm logic module for CPU II
3.3 ML alarm logic module for ES
4 VD11 diode module (option)
5 SED 31 cabinet power supply diode
6 Local bus connector (connection distribution unit)
7 UI bus converter unit (option)
8 BL flashing pulse generator module

Fig. 2.6 AS 235 H cabinet power supply unit

2.6 Cabinet Configuration (Power Dissipation)

2.6.1 Power Loss

The power loss must be controlled when the AS cabinets (including the I/O modules) are configured. The AS 235 H automation system may be used without a fan module if the permissible cabinet power loss values are not exceeded.

The following power loss limits P_{Smax} must be taken into account when the cabinets are configured: (=cabinet entry temperature)

=25 °C	P_{Smax} = 450 W	30 °C	P_{Smax} = 420 W
35 °C	P_{Smax} = 380 W	40 °C	P_{Smax} = 350 W

As long as P_{Smax} is not exceeded, the components installed in the basic and extension cabinet may be used without a fan. If the power loss of the cabinet exceeds P_{Smax} due to the use of I/O modules, the air flow rate must be increased. In this case, fan modules or heat exchangers have to be configured (option).

2.6.2 AS 235 H Basic Cabinet

1. If the power loss P_{Smax} is not exceeded in the cabinet and a value of 150 W is not exceeded in any of the extension units of the cabinet either, the cabinet can be used without forced ventilation up to the cabinet entry temperatures specified above.
2. An extension unit without forced ventilation may only be loaded up to a value of 150 W. A forced ventilation must be provided in the cabinet if this value is exceeded.
3. If the cabinet is equipped with a lot of I/O modules with a higher power loss value, the modules should not be installed next to each other but be distributed in the subracks so as to prevent hot spots.

Configuration rules for the AS 235 H basic cabinet

The following values must be used for calculating the thermal load of the cabinet:
Configuration value of base AS configuration:
P_{Gmax} 150 W + N×7 W; N=number of EAVUs
Typical average power loss of an I/O module: $P_{I/O\ module}$=5.4 W
Typical maximum power loss of an I/O module: $P_{I/O\ module}$=7 W

Maximum power loss of an I/O module: see PLT 111 Catalog, Edition 1993.

Basic cabinet

Formula: $P_{I/O\ max} = P_{Smax}$ Power loss I/O $_{max}$ cabinet

Typical permissible number of I/O modules in the cabinet: (at 40°C)

$$A_{I/O\ typ} = \frac{200\ W}{5.4\ W/module} = 37\ modules_{typ}$$

Permissible number $_{typ.,min}$ I/O modules in the cabinet: (at 40°C)

$$A_{I/O\ min} = \frac{200\ W}{7\ W/module} = 28.6\ modules_{typ.,min}$$

The base value P_{Smax} must be adapted according to the table (see above, under item 2.6.1).

This rough calculation can be used to determine whether or not the typical/maximum power loss resulting from I/O modules has been exceeded. (Rule of thumb: 2 completely filled I/O subracks with 13 I/O modules each).

From 28 I/O modules onwards, checking against the power specifications in the PLT 111 Catalog (Edition 1993, Catalog Section 5, "I/O Modules") is recommended. The process signals should be included if necessary (maximum number: 39).

Different distribution (e.g. in an additional extension cabinet) or a fan module is required if the I/O modules exceed the power loss P_{Smax}.

2.6.3 AS 235 H Extension Cabinet

1. With a typical module configuration, the power loss limit of the cabinet is not exceeded if the AS 235 H extension cabinet is used without a fan. (Up to 52 I/O modules, without EAVU modules).
   Only in the case of an atypical configuration (many identical I/O modules, modules >8 W) a more detailed checking is recommended.
   If the power loss P_{Smax} is not exceeded **and** a value of 150 W is not exceeded in any of the extension units in the cabinet either, the cabinet may be operated up to the specified cabinet entry temperature without forced ventilation (see Chap. 2.6.5) .
2. An extension unit without forced ventilation may only be loaded up to a value of 150 W. A forced ventilation must be provided in the cabinet if this value is exceeded.
3. If the cabinet is equipped with a lot of I/O modules with a higher power loss value, the modules should not be installed next to each other but be distributed in the subracks so as to prevent hot spots.

Configuration rules for the AS 235 H extension cabinet

In maximum configuration, each of the four extension racks in the extension cabinet may be equipped with one EAVU module (power loss 7 W).

A value of 28 W can therefore be assumed as a configuration value of the base configuration P_G of the four extension units.

The maximum number of I/O modules is 4×13=52 (without EAVUs).

The following formula shows that a typical configuration does not cause the power loss of the extension cabinet to be exceeded:

Formula: $P_{I/O\ max} = P_{Smax} - 28\ W$ Power loss I/O $_{max}$ cabinet

Typical average power loss of an I/O module: $P_{I/O\ module} = 5.4\ W$

Typical maximum power loss of an I/O module: $P_{I/O\ module} = 7\ W$

Typical permissible number of I/O modules in the cabinet: (at 40°C)

$$A_{I/O\ typ.} = \frac{322\ W}{5.4\ W/module} = 59\ modules_{typ.}$$

Permissible number of $_{typ.,min}$ I/O modules in the cabinet: (at 40°C)

$$A_{I/O\ min} = \frac{322\ W}{7W/module} = 46\ modules_{typ.,min}$$

A fan module must be provided or the distribution of the I/O modules in several extension units changed if the power loss of the I/O modules in an extension rack exceeds 150 W.

One or two fan modules must be added according to the above-mentioned configuration rules if the total power loss exceeds P_{Smax}.

The P_{Smax} base value must be adapted in accordance with the table (see 2.6.1 above).

This rough calculation can be used to determine whether or not the typical */* maximum power loss resulting from I/O modules has been exceeded.

From three filled extension units onwards or in the case of an atypical configuration, checking against the power specifications in the PLT 111 Catalog (Edition 1993, Catalog Section 5, ”I/O modules”) is recommended. The process signals should be included if necessary.

A fan module is required if the I/O modules exceed the power loss P_{Smax}.

2.6.4 AS 235 H Cabinet with Forced Ventilation

Depending on the thermal load (power loss) of the I/O modules, up to two fan modules (6DS9 943-8AA) may be required in the TELEPERM M cabinet, basic and/or extension cabinet.

2.6.5 AS 235 H Cabinet without Heat Exchanger (WT)

If the power loss (Ps)

>350 W at a cabinet entry temperature of 40°C

>380 W at a cabinet entry temperature of 35°C

>420 W at a cabinet entry temperature of 30°C

>450 W at a cabinet entry temperature of 25°C

or if a subrack is equipped with modules whose total power loss >150 W, a fan module is required in the basic cabinet at installation location 13 or in the extension cabinet at installation location 9.

If both criteria apply, each cabinet must be equipped with two fan modules.
In the basic cabinet, the second fan module must be fitted in installation location 29 and in the extension cabinet in installation location 25.
The following power loss limits apply in this case:

Ambient temperature	40°C
Power loss of the cabinet	700 W

Cabling and fusing have been laid out for the connection of a maximum of two fans per cabinet.

2.6.6 AS 235 H Cabinet with Heat Exchanger

1. If the total cabinet power loss P_S does not exceed a value between 350 W and 450 W (depending on the ambient temperature) and if the power loss in each individual extension unit (EE) is less than 150 W, the cabinet (with heat exchanger) may be used **without** an additional fan module.
2. Up to a total power loss P_S of 700 W at an ambient temperature of 40°C **and** provided that the power loss in each individual extension unit (EE) is less than 150 W, the cabinet (with heat exchanger) may be used **with one** fan module.
   The fan module must be installed in the basic cabinet between the base unit and the 1st EE at installation location 13 and in the extension cabinet between the 4th EE and 5th EE at installation location 9.
3. If the power loss in one of the three or four extension racks exceeds the limt of 150 W **or** the total power loss P_S>700 W, a second fan module must be installed in the base cabinet between the 2nd EE and 3rd EE (installation location 29) or in the extension cabinet between the 6th EE and the 7th EE (installation location 25) .

   In this case P_{Smax}=1000 W can be reached at an ambient temperature of 40°C .

2.6.7 Fan Module (Option)

The fan module 6DS9 943-8AA is used to provide forced-air cooling. A fan module features 3 fan motors each of which is monitored for speed; an electronic short-circuit fuse is integrated.

The fan monitors of the fan modules and the heat exchanger are connected in series and applied to the basic unit as alarm signal LK.

The following cable sets are available (option) :

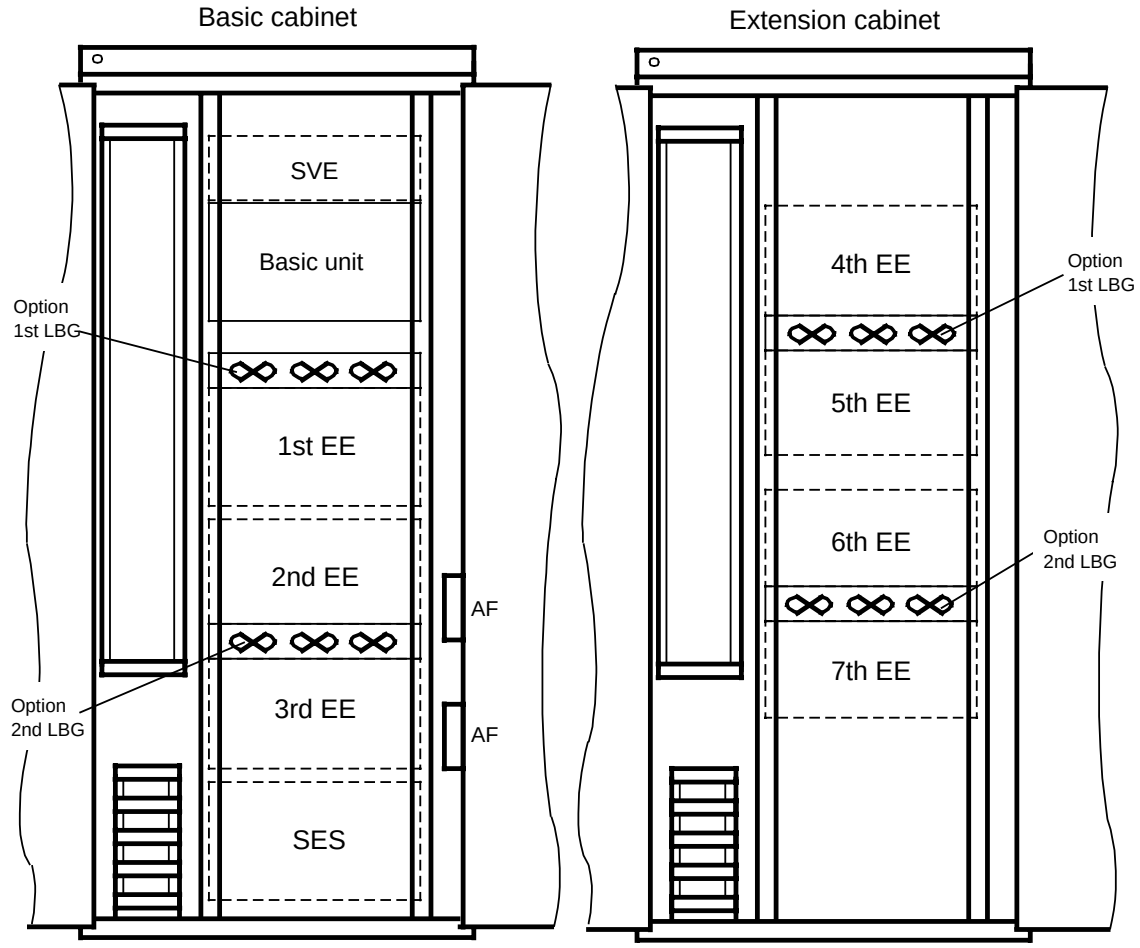
C79195-A3831-H220	to connect one fan module (supply and alarm output) in the basic cabinet (L=2.2 m)
C79195-A3831-H450	as for -H220, but for the extension cabinet (L=4.5 m)
C79195-A3828-H230	to connect one heat exchanger (alarm output) in the basic cabinet) (L=2.3 m)
C79195-A3828-H390	as for -H220, but for the extension cabinet (L=3.9 m).

One cable set is required per fan module. It includes the connection of the power supply and the alarm signal; as far as the heat exchanger is concerned, wiring of the series connection of the alarm signal is included.

The operating voltage is supplied via a cable at the rear of the module. The alarm signals from the monitoring circuit also run via the 6-pin connector of this cable.

The fan module is used to provide forced ventilation of module subracks in AS 235 H system cabinets. The fan module unit is designed for operation with DC 24 V.
The module has the same dimensions as an ES 902 subrack and like the latter can be installed in main frames.

The fan motors issue a square wave signal wih a frequency that is proportional to the speed. The square wave pulses are fed to the monitoring circuit which monitors the lower frequency (speed) limits of the individual motors. (See Fig. 2.7 for the installation locations of fan modules).



LBG Fan module

Fig. 2.7 Cabinet layout, location of fan modules (options)

A red LED lights up and a floating changeover contact is actuated if the speed of a motor falls below the minimum rate.

- The LED is used for fault location
- The changeover contact can be used for issuing a fault signal via an external signal line or for triggering external signals or switching activities.

Error messages are suppressed during start-up after the supply voltage has been switched on.
The changeover contact function can be selected by setting the plug-in jumper X16:

- active non-fault alarm=passive fault alarm
  The relay drops in the case of a malfunction (when LED is ON).

Upon delivery, the X16 plug-in jumper is set for active fault alarm.
The fan module connecting cables C79195-A3828-H220 (length 2.20 m) are used for power supply and signal line connection in the basic cabinet (fan module 1 or 2), or 79195-A3828-H450 (length 4.50 m) for fan modules in the extension cabinet.

Warning

Ensure that the fan module is not used without the finger guard!

The fan module is maintenance-free.

Based on the fan service life (approx 40,000 h) specified by the manufacturer, it is recommended to replace the fan or the fan module every 4 years.

Settings to be made after the module has been replaced: jumper setting for alarm signal (see Fig. 2.8).

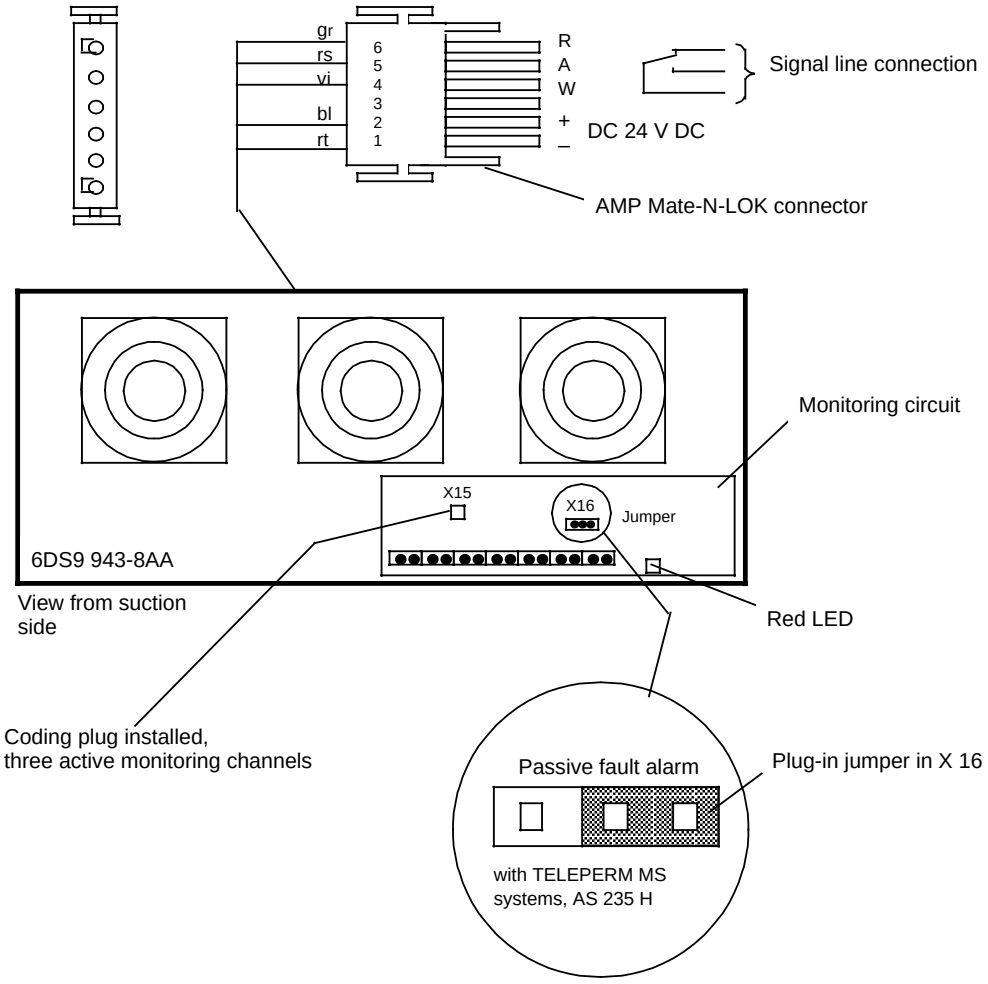


Fig. 2.8 Fan module

Automatic circuit breakers (F) are provided in the SES for the connection of fan modules:

Fan 1 fused via F19 (KL 43) in the basic cabinet and via F21 (KL 49) in the extension cabinet.

Fan 2 fused via F20 (KL 46) in the basic cabinet and via F22 (KL 52) in the extension cabinet.

The alarm signals of the fan(s) and*/*or the heat exchanger are connected in series via the marshalling rack (RV) in the SES and fed from there to the AS system.

The heat exchanger (230 V AC) is fused externally.

3 Method of Operation

3.1 System Configuration

Method of operation and configuration of the AS 235 H automation system are defined by the requirements of increased availability. This availability is mainly achieved by CPU redundancy where the same data is processed by two CPUs which operate independently at synchronous clock pulses.

Both CPUs are equivalent and have the same priority level, although the I/O comparator and switchover module (EAVU) routes only the signals from one CPU to the I/O modules. Also the communication via the CS 275 bus system does only take place via the N-AS or N8-H module of **one** CPU. This CPU is known as "master CPU".

CPU I assumes master function and thus process control if both CPUs are started simultaneously. CPU II becomes passive and, after updating, automatically assumes the function of the backup CPU which is able to take over mastership at any time. This enables the system to continue process operation without interruption after a tolerable fault has occurred.

Either CPU can assume one of the following states:

Master	(M)	Only master mode enables a CPU to actively control the process.
Standby	(R)	A CPU in backup mode executes the same instruction sequence as the master CPU.
Passiv	(P)	The CPU is separated; the two CPUs operate in asynchronous mode.
Backup	(B)	The CPU accepts the memory contents of the master CPU.
Fehler	(F)	The system software has located a fault in the CPU.

3.2 Faultless Operation

Both CPUs run synchronously during normal faultless operation.

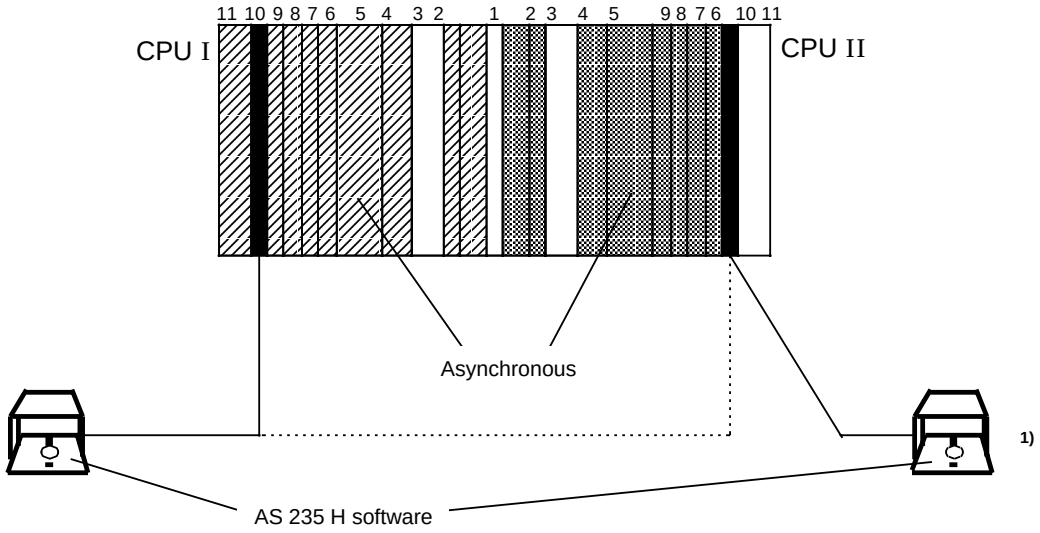
At first, both CPUs start up asynchronously. During commissioning, the same system software is loaded into the memories of the central processing units. This is performed either in succession (with one floppy disk drive) or in parallel (with two floppy disk drives). Subsequently, the system can be synchronized.

The memory contents of both memories are identical in synchronous operation. This means that identical data is read and written. The central processors provide control signals and addresses synchronously. The comparator coupler module (VKB) compares all incoming and outgoing data and signals of the central processing units.

One I/O comparator and switchover module (EAVU) per extension unit performs this comparison on the I/O level.

Each operator terminal possesses two operator input channel interface modules, one in CPU I and one in CPU II.

Although there are two local bus interface modules (N-AS or N8-H), if communication is performed via the CS275 bus system, only the N-AS**/**N8-H of the master CPU is active. (A single N-AS**/**N8-H module is not expedient since the connection to the CS 275 bus system would be interrupted if mastership were changed.)



1	Comparator coupler module (VKB)	(6DS1 142-8AA)
2	Synchronization module (SB)	(6DS1 143-8AA)
3	Diagnostic unit interface module (DGA)	
4	Memory module (SP)	(6DS1 837-8DA**/**-8EA**/**-8FA and 6DS1 844-8..)
5	Central processing unit (CPU)	(6DS1 141-8AA)
6	I/O bus interface module 1 (EABA1)	(6DS1 312-8BB)
7	Operator input channel interface module 1 (BKA1)	(6DS1 330-8CA)
8	I/O bus interface module 2 (EABA 2)	
9	Operator input channel interface module 2 (BKA2)	
10	Mini floppy disk interface module (MDA)	(6DS1 326-8BB)
11	N-AS or N8-H local bus interface module	(6DS1 223-8CA or 6DS1 220-8AA)

Fig. 3.1 Start-up and loading

1) Although only one mini floppy disk unit is sufficient for loading the system software and the user program, two mini floppy disk interface units are required. For booting, the mini floppy disk unit is connected to CPU I and CPU II in succession. Both interfaces must, however be installed.

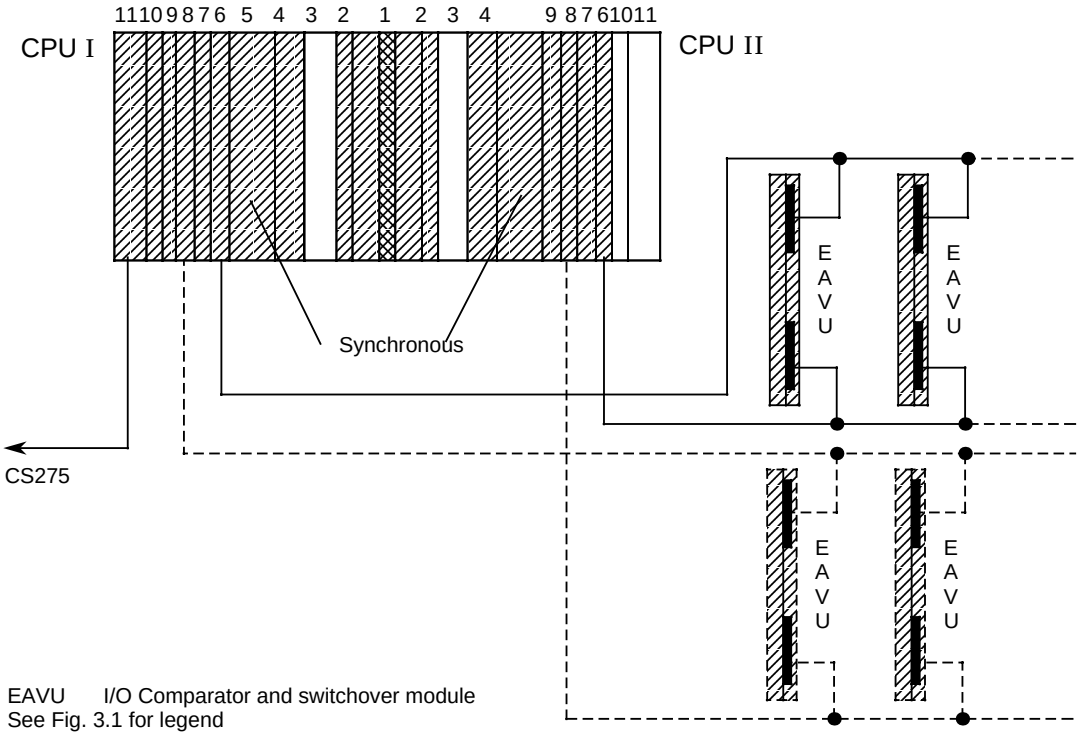


Fig. 3.2 I/O connection via EAVU, synchronous operation, CPU I is master

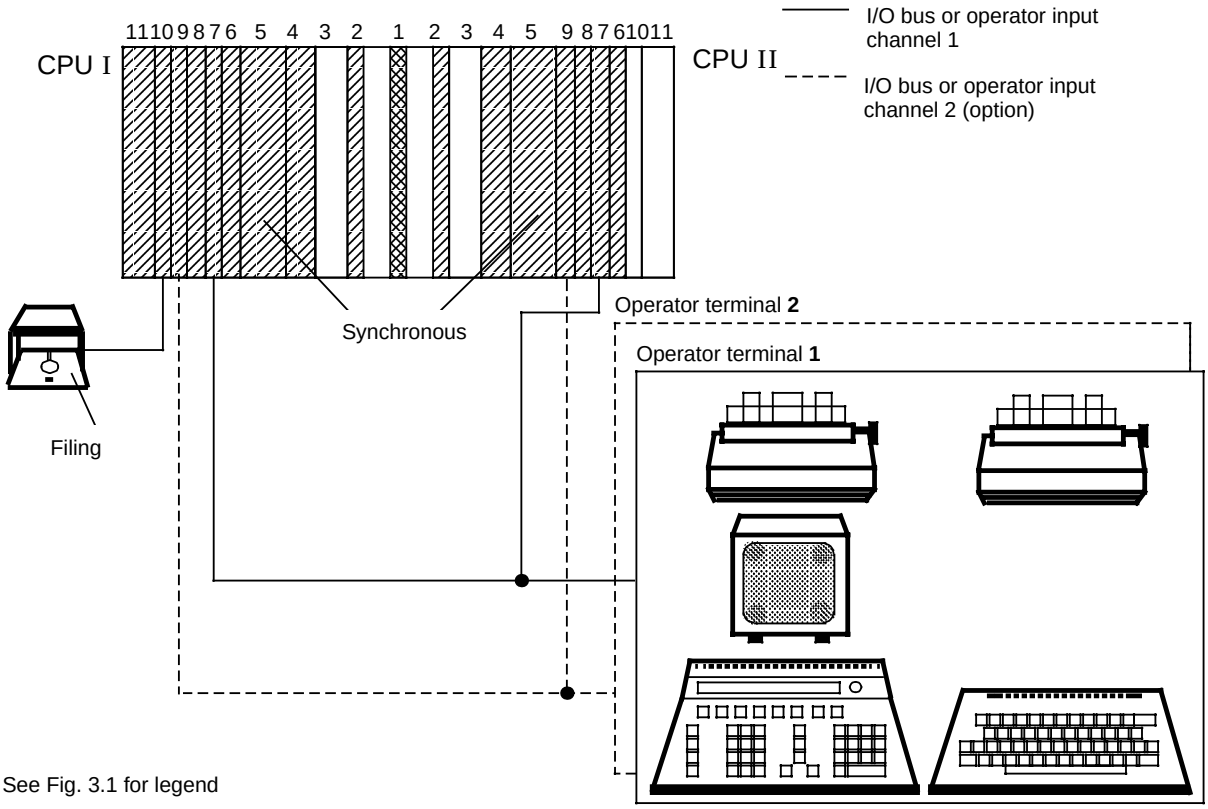


Fig. 3.3 Connection to operator input level, synchronous operation, CPU I or CPU II is master

3.2.1 Central Unit Functions

The fault-tolerant functions of the central unit with its two identical central processing units can only be performed if the specified configuration has been established.

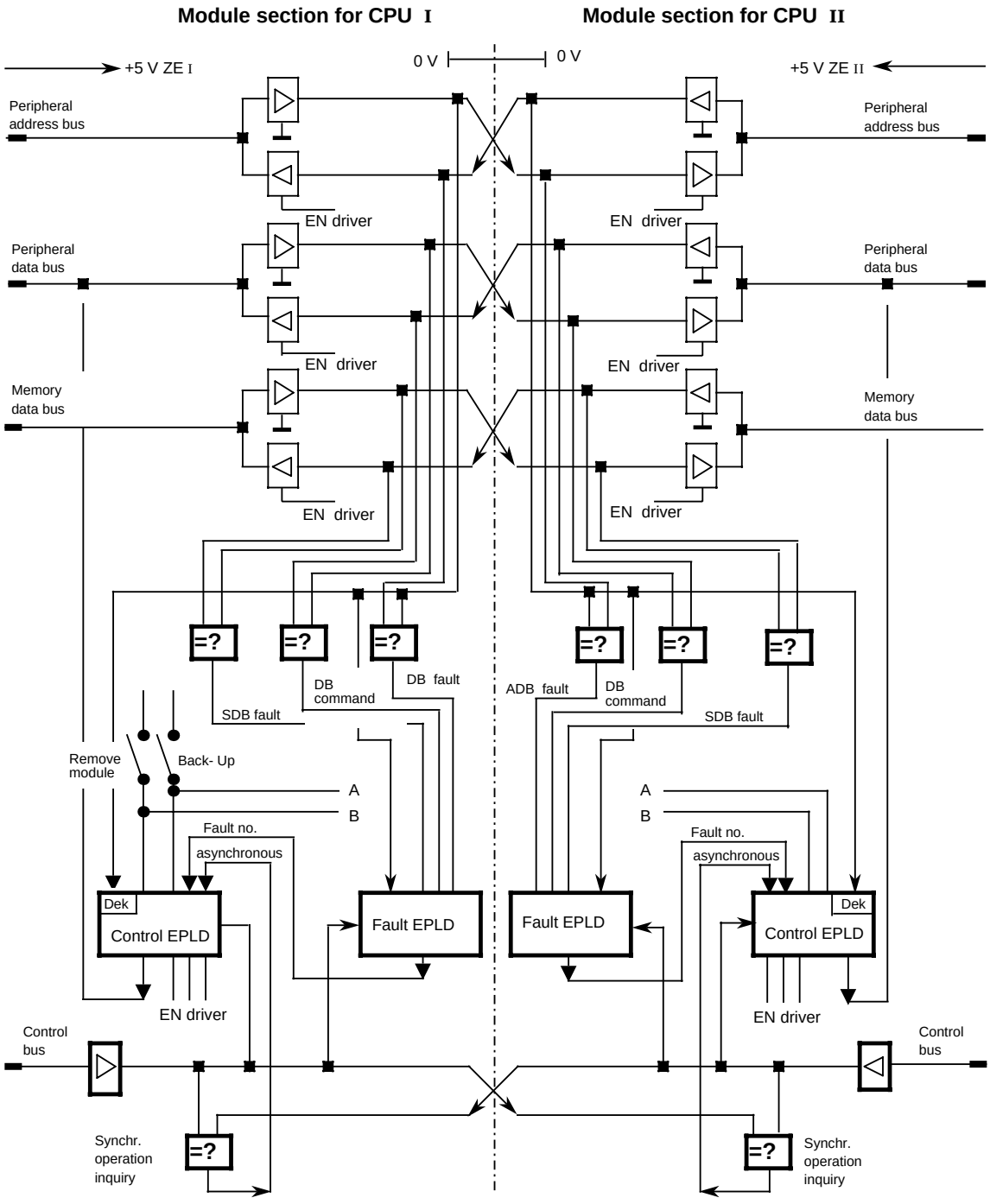
- Comparator coupler module (VKB)

The comparator coupler module (Fig. 3.4)

- compares the bus signals of both CPUs
- interconnects the parallel buses of both CPUs
- branches a single-channel input information to both CPUs
- transfers all read data items during backup operation from the memories/registers of the master CPU to the memories**/**registers of the second CPU.

Caution

The VBK may not be removed during operation unless the switch on the front is in AUS (OFF) position.
The switch itself may only be actuated during asynchronous operation.



EN = enable
=? = comparator
EPLD = Erasable programmable logic device

Fig. 3.4 Block diagram of the comparator coupler module (VKB)

- Synchronization module (SB)

The synchronization module (Fig. 3.5) provides the basis for synchronous operation of the two CPUs. It

- generates the processor and system clock pulses,
- synchronizes the CPU base clock pulse,
- synchronizes read and write data,
- synchronizes interrupt signals,
- supplies status messages to the CPU,
- controls synchronization.

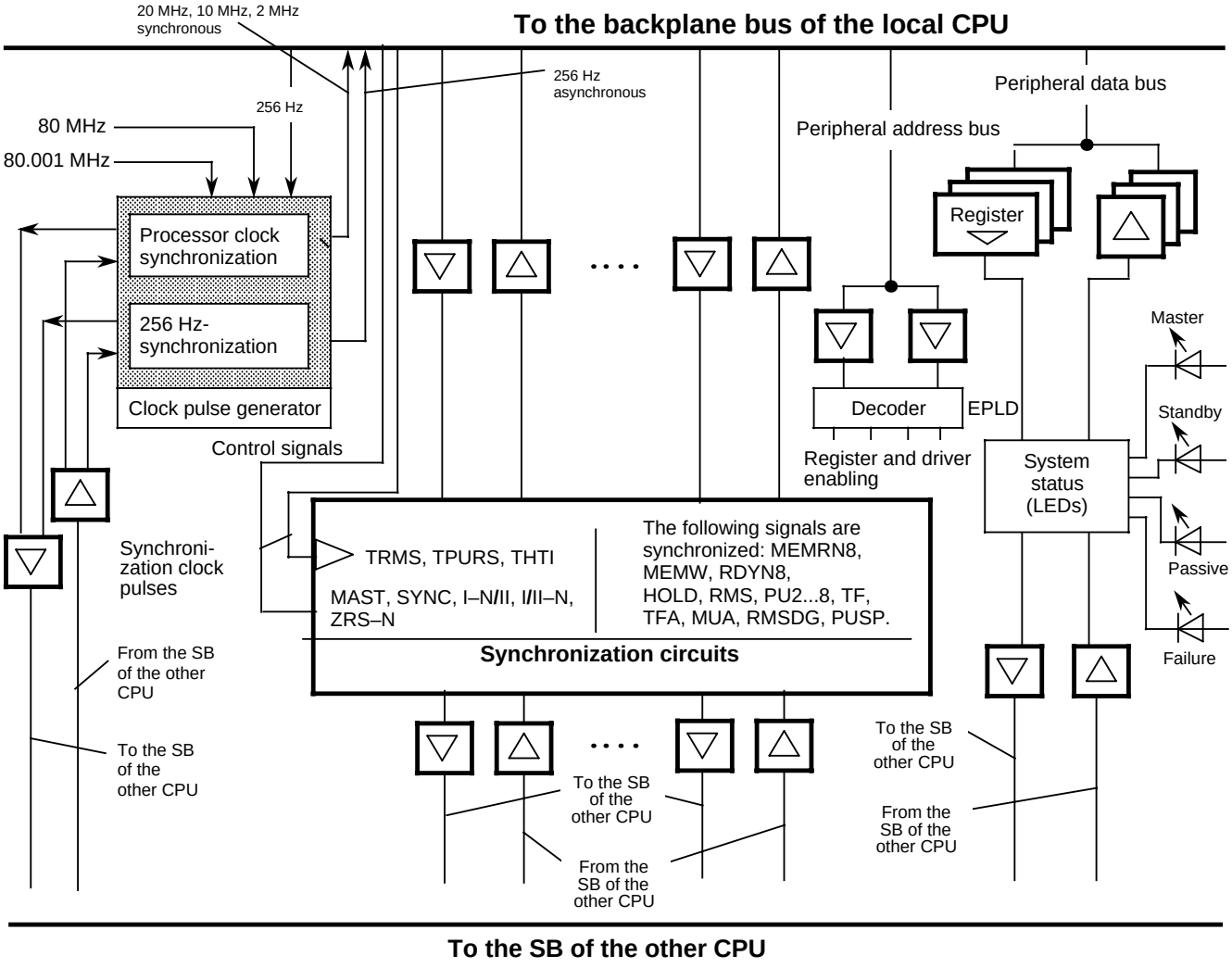


Fig. 3.5 Block diagram of the synchronization module (SB)

Memory Module

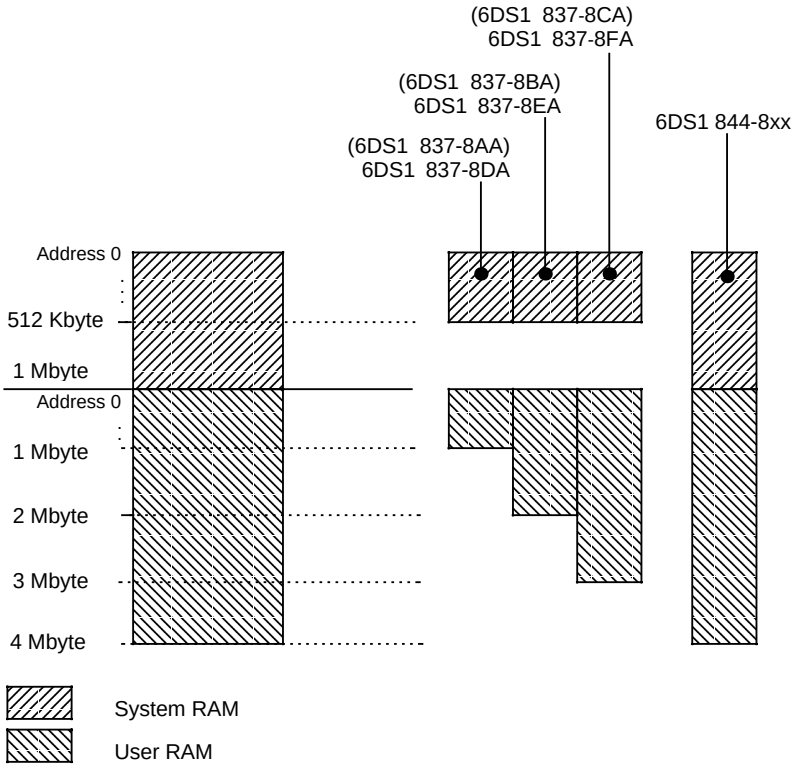
– 512 Kbyte system memory with memory module 6DS1 837-8xA *or*
  1 Mbyte system memory with memory module 6DS1 844-8xx
– 1, 2 or 3 Mbyte user RAM with memory module 6DS1 837-8xA *or*
  4 Mbyte user RAM with memory module 6DS1 844-8xx
  (4000 Kbyte are available for the user from a total of 4 Mbyte)
– Back-up battery
– Battery failure logic circuit
– Parity monitoring (byte per byte)
– Error and control register
– Error display and state display with LED on the front plate
– BOOT logic.

If a parity error is detected when a word is read, then this error is signalled with a PAF signal (parity error) and processed from the system programs.

	6DS1 837-8xA	6DS1 844-8xx
Cycle time Access time	500 ns 300 ns	500 ns 300 ns

Table 3.1 Memory module cycle time

Memory design



- Central processing unit (CPU 235 H)

The central processing unit

- contains a 16/32-bit processor,
- is responsible for system start-up and microprogram start-up,
- processes the automation functions according to the program in the user memory.

Caution

Some of the backplane connector pin assignments of CPU 235 H (6DS1 141-8AA) and CPU 235 (6DS1 140-8AA) are different due to the following modifications that are required for synchronous CPU operation:

- External supply of the 20-MHz and 10-MHz processor clock pulses via the two SB modules (the G1 and G2 quartz oscillators have not been installed on the CPU 235 H).
- The 1/256-Hz time clock pulse is routed via the SB module for synchronization.
- The TPURS signal is issued to the SB module.

Due to the different connector pin assignments, the CPU module could be destroyed if a CPU 235 H were installed in a standard AS 235 system and vice versa.

- I/O bus interface module (EABA)

The I/O bus interface module

- transfers data and signals from the CPU to the EAVUs,
- receives data and signals from the EAVUs and transfers them to the CPU.

- Operator input channel interface module (BKA)

The operator input channel interface module (Fig. 3.6)

- establishes the connection to the operator input unit.

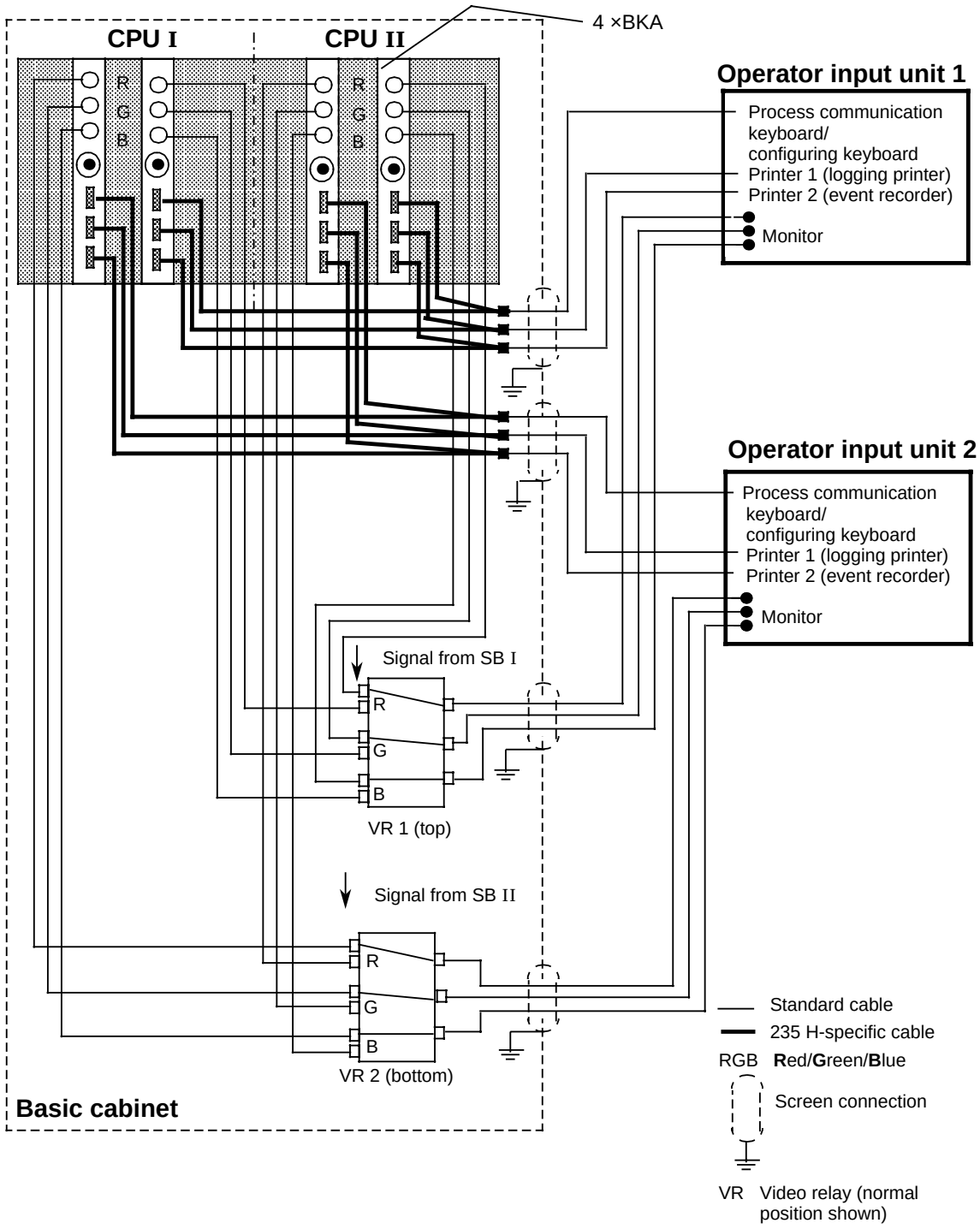


Fig. 3.6 Connecting the operator input units

- Mini floppy disk interface module (MDA)

The mini floppy disk interface module

- controls the mini floppy disk drive which is used for loading and filing.

Note:

Both interface units must be installed although only one MDE is required (which is to be connected to the current master CPU).

- Local bus interface module (N-AS)

The N-AS local bus interface module

- provides the connection to other systems via the CS275 bus system. Instead of the N-AS local bus interface module, you can also use the N8-H local bus interface module. The combination of N-AS and N8-H in one AS 235 H system is permissible as well.

- Diagnostic unit interface module (DGA)

The diagnostic unit interface module

- provides the connection to the diagnostic unit.

A diagnostic unit can be:

- PG 685
- PG 750.

The following points must be observed when using a DGA:

In **asynchronous operation**, the DGA must be connected to the CPU in which diagnostic functions are to be performed. The "DG-Betrieb" [DG mode] switch on the front panel of the SB module concerned must be in EIN [ON] position.

In **synchronous operation**, the DGA must always be connected to CPU I since all functions act synchronously on both CPUs. The "DG-Betrieb" [DG mode] switch on both modules must be in EIN [ON] position (the CPUs become asynchronous if the switch position differs on the modules).

Caution

The "DG-Betrieb" [DG mode] switch disables important monitoring functions when it is set to EIN [ON]. The switch may therefore only be set to EIN [ON] for service or diagnostic purposes.
The switch must be in AUS [OFF] position during normal operation.

3.2.2 I/O System Functions

The I/O system of the AS 235 H automation system is accommodated in the extension units (EE). The I/O system configuration depends on the user requirements. An exception is the EAVU module which, due to the fact that the redundant I/O buses are connected from the front, must always be installed in slot 14 (right-hand side) of an extension unit.

Another exception is the group interrupt module (binary input module 6DS1 601-8BA or 6DS1615-8AA). This module must always be installed in slot 13 of the extension unit(s) in the basic cabinet.

- I/O comparator and switchover module (EAVU)

The EAVU is the interface of the extension unit to both central processing units. All data and commands to the I/O modules are routed via the EAVU module. It converts the redundant signals from the synchronous CPUs to the single-channel I/O bus of the extension unit and branches the single-channel signals from the I/O modules to both CPUs.

The EAVU (Figs. 3.7 and 3.8)

- verifies the identity of redundant address, data and control signals from and to the central processing units;
- generates an error signal if it detects a discrepancy;
- determines the range concerned by a given I/O command;
- provides information regarding
  jumper setting
  last I/O access
  last register access
  comparator and status information
  via internal registers;
- influences
  the actual mastership
  checking the local extension unit
  clearing the error registers
  via internal registers;
- provides fault finding utilities
- verifies that the supply voltages (24 V and 5 V) are within the tolerance limits
- generates alarm and signal voltages for the local extension unit range (both voltage circuits are provided with a 1.6-A fuse)
- prevents the propagation of faults from one central processing unit to another and among the extension units.

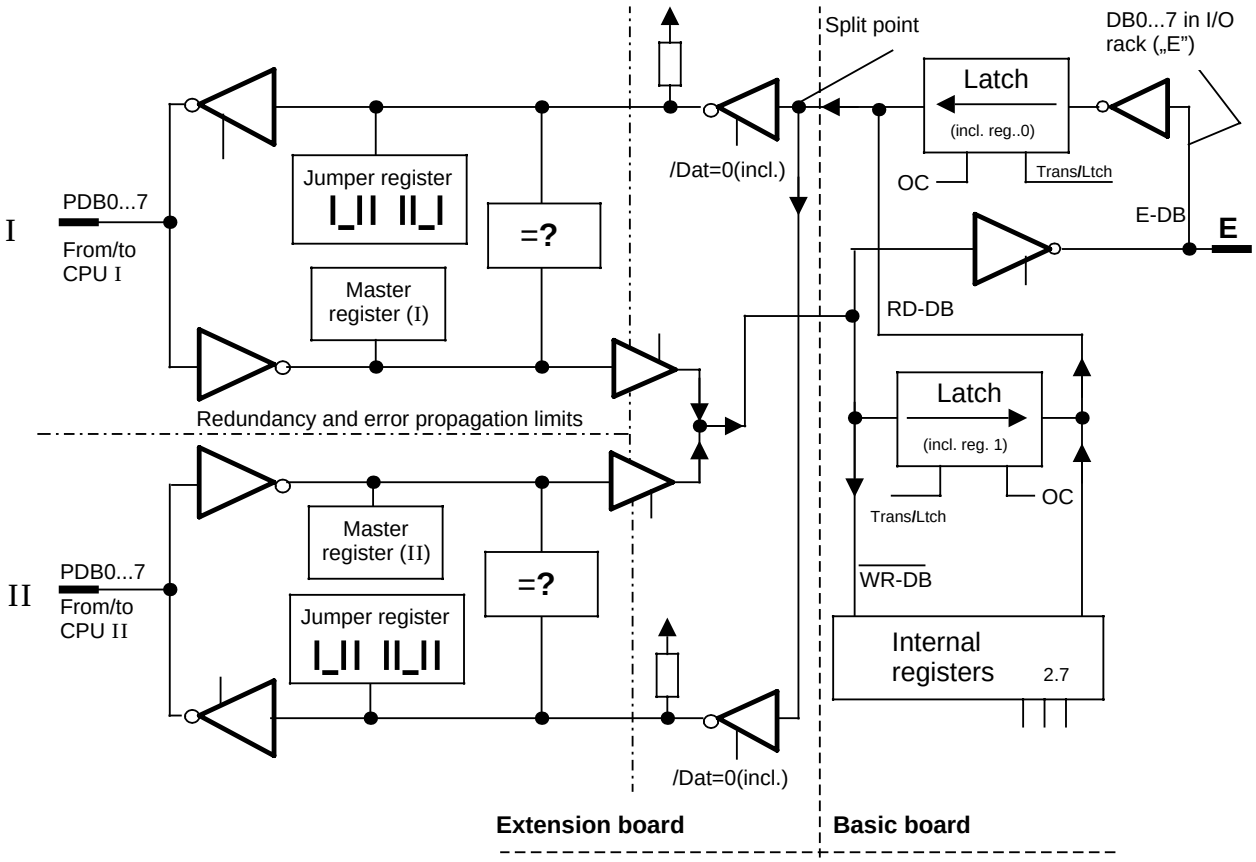


Fig. 3.7 EAVU data path structure

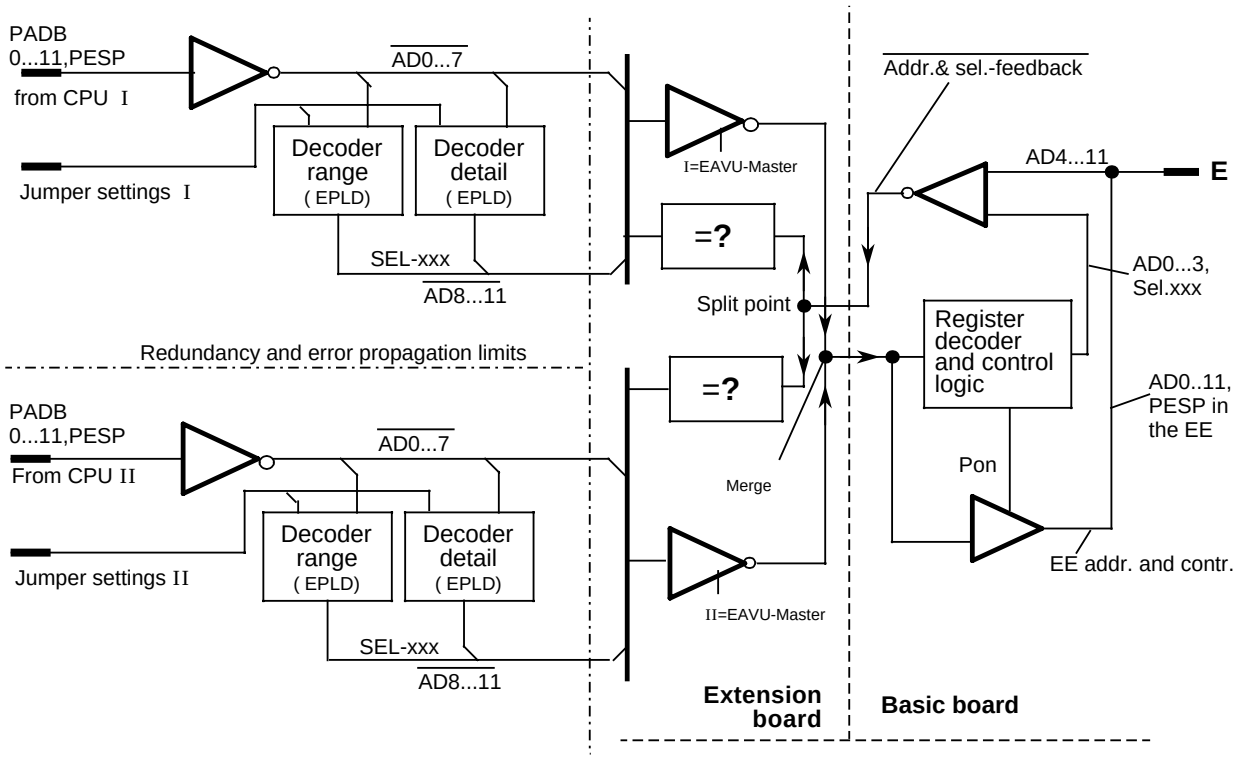


Fig. 3.8 EAVU address path structure

- The group interrupt module

The binary input module 6DS1 601-8BA (or also 6DS1615-8AA) is used as a group interrupt module in the AS 235 H system.[1)] Under address SF61 (the I/O range runs from SF00 to SF60), the module provides the system software with the state of up to 48 process alarms (1-active PINT signals) coming from the subordinate group interrupt modules (standby) 6DS1601-8BA or 6DS1615-8AA each with up to 48 process inputs. Further details are given in Chapter 1.10.3 (binary input with interrupt) of the AS 235 Description (Variant F), Order No. C79000-P9076-C088.
To ensure that a failure on the group interrupt module does not interrupt the acquisition of process alarms, two or three group interrupt modules (SF61) can be installed (double/triple redundancy) as shown in Fig. 3.9. Also see the EAVU description (Order No. C79000-T8076-C343) in this Manual.

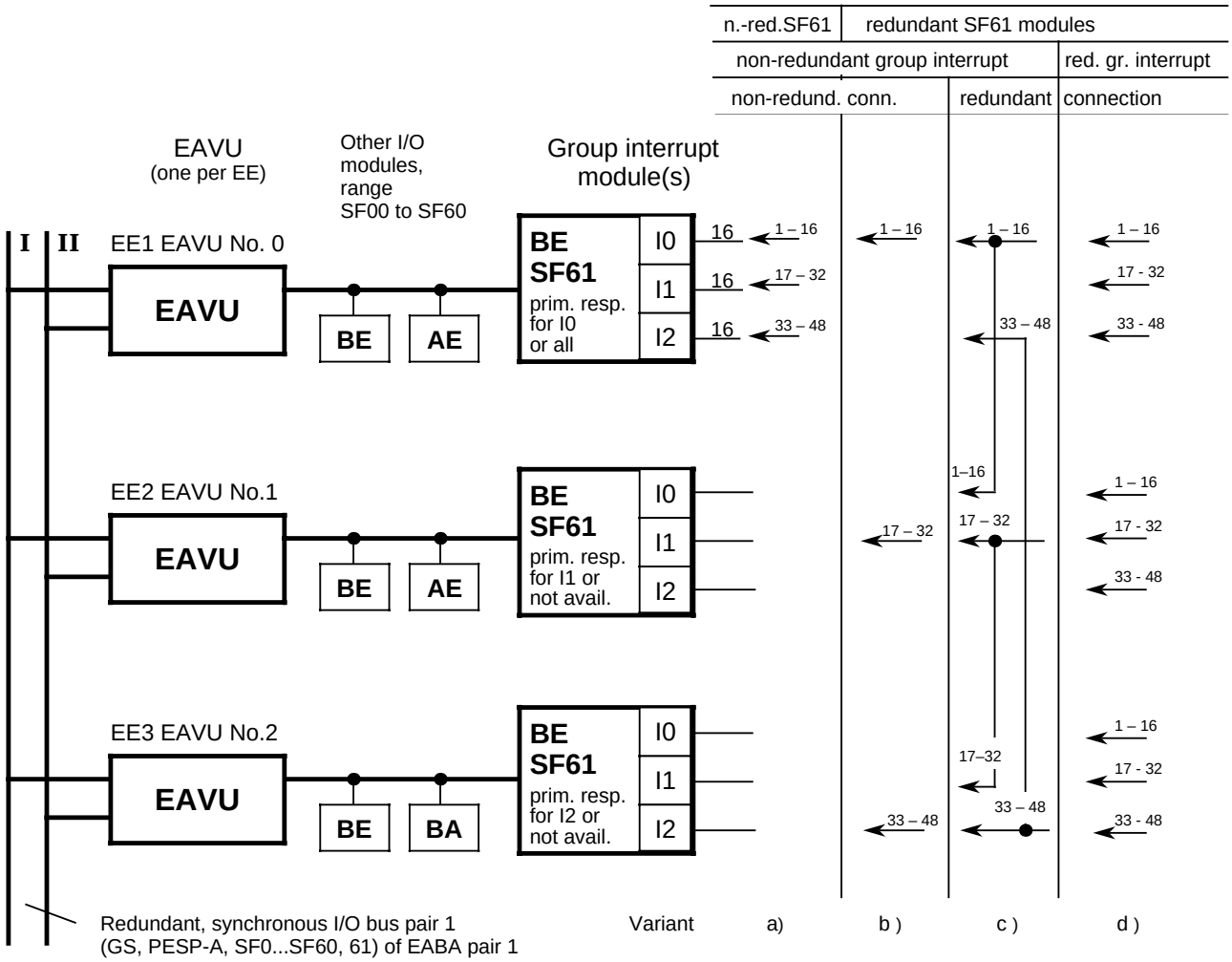


Fig. 3.9 Redundant configuration of group interrupt modules

The EAVU blocks alarm interrupts, as soon as their rate of occurrence exceeds a permissible value (interrupt inhibit due to faults). An alarm which occurs too often by mistake, e.g. due to a ”chattering” transmitter, also blocks further alarms which are only routed via the EAVU or SF61 concerned (in a non-redundant manner).

By connecting alarm signals to several SF61 modules which are redundant towards each other, you can not only prevent the loss of this alarm resulting from an SF61 or EAVU failure but also an alarm inhibit resulting from an error. Yet, on the other hand, an alarm signal connected several times would inhibit several SF61 if it occurred too often by mistake.

In this case, you must weigh the importance of the alarm against the probability that it will disturb ”chattering” signals.

In case of doubt, provide two (i.e. redundant design) interrupt generating signal transmitters (ASG) and two interrupt generating binary signal input modules (ABE) for important alarms and always route the alarm signals of redundant ABEs to redundant SF61 modules.

Fig. 3.9 shows examples of four variants of group alarm interconnections (PINT signals from interrupt-generating binary input modules) with SF61 group interrupt modules. As with an AS 235 system, up to 48 group alarms can be gathered, irrespective of the number of SF61 modules installed (1 to 3). In this respect there is no difference in the configuration of an AS 235 H system and a standard AS 235 system. Variants b), c), and d) contain double- or triple-redundant SF61 module configurations.

The individual items of the following summary mean:

Redundancy of ABE	:	Redundancy of the interrupt-generating binary input modules.
Redundancy of ASG	:	Redundancy of the interrupt-generating transducers or sensors that are connected to the interrupt-generating binary input modules.
Blocking of alarms	:	The extent of blocked alarms due to an excessive number of alarms that have been caused by a malfunction (e.g. ”chattering” interrupt-generating devices). The EAVU blocks alarms if the interrupt frequency exceeds a permissible value (interrupt inhibition due to a malfunction).
Interconnection	:	Group alarm interconnections (PINT signals from interrupt-generating binary input modules) with SF61 inputs.

Variant a):

Number of SF61	:	One, not redundant
Redundancy of ABE	:	None
Redundancy of ASG	:	None
Blocking of alarms	:	All alarms
Interconnection	:	Any SF61 input per group alarm
Disadvantage	:	All alarms will be lost after an interrupt inhibition due to a malfunction or when the SF61 module, its EAVU or its extension unit is switched off.

Variant b):

Number of SF61	:	Two or three, redundant.
Redundancy of ABE	:	None | double | triple
Redundancy of ASG	:	None | none or double | triple
Blocking of alarms	:	One out of 2 or 3 SF61 modules.
Interconnection	:	Distributed to the SF61 modules; only to SF61 inputs with primary responsibility.

Advantage	:	Up to 2/3 of the alarms remain functional due to the SF61 redundancy, even if one SF61 module (EE, EAVU) fails.
Disadvantage	:	The alarm from an interrupt-generating input module will be lost, even if this module, that has been (primarily) assigned to a defective SF61 module is not affected by the failure of this SF61 module (because it is installed in a different extension unit, for example), its extension unit, or its EAVU. Variants c) and d) avoid this advantage.

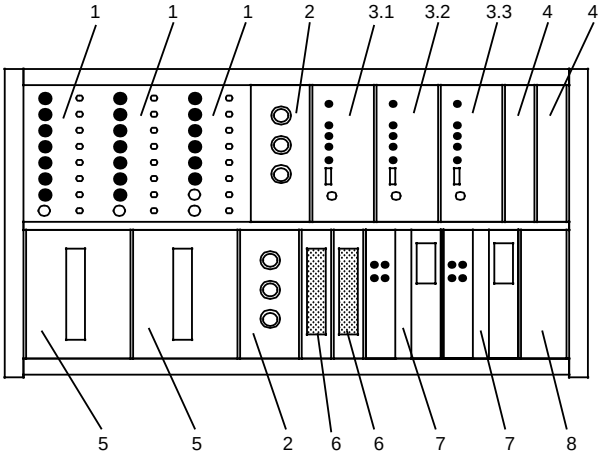
Variant c):

Number of SF61	:	Two or three, redundant.
Redundancy of ABE	:	None
Redundancy of ASG	:	None
Blocking of alarms	:	2 out of 3 SF61 modules
Interconnection	:	Branched to two identical SF61 inputs with primary and secondary responsibility
Advantage	:	Due to the multiple connections to the same inputs of several SF61 modules, the interrupt remains effective even if one of these SF61 modules has failed or is blocked.
Disadvantage	:	Due to the multiple connections to the same inputs of several SF61 modules, two out of three possible SF61 modules will be blocked if an excessive number of alarms occurs after a fault.

Variant d):

Number of SF61	:	Two or three, redundant.
Redundancy of ABE	:	Double | triple
Redundancy of ASG	:	Redundant or double | triple
Blocking alarms	:	One SF61 module if redundant interrupt-generating sensors have been used.
Interconnection	:	The two or three redundant group alarms are individually connected either to all three identical inputs or to the same inputs of the SF61 modules with primary or secondary responsibility.
Advantages	:	Only one ”logic” alarm (out of 48 possible alarms) is used for redundant group alarms. The user software only sees one single alarm, despite redundant interrupt-generating modules and redundant group alarms. This transparency of the group alarm redundancy simplifies programming in the alarm cycle.

3.2.3 Cabinet Power Supply Unit



1 Circuit breakers (F) for:

F1	CPU I	F9	EE 1	F17	PÜ 1
F2	CPU II	F10	EE 2	F18	PÜ 2
F3	PBT 1	F11	EE 3	F19	Fan 1 for GS
F4	PBT 2	F12	EE 4	F20	Fan 2 for ES
F5	MDE 1	F13	EE 5	F21	Fan 1 for ES
F6	MDE 2	F14	EE 6	F22	Fan 2 for ES
F7	UI	F15	EE7	F23	Heat exchanger for GS
F8	Reserve	F16	Reserve	F24	Heat exchanger for ES

2 Socket outlets for keyboard and mini floppy disk unit
3.1 ML alarm logic module for CPU I
3.2 ML alarm logic module for CPU II
3.3 ML alarm logic module for ES
4 VD11 diode module (option)
5 SED 31 cabinet power supply diode
6 Local bus connector (connection distribution unit)
7 UI bus converter unit (option)
8 BL blinking clock-pulse generator module

Fig. 3.10 AS 235 H cabinet power supply unit

- Circuit breakers

These circuit breakers enable individual areas to be switched on or off.

- Socket outlets

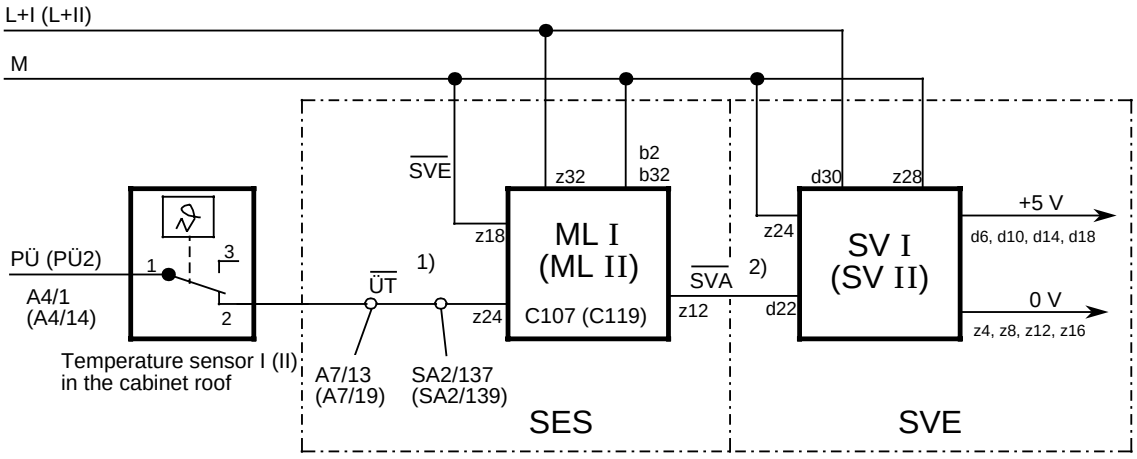
These socket outlets supply the 24-V voltage required for floppy disk drives and keyboards (2 per operator input unit).

- Alarm logic modules (ML)

The alarm logic modules I and II perform redundant processing of the cabinet alarms overtemperature (ÜT), fan contact (LK) and door contact (TK) for CPU I and CPU II. The signals from door and fan contacts are branched to the inputs of both alarm logic modules and are thus available in both CPUs. The two temperature sensor contacts of the basic cabinets are connected individually to ML I and ML II in order to prevent the two CPUs from being switched off due to an overtemperature signal (which might be faulty)
A CPU is shut down one minute after the associated temperature sensor in the basic cabinet has signalled that excess temperature has been reached.
The effect of the separation is that a fault of one ML or of one temperature sensor is tolerated.

In asynchronous mode, an I&C alarm (LTM) (S340) is issued by the associated CPU if a temperature sensor has responded. In synchronous mode, an I&C alarm (S340) is only issued after the temperature sensor of CPU I has responded; an I&C alarm is not issued for CPU II. The 5-V voltage to the CPU concerned is switched off one minute after the associated temperature sensor has responded (see Fig. 3.11).
Since the system has no fan in its standard configuration, the fan signal is connected such that an alarm is not pending. If fan modules are to be used in the system (e.g. heat exchanger contact or rack fans), the LK input can be connected to the alarm signal line of a fan assembly.
Setting the jumper X10/3-14 on the alarm logic modules I and II causes the two central units to be switched off after 1 minute (as for excess temperature). As this jumper setting reduces system availability, it should only be used as an exception. A rack fan or heat exchanger has only one fan contact and can therefore not act selectively upon one CPU. This means that both CPUs would be shut down one minute after one of these contacts had closed.

The third alarm logic module is responsible for monitoring the fuses and the extension cabinet



1) "1" signal (24 V) in faultless operation
2) "1" signal (5 V) in faultless operation

Fig. 3.11 Shutdown of the 5-V voltage for CPU I (CPU II) after an overtemperature state has been detected (the values for CPU II are in parentheses).

- VD11 diode module

This module isolates static and dynamic fault alarms and feeds them individually to an alarm system. The signals may be ORed and used, for example, for triggering a conventional signalling system (KM 17).

- SED cabinet power supply diode

Redundant and isolated 24-V cabinet power supply is performed via two SEDs.

Note:

Only really independent external supplies guarantee the desired redundancy.

- Local bus connection distribution unit

This unit is used for connecting the local bus line inside the cabinet with a local bus line from external devices.

- UI bus converter unit

The UI bus converter unit is the remote bus interface which converts the signals of the 20-m local bus into the 4-km remote bus signals. The line redundancy of the CS275 bus system is completely independent of the redundancy selected for the N-AS*I*N8-H local bus interface module.

- Blinking clock-pulse generator module (BL)

This module has the following functions:
- it provides the blinking clock pulse for the EAVU and I/O modules;
- it performs the lamp test (LT) of the field devices (optional via user wiring);
- it isolates the time synchronization signals (external minute pulses).

Blinking clock pulse

The blinking clock-pulse generator centrally generates two blinking signals (for basic and extension cabinet). This makes the fault LEDs on the I/O modules and EAVUs to blink synchronously in the event of a failure.

The fault LEDs on both cabinets may also be synchronized by a corresponding selection on the blinking clock-pulse generator.
The two blinking signals are protected by the PÜ1 and PÜ2 fuses on the clock-pulse generator module.
The LEDs on the blinking clock-pulse generator module front panel indicate that the voltages for BS, LT and clock synchronization are available.

Lamp test

The LT switch feeds a lamp test signal for cabinet 1 (SK1) and cabinet 2 (SK2) to the I/O subrack. The lamp test signal is protected by the LTV fuse.

Time synchronization

The system time can be synchronized by external minute pulses which must be connected to the blinking clock-pulse generator.
The two external signal lines (signal line + reference potential) are to be connected to the two (floating) inputs d22 and z20 by flat push-on connectors (6.3x0.8 mm).

3.2.4 Power Supply Unit

The SED31 cabinet power supply diodes are used for setting up a fault-tolerant 24-V bus.

The following voltages are derived from this +24 V voltage:

- L+ CPU I (and 5 V for CPU I via SV I)
- L+ CPU II (and 5 V for CPU II via SV II)
- 8 x L+ for extension units (and 5-V bus via SVME)
- L+ for fans, ML and operator interface units
- +24 V supply for directly connected configuring keyboard (without PBT)
- +24 V supply for mini floppy disk unit (MDE) and process communication keyboard (PBT).

The power supply units (SV I and SV II) in the basic unit are fed by +24 V from the cabinet power supply unit (SES). They are protected by the SES circuit breakers which can also be used for switching the power supply units on or off.

Each extension unit is provided with L+ (24 V) and M (0 V) via a circuit breaker in the cabinet power supply unit.

A power supply module at the rear of each extension unit generates the +5 V required for feeding the I/O modules via the bus board from this voltage.

PM and PS are fed to the extension units via fuses on the EAVU.

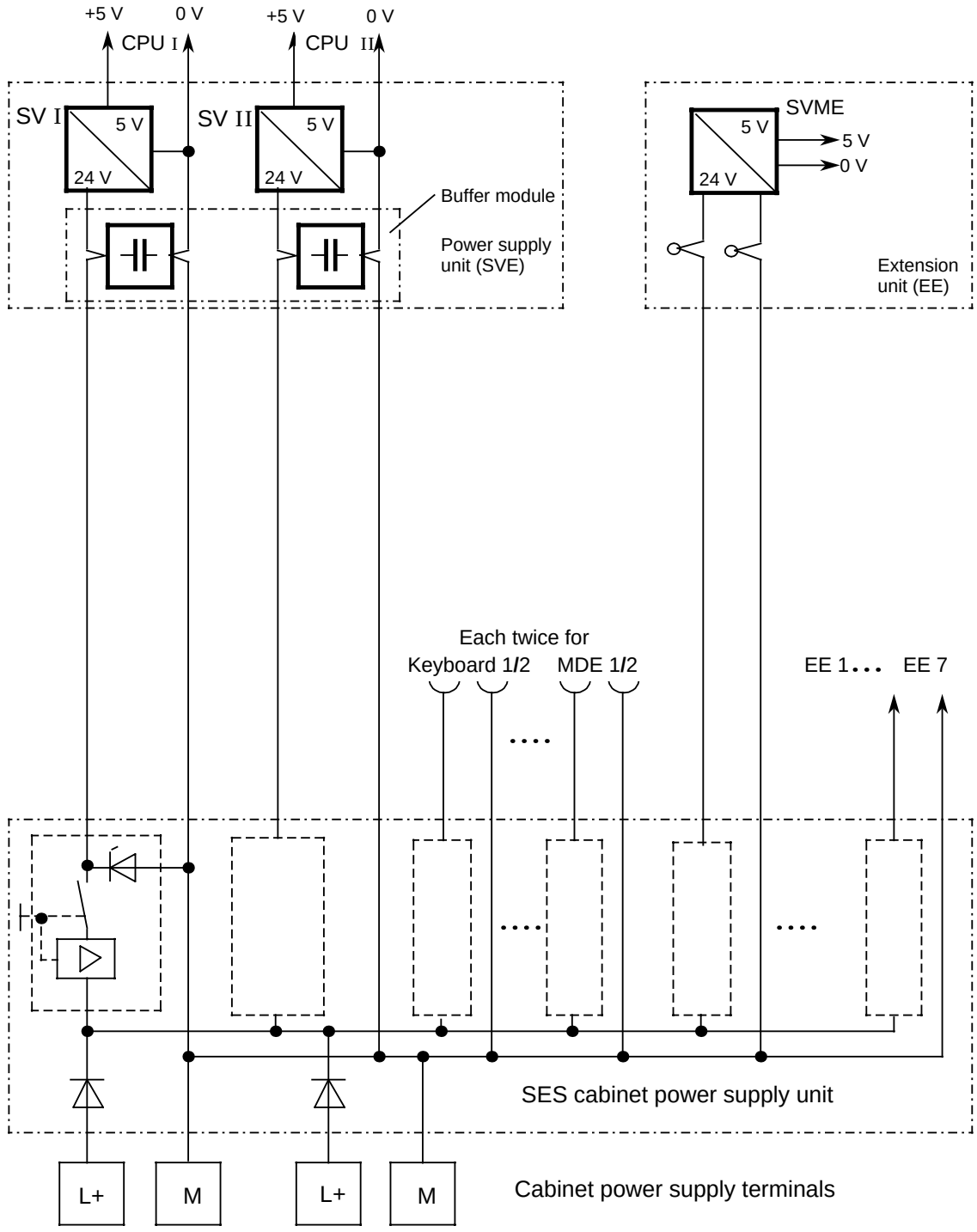


Fig. 3.12 Block diagram of the power distribution system in a cabinet

3.3 Failure

A fault locating diagnostic routine is started by an interrupt in each CPU if, during redundant operation, the system detects a discrepancy in the address, data or control signals of the two CPUs that has been caused by a hardware fault.

The following tests have been implemented in this diagnostic routine:

- CPU test
- test of the 8-bit bus
- test of the operator input channel interface modules
- test of the I/O bus
- test of the I/O bus interface modules
- test of all I/O comparator and switchover modules (EAVU)
- memory test

Fault finding may yield three different results:

1) The diagnostic routines cannot find a fault in either of the CPUs.

   The master CPU retains mastership; the other CPU transitions to passive mode.

2) A diagnostic routine can locate a fault in its local CPU.
   The master CPU transitions to failure mode and the standby CPU assumes mastership if the master CPU is faulty and in M/R or R/M state.
   The master CPU remains in master mode while the other CPU assumes passive mode if the master CPU is faulty and in M/B or B/M state. (Fault finding cannot be performed in backup mode. The subsequent state is therefore passive mode.)
   The backup CPU clears its user memory that contains inconsistent data if the fault has occurred in M/B or B/M state.
   The non-master CPU transitions to failure mode if it contains the fault.

3) Both diagnostic routines locate a fault in their respective CPU.
   The master CPU remains master, and the other CPU assumes failure mode. (This result is very unlikely as it implies a double fault.)

The CPU goes to STOP, and the other CPU assumes mastership at once if the diagnostic routine finds a fatal hardware fault.

A fault in backup mode causes the backup CPU to perform a restart which clears the user memory. Fault finding in the backup CPU is not performed in this case.

Fault finding is not performed either if a fault occurs during loading in synchronous operation. Loading is aborted, and both CPUs clear their memory contents.

The system responds to a fault after approximately 1 to 50 milliseconds (depends on the fault). The user program is not executed during this time which is required for executing fault finding routines (dead time).
Automatic synchronization after unsuccessful fault finding can be parameterized (see Chapter 2.5.1.1 in the AS 235 H Description, C79000-T8076-C484, in the Manual C79000-P9076-C084).

Since, in synchronous operation of CPU I, keyboard inputs are not read from BKA 2 or, in synchronous operation of CPU II, keyboard inputs from BKA 1 (by the USARTs), the following I&C alarms can be issued after both CPUs have entered asynchronous operation:

CPU signals: SYST.E3 * S 331
SYST.E3 * S 312

CPU signals: SYST.E2 * S 330
SYST.E2 * S 312

This indicates a character overflow in the USART of the corresponding BKA.
It is thus possible that the last keyboard input of the corresponding operator input channel has not been received correctly. Input should then be repeated.

3.3.1 Fault Delimitation

According to the requirements placed on a fault-tolerant system, the AS 235 H has its delimited (comprehensible) fault areas. Due to the fault-tolerance of the system, any hardware fault (provided that it does not occur repeatedly) can only cause a loss of redundancy. This only applies to an individual I/O module in the I/O system if a second redundant I/O module has been configured.

The fault delimitation areas (central processing unit, extension unit) are isolated from one another; a fault in a specific area has therefore no effect on other areas.

Early fault detection has been considered an important point in the implementation concept of fault delimitation and tolerance. It has been made possible by comparing in each cycle the data that has been processed in both CPUs.

Despite swift detection of individual faults, delays in process execution may occur after a fault has occurred (dead time 1 to 50 ms, typical: 5 ms). This dead time can be caused by fault locating software routines which delay input scans or output changes.

3.3.2 System Behaviour

Both CPUs read and write their data synchronously in normal or redundant operation.

Comparator coupler module (VKB) and I/O comparator and switchover modules (EAVU) monitor synchronous operation (data identity). The VKB or an EAVU sends a **PU5 interrupt** to both central processing units if it detects a discrepancy on the monitored system buses. As a result, both CPUs halt process execution.

Initiated by the PU5 alarm, the (identical) software stored in the memories of both CPUs begins a fault locating routine which scans the other CPU for primary fault signals. The faultless CPU assumes (or retains) mastership, and process execution is continued if the fault can be located during this procedure.

If the primary fault location does not yield the expected result, either CPU starts a selftest which includes the CPU itself, the memory module and the data paths to the process level, including the EAVU.

While the primary fault location is terminated after a few milliseconds, the extensive selftest routines may cause long delays in process execution (up to a dead time of 50 ms).

Any fault which is detected by permanent comparison causes asynchronous operation of the two CPUs. The same result can obviously be achieved by direct intervention (e.g. de-activating or resetting one CPU). Asynchronous operation means that all connections between the central processing units (including I/O buses) are cleared. Comparison is not performed either. In order to facilitate fault location, address and control signals are written into dedicated registers on the VKB and EAVU modules at the moment when the fault occurred. These registers are then used as starting points for fault analysis.

Once they operate asynchronously, both subsystems react as two individual systems. The fault tolerance in the CPU has ceased until the next synchronization run is performed.

- The three signals NAU, DS, ZRS

Three signals - NAU, DS, and ZRS - enable the CPU to be started or stopped in a controlled manner:

NAU = power failure alarm
D = data save (protective signal for the memory module)
ZRS = central reset

Once the processor recognizes an active **NAU** signal, it terminates the currently executed instruction and becomes inactive. The next instruction from the memory is not executed. The memory is disabled by the **DS** signal once the last instruction has been terminated. The above signal sequence is maintained when the system is switched on. The CPU cannot access the memory as long as the memory is disabled by an active **DS** signals.

The supply voltage disappears:

NAU becomes active: A certain time is left for the central processor to terminate instruction execution.
DS becomes active: The memory is disabled. The processor can neither read from the memory nor write into the memory.

The **ZRS** signal causes the central processor to start from a defined basic state or to remain in this state.

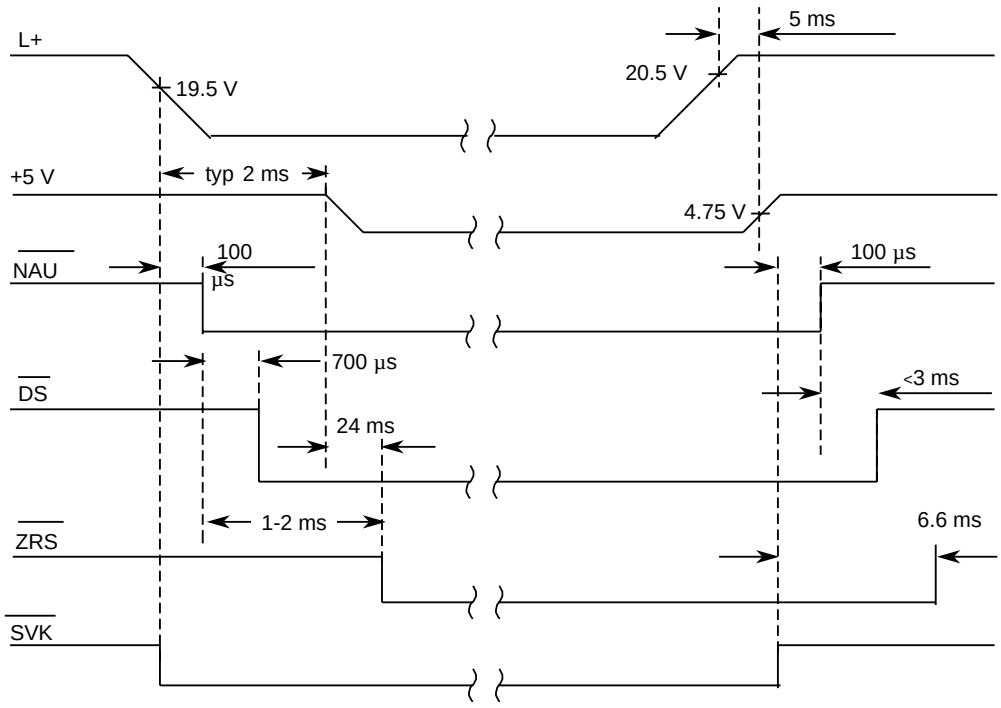


Fig. 3.13 Control signals from the power supply module to the central processor

A minimum delay of 700 µ is necessary between the NAU and DS edges when the power supply unit is switched off.
The central processor first executes an initialization routine after the supply voltage has been switched on or recovered after a failure.

- Indications and messages

A system message can be a status or fault message from the system. In the event of a failure, the cause of the fault is determined and signalled by system routines during operation. A code is displayed on the VDU message line after each fault message. This code can be used for analyzing the fault.
The codes and the associated explanations can be found in the AS 235 Description (AS 235: C79000-G8076-C416).

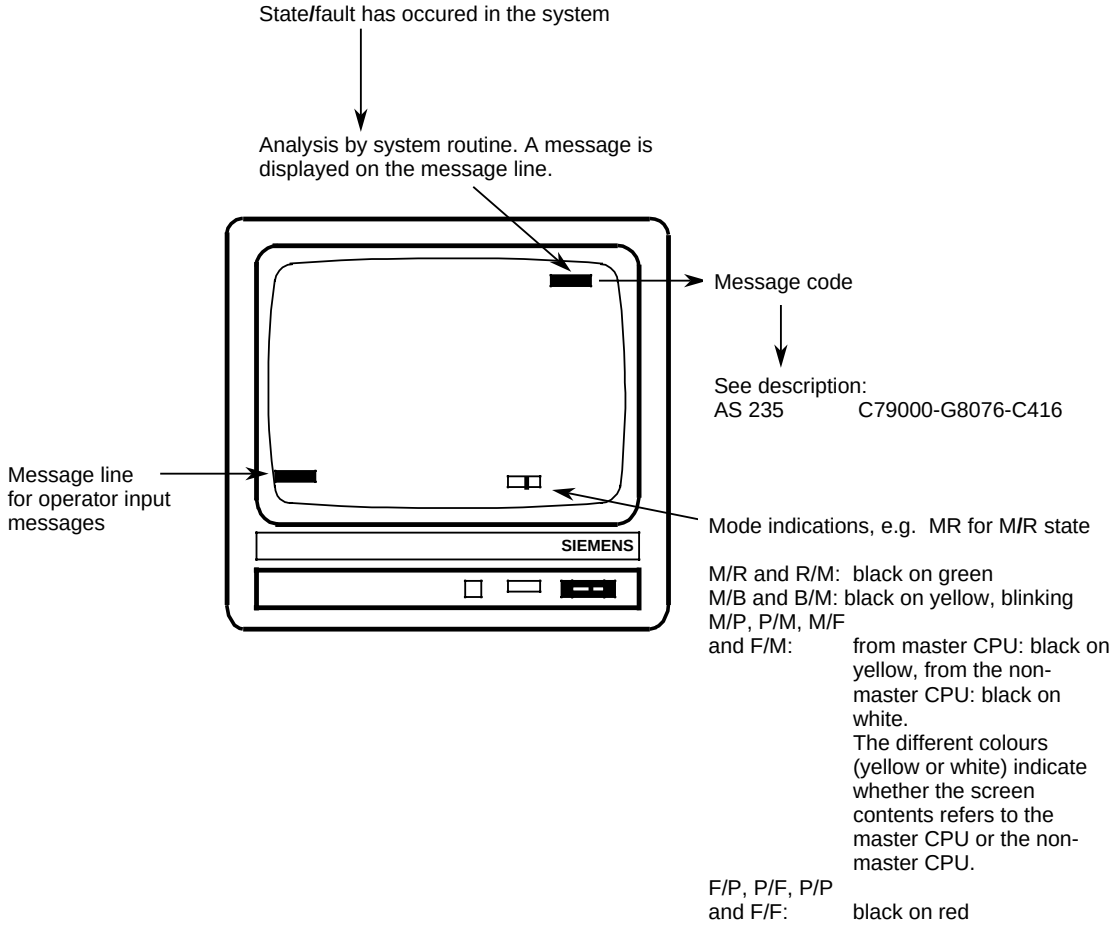


Fig. 3.14 System message on the color monitor

Fault messages as a reaction to command inputs are displayed on the operator input message line.

Example:
An attempt has been made to file the RAM contents on a floppy disk which has not been formatted properly.
The system detects this deficiency and issues the error code F447 on the VDU message line once the filing command has been entered.
In the AS Description, error code F447 is explained as " floppy disk not formatted".

Certain functions and faults are indicated on the EAVU and the central processing unit modules in addition to the system messages on the monitor.

– Memory module (SP)

The mode or faults are only indicated during initial loading.

LED		Function/fault
red	green	
OFF	ON	Initial loading in progress
OFF	OFF	Initial loading terminated without fault
Blinking	OFF	No system floppy disk
ON	OFF	Fault: - mini floppy disk interface defective - drive not ready - file 1 defective - backup file defective - label read error - checksum error
ON	ON	Defective RAM module or floppy disk

– CPU 235 H

The STOP lamp indicates a stop of the CPU which has been caused by a memory fault or a hardware fault in the central processing unit.

The CPU can also be stopped after start-up if the user memory structure has been disturbed by illegal interferences.

The CPU is set to a defined stop before an indicated power failure (NAU) occurs.

Caution

The CPU may also be stopped by "Halt" input (in STO mode). ZRS returns the CPU to RUN mode (during service work only).
In "halt" state there is no further processing because there is no redundancy.

– Mini floppy disk interface module (MDA)

The red LED is lit during the start-up phase of the module.
The module is ready when the LED is extinguished. The LED lights up if a fault is detected during initialization.

A defect in the FIFO, RAM or FDC is indicated by the following blinking sequence:

1 x blinking	FIFO defective	(queuing hierarchy disturbed)
2 x blinking	RAM defective	(write/read memory defective)
3 x blinking	FDC defective	(floppy disk controller defective)

The module is defective in all these cases.

- I/O bus interface module (EABA)

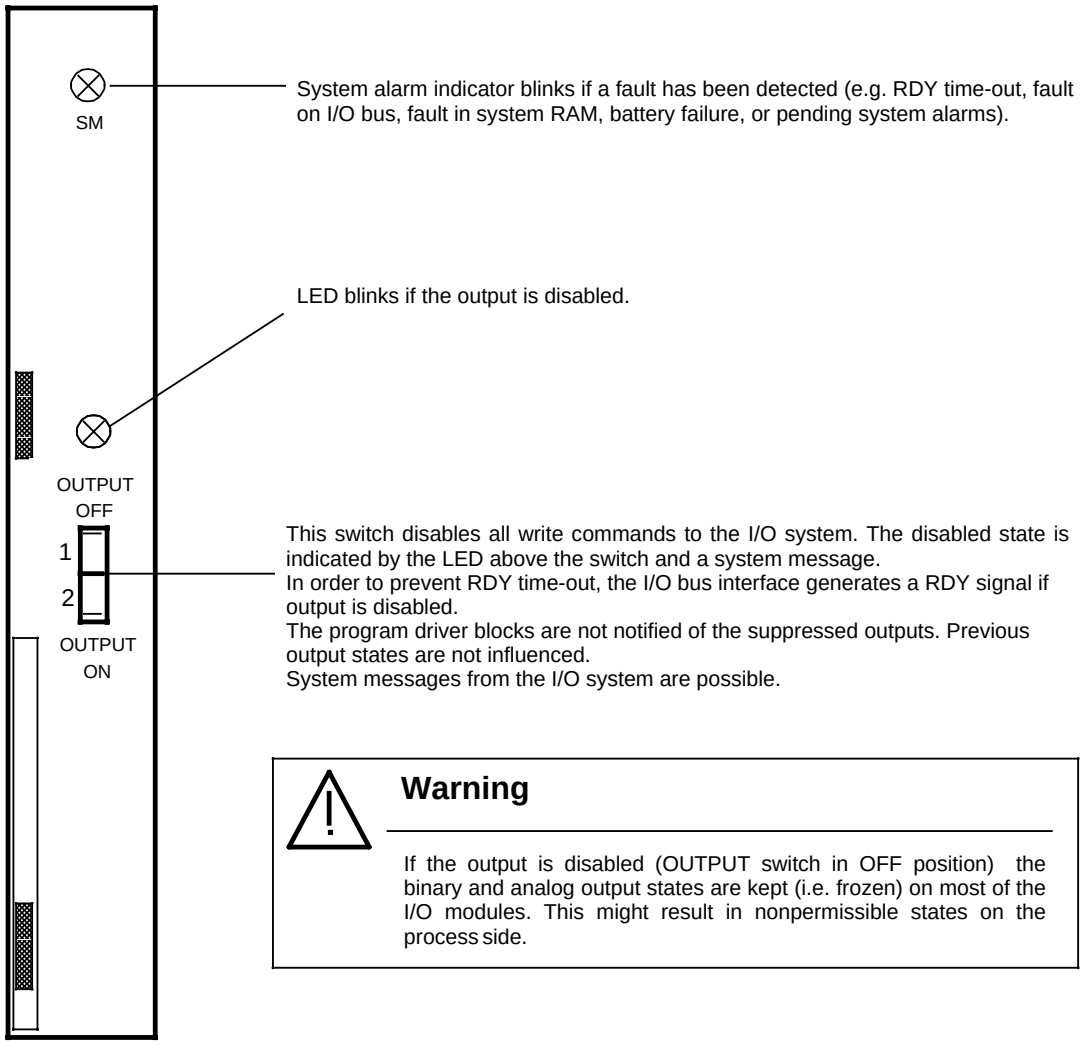


Fig. 3.15 EABA front panel (6DS1 312-8BB)

- Comparator coupler module (VKB)

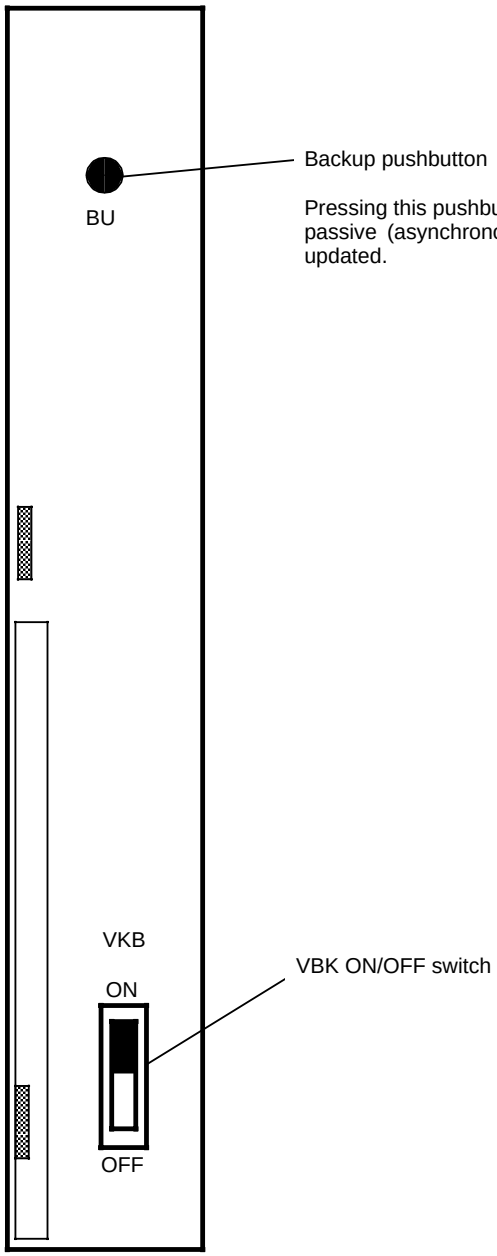


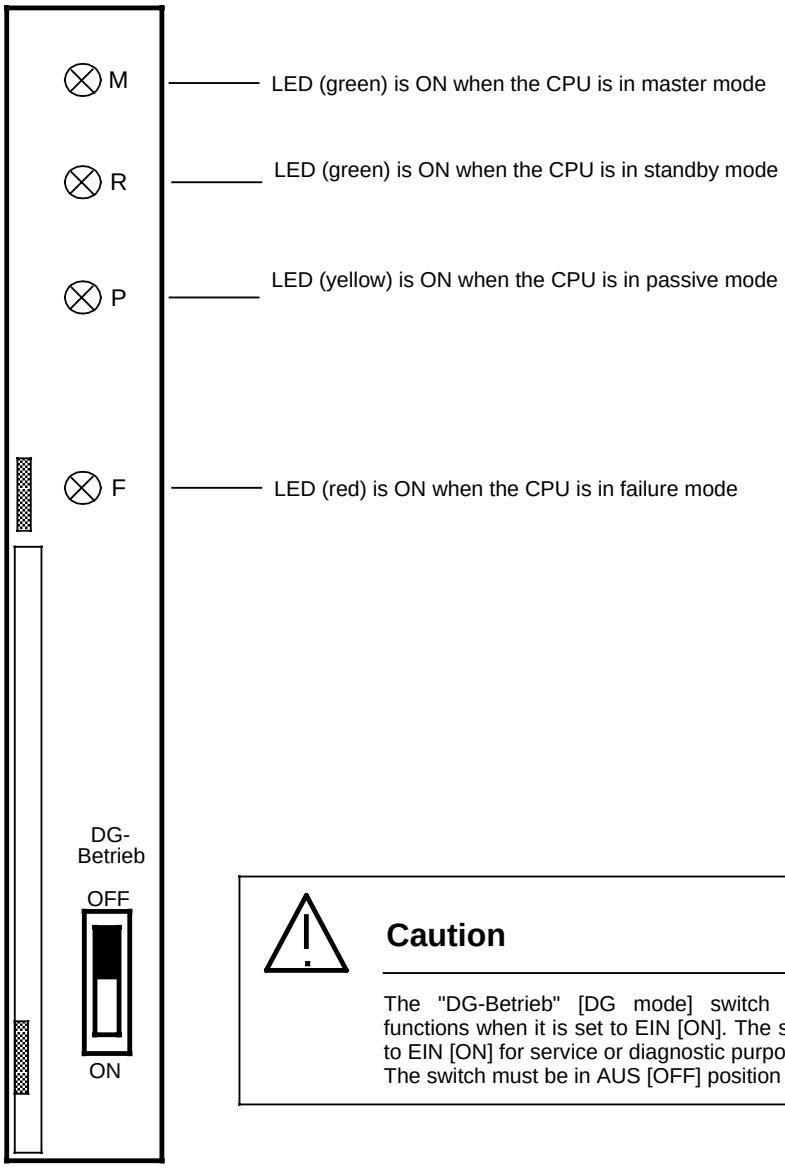
Fig. 3.16 VKB front panel

The states and messages stored on the module are read and may be output via monitor or printer.

Caution

The comparator coupler module (VKB) may only be removed during operation after the front panel switch has been set to AUS [OFF].
The switch may only be actuated in asynchronous operation.

– Synchronization module (SB)



Caution

The "DG-Betrieb" [DG mode] switch disables important monitoring functions when it is set to EIN [ON]. The switch may therefore only be set to EIN [ON] for service or diagnostic purposes.
The switch must be in AUS [OFF] position during normal operation.

Fig. 3.17 SB front panel

The P and R LEDs light up simultaneously if one of the CPUs is in backup mode. All LEDs are OFF for approximately two seconds during start-up.
An LED failure can be detected by comparing the mode indicators on the SB modules with the mode information on the monitor.

The states and messages stored on the module are read and may be output on the monitor or printer.

– I/O comparator and switchover module (EAVU)

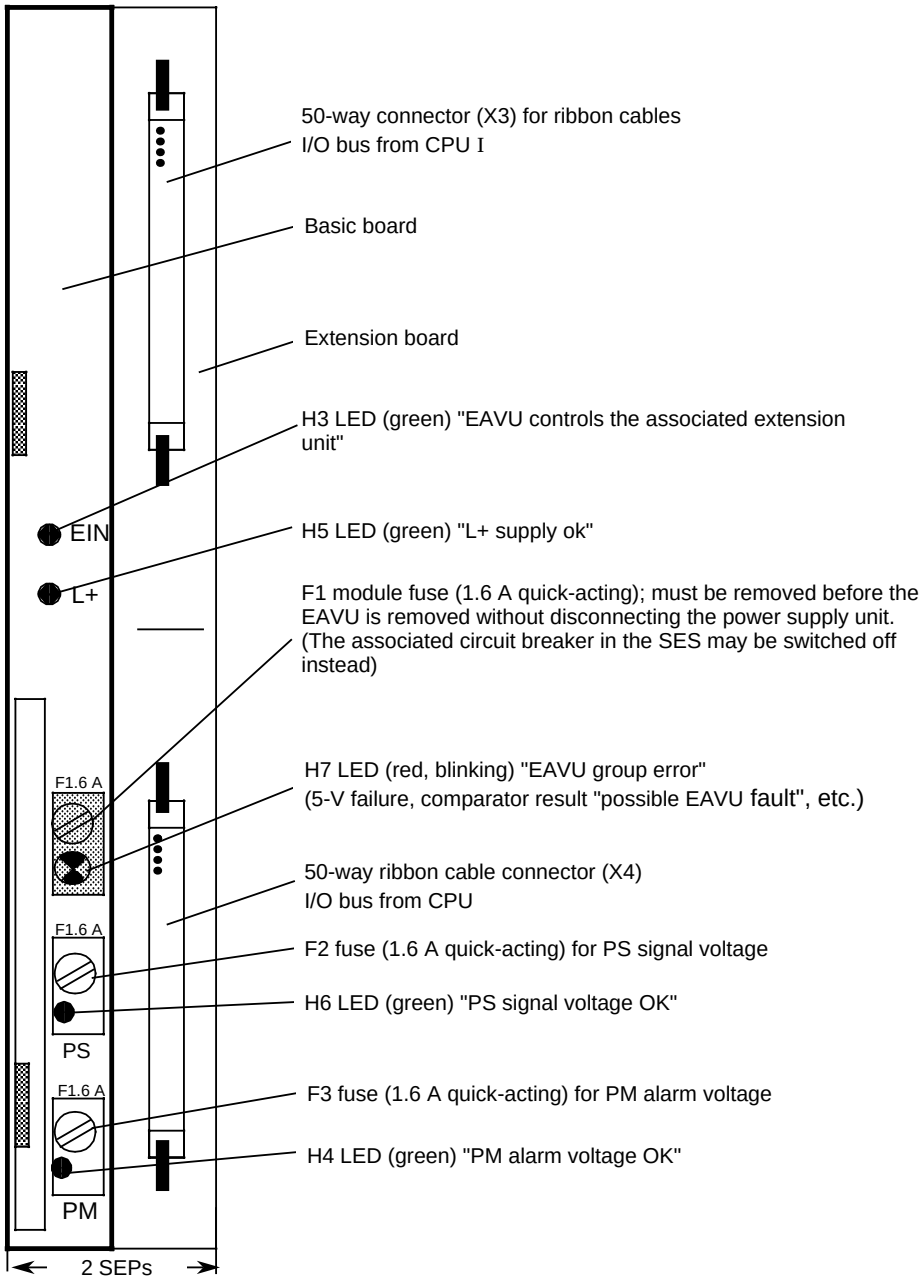


Fig. 3.18 EAVU front panel

3.3.3 Cold Restart, Warm Restart

The following reactions are possible after a CPU restart in the AS 235 H automation system has been performed:

- Restart after a power failure

There are two possibilities for a restart after a power failure:

RAM is battery-backed:	The system continues operation with the interrupted user structure once voltage has recovered. The individual cycle levels are restarted for execution. The internal time-of-the-day is cleared with 6DS1837-8.. operation.
RAM is not battery-backed:	The system clears the entire RAM area and is ready for loading after voltage recovery. This means that the system software must be loaded.

- Restart after a processor reset (ZRS)

A hardware reset that has been initiated by pressing the ZRS pushbutton on the CPU module has the same effect as a restart after voltage recovery. The mode at the moment when ZRS was pressed is retained (STA or STO mode, i.e. block execution started or stopped). The connected standard and process peripherals are put in their initial states.

- Restart after a system software reset (RSOF)

"RSOF;" input is only accepted by the system after execution has been stopped in the automation system ("STO;" input). RSOF re-organizes the whole main memory. The memory is compressed and any gaps that have been caused by configuration and programming (clearing blocks and instructions) are removed. The system is in STO mode once re-organization has been terminated; the time-of-the-day is retained.

The system starts a **one-time** execution of all specified RESTART programs during each restart. The user must specify his special requirements for such a case in separate RESTART programs in order to prevent difficulties during restart.

The following points must be observed if filing must be performed in STA mode (i.e. in on-line mode):

- I&C alarms may not be pending (enter QF; to check).
- The filed memory contains the latest states of all field devices connected.
- This data is used when such a dump is re-loaded.
- The user must ensure that the field devices of such a system are set to defined states when the system is restarted. This should be implemented in RESTART programs. These include, for example:

  Setting process image default values
  Establishing defined actuator positions
  Setting controller modes, etc.

The mode after start-up may be master, passive or failure. Cf. Manual (C79000-G8076-C416).

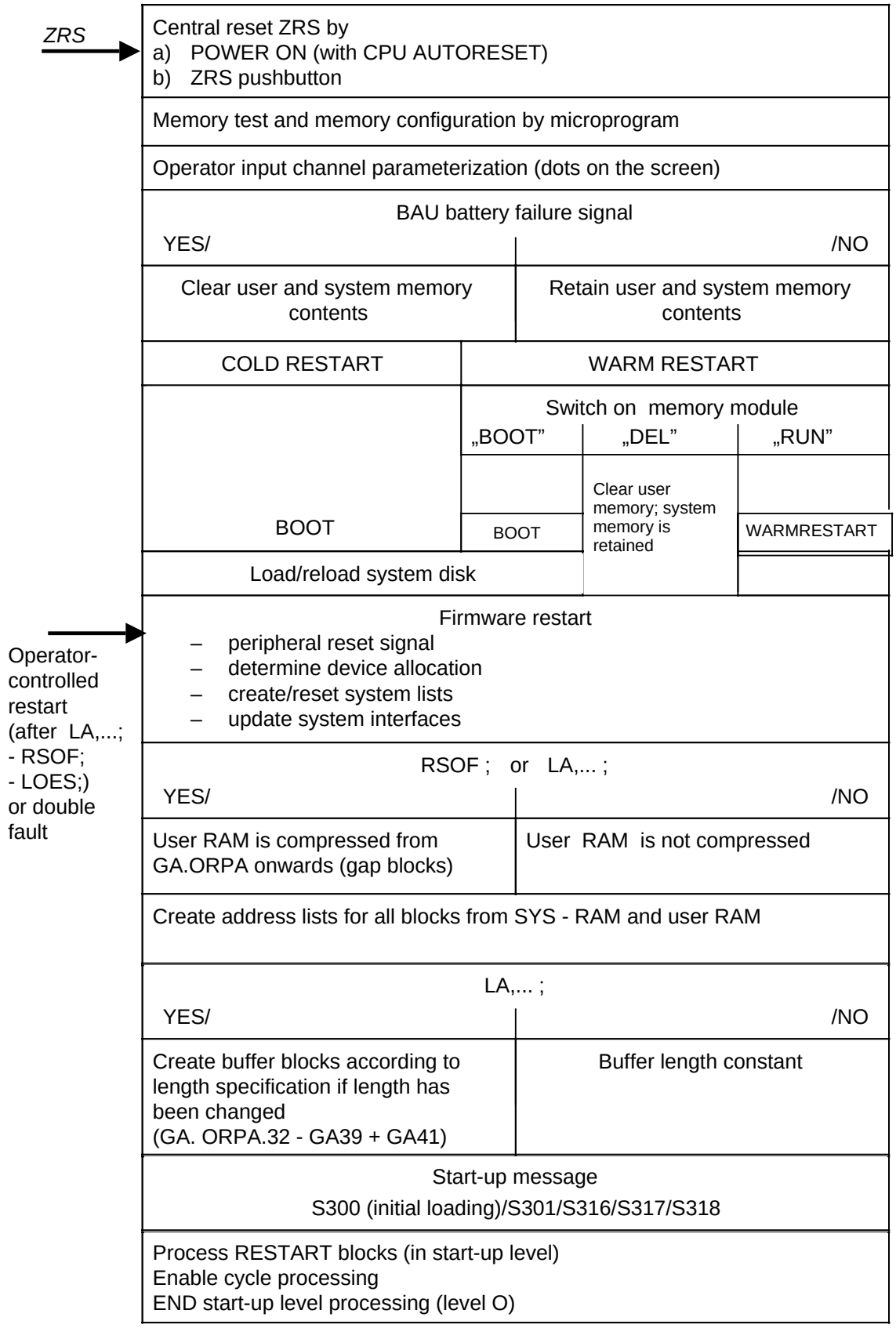


Fig.3.19 Cold restart/warm restart execution level

4 Installation

4.1 General

TELEPERM M is a distributed system. The cabinets are designed for the ambient temperatures prevailing at the point of installation. They are fitted with modules and are system-tested before shipment. Any transportation damage to the cabinets or their contents must be reported to the sales department without delay.

Rooms intended for the installation of cabinets should be amply dimensioned and should have a clear height of about 3 m for effective removal of the heat loss and to permit top cable entry if required.

The clear openings required for hauling the cabinets into the rooms must be at least 2500 mm x 2000 mm for three-unit cabinet groups (2500 x 1000 mm for individual cabinets).

Cabinet rooms should be air-conditioned if the specified ambient conditions cannot be met.

Anti-dust floor coverings having a discharge resistance of 10^8 must be used. The corresponding value for control rooms with AS 235 H systems should preferably be 10^7 . The indentation hardness should be 80 to 100 N/mm^2. Free-standing cabinets in large factory areas should be installed at a distance of at least five meters from interference sources (e.g. welding stations, transformers, power converters, or relays).

The installation team verifies before installation whether the required values are met.

Earthing and screening regulations must be met in order to enable a noise-immune function concerning the electromagnetic compatibility (EMC) to be maintained.

When connecting external units, no connection is permitted between the local earth or the protective earth of the units and the signal lines to the cabinet. Exception: isolating inputs or outputs.

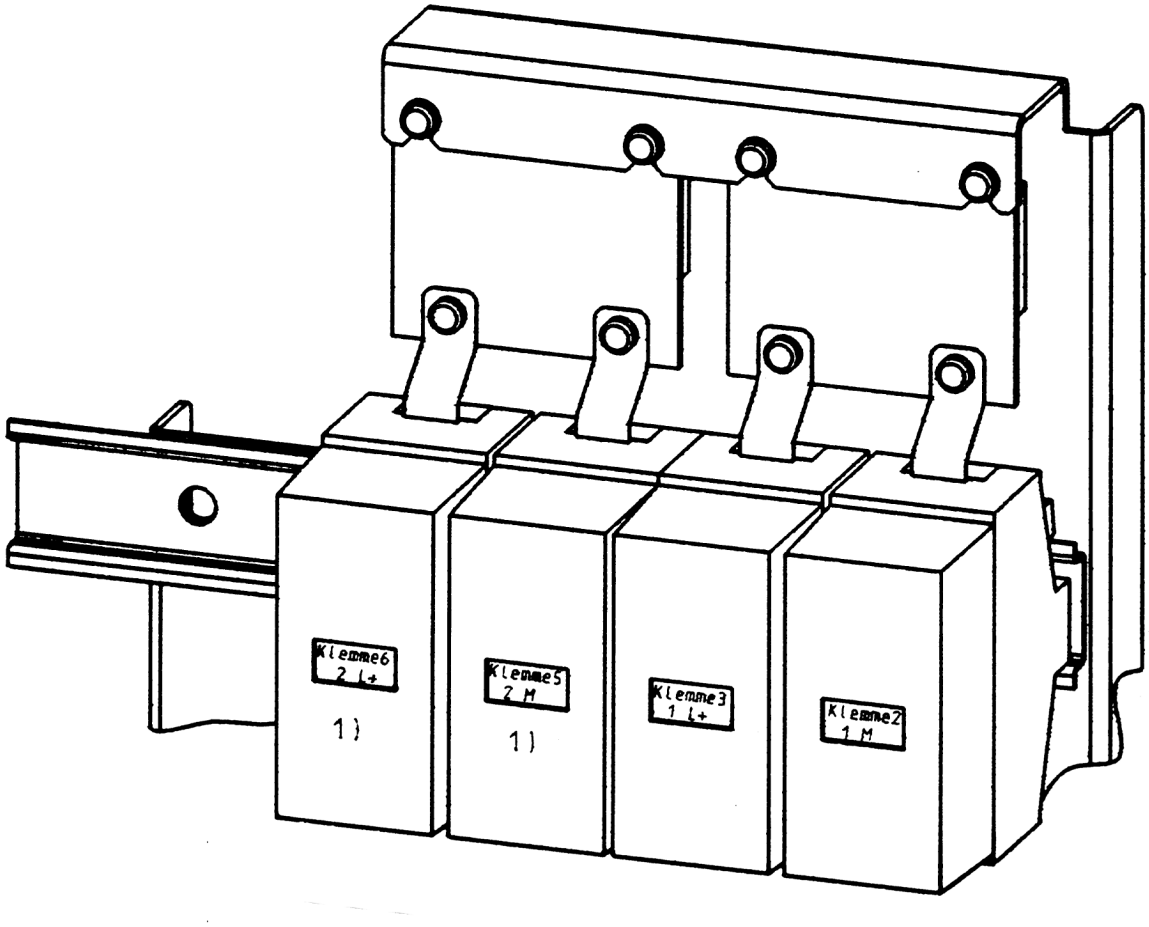
Measuring and signal cables must be laid separately from power or high-voltage cables.

All signal lines must be screened; both ends of the screens must be connected to earth.

The system supply voltages must be switched off when the system is installed.

Rooms intended for the installation of operator control and monitoring units must be adequately ventilated and illuminated.

4.2 Connecting the Supply Voltage



L+ 24 V cabinet supply voltage
M Reference potential of the 24 V
1) Option

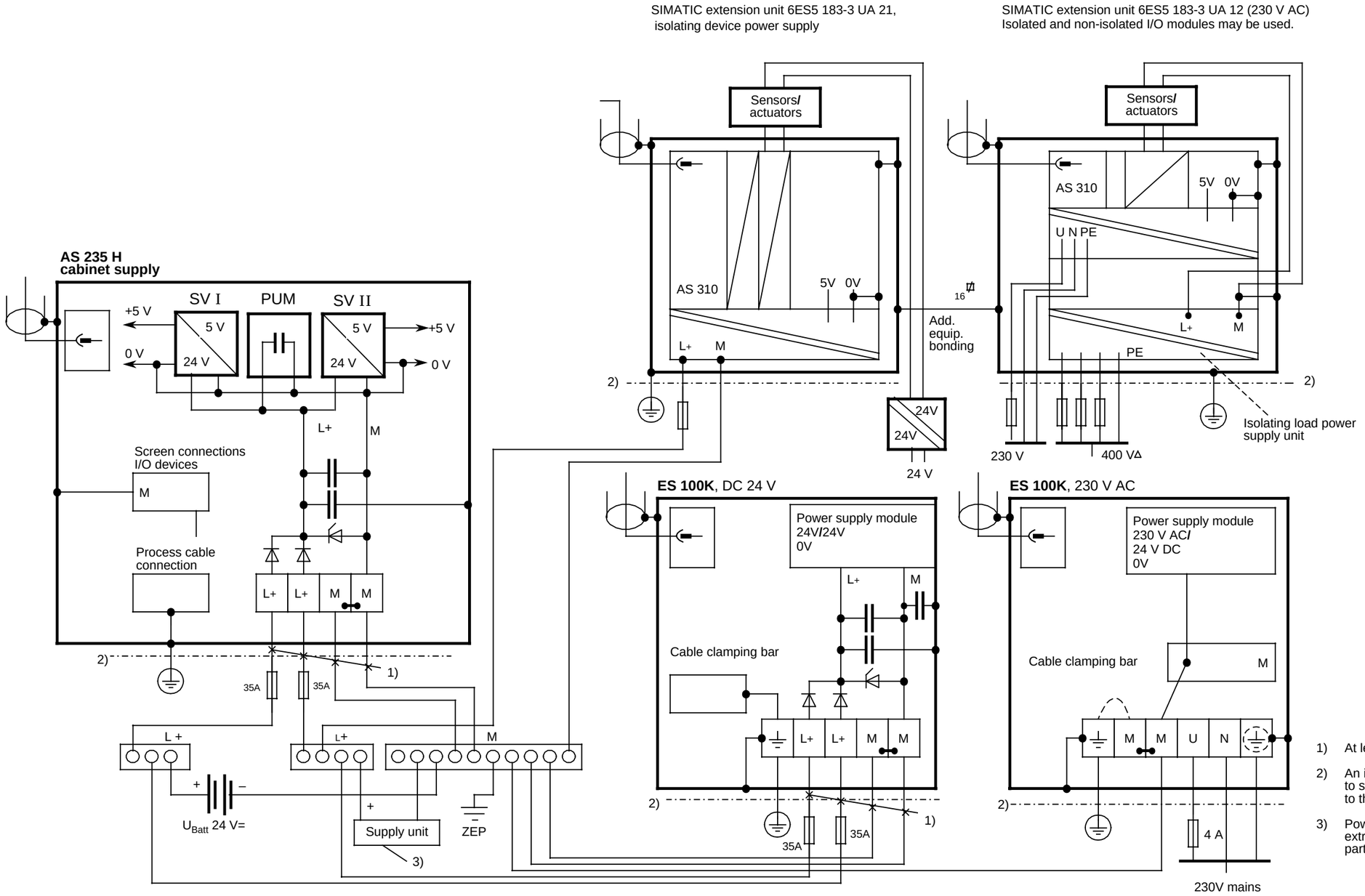
Fig.4.1 Assignment of cabinet supply terminals

Caution

Only voltages ”generated in an electrically safe and separated manner” may be used as supply voltages.

The supply terminals are accessible from the rear. They accommodate multi-core conductors with a cross-section between 35 and 120 mm^2.

4.3 Grounding Concept



1) At least 10 , depends on configuration

2) An isolated facility should be provided to switch off the supplied voltage prior to the point of entry into the cabinet.

3) Power supply unit with safely isolated extra-low voltage (to VDE 0100, part 410 and VDE 106, part 101).

Fig. 4.2 Connecting the AS 235 H system with other systems

4.3.1 Central Grounding Point

The central grounding point consists of two bars for

M Reference potential of L+
E Ground

The two bars are connected by removable straps. Switch off the system, remove the straps, and check for ground faults if necessary.

The central grounding point should be installed in the vicinity of the location where most of the cabinets have been installed. A suitable place is, for example, the room that accommodates the 24-V DC power supply.
Connect the central grounding point via several grounding cables (e.g. copper cables of 70mm^2 each) that have been laid as straight as possible with different points of the grounding network of the internal building grounding system. Star-shaped grounding is preferred, loops should be avoided (see Fig. 4.4).

Choose short ways between the central grounding point, the 24-V system, and the electronics cabinet.

The required minimum conductor cross section of power supply cables is 35 mm^2 provided that the configuring department does not require larger cross-sections. Screened cables should be used if the distance to the 24-V system is greater than 25 meters or if interference is to be expected. The screen should then be connected to ground at both ends (see Fig. 4.5).
Connect the screens of process cables via incosporated screen bars to the grounding point of the building ground with 4 screw connections (see Fig. 4.3).
The screen connections of bus components and peripherals are directly connected to cabinet earth.
The screens of the measuring and signal cables are only connected inside the same grounding area (central grounding point).
Cabinet mounting frames (e.g. anchoring rails, flat or U-shaped steel bars) must repeatedly and via different paths be connected to the grounding line. The mounting frames for adjacent rows of cabinets must be linked by additional transverse bars (e.g. made from hot-galvanized steel tape, 305 mm; at distances of approx. 2 meters, see Fig. 4.4). Ensure, when installing the cabinets on a false floor, that the supporting structure represents a conductive connection of the cabinet rows.

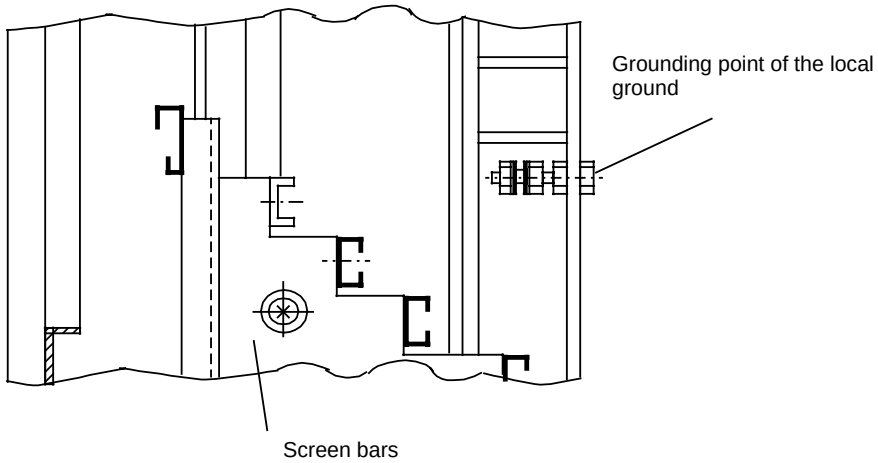
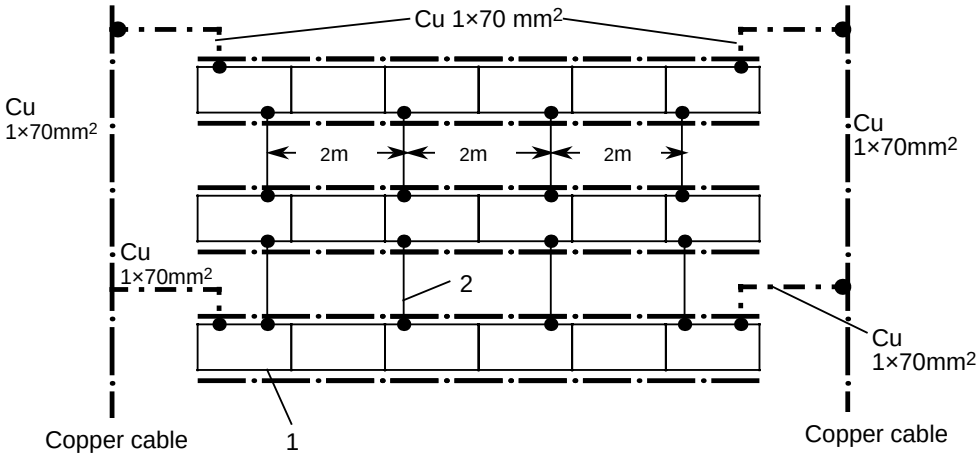


Fig. 4.3 Ground connection of screen bars



1 Cabinet row
2 Ground connection

Fig. 4.4 Grounding of cabinet rows

If rectifier units are used for producing the DC 24 V voltage for the components of the TELEPERM M process control system, these supplies must be connected to a TN-C or TN-S mains to VDE 0100 part 310.

Connect the star point of the primary circuit of the supply unit to N or PEN of the mains.

Please contact the configuring department if there is an IT mains without N on site.

In order to guarantee protection against hazardous electric shocks, the DC 24-V voltage and the devices with a metallic enclosure that are fed by the 24-V DC must satisfy the requirements placed upon "functional extra-low voltages" with safe isolation to VDE 0100, part 410.

The cabinet itself must be connected to the protective ground conductor via the ground connection provided:

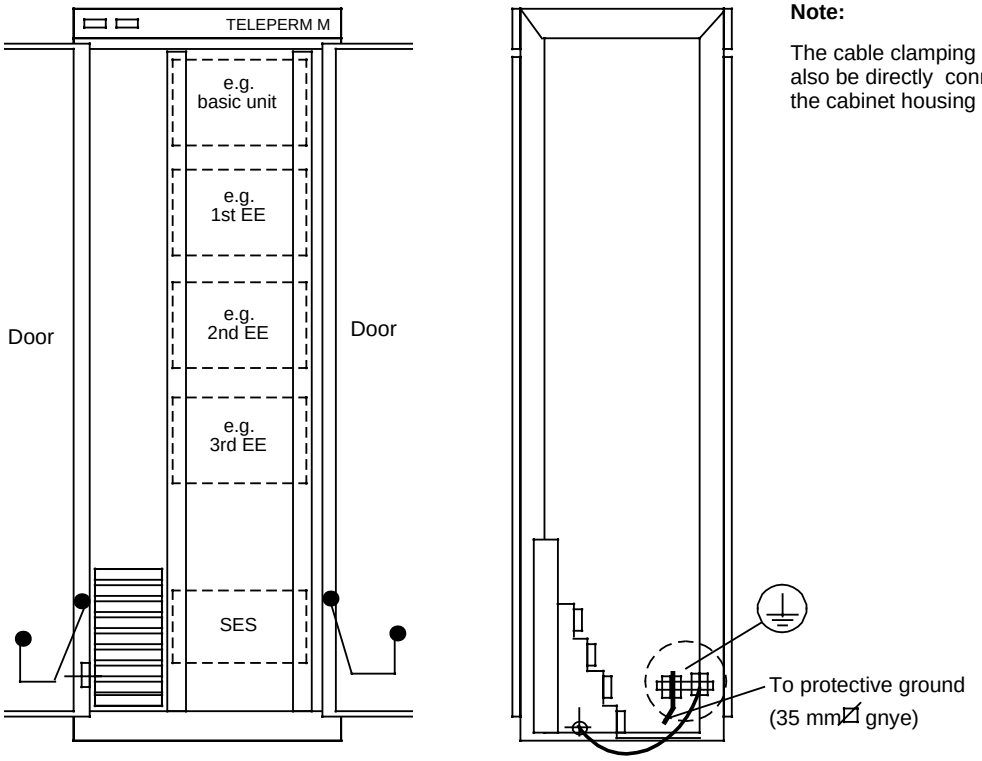


Fig. 4.5 Connecting the cabinet to protective ground

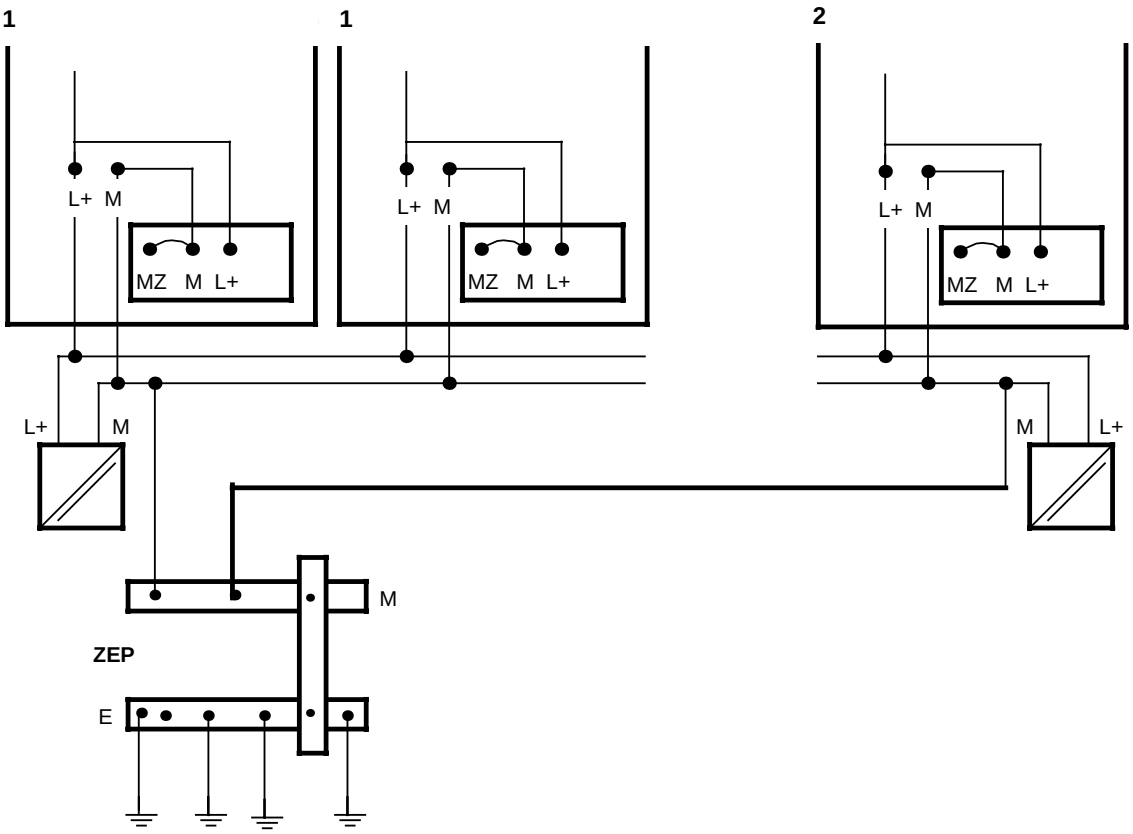
If possible connect each cabinet to the grounding system via a copper cable 16 mm^2. While cabinet groups up to 3 m require at least one connection, cabinet groups that are longer than 3 m must be grounded at both ends.
It is assumed that all metallic enclosures of subracks and modules inside the cabinet be connected with the grounding connection.

4.3.2 Grounding the M Potential

The M bars of all 24-V switchgears are combined at the central grounding point and connected to the grounding bar via a removable strap. The reference potential M has thus only one common point with ground.

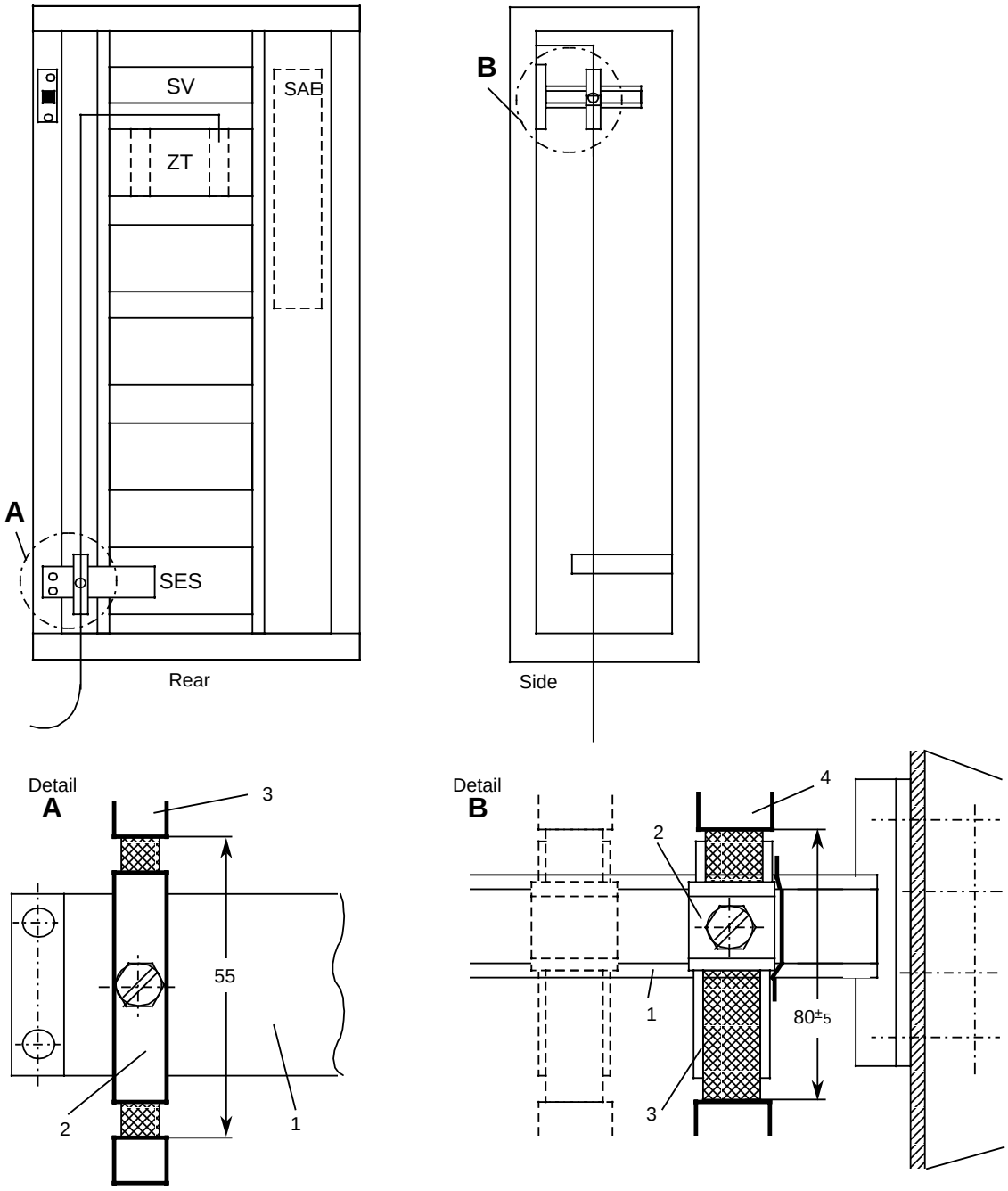
A system which is known as "0-V islands" is set up inside the cabinets. A 0-V island consists of one or more electronic unit(s) with a common M or MZ. A 0-V island is always assigned to a power supply unit.

Data communication between the individual devices of a 0-V island takes place via the 20-m local bus. The 0-V islands of a system are interconnected via the 4-km remote bus. Direct connections for analog or binary signals are possible between two 0-V islands. The signal connections must either be of high impedance or electrically isolated in order to avoid equalizing currents on the signal lines.



1 Two islands with a common power supply unit
2 One island with a separate power supply unit
M Current-carrying earth
MZ Dead earth (for voltage measurement only)

Fig. 4.7 Grounding the M potential



1 Grounding bar
2 Cable clamp
3 Keyboard and printer cable

1 C bar
2 Cable clamp
3 Cradle
4 Monitor cable

Fig. 4.8 Connecting cable screens of monitor, printer and keyboard cables

The end of the monitor cables inside the cabinet should be long enough that they can either be connected to the video relay output or to the corresponding input of the operator input channel interface module.

4.4 Connecting the Process Signal Cables

Process signals must always be conveyed on screened cables and separated from circuits that carry voltages above 60 V. The cables must consist of twisted pairs; each signal circuit should be connected to one pair. Crosstalk can be avoided if separate cables are used for analog and binary signals. Analog position feedback signals and actuator limit switch signals can be combined in one cable.
The process cables enter the AS cabinet from the top or the bottom. The cable screens must be connected to the cable clamping bars. Distinction must be made between braided screens (Fig. 4.11) and foil screens (Fig. 4.12). The process cables are connected in maxi-termi-point technique to the SAE process connection element or directly to the extension units.

- Cable types

Any installation cables for industrial electronics (SIMATIC cables) with twisted pairs of colour-coded cores grouped in bundles may be used as process signal cables. These cables with stranded or solid core (0.5 mm^2 cross section, 0.8 mm diameter) have a static screen.

Cable designation			Used for
A-Y (ST)	YY	n x 2 x 0.8/1.4 BdSi	Underground cable routing [1)]
J-Y (ST)	Y	n x 2 x 0.8/1.4 BdSi	Normal applications
J-LiYY		n x 2 x 0.5/1.6 BdSi	Miniaturized control rooms
J-LiYCY		n x 2 x 0.5/1.6 BdSi	Vibration and shock, connectors

1) Underground cable routing is not recommended. If underground routing is absolutely necessary ensure that the transmitted signals are not corrupted.

A Outdoor cable
C Braided screen
Bd Bundling
Si SIMATIC colors
J Installation cable
(ST) Static screen
Li Stranded conductor
Y PVC insulation

Table 4.1 Installation cables for industrial electronics

- Core color code

The twisted pairs are identified by the eight basic colors of the insulator.

Core	1	2	3	4	5	6	7	8
Pair	1		2		3		4	
Color	bl	rd	gr	ye	gn	br	wh	bk

bl - blue
br - brown
bk - black
gn - green
gr - grey
rd - red
wh - white
ye - yellow

Table 4.2 Basic colors of the core insulators in a bundle

One color group consists of four pairs that make up a bundle. The individual cores of a bundle have an additional ring code which helps avoiding confusion of the same color from different bundles. Bundle count starts with the inner layer.

- Laying process cables

Process cables should be laid in earthed cable racks, separate from power cables (200 mm minimum clearance). Outdoor cables should be laid in cable ducts; they must be provided with an additional earthed screen (armour). All cores must be provided with suitable surge protectors (lightning) at the building entry point (see the applicable regulations for lightning protection).
Units which are connected via process cables may not generate any interference voltage. The connections of relays or solenoid valves, for example, which are controlled by binary outputs must therefore be provided with suitable protective circuits (anti-surge diode, VDR) that are directly connected to the units.

- Connections via signal distribution cabinets or directly to the process termination panel

Process cables may be directly connected to the SAE cabinet connection element or to the MTP pins of the extension unit (female multi-point connector with pins 0.8 x 2.4 mm for solderless termi-point connections).
Special signal distribution cabinets ar available which provide a clear interface between the process and electronic cabinets. The individual cores may be separated in these cabinets and, using appropriate marshalling facilities, be rearranged such that a dedicated core bundling for the individual cabinets can be achieved.

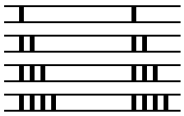
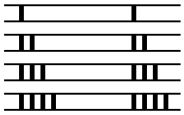
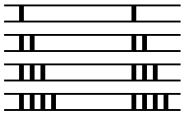
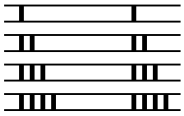
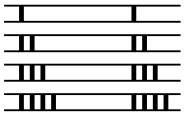
Bundle No.	Ring color	Ring group / Code	Bundle coil
1 2 3 4	pink		———
5 6 7 8	orange		———
9 10 11 12	violet		———
13 14 15 16	pink		blue
17 18 19 20	orange		red

Fig. 4.9 Core bundle identification

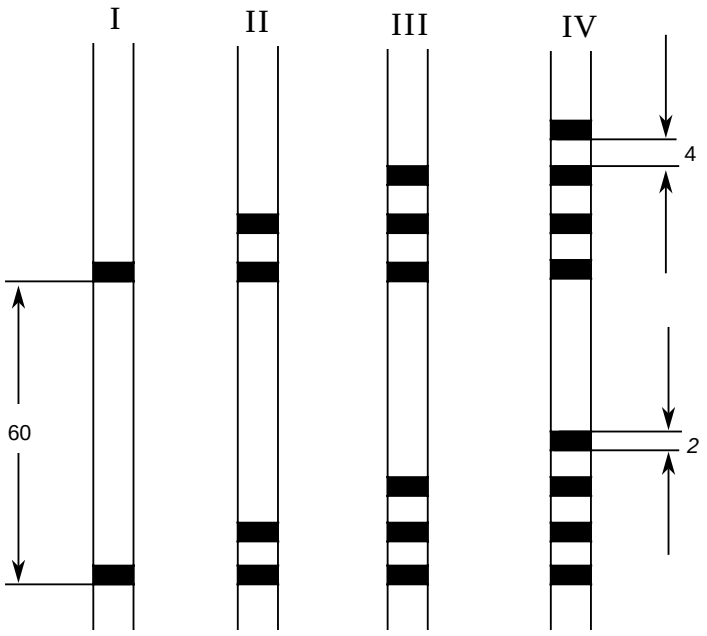


Fig. 4.10 Core identification, ring groups

- Connecting cables with braided screens

Approximately 50 mm of the outer sheath must be removed from the area where the screen is to be connected.

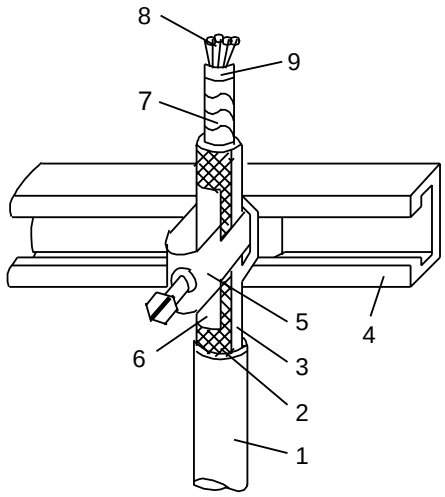
Use a cable clamp and two cradles to attach the cable to the cable clamping bar. One single clamp may also be used for fixing two thin cables. The insulation should possibly not be removed before the process termination panel where the individual cores can be separated.

In order to ensure a large-surface contact, cable clamps with cradle and counter-cradle should be used [e.g. PUK, Köln Werke GmbH, model "H" cable clamp, "K12" (12) to "K20" (20) and cradles "LW12" (12) to "LW20" (20)].

One set of cable clamps and cradles is supplied with the equipment.

Additional installation material must be ordered according to the cable specifications.

Remove the plastic elements from the clamps.



1 Signal cable with braided screen
2 Braided screen, insulation removed over 50 mm
3 Cradle (e.g. PUK,model H, type LW12...LW20), 40 mm long
4 Cable clamping bar
5 Cable clamp (e.g. PUK, model H, type K12...K20)
6 Clamp cover, screw adjustment
7 Sheath
8 Pairs to the MTP connections
9 Adhesive tape or sleeve

Fig. 4.11 Connecting cables with braided screens

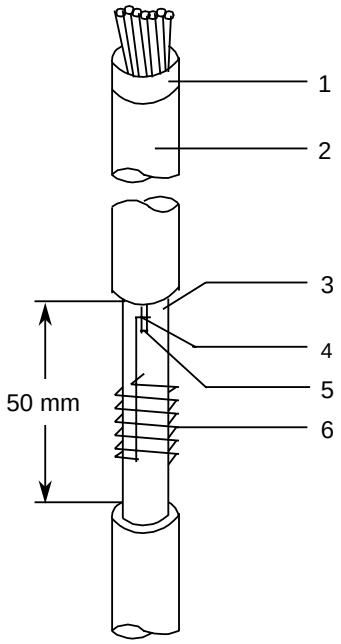
- Connecting cables with foil screen

Approximately 50 mm of the outer sheath must be carefully removed (do not damage the foil screen).

Solder a length of tinned wire (0.8) to the exposed pull wire and wind the tinned wire closely around the exposed foil (see Fig. 4.12).

Use a cable clamp for connecting the foil cable to the screen support (see Fig. 4.11).

Do not overtighten the cable clamp screw, the foil screen might be damaged.



1 Adhesive tape or sleeve
2 Sheath
3 Foil screen
4 Soldered connection
5 Exposed pull wire
6 Wire coil (e.g. tinned wire, 0.8)

Fig. 4.12 Connecting cables with foil screen

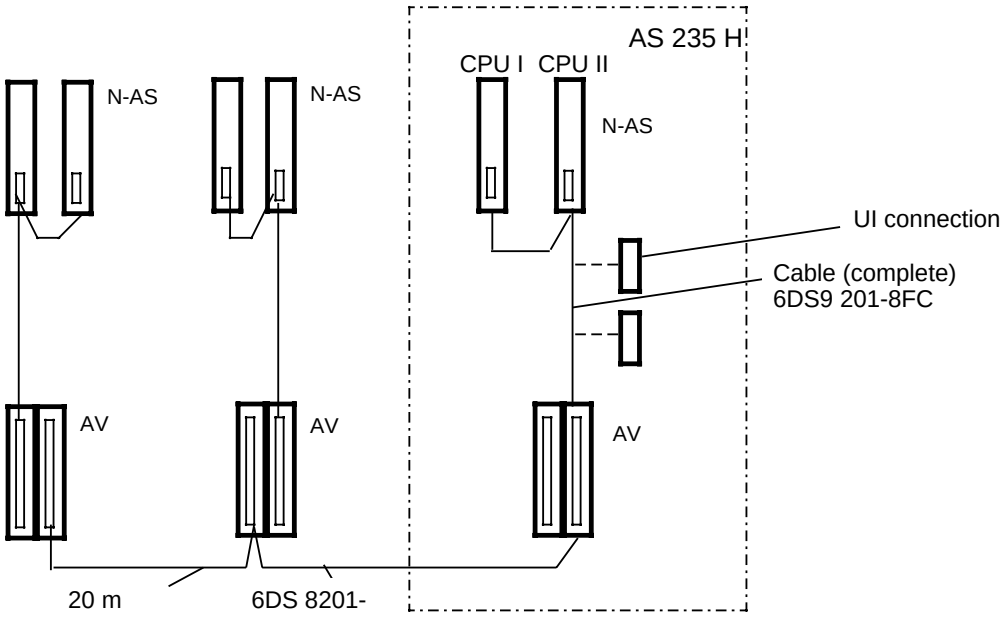
4.5 Using the Bus Components

The CS 275 bus system enables information exchange between the devices of the TELEPERM M process control system over a distance of 20 m (local bus) or 4 km (remote bus). The local bus is redundant in its standard version; the remote bus can be made redundant if required.

> **Caution**
>
> The maximum distance between devices on the local bus is 20 m; the earth potential difference between the systems may not exceed 0.2 V.

Further remote systems can be interconnected via the 4-km remote bus (inductive connection). Up to 32 local buses with up to 99 participants can communicate with each other.More details concerning the CS 275 bus system in the Manual CS 275,
Order No. C79000-G8076-C006.

4.5.1 Local Bus



AV = Connection distribution in the SES

Fig. 4.13 Local bus connection

The AS may be linked with other AS or OS systems via the local bus interface module 6DS1223-8AA (N-AS) or 6DS1220-8AA (N8-H) and the connection distribution unit. The connecting cable between the systems has only a connector at one side; the open end must be connected to the connector of the next connecting cable (1:1 with regard to core color code and number of rings). A single front connector 6DS9 200-8AA must be connected to the open end of the last connecting cable.

> **Caution**
>
> The S11 and S12 switches must be set to EIN [ON] position if N-AS/N8-H is used. Both switches must be set to AUS [OFF] if an N-AS/N8-H module has not been installed.

The S11 and S12 switches on the basic unit backplane are accessible from the front if the N-AS module has not been installed.

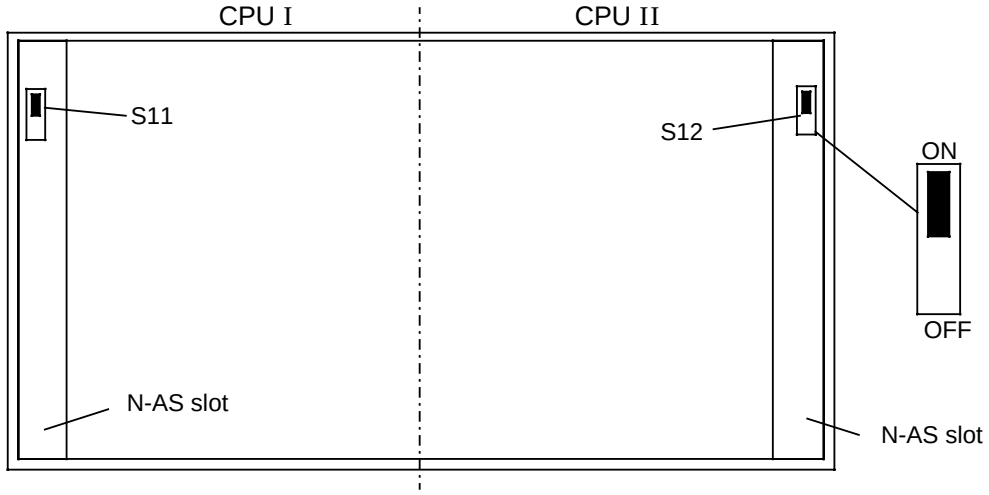


Fig. 4.14 Location of the S11 and S12 switches

4.5.2 Remote Bus

- UI bus converter unit

The inductive bus converter unit (UI) 6DS4400-8AB is the active element on the remote bus of the CS 275 bus system. It is the link between the remote bus and the local bus line which converts the remote bus protocol into the local bus protocol and vice versa.

Up to two inductive bus converter units (and two remote bus connector boards) are possible in an AS 235 H automation system. This enables operation in a redundant bus system.

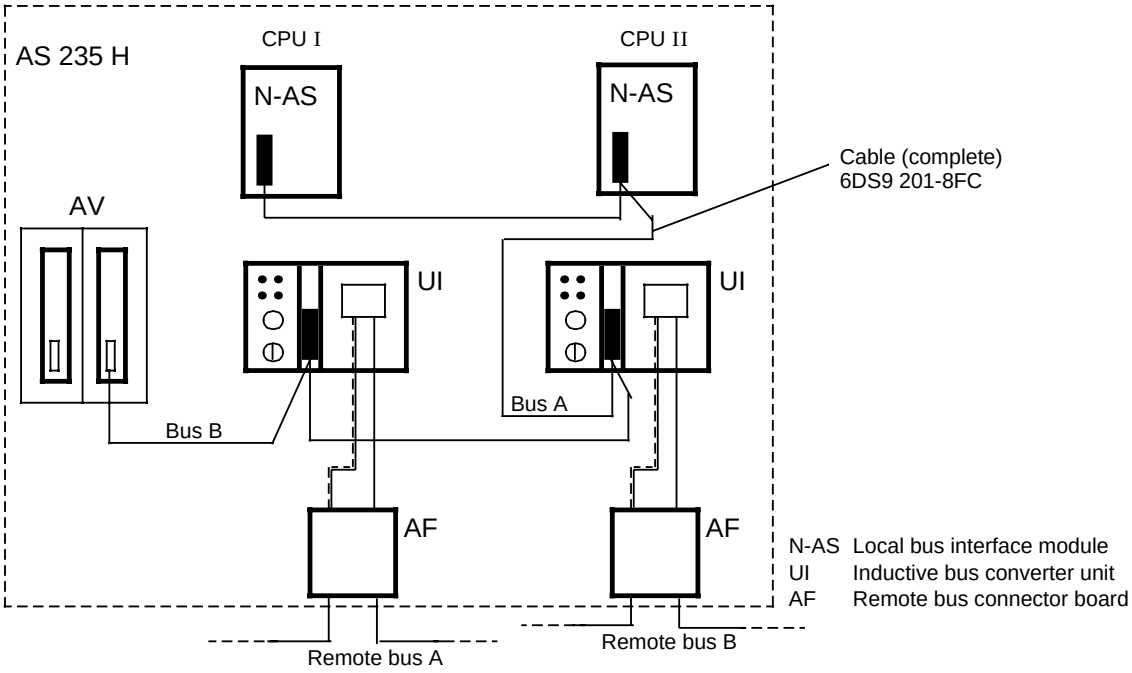


Fig. 4.15 Redundant bus configuration

4.5.3 Computer Connection via N-V.24

- N-V.24 interface 6DS1 202-8AB

The N-V.24 interface module for 20-m local bus, V.24 or TTY interfaces (6DS1 202-8AB) enables SICOMP PC personal computers and host computers to be connected to the CS275 bus system.

SICOMP PC personal computers and host computers may be connected via a V.24 or TTY interface at a selectable baud rate between 110 and 9600 bits/s.

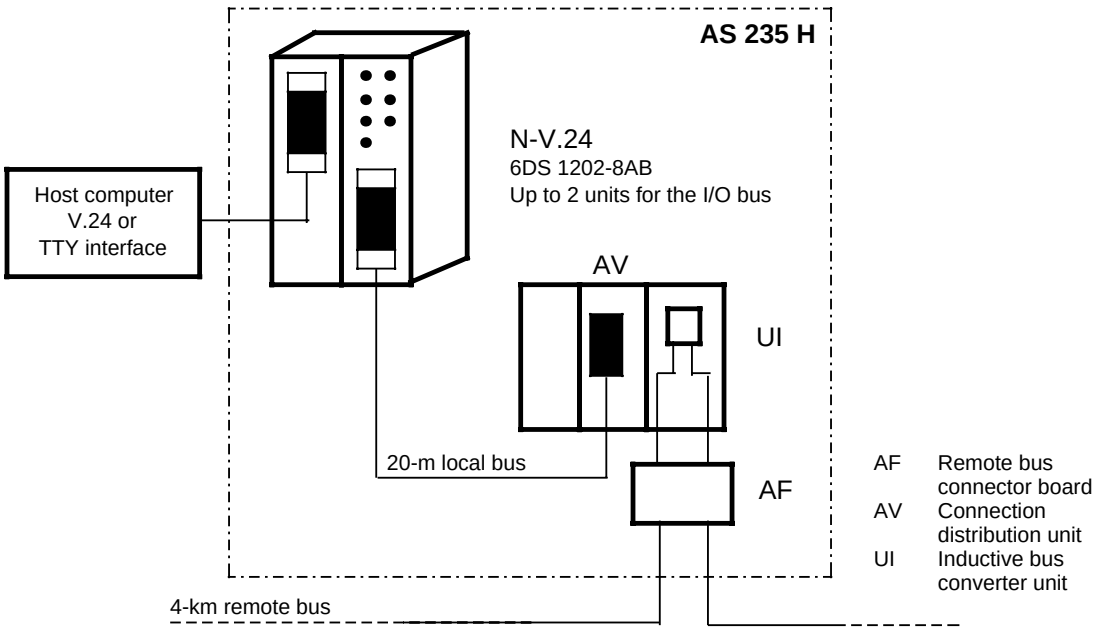


Fig. 4.16 N-V.24 interface

Various data traffic job types for communication between the TELEPERM M units (AS***/***OS) have been defined in the CS 275 bus system. A host computer that communicates with the TELEPERM M system must also use these jobs (messages)

Detailed specifications of format, coding and acknowledgement mode of the job types for host computer communication are contained in the CS 275***/***N-V.24 Manual, Order No. C79000-G8076-C087.

- Interface module installation and power supply

There is no pre-configured slot for the 20-m local bus, V.24 or TTY interface (N-V.24) in the TELEPERM M system. It can be installed in any free slot. The N-V.24 interface merely requires a 5-V supply via pin z2 of the X1 backplane connector. Earth contact is provided via the contacts b2 and b32 (2.4 A power consumption).

The module may only be removed or inserted after the 5-V bus has been switched off.

These connections exist in any I/O slot. A maximum of one interface module may be installed in an extension unit. Since an extension unit is also a fault delimitation area, failure of the extension unit also de-activates the interface.

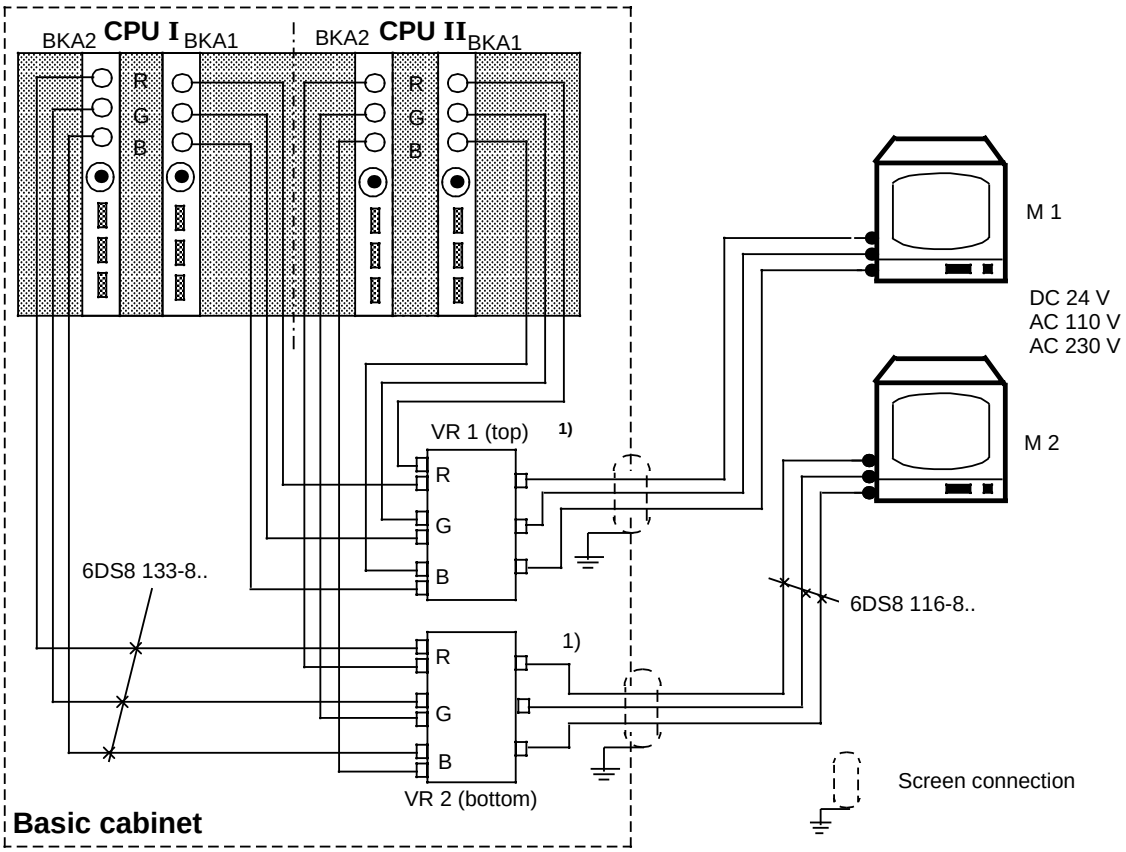
Please refer to the CS 275 Manual, Order No. C79000-G8076-C006 for further information.

Note

As with all central modules, the N-V.24 or CP581-TM may only be removed or inserted after the power supply has been switched off.
Unlike I/O modules, however, there are not supplied with L+ (DC 24 V) but with +5 V which is applied to the I/O bus of the subrack.
Switch off the logic voltage during handling.
Either use the switch on the power supply unit (SV) of the basic unit (this also switches the L+ of the 6 I/O modules) or use switch S2 of the basic unit (logic voltage of the central processor only).
In case of non-observance of the above, the current surge may - depending on the configuration - corrupt data access or reset sytems.

4.6 Connecting the I/O Devices

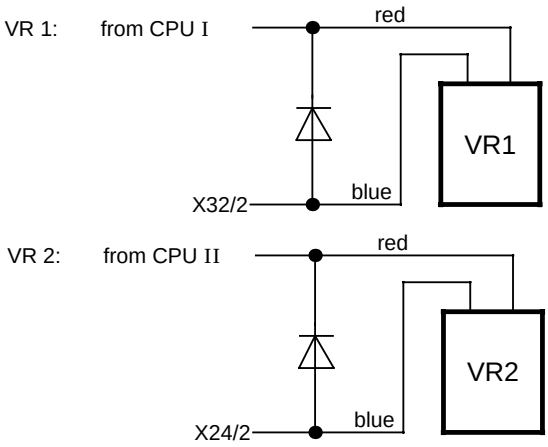
4.6.1 Process Monitors



1) The monitor cables inside the cabinet should be long enough to enable direct connection to the BKAs

BKA Operator input channel interface module
VR Video relay screen connection
RGB Red, green, blue

Fig. 4.17 Connection of the color monitors M1 and M2



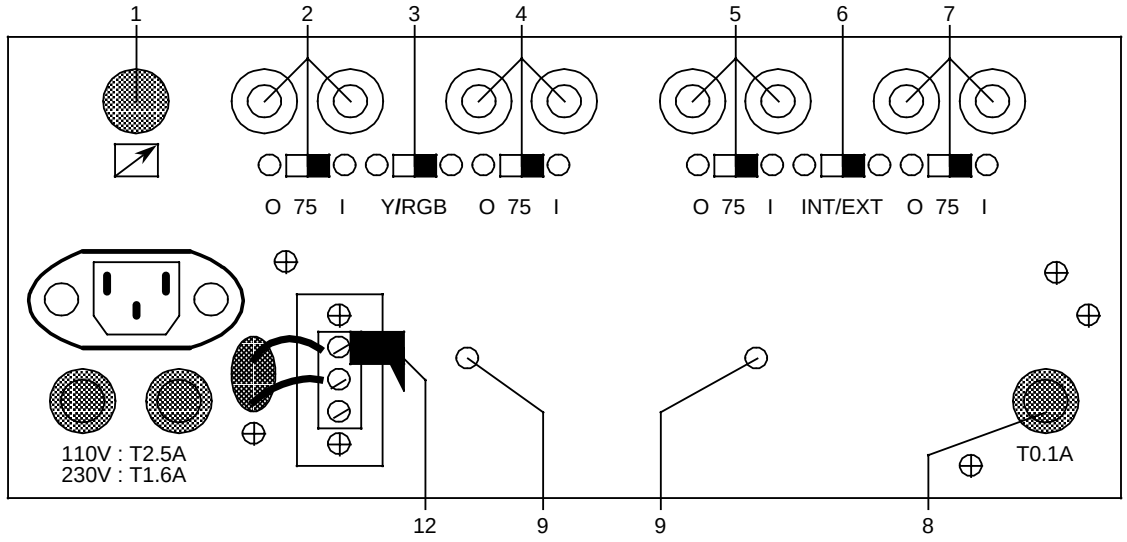
The VR connecting lugs should point upwards

Fig. 4.18 Video relay control

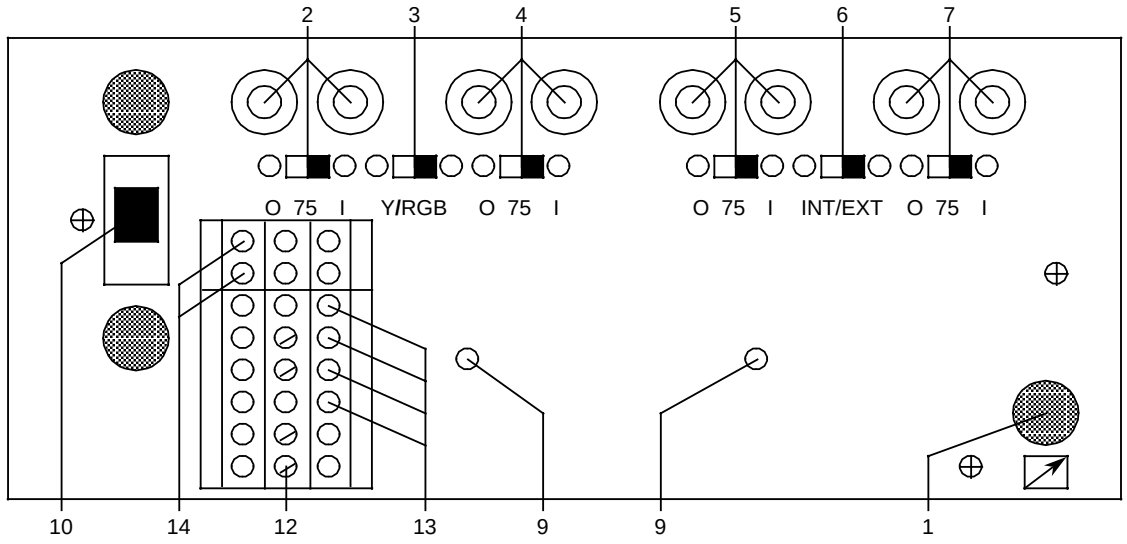
The color monitors have specifically been designed for process control purposes and are utilized for representation of alphanumeric and graphic information.

Caution

Since TELEPERM M systems have a central grounding point, video earth must be separated from protective earth. This is done by removing the jumper (video**/**protective earth separation) from the color monitor connector board.
The mains voltage selected (AC 110 V**/**AC 230 V) must match the voltage available at the mains connections.
Units operating on DC 24 V may only be connected if power and mains switch have been switched off.
A unit is only de-energized after the associated power cable has been removed.



Connector board, AC 110/230 V version of the 6DS3 401-8BK monitor



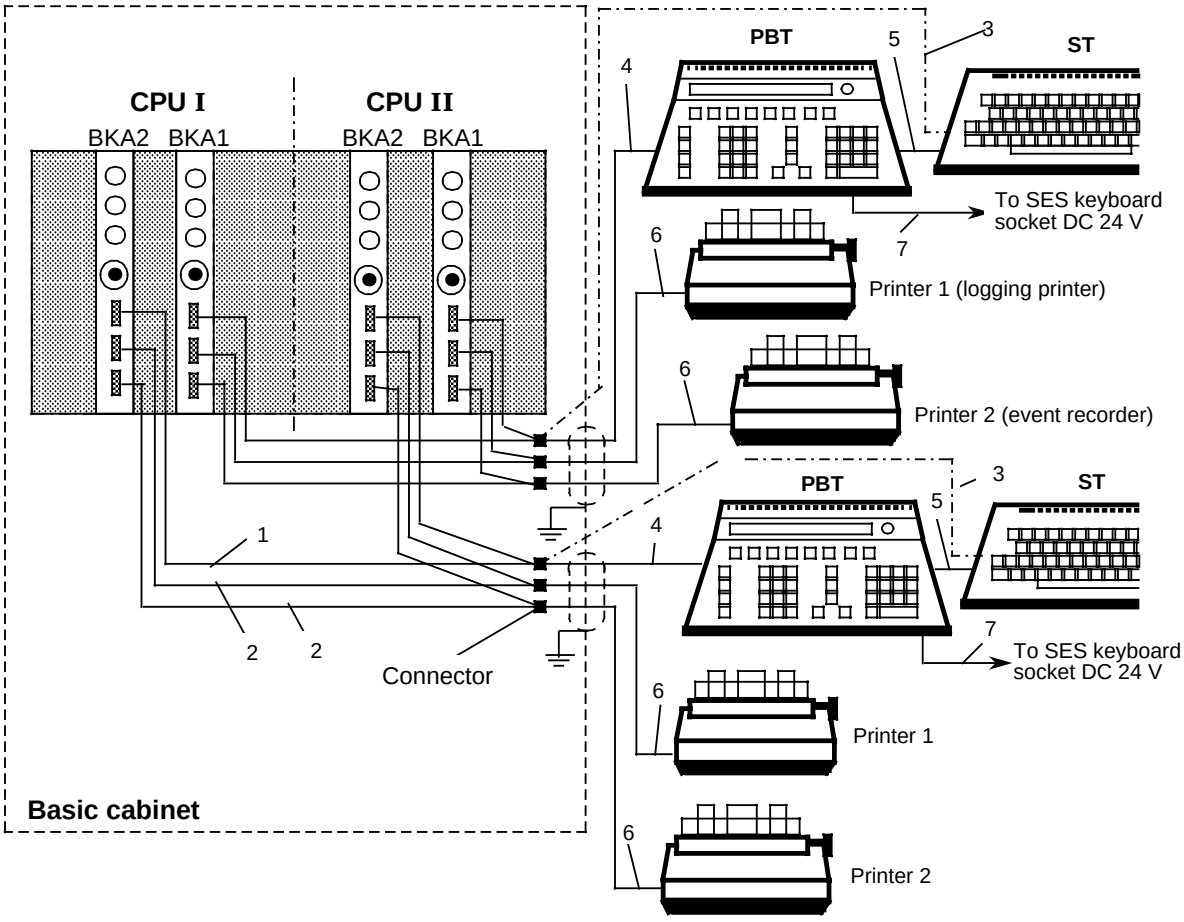
Connector board, DC 24 V version of the 6DS3 401-8BL monitor

1 Remote control connection
2 Color signal "red" connector with 75 contact terminator resistance via a switch contact
3 Selector for color (RGB) or black-and-white mode (Y)
4 Color signal "green" or Y connector with 75 terminator resistance via a switch contact
5 Color signal "blue" connector with 75 terminator resistance via a switch contact
6 Synchronization selector switch
7 Connections for synchronization with 75 terminator resistance via a switch contact
8 Fuse of remote control relay power supply unit
9 Holes for fixing the grounding bar
10 Main circuit breaker (AC 110 V/**AC** 230 V), power switch (24)
11 Mains cable connection
12 Video/protective ground separation point
13 24 V connection
14 Operation control signal via switch contact (23 V, max. 10 mA)

Fig. 4.19 Monitor connector boards

Please refer to the process monitor descriptions for further information.

4.6.2 Keyboards and Printers



BKA 1/2 Operator input channel interface module 1/2
PBT Process communication keyboard
ST Configuring keyboard, may also be connected directly

1	Keyboard distribution cable	(TV)	C79165-A3012-B421
2	Printer distribution cable	(DV)	C79165-A3012-B422
3	Connecting cable	ST-TV	6XV2 167-8BB...8BU
4	Connecting cable	PBT-TV	6XV2 167-8CB...8CU
5	Connecting cable	PBT-ST	6XV8 102-8...
6	Connecting cable	Printer-DV	6XV2 167-8AB...-8AU
7	Connecting cable	PBT-SES	6XV8 103-8...

Fig. 4.20 Connection of operator input units

The units are connected in parallel to both CPUs via the keyboard or printer distribution cables.

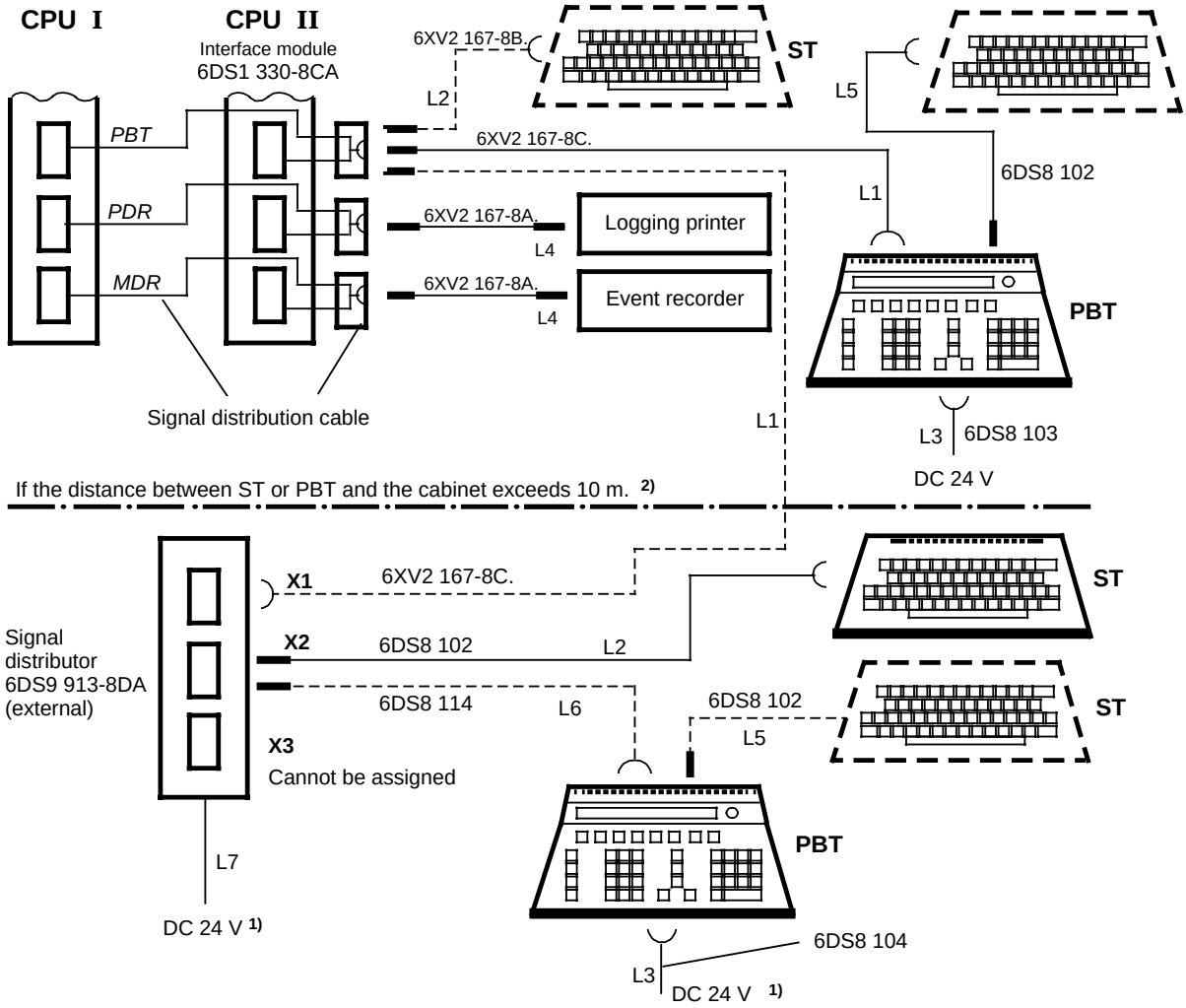
Distances > 10 m require system distribution units to be used between operator input channel interfaces and keyboards.

Connecting cable: 6XV2 167-8CB...-8CU					
BEDI 235			Process communication keyboard		
Signal name	Connector A 15-way male	Core pair	Core color	Connector B 15-way female	Signal name
– TXD1	3	1	bl	3	-E11
+ TXD1	4		rd	4	+E12
– RXD1	1	2	gr	1	-S11
+ RXD1	2		ye	2	+S12
-	Housing	Screen		Housing	

Connecting cable: 6XV2 167-8AB...-8AU					
BEDI 235			Printer		
Signal name	Connector A 9-way male	Core pair	Core color	Connector B 25-way female	Signal name
– TXD2/3	3	1	bl	9	Receive data
+ TXD2/3	4		rd	10	
– RXD2/3	1	2	gr	18	Transmit data
+ RXD2/3	2		ye	21	(Busy)
-	Housing	Screen		Housing	-
-	-	-		-	-

Connecting cable: 6XV2 167-8BB...-8BU				
BEDI 235		Configuring keyboard		
Signal name	Connector A 15-way male	Core color	Connector B 15-way female	Signal name
– RXD1	1	wh	1	-S1
+ RXD1	2	br	2	+S2
– TXD1	3	-	-	-
+ TXD1	4	-	-	-
0V(Earth)	6	gn	6	0V
24V (L+)	8	gr	8	24V
-				-
-	Housing	Screen	Housing	-
0V(Earth)	13	pk	13	0V
24V (L+)	15	rd		24V

Table 4.3 Signal line pin assignments



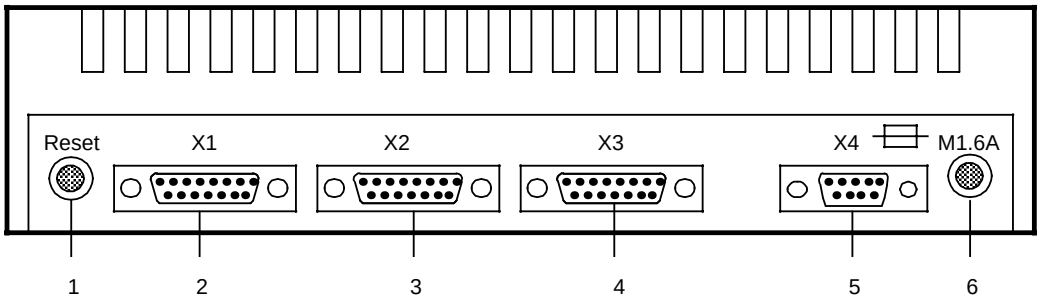
Cable connector	Length in m	Conditions
6XV2 167-8CB...-8CU	L1 150 L1 10	L3 to DC 24 V external 1) L3 to DC 24 V cabinet (SV tier)
6XV2 167-8BB...-8BU	L2 10 L1+L2 150 L1+L6 150	L3 to DC 24 V external 1)
6DS8 103-8.. 6DS8 104-8..	L3 10 L3 10	
6XV2 167-8AB...-8AU	L4 100	PT 88, 89, 90
6DS8 102-8..	L5 30	
6DS8 114	L6 10 L1 + L6 150 L7 = 2	2) Fixed connection to signal distributor

1) External DC 24-V supply (22...30 V) (supplied by others)
2) External power supply must be provided and the units integrated in the plant grounding system if the distance between the keyboards and the cabinet exceeds 10 m. (Installation in cabinets is not permitted with the specified cable lengths.)

Fig. 4.21 Keyboard printer cable lengths.

- Process communication keyboard 6DS3 305-8AA (PBT)

The connecting cables are plugged into the rear of the PBT unit.



1 Reset pushbutton
2 X1 connector for configuring keyboard
3 X2 connector (not used in AS 235 and AS 235 H systems)
4 X3 connector for keyboard distribution cable
5 X4 connector for power supply cable
6 Fuse M1.6 A for 24 V supply voltage

Fig. 4.22 Process communication keyboard, rear panel with connectors

The PBT must be supplied with DC 24 V. The supply voltage is protected by a M 1.6 A fuse. A message is issued to the system if a voltage is out of tolerance.

The PBT has no power switch. The unit is ready once the voltage has been connected via the X4 connector. The green LED at the right-hand side of the display indicates that the unit is ready. The red LED is ON if a failure has been detected in the system or the peripherals.

The PBT features two serial interfaces.
The 20-mA current loop is always supplied by the subordinate device (i.e. from the PBT to the AS and from the configuring keyboard to the PBT).

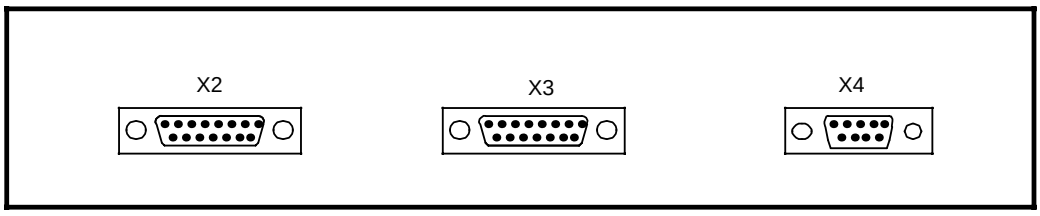
- The baud rate to the higher-order system is 1200 bits/s, and cannot be changed.

- Process communication keyboard 6DS3 305-8BA (PBT)

The process communication keyboard has a dust and splashproof touchpad keyboard and an LCD unit.

Operation and handling is identical to that of the version 6DS3 305-8AA.

There are three connectors at the rear (Fig. 4.23).



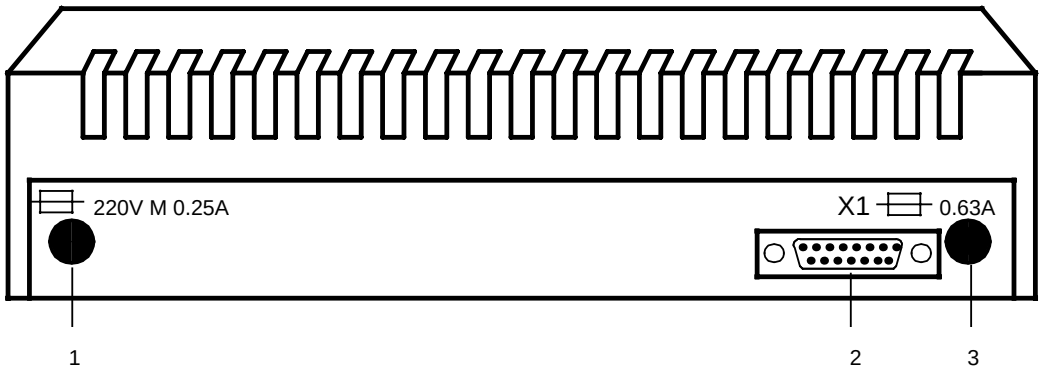
Connector X2 for: configuring keyboard
Connector X3 for: higher-level system (e.g. AS 235)
Connector X4 for: voltage supply cable

Fig. 4.23 Process communication keyboard 6DS3 305-8BA, rear panel with connectors

It is possible to upgrade the process communication keyboard to the degree of protection IP 65 using a kit (Order No. C79372-A3018-D1) in order to protect the rear connectors against environmental influences (dust, splashing and gases).

- Configuring keyboard 6DS3 303-8AA (ST)

The configuring keyboard connects to the PBT via the connecting cable 6DS8 102-8... or directly to the AS keyboard distribution cable via the connecting cable 6XV2 167-8... The connecting cable also carries the DC 24-V supply voltage to the unit.



1 Not used
2 Connector
3 Fuse

Fig. 4.24 Configuring keyboard, rear panel

The DC 24-V supply voltage is protected by a T 0.63 A fuse which is located on the back panel next to the X1 connector.

The label "220 V/0.25 A" has no meaning (the component has not been connected).

The unit is ready once the voltage has been connected. The unit has no power switch.

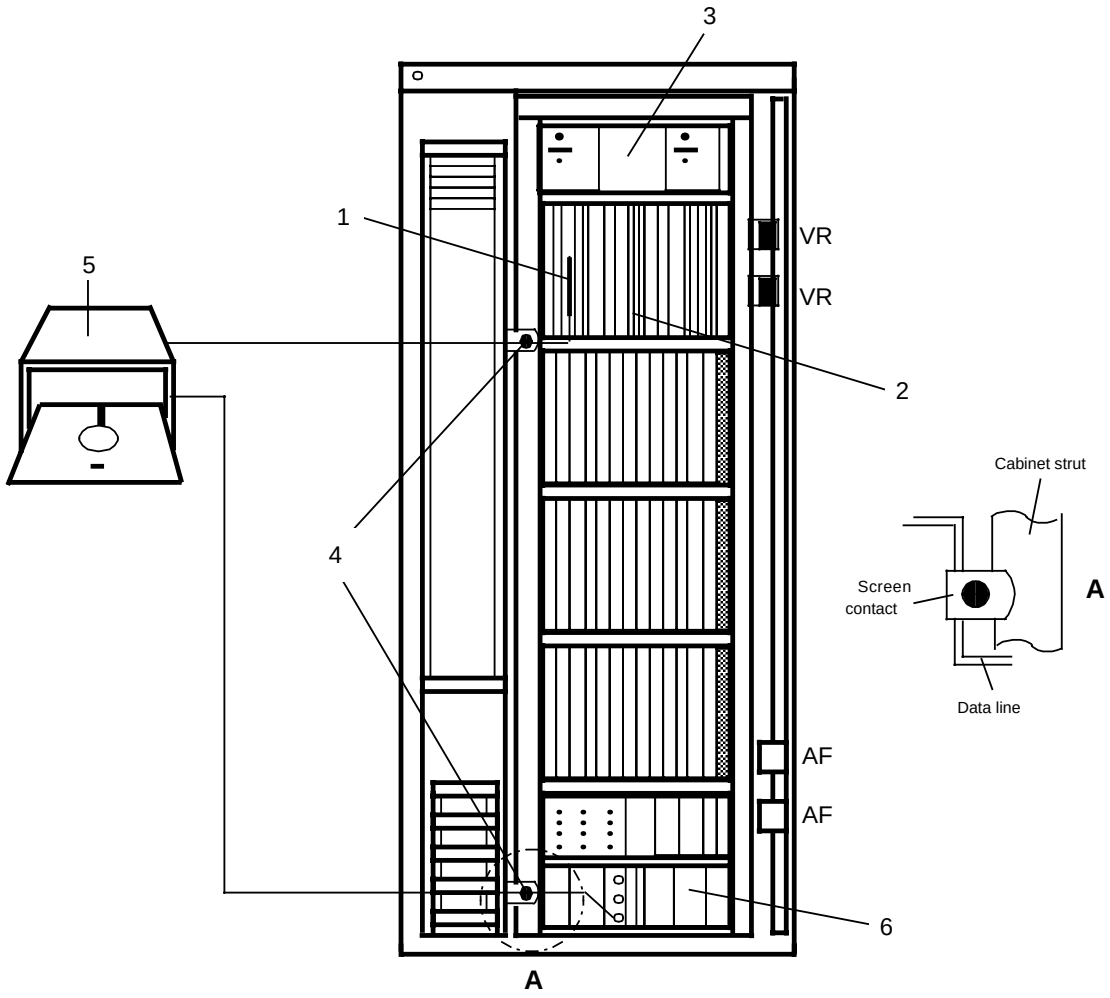
The serial interface is activated by jumper settings (default setting).

4.6.3 Mini Floppy Disk Unit (MDE) 6DS3 900-8AD

The signal cable (rectangular connector) connects the MDE to the 6DS1 326-8BB mini floppy disk interface module (MDA) (1, Fig. 4.25).

The power supply cable (round connector) must be connected to the socket provided in the cabinet power supply unit (SES).

Both screen contacts (4, Fig. 4.25) must be connected to the cabinet frame in order to guarantee faultless operation.



1 Mini floppy disk unit interface module (MDA) 6DS1 326-8BB
2 Central unit
3 Power supply unit (SVE)
4 Screen connection to the rack
5 Mini floppy disk unit (MDE)
6 Cabinet power supply unit (SES)

Fig. 4.25 Connection to standard cabinet

The mini floppy disk units 6DS3 900-8AD with a revision level 4 can be connected to the AS 235 H system. Only one floppy disk format can be used.

- 80 tracks, double-sided, high density, 512 bytes/sector
  1 MB net capacity
  Floppy disk type: HD, Order No. 6AY2904-0AC00

The following number of floppy disks is used for a complete memory dump:

Memory size	80 tracks DS, HD
1 MB	1
2 MB	2
3 MB	3

DS: double-sided
HD: high density

The format is selected by the GB.ORPA parameters (cf. AS 235 Function Description in the manual C79000-G8076-C416). The ”NORM switch” on the mini floppy disk interface module (MDA) **must** be in position "EIN" [ON].

GB.ORPA 260	GB.ORPA 261	Format type
0	0	35 tracks, SS, SD
0	1	80 tracks, DS, SD
1	X	80 tracks, DS, HD

[ ] = default

The NORM switch on the MDA must be in position "EIN" [ON] if the default setting has been selected. The following or GB.ORPA selections or NORM switch positions on the MDA are required if existing user software from an AS 230 system is to be loaded (imported) into an AS 235 H system:

Floppy disk type	Drive type	GB. ORPA 260	GB. ORPA 261	Comment
35 tracks SS – SD	35 tracks 6DS3 900-8AC	0	0	1) 3)
35 tracks SS – SD	80 tracks 6DS3 900-8AD	0	1	1)
80 tracks DS – SD	80 tracks 6DS3 900-8AD	0	1	2)
80 tracks DS – HD	80 tracks 6DS3 900-8AD	1	X	2) =default

1) For SW D 0.1 (B..., C..., D0.1)
MDA NORM switch=”AUS” (OFF)
For SW>D 0.1 (D..., E...,)
MDA NORM switch=”EIN” (ON)

2) Always
MDA NORM switch=”EIN” (ON)

3) nur in Sonderfällen

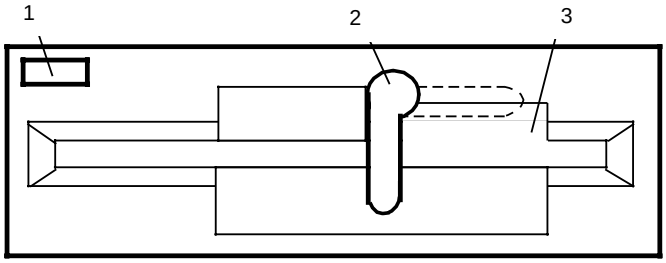
Note

When filing note the selected setting on the disk.
In case of setting errors of GB.ORPA and NORM switches some combinations with the directory entry, disk type, drive type on the disk can be in contradiction during loading and led to incompatibility in the AS 235 H (mit F447 error message).
Disks can only be loaded with the settings selected during filing.
The software filed on the 6DS3 900-8AD is **cannot** be loaded with the 6DS3 900-8AC drive.

Handling instructions:
- handle the floppy disk with care
- do not bend the floppy disk
- do not touch the data carrier surface
- protect the floppy disk from dust
- keep the floppy disk away from magnetic fields
- the floppy disk can be write-protected
- the floppy disk must be formatted before data can be filed
- ensure that a sufficient number of formatted floppy disks is available when filing is started. Formatting during filing is not possible.

Warning

Never open the drive lever while the drive is operating (red LED on MDE is ON). Data may be destroyed.

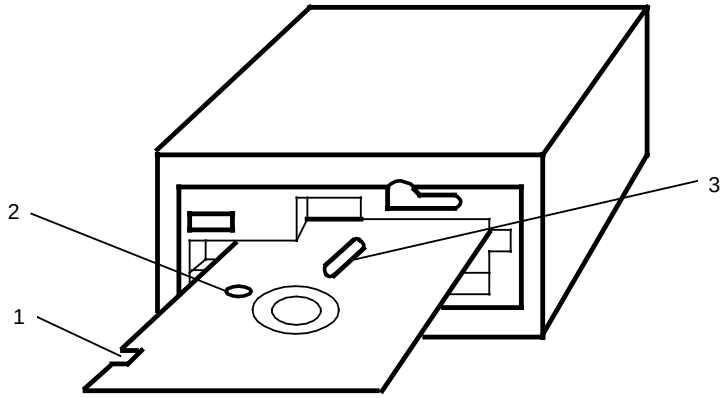


1 Operation LED (red)
2 Drive lever
3 Slot for floppy disk

Fig. 4.26 Floppy disk drive, front view

Handling

Insert the floppy disk such that the write protect slot (1) in the protective jacket points to the left-hand side and the read/write slot (3) is directed towards the drive.



1 Write protect slot
2 Sector hole
3 Read/write notch

Fig. 4.27 Inserting a floppy disk

4.7 Jumper Settings

Most jumpers are already properly set when the system is delivered and may not be changed by the user.
Warranty claims become void if the user manipulates jumper positions or jumper settings.

4.7.1 Central Processing Unit

- Comparator coupler module 6DS1 142-8AA (VKB)
  User-specific jumper setting is not required on the comparator coupler module (VKB).
- Synchronization module 6DS1 143-8AA (SB)
  User-specific jumper setting is not required on the synchronization module.
- Diagnostic unit interface module 6DS1 925-8AA (DGA)
  The jumper settings and the utilization description for TELEPERM M AS 235 are valid.
  The additional items of information in the Technical Description of the SB Synchronization Module (Order No. C79000-T8076-C344) and the VKB Comparator Coupler Module (Order No. C79000-T8076-C345) have to be observed.

- **Memory modules**

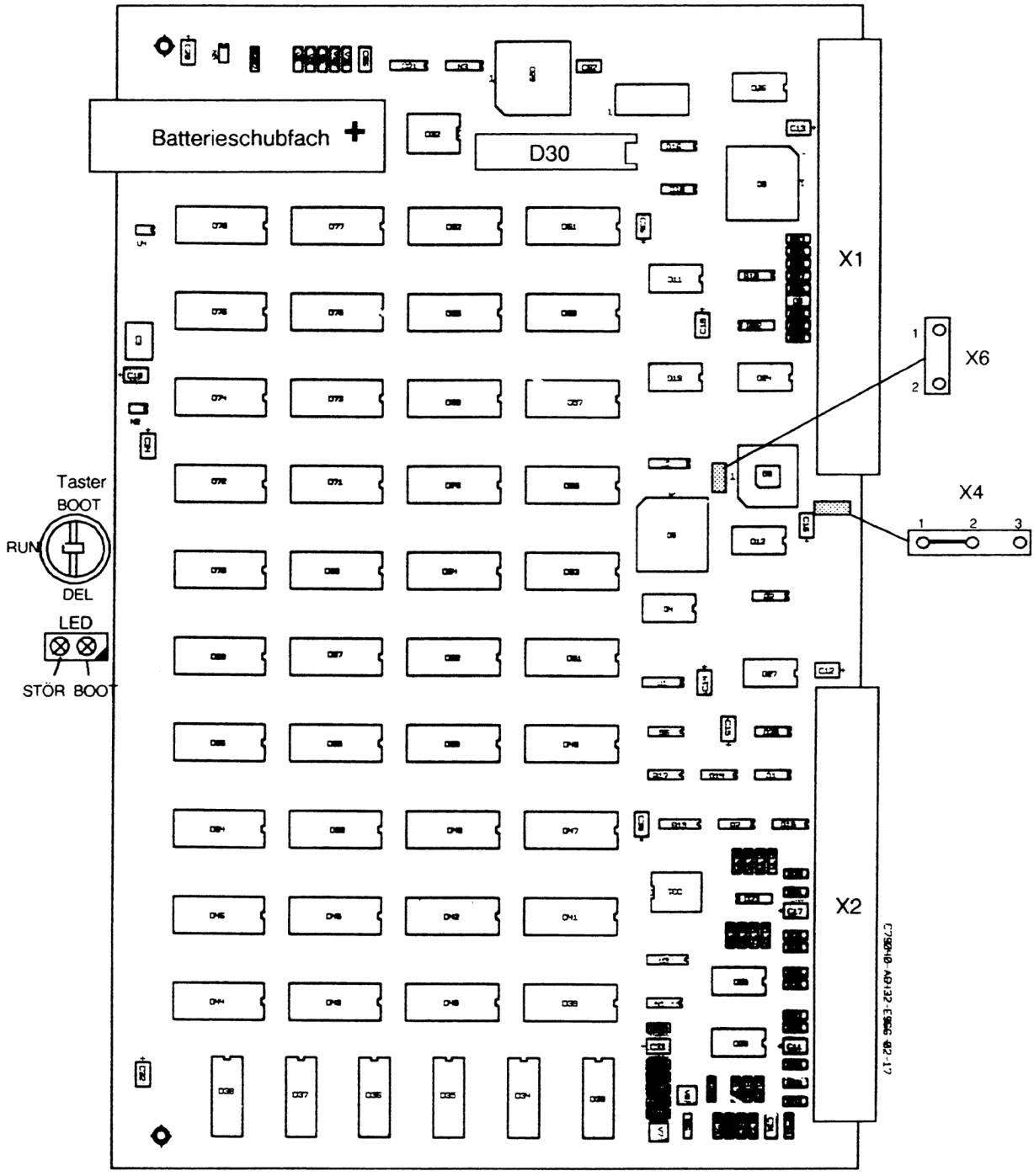
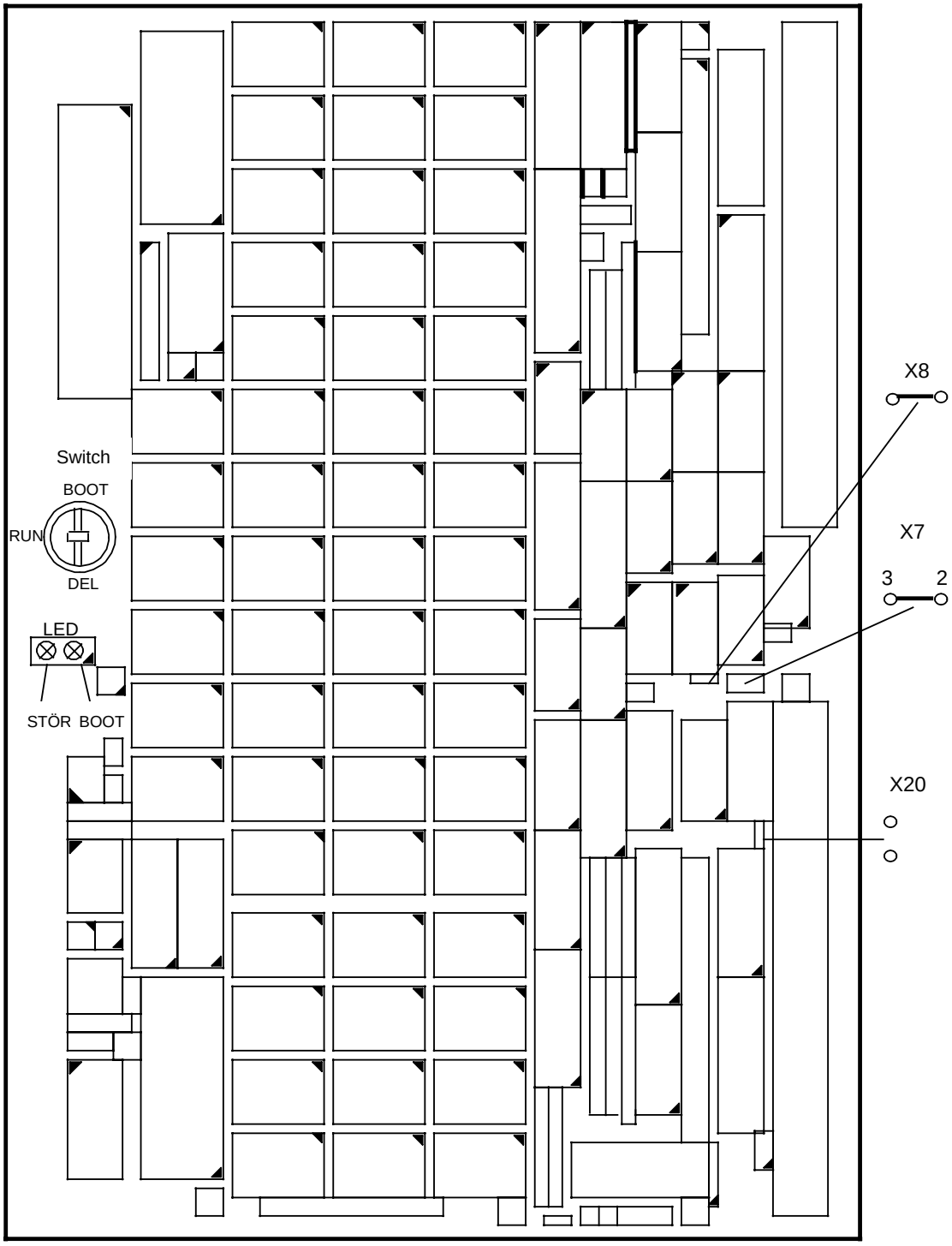


Fig. 4.28 Memory module 6DS1 844-8CA/8DA



RUN: Normal position
BOOT: Used for initial loading of new system software. The ZRS pushbutton on the CPU module **must** be pressed when this switch is in BOOT position.
DEL: Clears the user memory. The supply voltage need not be switched off. DEL must be selected while the ZRS pushbutton is pressed.

Fig. 4.29 Memory module 6DS1 837-8DA/-8EA/-8FA

The jumper settings are the same for all three memory modules. The jumpers are located on the mother board. They are required for test purposes and are put in the right position at the factory, before the module is delivered.

- Central processor module (**bottom board**) (CPU 235 H)

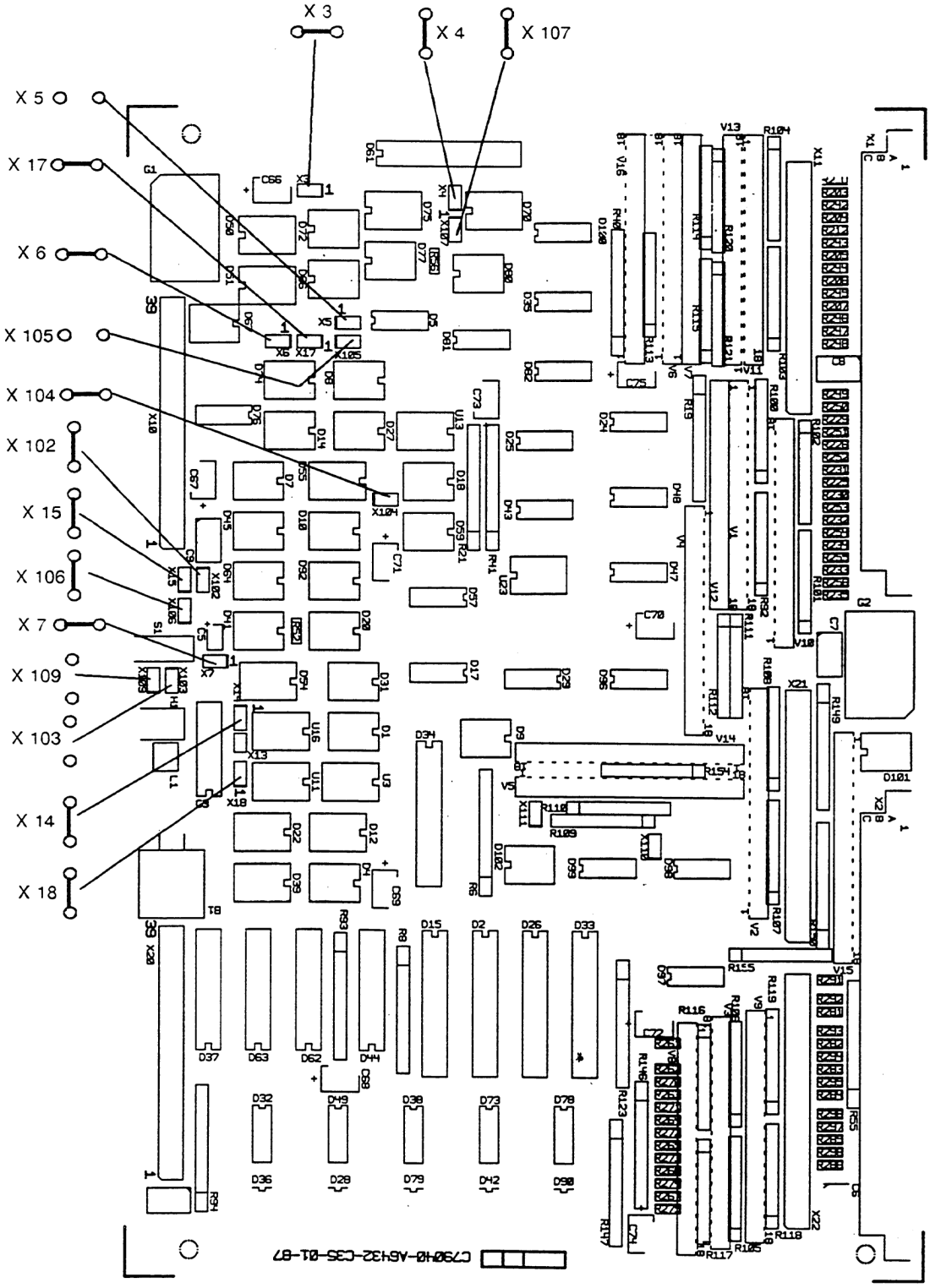


Fig. 4.30 CPU processor module 6DS1 141-8AA, bottom board (control unit)

Central processor module (**top board**) (CPU 235 H)

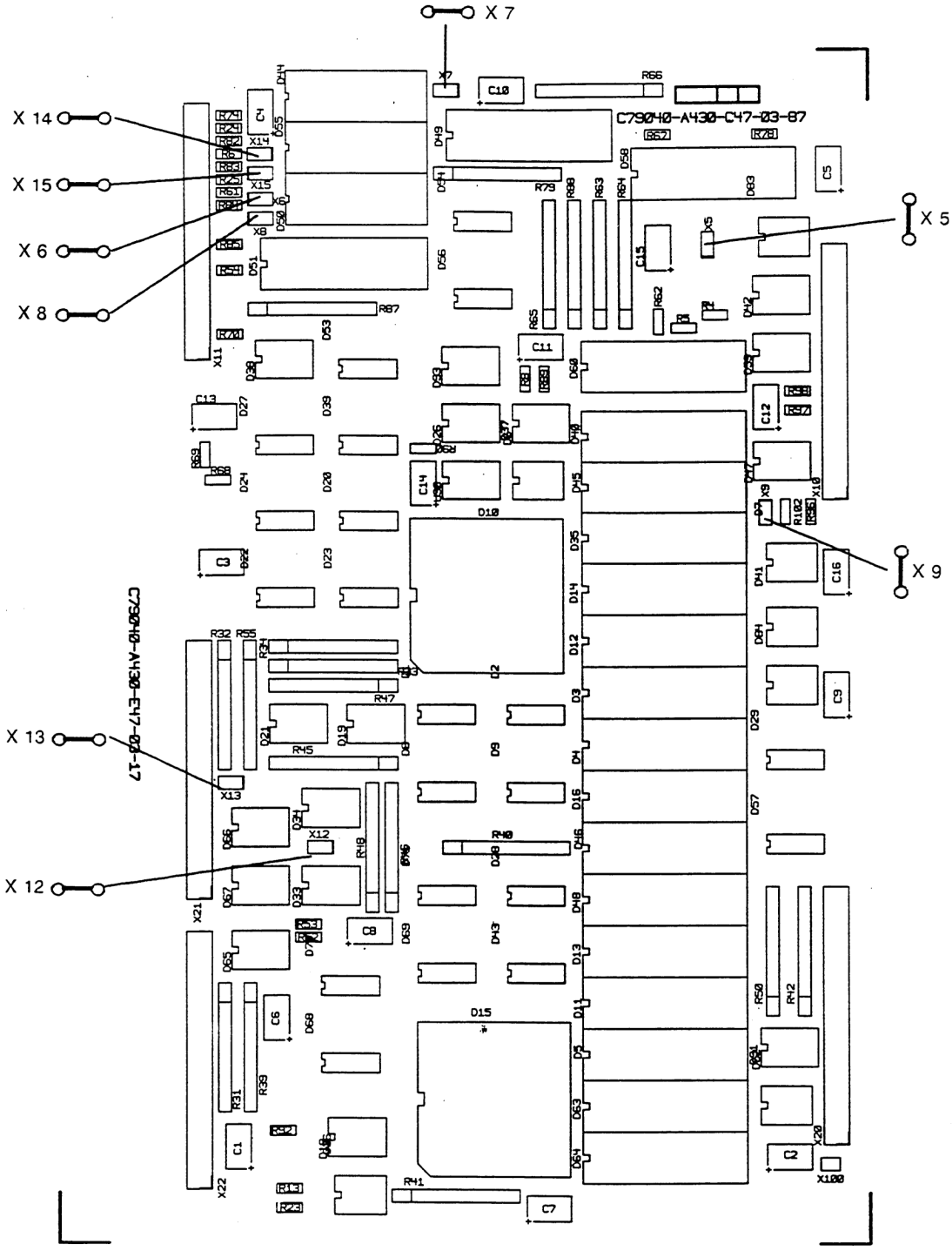
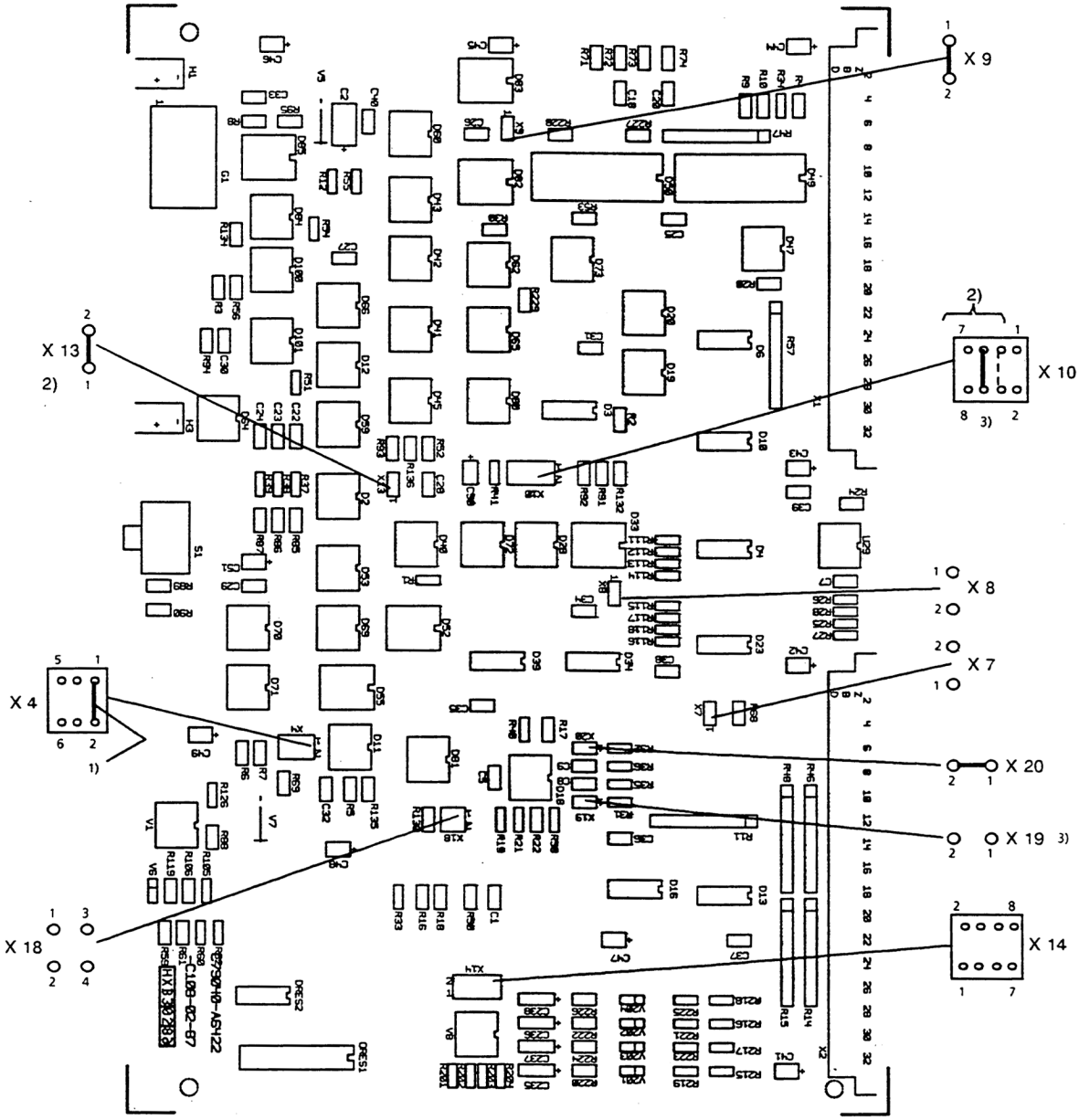


Fig. 4.31 CPU processor module 6DS1 141-8AA, top board (arithmetic unit)

- I/O bus interface units (EABA)
  Jumper assignments for **I/O bus 1 and I/O bus 2**



1) Jumper not inserted for EABA2

2) Insert jumpers (option)

3)

X10/ 3 - 4 inserted	Negative edge of external minute impulse is effective	One of the two jumpers must be inserted on EABA1 and EABA2
X10/ 5 - 6 inserted	Positive edge of external minute impulse is effective	
X10/ 7 - 8 inserted	Minute impulse triggers PU6 interrupt on EABA1	Remove the jumper X13/1-2 on EABA 1 if the minute impulses are to be used
X10/ 7 - 8 not inserted	No interrupt by minute impulse	The jumper X13/1-2 may be inserted

Fig. 4.32 I/O bus interface module 6DS1 312-8BB

- Operator input channel interface module (BKA)

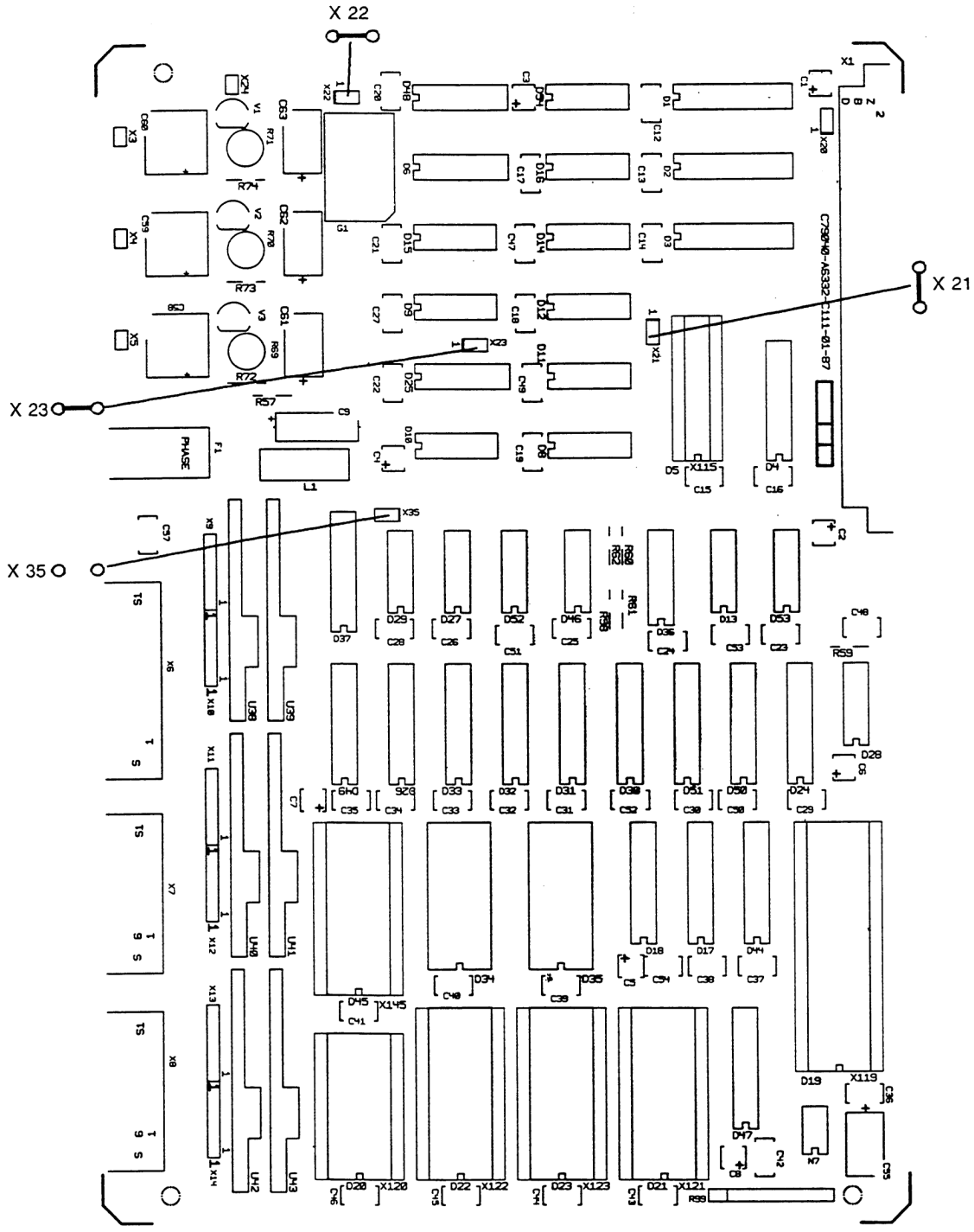
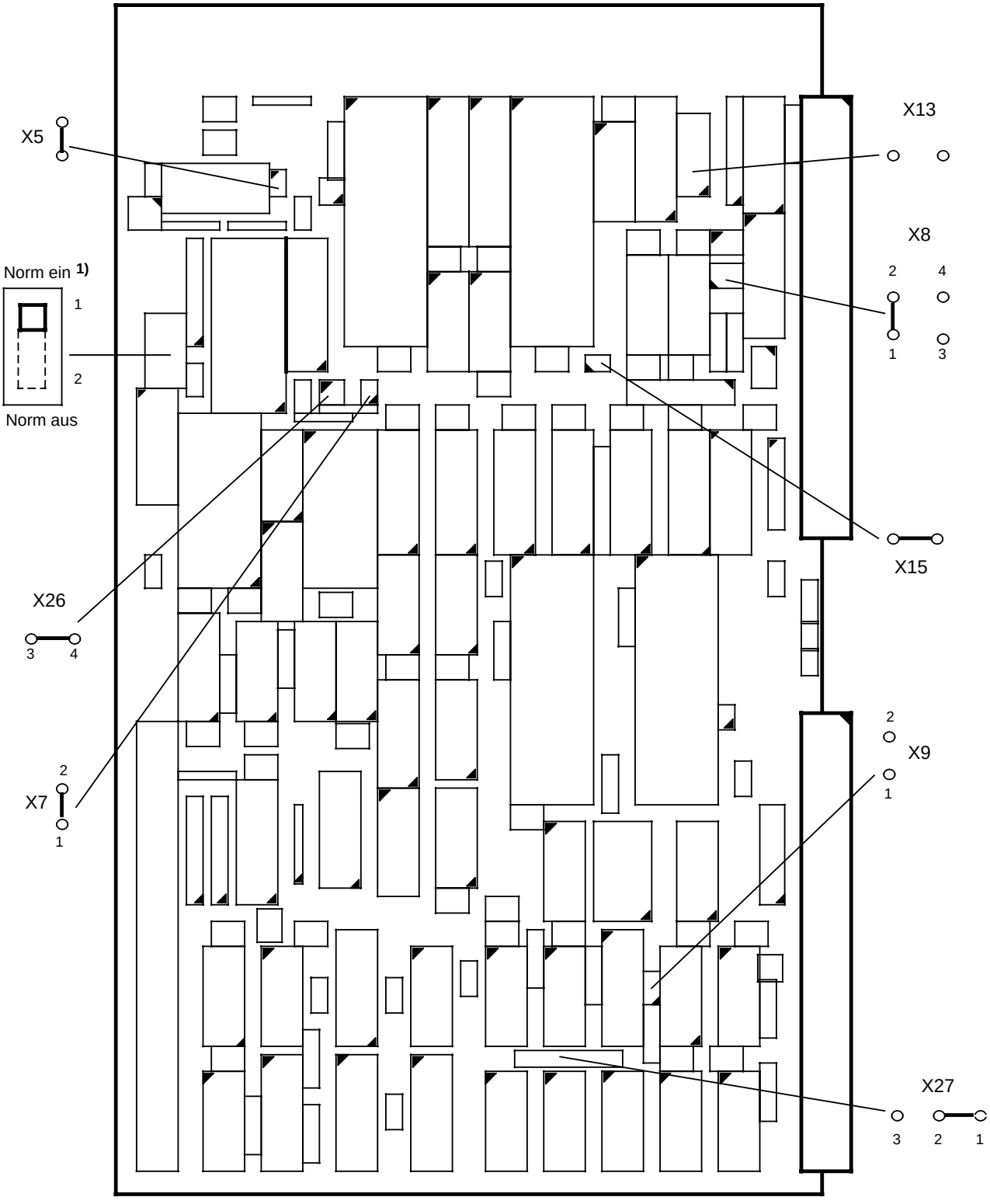


Fig. 4.33 Operator input channel interface module 6DS1 330-8CA

- Mini floppy disk interface module (MDA)

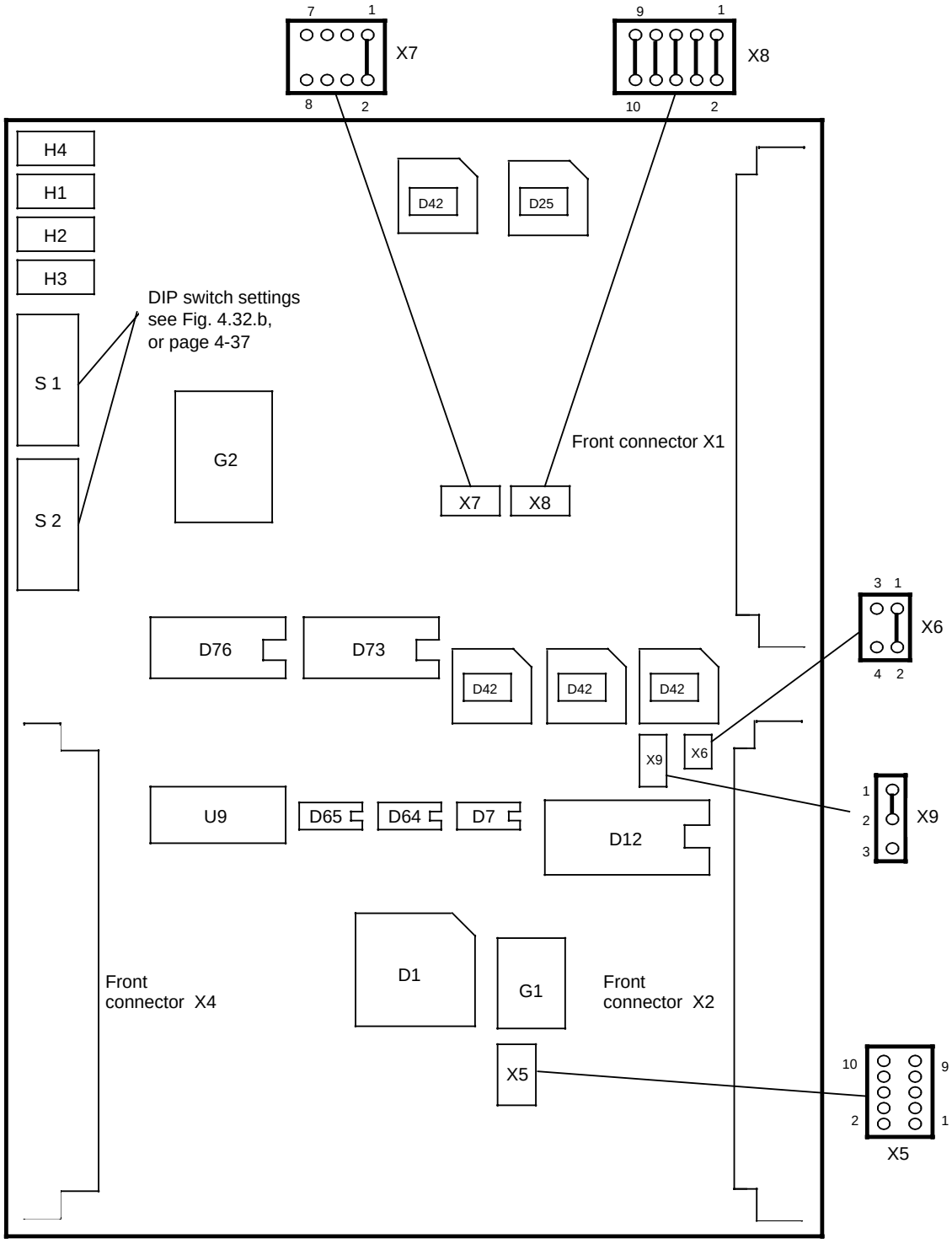


1) Switch position "NORM AUS" for loading of AS 230 floppy disks with software revision <D0.2 only. Position "NORM EIN" for loading and filing of any other system.

The module must be at least of revision level 3 if it is to be used in an AS 235 H system.

Fig. 4.34 Mini floppy disk interface module 6DS1 326-8BB

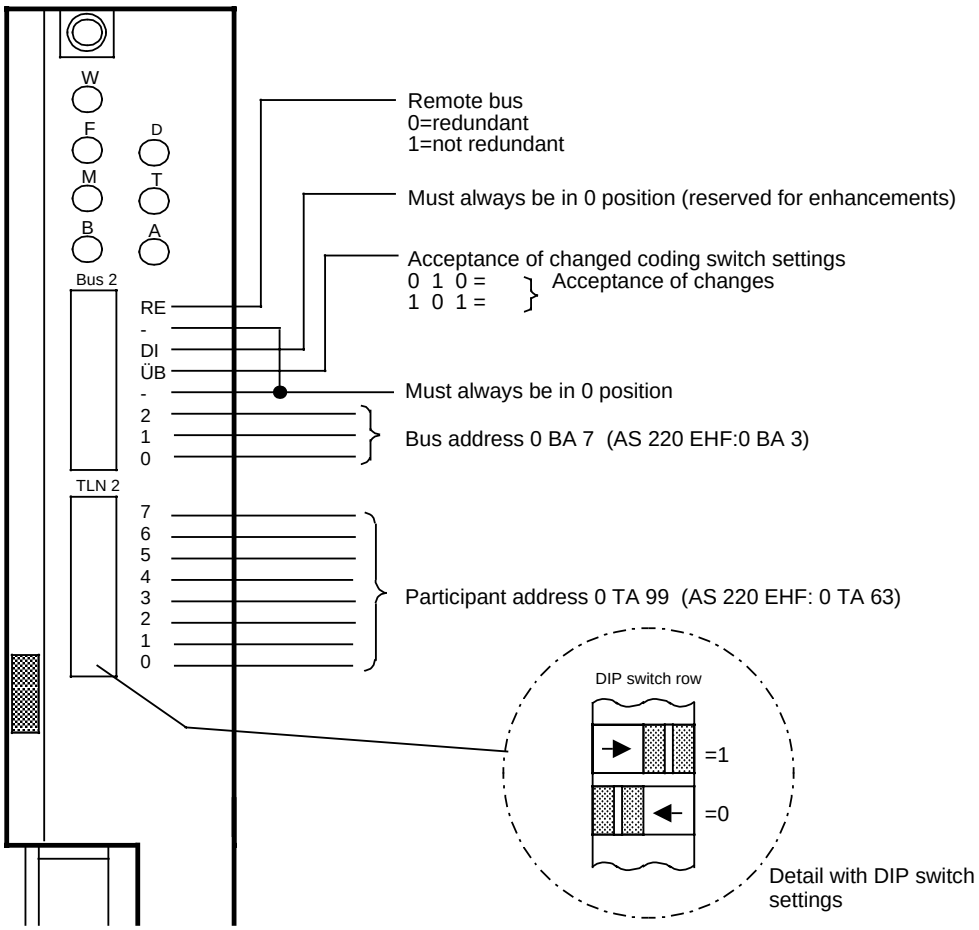
- **Local bus interface module N-AS** (6DS1 223-8AA)



Plug-in check local bus connector	X5 (9 1 / 10 2)	Local bus connector pin d18
With plug-in check Without plug-in check	0 0 0 0 0 1 0 0 0 0	Jumper inserted Irrelevant

0=Jumper removed
1=Jumper inserted

Fig. 4.35 Local bus interface module 6DS1 223-8AA



Participant address (TA)

The binary coded participant address is selected by the eight bottom DIP switches
Setting range: 0 TA 99 (AS 220 EHF: 0 TA 63)
The transmitter participant address must always be 31 if a common data (CD) link is used.

Bus address (BA)

The binary coded bus address is selected by the three bottom DIP switches of the upper switch row.
Setting range: 0 BA 7 (AS 220 EHF: 0 BA 3)

Warning

Setting BA=0 **and** TA=0 at the same time is not permitted.
Jumper setting of CPU I and CPU II must be identical.
CPU I bus address = CPU II bus address
CPU I participant address CPU I = CPU I I participant address

Bus redundancy (RE)

The CS 275 bus system permits operation on a redundant or single-structured remote bus. The required mode can be selected by the RE switch.

Setting: 0=redundant remote bus
1=non-redundant remote bus

Acceptance (ÜB)

Actuating the ÜB switch accepts the switch settings that have been changed (e.g. during the running operation).
Acceptance: 1 1 0 or 1 0 1

Fig. 4.36 Local bus interface module 6DS1 223-8AA (DIP switch settings)

- **Local bus interface module N8-H** (bus processor)

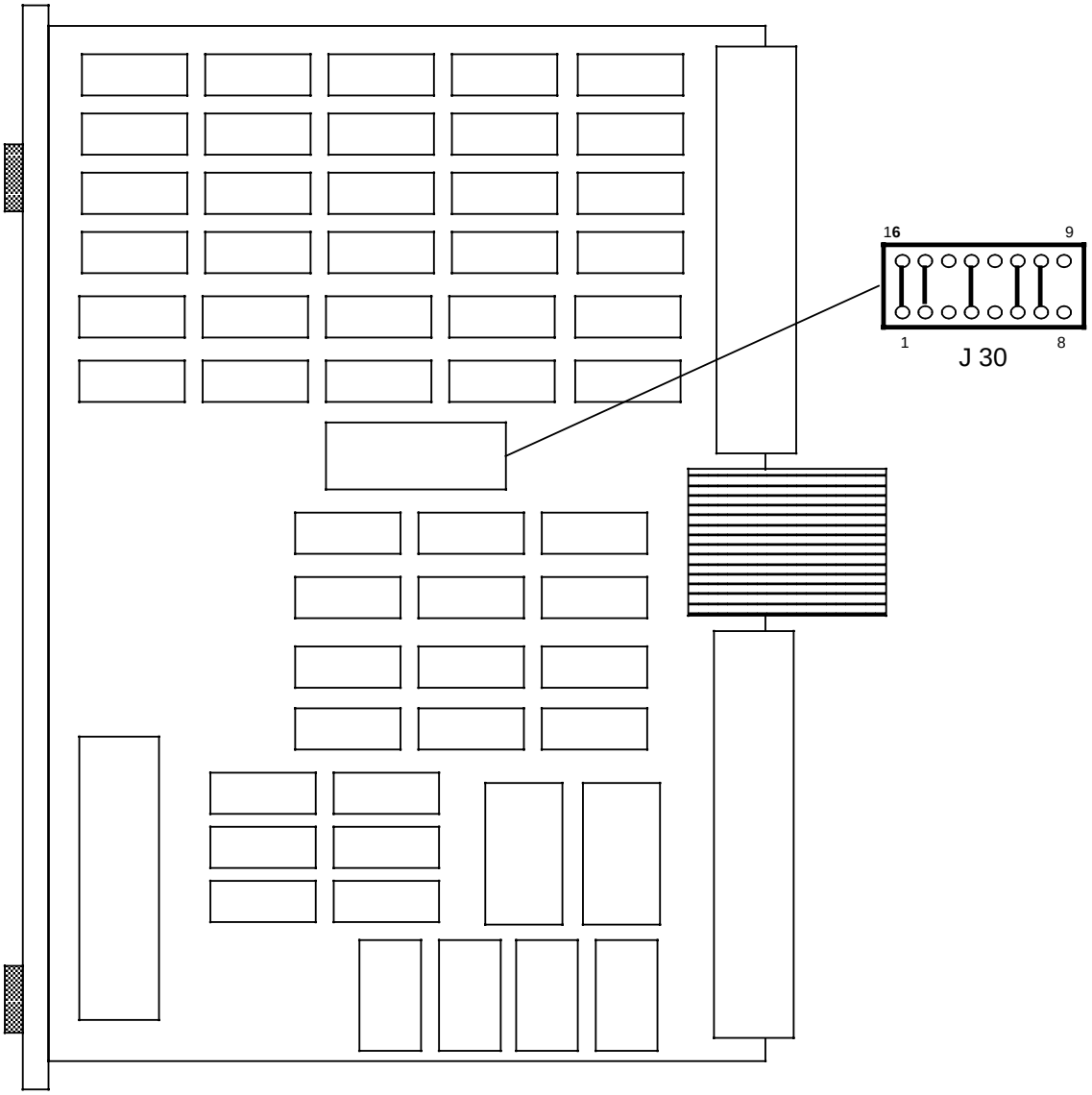
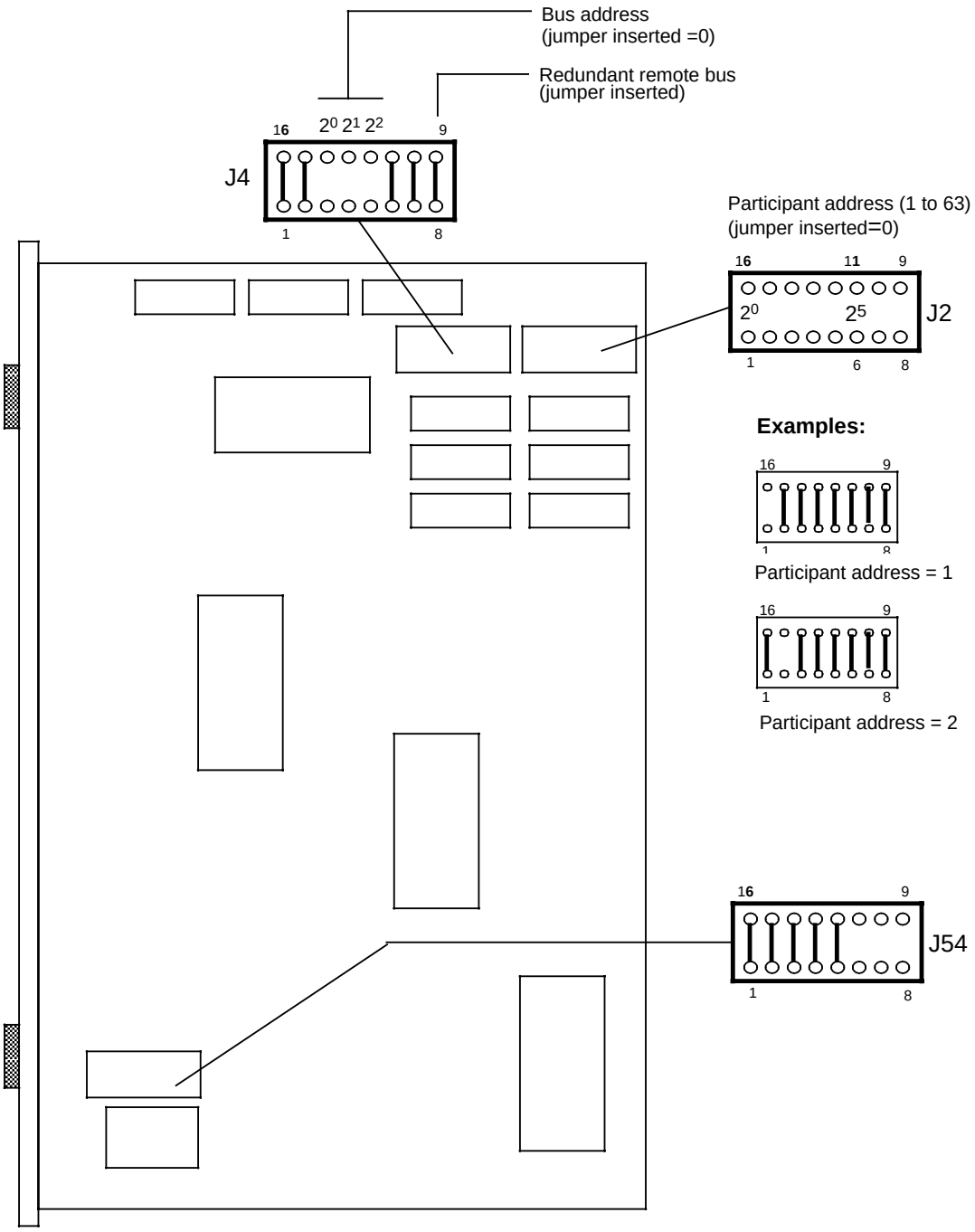


Fig. 4.37 Local bus interface module N8-H, 6DS1 220-8AA (bus processor)

The shown jumper configuration has been set up in the factory and must not be modified. The jumpers can only be accessed after the bus interface module has been removed from the bus processor module.

- **Local bus interface module N8-H** (bus interface)



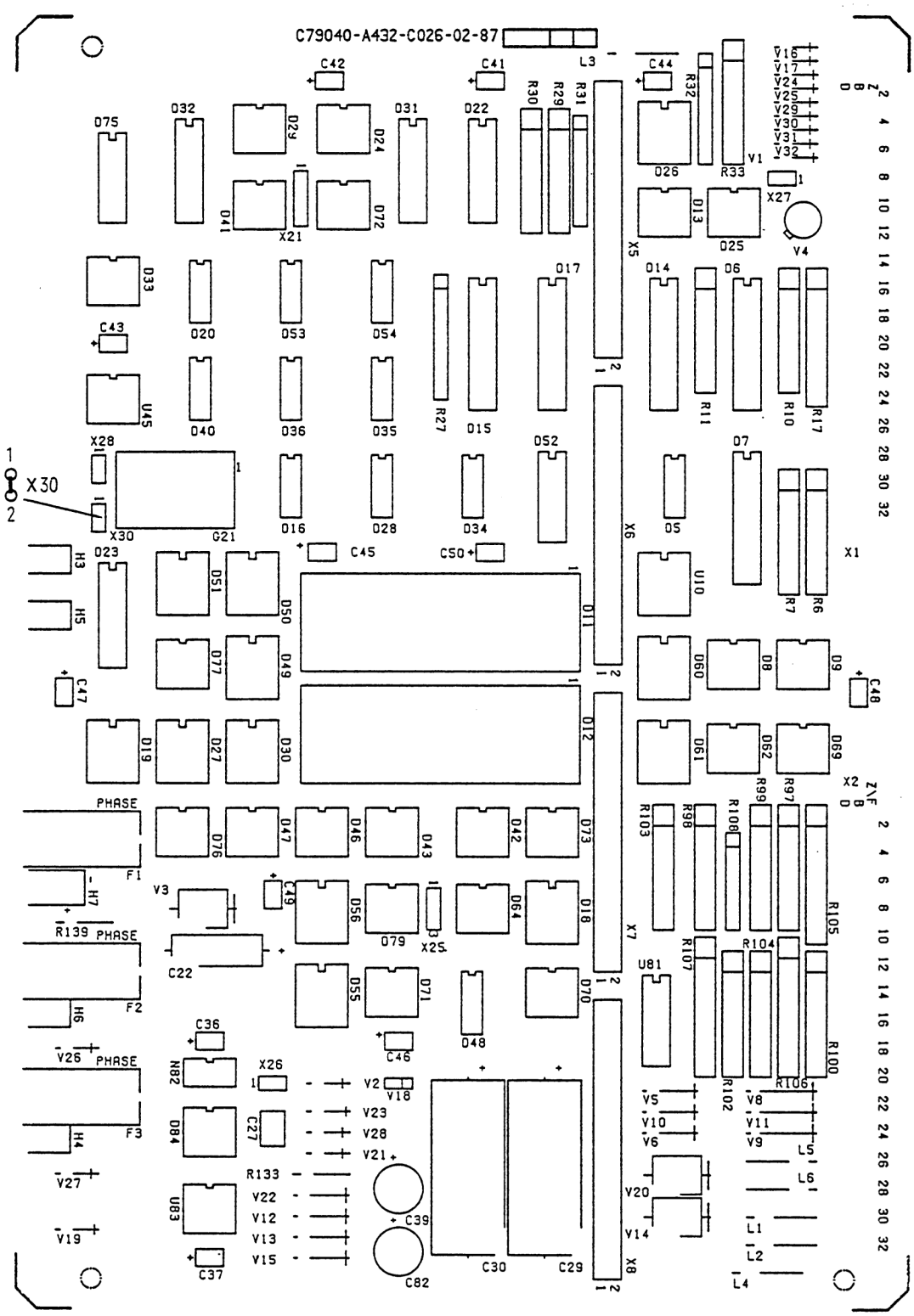
Jumper setting is to be performed in the same manner as if the module were to be used in a TELEPERM M AS 220 EHF or AS 220 H system.

Fig. 4.38 Local bus interface module N8-H 6DS1 220-8AA (bus interface)

Caution

Setting BA=0 **and** TA=0 (i.e. all jumpers of J2 and J4 inserted) is not permitted.
The jumper settings on CPU I and CPU II must be identical.
CPU I bus address = CPU II bus address
CPU I participant address = CPU II particpant address

4.7.2 I/O Comparator and Switchover Module (EAVU)



The jumper X30 must only be inserted on the basic board of the EAVU module. EE-specific jumper settings (EAVU number, I/O address range, etc.) are made by wire jumpers on the backplane connector X2 of the EAVU slot (see following Chapter 4.7.3)

Fig. 4.38 I/O comparator and switchover module, basic board

4.7.3 Wire Jumpers at the EAVU X2 Backplane Connector

The AS 235 H system can only function properly if the correct wire jumpers have been inserted at the rear of the X2 backplane connectors in the EAVU slots of the individual extension units.

Since these wire jumpers are installed together with the connections to the X2 backplane connector at the factory, they must be (like the PLAD 10 and PLAD 11 soldering jumpers for the extension unit number) specified during configuration. The wire jumpers are either set up as wire-wrap or as maxi-termi-point connections (depends on the extension unit type).

The following parameters are defined by wire jumpers:

- EAVU number (0...3)
- slot numbers of the I/O modules allocated to this EAVU
- SF61 enabling and routing of the 3x16 inputs of this module
- filter enabling for INT1 signals.

The meaning of these wire jumpers of the EAVU is discussed in the Technical Description of the EAVU (Order No. C79000-T8076-C343, Reg. 5 in this Manual). Section 4.4 of that Description explains and illustrates the necessary jumper settings.

Connection of ES 100 K systems

If there is an empty extension unit (EE) in either the basic cabinet (GS) or the extension cabinet (ES) it is possible to connect an ES 100 K system each instead. The interface module required in such a case (i.e. 6DS1322-8AA) has to be installed in one of the existing extension units.

Even if the basic cabinet and the extension cabinet are fully equipped with three or four EEs respectively, another two ES 100 K systems can be connected to the basic cabinet and one more ES 100 K to the extension cabinet.

In order to ensure that the additional I/O modules installed in an ES 100 K are addressable, the slot addresses (SF number) used in the ES 100 K must be enabled for the EAVU concerned by additional jumpers on the EAVU backplane connector (X2).

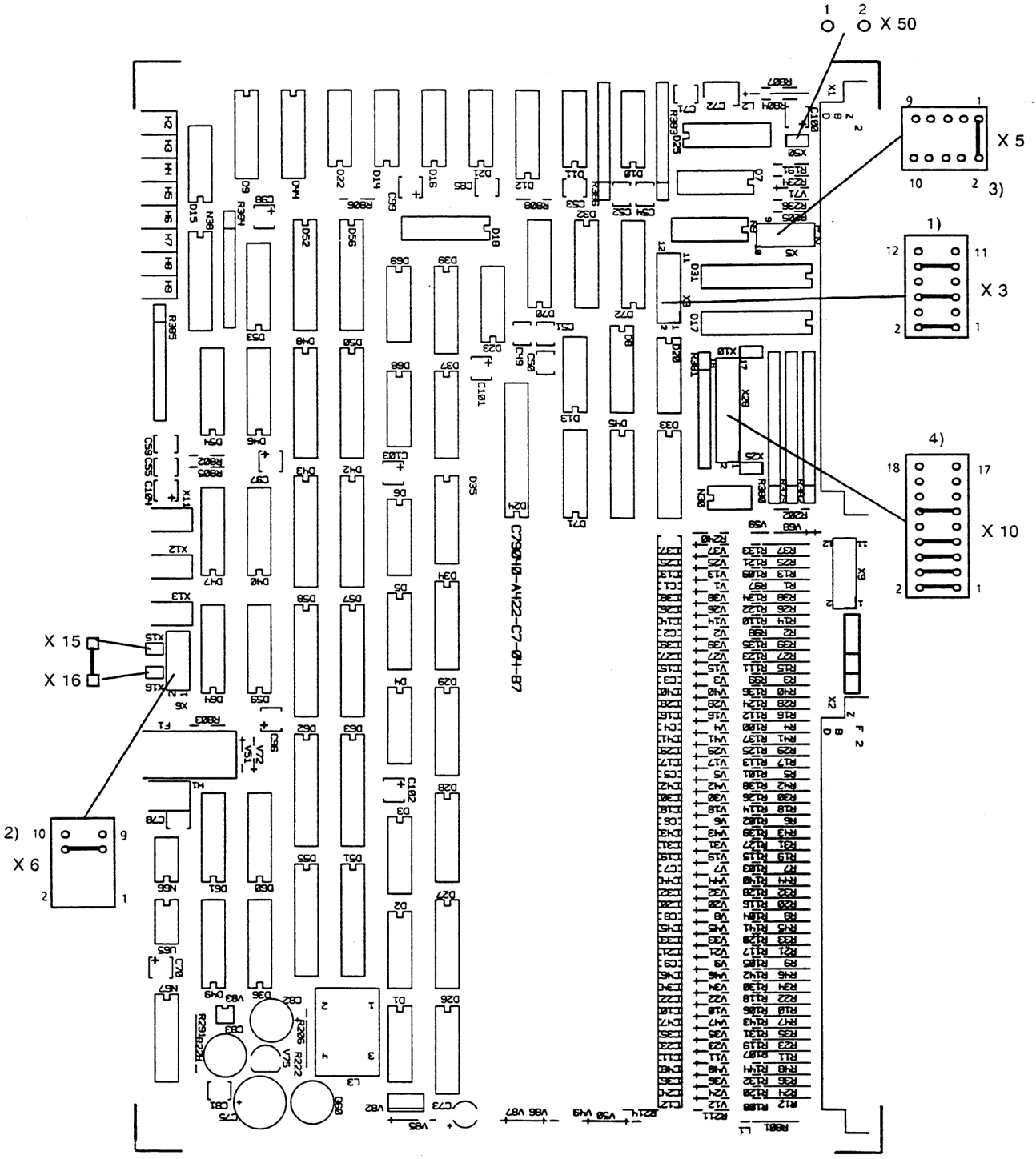
The jumper settings to be made on the backplane connector X2 of the EAVU in respect of ES 100 K systems are described in Chapter 4.7.6.

Caution

The jumper settings on the X2 backplane connector may only be changed during operation if the corresponding EAVU has been switched off.

4.7.4 SF61 Group Interrupt Module

(binary input module 6DS1 601-8BA or 6DS1615-8AA)



1) An interrupt is triggered by a positive edge on binary inputs 1...48.
2) The jumper X6/9-10 remains open if the blinking voltage is supplied from an external source.
3) The interrupt is issued on INT1 line (X1/z10).
4) The jumper setting corresponds to slot number 61.

Remarks on the use of 6DS 1615-8AA:
The jumpers X6/1-2, X6/3-4 and X6/5-6 for input filtering and interrupt delimitation as well as the jumpers at X9 for the 48-V contact voltage have to be set in addition as described in the instructions.

Fig. 4.40 Group interrupt modules (SF61) 6DS1 601-8BA and 6DS1615-8AA

4.7.5 Slot Addresses in the I/O Area

Notes on slot addresses

Each slot in the extension unit is assigned a firm address (SF number) via the backplane and the soldering jumpers PLAD11 and PLAD10.

I/O modules with automatic slot addressing are automatically assigned their respective slot address upon installation. For reasons listed below the I/O modules **without** automatic slot addressing should also be installed at the slot address planned for them:

- to ensure clarity during maintenance
- to avoid doubly assigned slot addresses
- In contrast to AS 235, an I/O module might not be addressable at a different slot address because the associated EAVU has blocked the address concerned due to its jumper setting.

Slot addresses in the central cabinet, EABA 1 (PESPA)

EE no. 1
EAVU no. 0
SF number

0	1	2	3	4	5	6	7	8	9	10	11	61 Int or 12	EA VU
0	1	2	3	4	5	6	7	8	9	10	11	12	13

Slot addresss AD9...6
Slot no. 1 2 3 4 5 6 7 8 9 10 11 12 13 14

Jumpers at the rear of the extension unit

PLAD11 PLAD10

EE no. 2
EAVU no. 1
SF number

16	17	18	19	20	21	22	23	24	25	26	27	61 Int or 28	EA VU
0	1	2	3	4	5	6	7	8	9	10	11	12	13

Slot address AD9...6
Slot no. 1 2 3 4 5 6 7 8 9 10 11 12 13 14

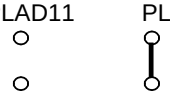
PLAD11 PLAD10

EE no. 3
EAVU no. 2
SF number

32	33	34	35	36	37	38	39	40	41	42	43	61 Int or 44	EA VU
0	1	2	3	4	5	6	7	8	9	10	11	12	13

Slot address AD9...6
Slot no. 1 2 3 4 5 6 7 8 9 10 11 12 13 14

PLAD11 PLAD10



Slot addresses in the extension cabinet, EABA 2 (PESPB)

EE no. 4
EAVU no. 0
SF number

100	101	102	103	104	105	106	107	108	109	110	111	112	EA VU
0	1	2	3	4	5	6	7	8	9	10	11	12	13
1	2	3	4	5	6	7	8	9	10	11	12	13	14

Slot address AD9...6
Slot no.

Jumpers at the rear of the extension unit

PLAD11 PLAD10

EE no. 5
EAVU no. 1
SF number

116	117	118	119	120	121	122	123	124	125	126	127	128	EA VU
0	1	2	3	4	5	6	7	8	9	10	11	12	13
1	2	3	4	5	6	7	8	9	10	11	12	13	14

Slot address AD9...6
Slot no.

PLAD11 PLAD10

EE no. 7
EAVU no. 2
SF number

132	133	134	135	136	137	138	139	140	141	142	143	144	EA VU
0	1	2	3	4	5	6	7	8	9	10	11	12	13
1	2	3	4	5	6	7	8	9	10	11	12	13	14

Slot address AD9...6
Slot no.

PLAD11 PLAD10

EE no. 7
EAVU no. 3
SF number

148	149	150	151	152	153	154	155	156	157	158	159	160	EA VU
0	1	2	3	4	5	6	7	8	9	10	11	12	13
1	2	3	4	5	6	7	8	9	10	11	12	13	14

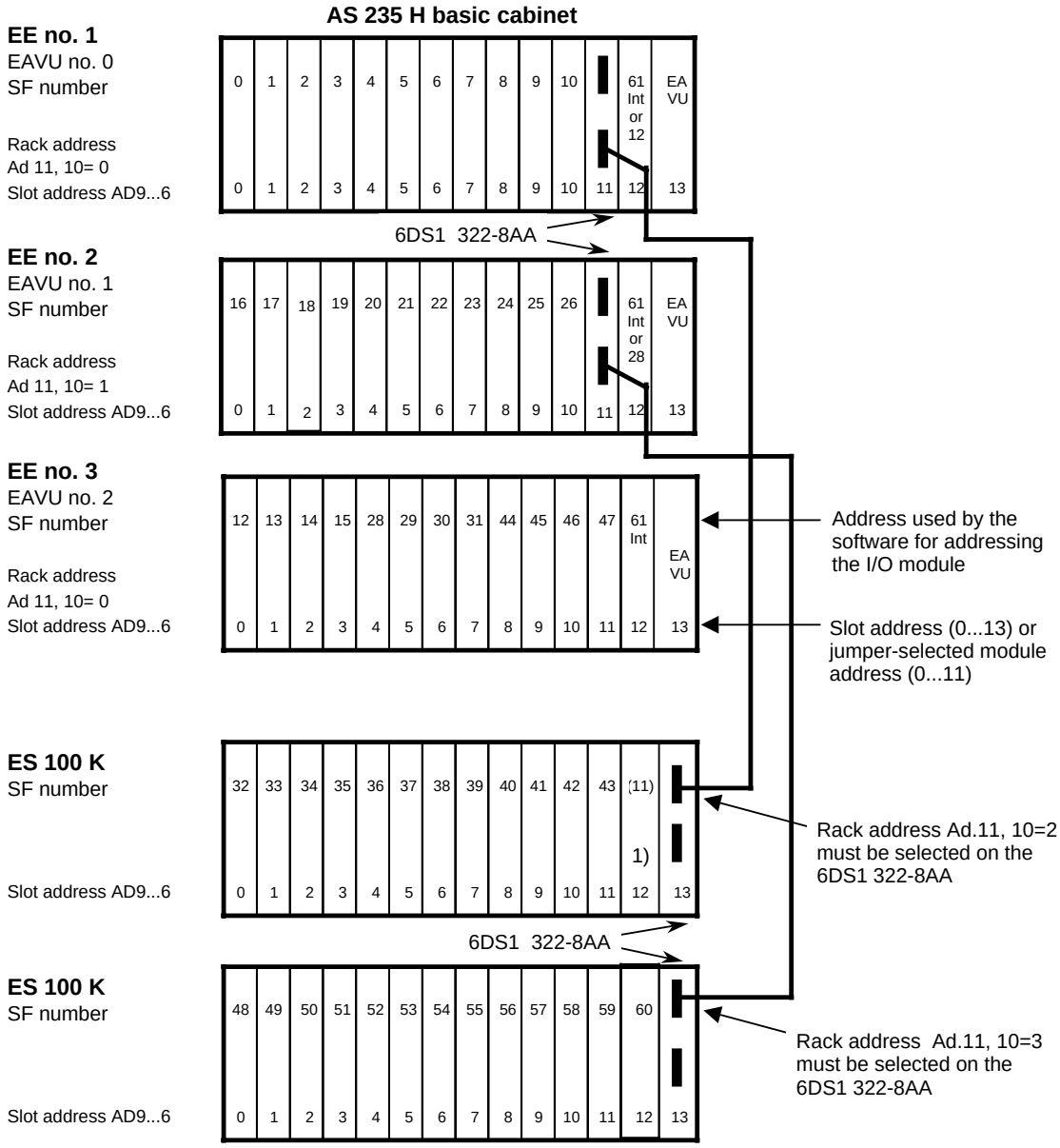
Slot address AD9...6
Slot no.

PLAD11 PLAD10

4.7.6 Slot Addresses and Jumper Settings for ES 100 K

The following configurations are suggested if the ES 100 K extension system is to be used as an extension of the AS 235 H system.

Configuration suggestion 1

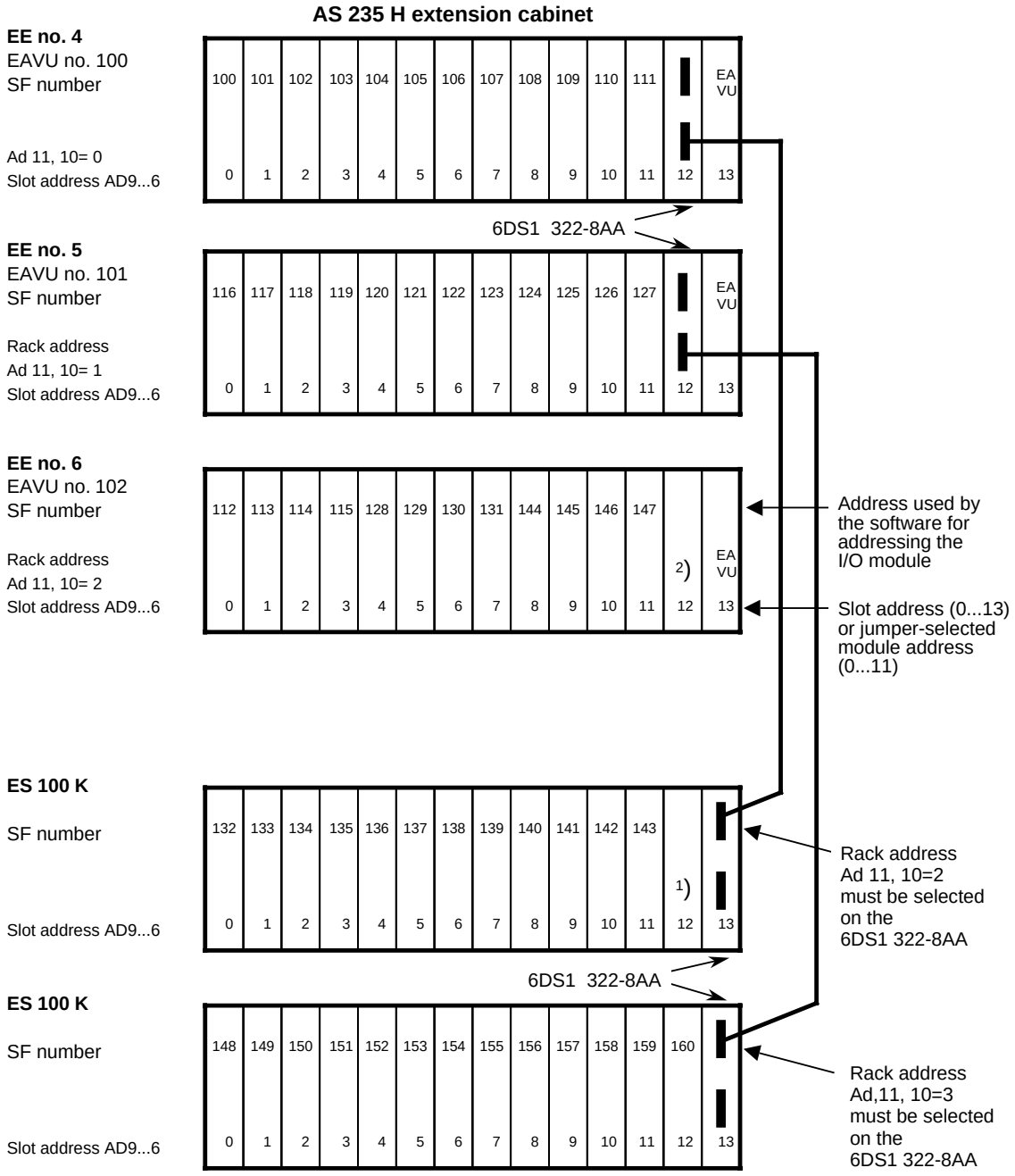


Jumper, jumper pair	Name	Set (B) on extension unit EE1	EE2	EE3	
f12–d12 , f24–d24 f10–d10 , f22–d22	NrLSB NrMSB	B B	– B	B –	–
f14–d4 , f16–d16 b4–d4 , b16–d16	/Pe0Fg /Pe1Fg	B –	– B	– –	
f6–d6 , f18–d18 b6–d6 , b18–d18	/Pe2Fg /Pe3Fg	B –	– B	– –	
b10–z10 , b22–z22	/MitL	–	–	B	
f8–d8 , f20–d20 b8–d8 , b20–d20 z8–z6 , z20–z18	/I0Fg /I1Fg /I2Fg	B – –	– B –	– – B	
Soldering jumper on EE Soldering jumper on EE	PLAD10 PLAD11	B B	– B	B B	

1) This slot may only be used for I/O modules without automatic slot addressing.

B=Jumper (pair) set

Configuration suggestion 2



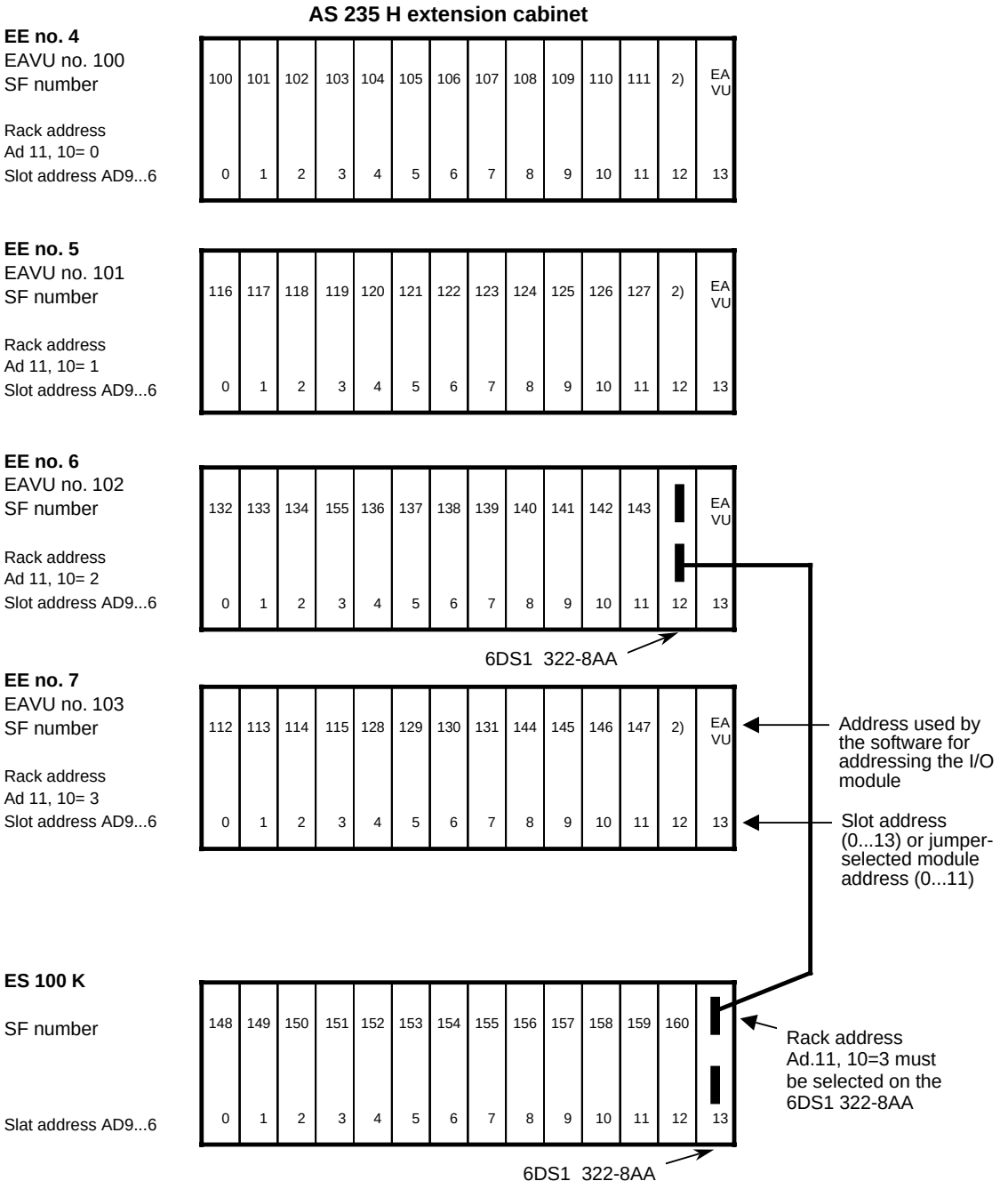
Jumper, jumper pair	Name	Set (B) on extension unit		
		EE 4	EE 5	EE 6
f12–d12 , f24–d24 f10–d10 , f22–d22	NrLSB NrMSB	B B	– B	B –
f14–d4 , f16–d16 b4–d4 , b16–d16	/Pe0Fg /Pe1Fg	B –	– B	– –
f6–d6 , f18–d18 b6–d6 , b18–d18	/Pe2Fg /Pe3Fg	B –	– B	– –
b10–z10 , b22–z22	/MitL	–	–	B
f8–d8 , f20–d20 b8–d8 , b20–d20 z8–z6 , z20–z18	/I0Fg /I1Fg /I2Fg	– – –	– – –	– – –
Soldering jumper on EE Soldering jumper on EE	PLAD10 PLAD11	B B	– B	B B

1) This slot may only be used for I/O modules without automatic addressing. The slot addresses (100 to 111) set via jumpers may not be used in EE4, i.e. the slot concerned in the EE4 cannot be used then.

2) This slot cannot be used for I/O modules.

B) = Jumper (pair) set

Configuration suggestion 3



Jumper, jumper pair	Name	set (B) on extension unit			
		EE 4	EE 5	EE 6	EE 7
f12–d12 , f24–d24 f10–d10 , f22–d22	NrLSB NrMSB	B B	– B	B –	– –
f14–d4 , f16–d16 b4–d4 , b16–d16	/Pe0Fg /Pe1Fg	B –	– B	– –	– –
f6–d6 , f18–d18 b6–d6 , b18–d18	/Pe2Fg /Pe3Fg	– –	– –	B B	– –
b10–z10 , b22–z22	/MitL	–	–	–	B
f8–d8 , f20–d20 b8–d8 , b20–d20 z8–z6 , z20–z18	/I0Fg /I1Fg /I2Fg	– – –	– – –	– – –	– – –
Soldering jumper on EE Soldering jumper on EE	PLAD10 PLAD11	B B	– B	B –	B B

2) This slot cannot be used for I/O modules

B=Jumper (pair) set

All I/O slots may be equipped in any order with the permissible modules of the TELEPERM M standard spectrum or a permissible selection of TELEPERM ME modules.

Achtung

Use **all** I/O modules with an address identical to the slot addressing.
Observe the exception below.

In this way, these modules assume in their slot the address preset in the subrack.

Exception:

Individual modules of the TELEPERM M standard spectrum can **only** be operated with jumper settings. Set the associated slot address on these modules.

N-V.24 or CP581-TM interface modules may only be installed in one extension unit (EE) (not in ES 100 K).

Only one N-V.24 or CP581-TM module is permitted per extension unit.

These modules do not occupy a slot address.

4.7.7 Blinking Clock-Pulse Generator 6DS1 922-8AA (BL)

The blinking clock-pulse generator must be inserted in the power supply subrack in slot G165.
It has the following functions:

- Central blinking pulse for I/O modules
- Lamp test for process peripherals
- Electrical isolation of time synchronization signals by external minutes pulse.

• Blinking pulse

A blinking signal (BS1 + BS2) is generated centrally by the blinking clock-pulse generator for the I/O subracks of the basic and extension cabinets. The fault LEDs on the I/O modules and the EAVUs then flash synchronously in the event of a fault.
The fault LEDs of the two cabinets can also be synchronized using settings on the blinking clock-pulse generator.

The two blinking signals are fused by PÜ1 + PÜ2 on the blinking clock-pulse generator.
The LEDs on the front panel of the module indicate whether the voltages are present for BS and time synchronization.

• Lamp test

To enable a lamp test, a signal for cabinet 1 (SK1) and cabinet 2 (SK2) can be connected to the I/O subracks by the switch LT.
Like the blinking signals, the lamp test signal is fused by LTV.
The wiring of the signal BS from the blinking clock-pulse generator is shown in the circuit diagram for the basic and extension cabinets. LT must be wired by the user for each I/O module specific to the slot in order to prevent an abrupt overloading of L+ in the extension units.

• Time synchronization

The system can be synchronized by an external timing pulse (minute pulse).
This external pulse must be connected to the blinking clock-pulse generator.
The two external signal lines (signal line + reference potential) can be connected as desired to the two (floating) inputs d22 and z20 using flat tabs (6.3 x 0.8 mm).

The jumper settings have to be modified on the 1st I/O bus interface module accordingly.

• Spare alarm (RES1)

If the input is not required for time synchronization via minute pulses (e.g. with bus-coupled systems), it can also be used for any other externally controllable I&C message (S349).

The external signal (24-V level) is connected to d22 of the blinking clock-pulse generator, z20 is assigned to the ground**/**reference potential of the alarm signal. Alarm= no current flow.

The jumper settings on the 1st EABG correspond to the default setting. The jumper is removed from the power supply subrack (default = 24 V).

- Blinking clock-pulse generator

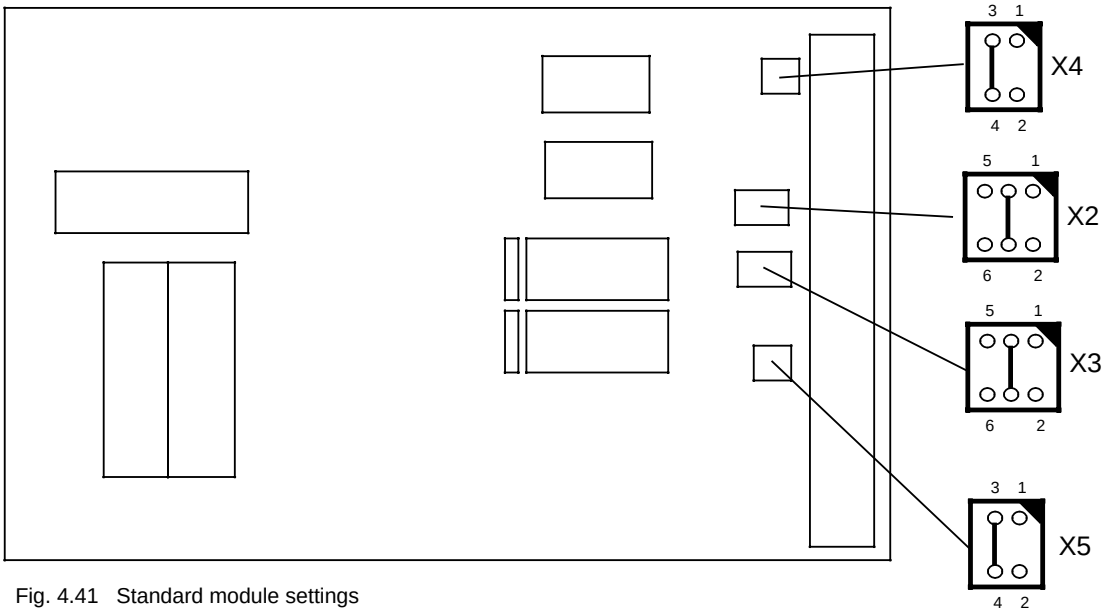


Fig. 4.41 Standard module settings

– Lamp test settings at X2 for SK1 and X3 for SK2

Jumper 1-2: The lamp test outputs are relay outputs

Function of outputs	Outputs for	
	SK1	SK2
W (common point)	b12	b14
A (NO contact)	d12	d14
R (NC contact)	z12	z14

Jumper 3-4: The lamp test outputs are signal outputs. With the switch in the center position, the L+ voltage is applied to z12 and z14.
With switch position SK1, L+ is output at d12 and z14.
With switch position SK2, L+ is output at z12 and d14.

Jumper 5-6: Function as jumper 3-4 except that the reference potential M is output instead of L+.

– Synchronization of blinking signal X4

Jumper 1-2: BS1 is synchronized by BS2
Jumper 3-4: BS2 is synchronized by BS1

– Synchronization of blinking signal X5

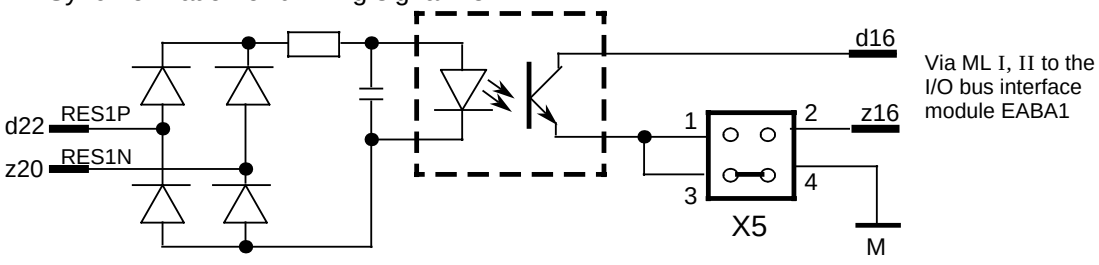
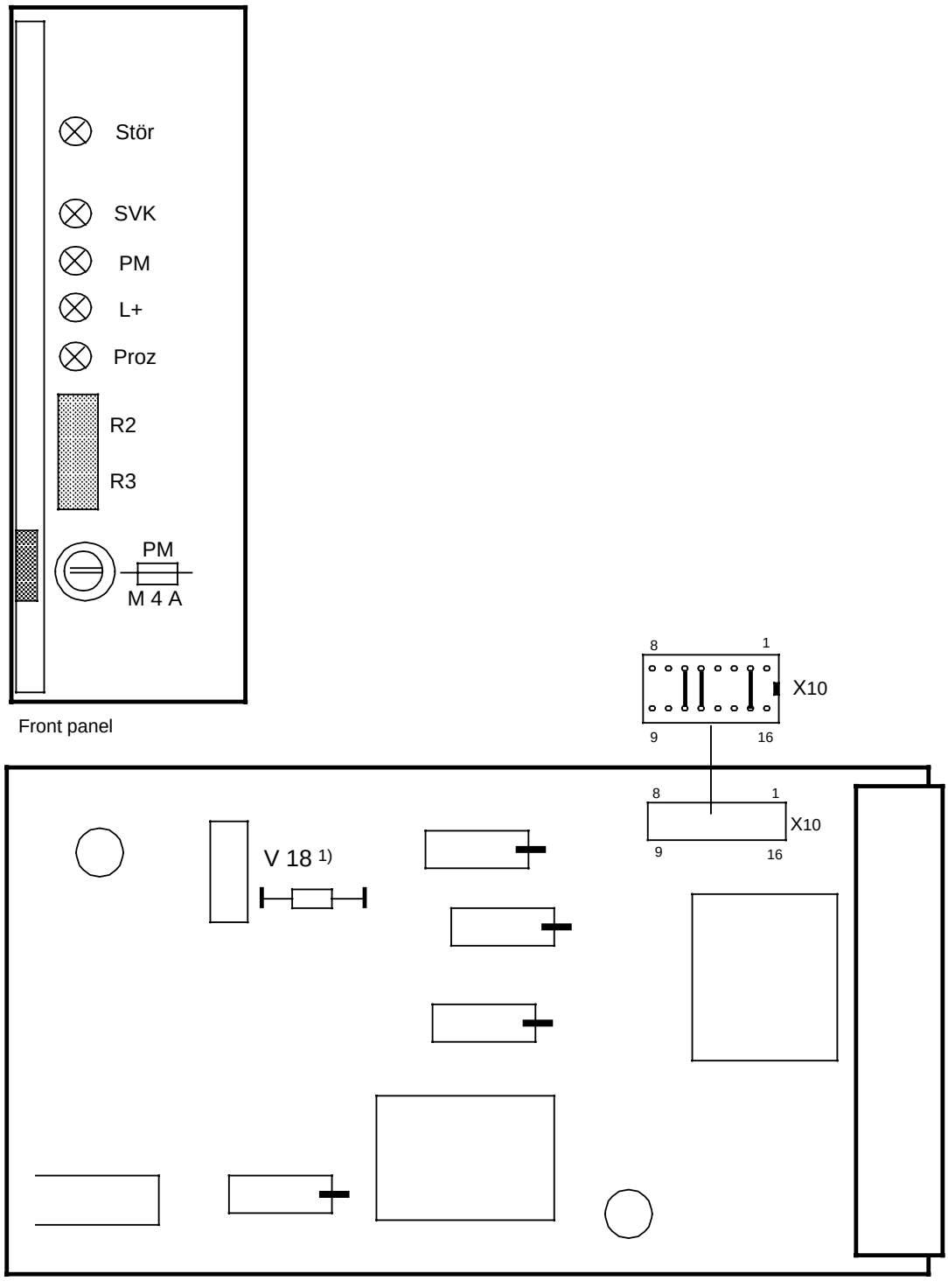


Fig. 4.42 Jumper assignment on the blinking clock-pulse generator (BL) with time synchronization via minutes pulses

4.7.8 Cabinet Power Supply Unit (SES)

- Alarm logic module (ML)



1) V18 must be removed

Fig. 4.43 Alarm logic module 6DS1 901-8AA

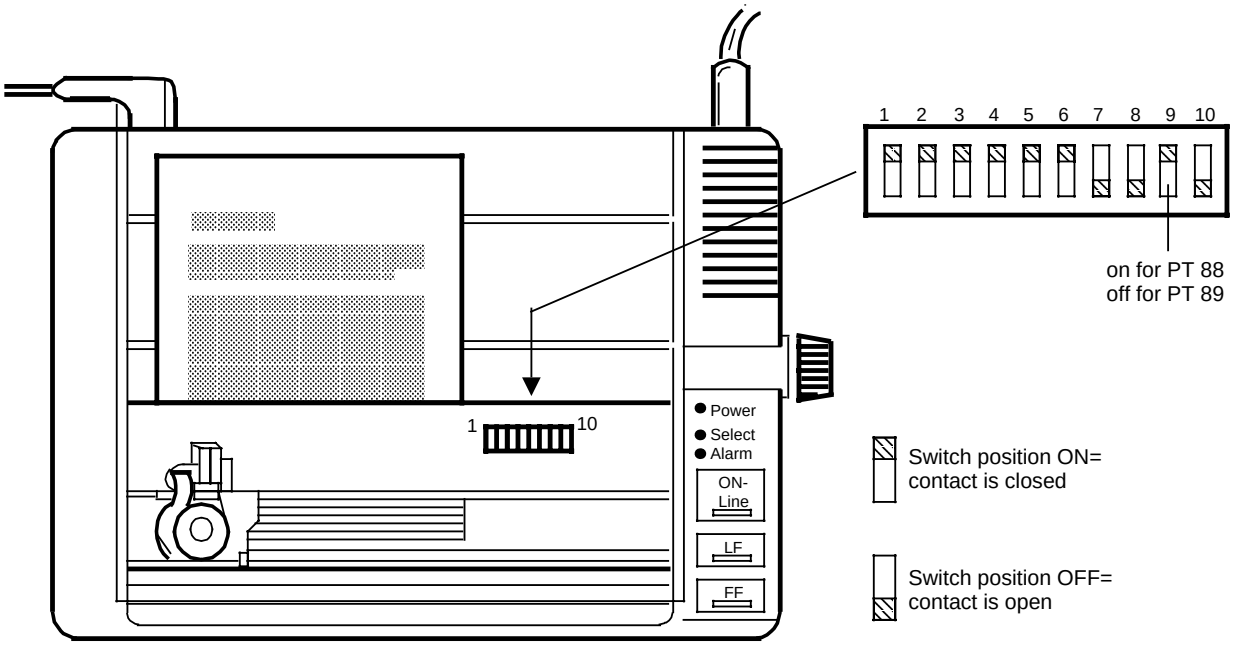
4.7.9 Setting up the Event Recorder and Logging Printer

4.7.9.1 PT88/89 Printer

– Setting the DIP switches

The DIP switches are underneath the cover on the central control unit ZS and may be accessed after the front door of the printer housing has been opened. The state upon delivery is represented Fig. 5.14).

Different standard functions and the desired font are selected with the ZS coding switch .The user-selected switch positions are read by the controller after "Power on" or "input prime".
Changing the switch positions has no effect as long as the printer remains switched on. The default selections specified before power has been switched on are accepted once the commands "reset to normal position" or "reset parameters" have been received.



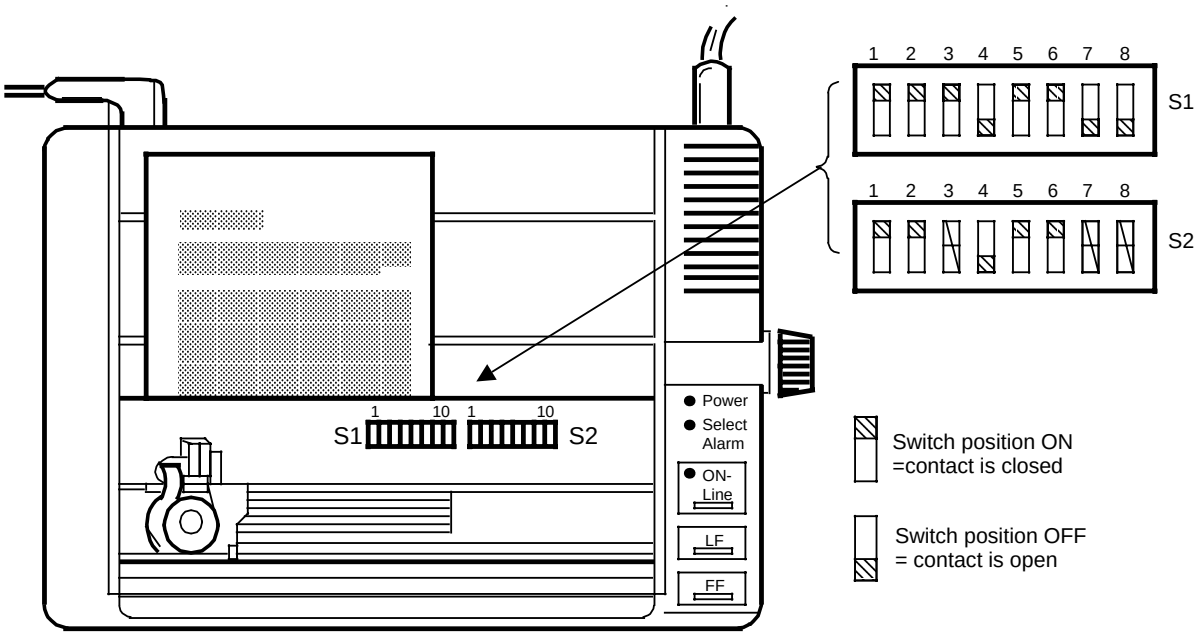
Switch 1 2	Fonts, special characters												
● ● ●	ASCII	#	$	@	[	\	]	^	`	{	|	}	-
● ● ○	S/SF	§	¤	É	Ä	Ö	Å	^	é	ä	ö	å	ü
● ○ ●	GB	£	$	@	[	\	]	^	`	{	|	}	-
● ○ ○	E	#	$	@	¡	Ñ	¿	^	`	^	´	ç	¨
○ ● ●	IA Nr. 5	#	¤	@	[	\	]	^	`	{	|	}	-
○ ● ○	D	#	$	§	Ä	Ö	Ü	^	`	ä	ö	ü	ß
○ ○ ●	DK/N	#	¤	É	Æ	Ø	Å	Ü	é	æ	ø	å	ü
○ ○ ○	F/B	£	$	à	°	ç	§	^	`	é	ù	è	¨

● ON ; ○ OFF

Switch	ON	OFF	Comment
4	**LF = LF**	LF=CR+LF	Paper feed
5	**CR = CR**	CR=CR+LF	
6	even (no parity: Bit 8=H during trans.)	odd (no parity: Bit 8=H during trans.)	Parity
7	off	**ein**	
8	11"	**12"**	Page length
9	**1/6"**	1/8"	Line feed
10	**PT 88**	**PT 89**	Paper width

= Switch position to be performed

Fig. 4.44 PT88/89 settings



All switches are on ON position when delivered.

Coding switch S1

Switch functions		Switch 1	2	3	4	5	6	7	8
Font	ASCII	●	●	●					
	Swedish	●	●	○					
	British	●	○	●					
	Spanish	●	○	○					
	IA No.5	○	●	●					
	German	○	●	○					
	Danish	○	○	●					
	French	○	○	○					
Paper feed	with line feed				●				
	without line feed				○				
	LF=CR+LF					●			
	LF=LF					○			
Print mode	Normalschrift						●		
	Schönschrift						○		
Zero	Zero = 0							●	
	Zero = 0							○	
Page length	11 inches								●
	12 inches								○

Coding switch S2

Switch functions		Switch 1	2	3	4	5	6	7	8
Line feed	1/6 inch	●							
	1/8 inch	○							
Skip over perforation	1 inch		●						
	off		○						
Parity	none				●				
	even				○	●			
	odd				○	○			
Buzzer	on						●		
	off						○		
Switches 3, 7 and 8 are not used									

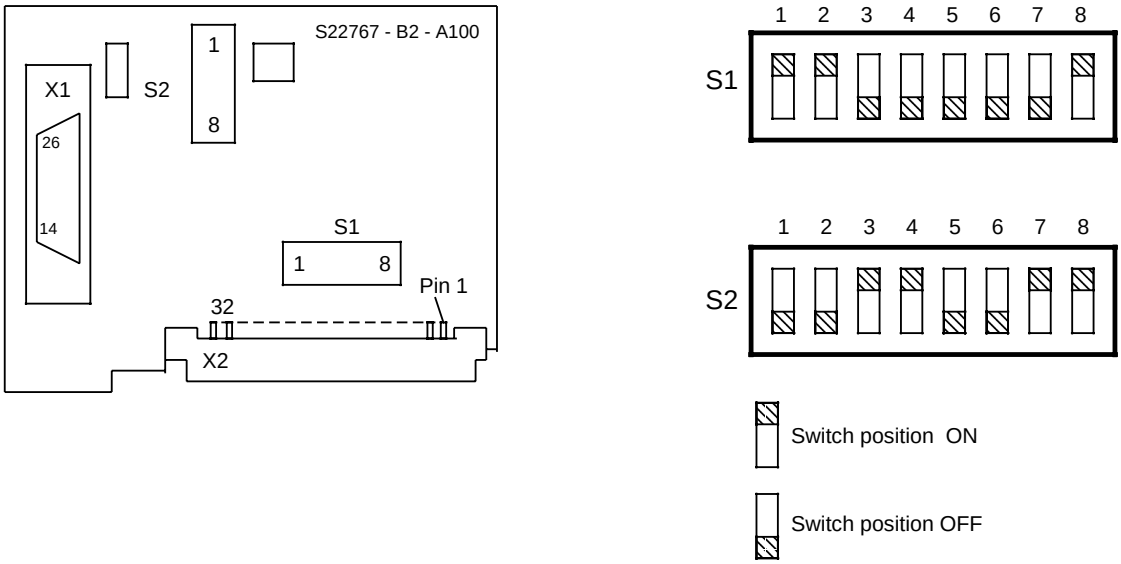
● ON ; ○ OFF

Preferred setting

Fig. 4.45 PT88/89 settings

- Setting the TTY 20 mA mode selector switch (SAP-S2)

The following overview summarizes the settings of the S1 and S2 mode selector switches that are required for the individual modes.



Switch S1 SAP-S1, SAP-S2	Baud rate bit/s							
	110	200	300	600	1200	2400	4800	9600
1	○	●	○	●	○	●	○	●
2	○	○	●	●	○	○	●	●
3	○	○	○	○	●	●	●	●

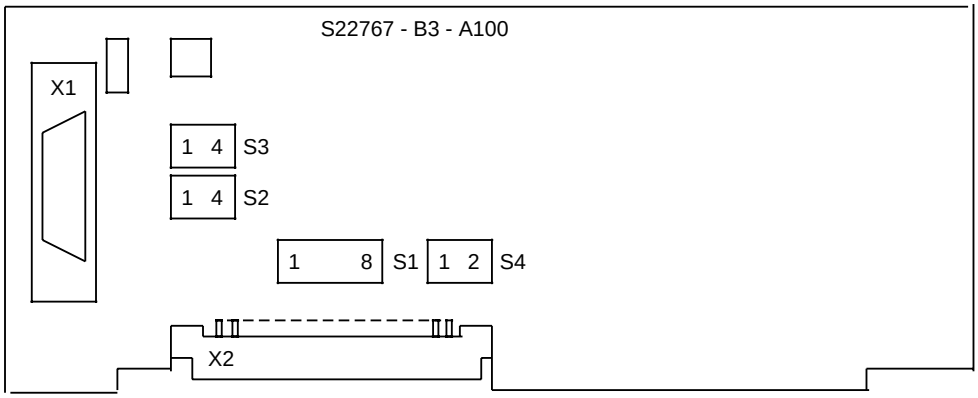
Mode		S1					S2							
		4	5	6	7	8	1	2	3	4	5	6	7	8
X-ON/X-OFF protocol		●	○	●	○									
BUSY	Current	○	○	○	●	○								
	No current	○	○	○	○	●								
Internal supply							○	○	●	●	○	○	●	●
Extern. supply with protective resistor							●	○	○	○	●	○	○	○
Extern. supply without protective resist.							○	●	○	○	○	●	○	○

Required setting ● = ON ○ = OFF

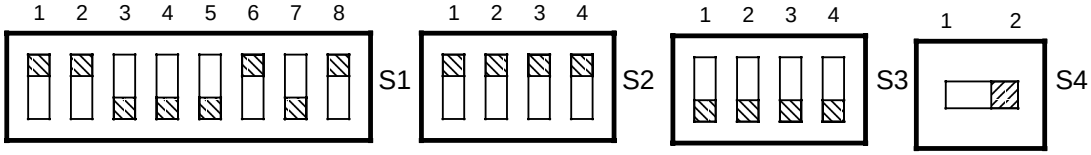
Fig. 4.46 TTY interface mode selection

- Setting the V.24/TTY combination interface mode selector switch

The S1 ... S4 mode selector switches on the combination interface modules are to be set according to the following specifications:

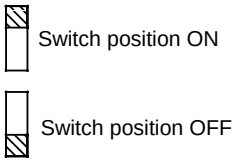


Multiple interface adapter



Baud rate

bit/s	S1		
	1	2	3
110	○	○	○
200	●	○	○
300	○	●	○
600	●	●	



Mode		S1					S2				S3			
		4	5	6	7	8	1	2	3	4	5	6	7	8
X-ON/X-OFF protocol		●	○	○	●									
BUSY	Current	○	●	○	○	●								
	No current	○	○	●	○	●								
Internal supply							●	●	●	●	○	○	○	○
Extern. supply with protective resistor							○	○	○	○	●	●	○	○
Extern. supply without protective resist.							○	○	○	○	○	○	●	●

Required setting ● = ON ; ○ = OFF

Fig. 4.47 V.24/TTY interface mode selection

Instructions for use:

- The baud rate is 600 bits/s
- The cable length is limited to 100 m (from the cabinet)
- Possible connection with TTY interface only
- 4-kB data buffer for the printer is required
- The printer cannot detect FF control holes
- Italic print is not possible
- The printer may only be used if the control characters for italic print have been removed from the AS 235 user program.

The following components must be installed in order to be able to use the PT88**/**89 printer:

TTY 20 mA	S22767-B2-A100 or
RS-232-C/TTY 20 mA	S22767-B3-A100
4 kB data buffer	S22761-L301
Connecting cable	6XV2155-8A..

PT88/89 operator input channel interface module

4.7.9.2 PT90 Printer

The following DIP switch settings are required on the interface module:

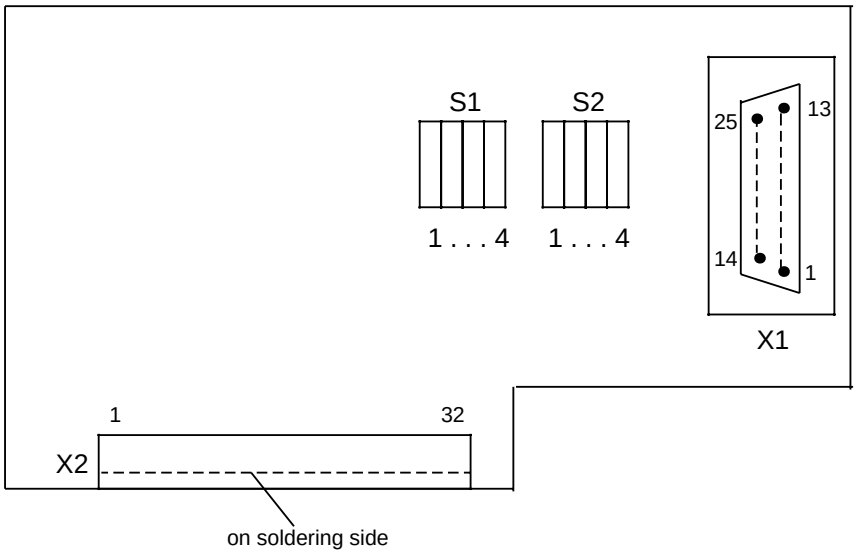


Fig. 4.48 Location of the X1 interface connector and the S1 and S2 mode selector switches on the module

Mode		Mode selector switch S1 1	S1 2	S1 3	S1 4	S2 1	S2 2	S2 3	S2 4
Internal supply	Transmitter	○	○					●	●
	Receiver			○	○	●	●		
External supply with protective resistor	Transmitter	○	●						
	Receiver			○	●				
External supply without protective resistor	Transmitter	●	○						
	Receiver			●	○				

● On
○ Off

Points a1 and a2 carry positive voltage if internal supply has been selected.

Fig. 4.49 Setting of the S1 and S2 mode selector switches

The other printer parameters are set in menu-driven operation.
Menu selections (also see PT 90 Description)

PT90 menu mode ON
Program version Siemens 2.2.3

1. Print parameters
2. Device parameters
3. Interface parameters
4. Test
5. Service

Keys: On Line = OFF, LF = NO, FF = YES

1. Print parameters

Page length (inch)	12
National character set	USASCII
Uni/bidirectional print	Bidirectional print
Character spacing	10 cpi
Character set	3
Vertical line spacing	6 lpi
Feeder cartridge	1
Graphics, dot group	1

2. Device parameters

Audible alarm	Enabled
Start of print	Variable
New line	LF
Shape of the numeral zero	No oblique
Dollar or asterisk	Dollar
Delete	Ignored
Bold columns	0
Graphic bit assignment	Bit 0 at top
Syntax errors	SMUDGE

3. Interface parameters

Character frame	7 bits, even parity
Baud rate	600 bits/s
Receive buffer	400
Receive buffer hysteresis	256
Transmit data line (serial)	BUSY inverted
Output lines (serial)	TTY/V.11
S1 and BUSY polarity (V.24)	P.20 S1, P.25 BUSY
Active inputs	None
ETX ACK (serial)	Disabled

4. Test

5. Service

PT 90 menu mode OFF

Note:

Instructions for setting the logging printer
(see Function Description AS 235 C79000-G8076-C416).

4.7.9.3 SICOMP DR 210-N / DR 211-N Printer

Also SICOMP DR 210-N**/**DR 211-N printers can be connected to AS 235 systems as event recorder and logging printers. For system reasons, the technical data are subject to limitations then.
The SICOMP DR 210-N and DR 211-N printers are equipped with a 9-needle matrix printing mechanism. Due to the low noise level of less than 52 dB(A) they are also suitable for control rooms.
Select the module with TTY interface and ECMA emulation as interface module.
The printers are operated via 4 function keys and 10 LEDs for displaying the parameter configuration and error messages. If the selected interface module has an ECMA emulation, these error messages can either be in German or English.

The printers offer the following functions for paper transport:

- ”Auto view" function

If the printer does, for instance, not receive any data for 1 second, the paper is automatically fed forward until the last printed line becomes visible. If further printing data are received, the printer paper is withdrawn and the new line printed without any gap.

- ”Auto tear-off”

The printed printer paper is fed forward to the tear-off edge and withdrawn to the printing position after the paper has been torn off.

- "Auto load"

Automatic adjustment of the first printing line when fan-fold paper is inserted.

The printing speed is 250 characters**/**s. A 17-Kbyte printing buffer must be selected when connecting the printer to AS 235 systems.

The two printers only differ in their respective form widths:

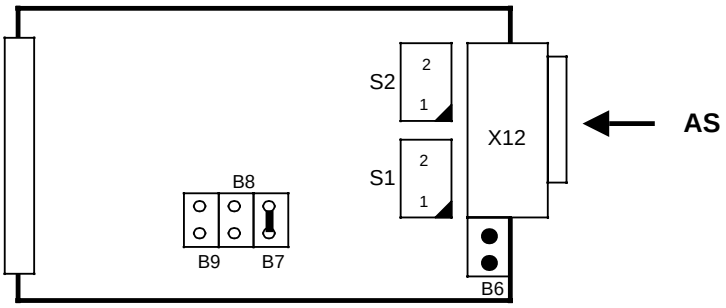
DR 210-N form width up to 254 mm (DIN A4)
DR 211-N form width up to 406 mm (DIN A3)

As transmission protocol, the setting takes place with READY**/**BUSY, the data format is 7 data bits, even parity, 1 stop bit.
The TTY interface has to be set to active mode on the transmitter and during reception.

A transfer rate of 600 bits**/**s has been configured (=default).

The connection to the AS takes place via the cable connector 6XV2 167-8AB...AU.

The following jumper and switch settings have to be made for AS 235 systems:



These jumper and switch settings have the following meaning:

B5 separates protective and signal earth
B7 applies READY-N to transmitter loop (=BUSY)
S1/2 position 2: active transmitter and receiver loop

Fig. 4.50 AS 235 jumper and switch settings

Operating the printer:

The printer has a control panel with four keys and one LED display matrix:

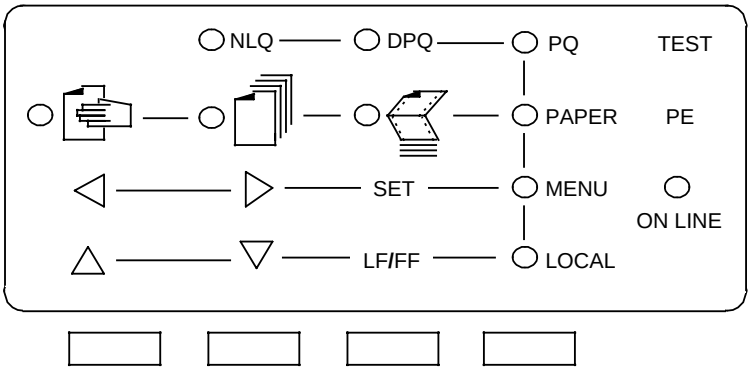


Fig. 4.51 Printer operation

All settings and parameter inputs are made via this control panel.

Printer settings: (parameter input)

MENU mode: (See Chapter 8 of the original Operating Instructions of the printer)
In this mode, the printer parameters are set for the first time or can be modified later on. The settings are made via the control panel.

Proceed as follows to set up the printer:
The current user configuration is activated when the printer is switched on.

- Call the MENU mode:

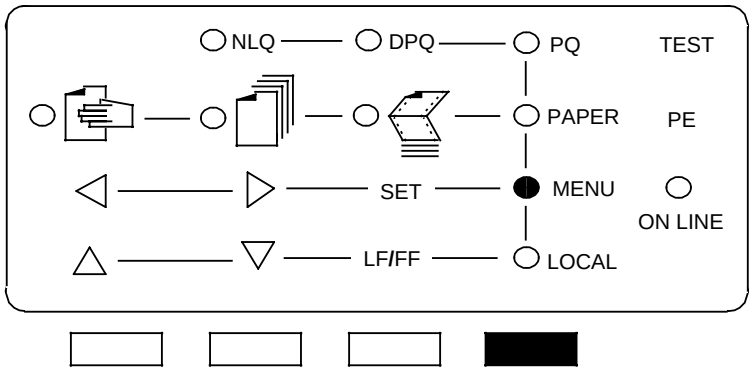


Fig. 4.52 Call the MENU mode

Press the key until the MENU LED lights up.
This is followed by:

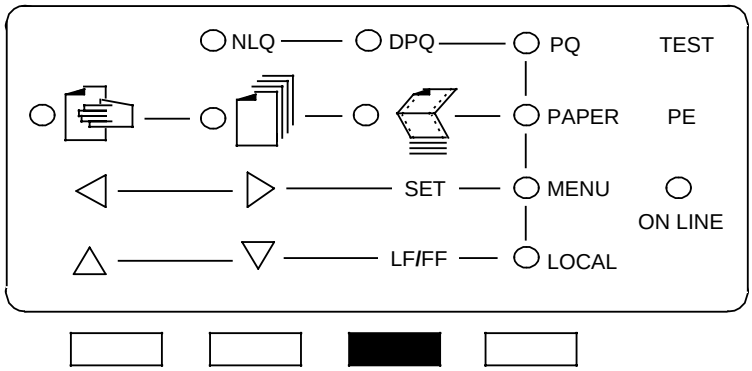


Fig. 4.53 Menu setting

Remove the front cover to set the menu.
The user menu and the technical menu can be configured now.

Print out the technical menu before modifying it.
(See Chapter 8 of the original SICOMP DR 210-N/DR 211-N Operating Instructions for operation and modification).

The following settings have to be made for the use with AS 235 systems:

Basic settings:	
Language	German
Character spacing	10 CPI,
Expanded print	no
Character representation	
Italics	no
Proportional	no
Zero with slash	yes or no
Character set	Courier Siemens ECMA
Character font	0= DRAFT
National character set	0= ASCII
Upper half of table	ISO 8859-1
Character features	
Bold type	no
Double impact	no
Double height	no
Line density	6 LPI
Paper format	
Form length	12"
Fold	0
Line length	80 with SICOMP DR210-N
	136 with SICOMP DR211-N
Printer options:	
Paper	not installed
Paper path	tractor
Ink ribbon	black
Color	black
Technical menu:	
Line feed control	
Paper command	+CR
Line overflow	CR+LF
CR	CR
LF	LF
Paper handling	OFF
Interface settings:	
Serial interface	
Receiver buffer	17 KB
Data bit	7 bits
Parity	even
Stop bit	1 stop bit
Baud rate	600
Status upon switching on	ON LINE
ESCAPE character	ESC

Technical settings

Printing offset	0
"Change paper" text	ON
Vertical increment:	1/72 inch
Device code	OFF

- Positioning the first printing line

For AS 235 systems, the setting is made in the user menu and in the technical menu with 20/72". The first printing line is then positioned 1. 41 cm below the perforation of the paper.

User menu:

1. Call the menu mode and select the user menu
2. Select "Paper format"
3. Select "Vertical adjustment"
4. Set = 20 for "Setting in 1/72 inch"
5. Select "Close" for storing the setting.

Make further adjustments or leave menu.

Technical menu

1. Print out "Technical menu"
2. Call "Technical menu"
3. Call "Technical settings"
2. Call "Phys. FORM settings"
3. Select "Continuous form"
4. Set = 20 for "Setting in 1/72 inch"
5. Select "Close" for storing the setting.

Make further adjustments or leave menu.

After the first printing line has been adjusted, the perforation of the paper (tear-off line) does no longer correspond to the tear-off edge of the printer. The position of the paper perforation must be set once more afterwards. (Also see original Operating Instructions of the printer and ”Operator input mode”.

- Operator input mode

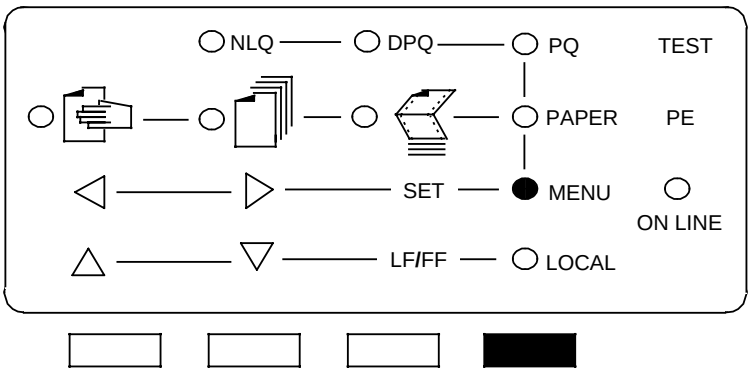


Fig. 4.54 Operator input mode

The operator input mode is switched over using the marked key. The associated LED lights up:

PQ	Set paper quality
PAPER	Paper feed
MENU	Printer configuration
LOCAL	Paper feed forward / backward
ON-LINE	Data communication AS - printer

Inserting the paper:
(See Chapter 4 of the original Operating Instructions of the SICOMP DR 210-N/DR 211-N printer.)

Tear-off function: for fan-fold paper
(See Chapter 7.2 of the original Operating Instructions of the SICOMP DR 210-N/DR 211-N printer.)

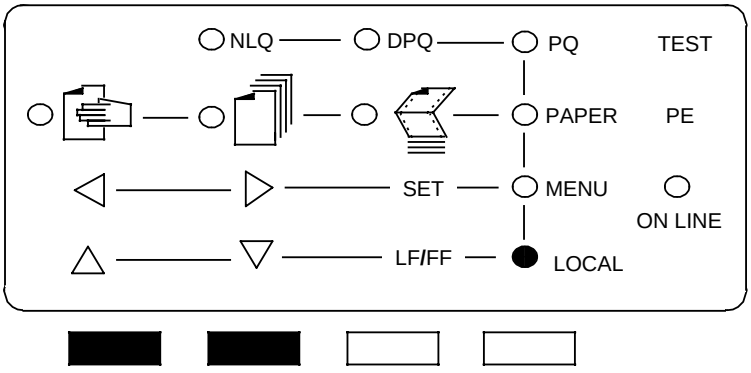


Fig. 4.55 Tear-off function

Bring paper into tear-off position. Press both marked keys simultaneously.

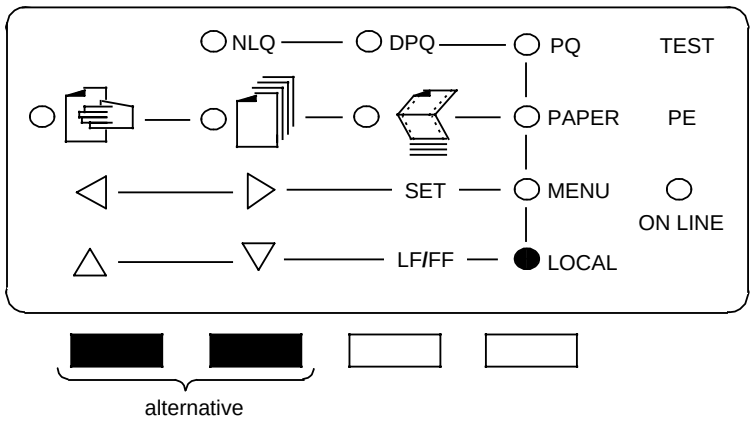


Fig. 4.56 Paper perforation corection

If the tear-off edge does not match the paper perforation, the paper perforation can be corrected by ±1 cm using the marked keys.

The tear-off function can be called both in ON LINE mode and in LOCAL mode.

This is followed by:

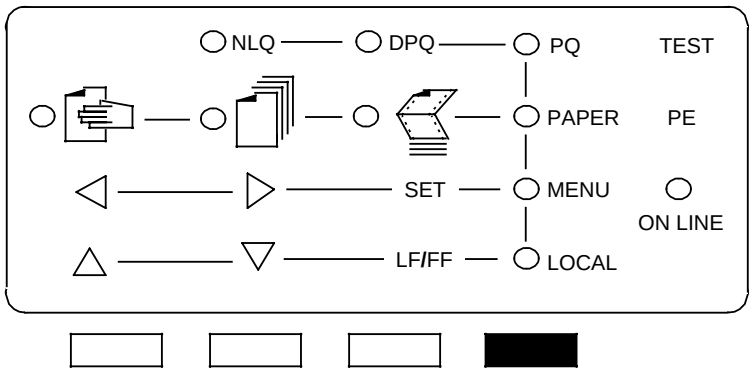


Fig. 4.57 ON LINE mode

This key serves to set the printer ON LINE.
The printer is now ready (moves to the first printing line).

4.7.9.4 DR 215-N/DR 216-N/DR 235-N and DR 236-N Printers (serial)

The DR 215-N, DR 216-N, DR 235-N and DR 236-N needle printers are used to output

- process messages,
- I&C error messages,
- operator input messages(e.g. limit modifications)
- or general logs during operation
- as well as feedback documentation of configuring data.

That is why they are used in the AS 235 automation system as event recorders and logging printers.

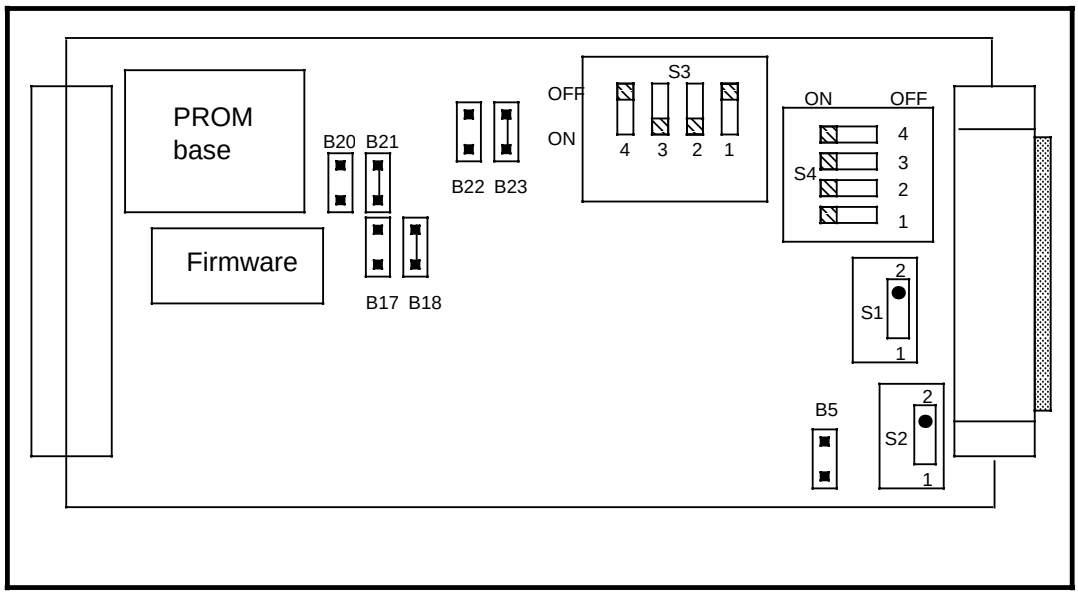
iThe DR 215-N and DR 216-N printers are equipped with a 9-needle printing mechanism, the DR 235-N and DR 236-N printers with a 24-needle printing mechanism. Due to the low level of less than 53 dB(A) they are also suitable for control rooms. Several carbon copies can be made (see Table 4.4).

Printer	DR 215-N	DR 216-N	DR 235-N	DR 236-N
Printing mechanism	9 needles	9 needles	24 needles	24 needles
Char. position/line	80	136	80	136
Carbon copies	6	6	5	5

Table 4.4 Printer design

Every printer must be equipped with an interface module for V.24/20-mA loop current when used with an AS 235 automation system. The interface module list has standard and ECMA emulation; for operation with AS 235 select the ECMA emulation.
To connect to the AS use the connecting cable 6XV2 167-8A.. .

Carry out the following jumper and switch settings on the interface module:



Jumper	Function
B5 open *)	no connection between GND and chassis
B17 open **/** B18 zu *)	2 MB PROM (firmware) DR 215-N/216-N
B17 closed **/** B18 open	4 MB PROM (firmware) DR 235-N/236-N
B20 open **/** B21 closed *) B22 open **/** B 23 closed *)	PROM base not equipped or with an additional 2 MB PROM

Switch	Function
S1 in position 2	T-loop active
S2 in position 2	R-loop active
S3.1 in position ON S3.2 in position OFF	
S3.3 in position OFF S3.4 in position ON	connects READY with pin 2
S4.1 in position OFF S4.2 in position OFF	no signal at pin 25
S4.3 in position OFF	
S4.4 in position OFF	with TTY 20 mA operation

*) Factory default setting

Fig. 4.58 Jumper and switch settings of the serial interface module

Note:

The jumpers and switches not mentionned are preset at the factory and must not be modified.

Software settings (see also the Instructions sipplied with the printer) have to be matched to the automation system. Use the setup menu according to Table 4.5.

Setup menu	AS
Font	Draft
CPI	10 CPI
LPI	6 LPI
Skip	0,0 Zoll
Emulation	ECMA 9011
Bidir	On
ZG-Tab	8859-1
CharSet	Extended
Land	GERMAN
0-Durch	Off
Auto-CR	On
Auto-LF	Off
Auto-Tear	View = 3s
Width	8 inch
Forml	12.0 inch
FarbOpt	Does not exist
PapOpt	None
Phys.Aj	0/72'
Buffer	64 kB
Interf.	Serial
Serial	
Baud	300/600
Format	7Bit Even 1Stop
Log	XON/XOFF
DevAttr	On
API	Off

Table 4.5 Printer setup menu for the automation system

Caution

Wrong settings/combinations could destroy components or cause erroneous functions (e.g. sporadic transfer errors) hervorrufen!

4.7.9.5 Printer Converter

The printer converter converts the the printer interfaces of the automation system (20-mA current loop/V.24) in a standard Centronics interface. That permits to connect standard printer with Centronics interface and IBM Proprinter font 2.
A parity error on the serial interface is declared as "Smudge" (B"H) on the printer.

A new installation with event recorder/logging printer requires the connecting cable 6DS8316-8xx (see Fig. 4.60) to connect the printer converter.
An adapter connecting cable is required between AS connecting cable (previous) and printer converter when an event recorder/logging printer with Centronics interface is retrofitted to an AS system.
Use a standard Centronics connecting cable to link the printer converter and the printer (paralle interface).

Apart from the printers DR 215-N, DR 216-N, DR 235-N, DR 236-N, DR 240-I and DR 241-I (each with Centronics interface) comparable printers from other competitors are also suitable if they fulfil the following conditions:

- Centronics interface with IBM Proprinter font 2
- Interference suppression Class B according to VDE 0871
- Print capacity: 150characters/s
- Print buffer at least 4 KByte
- Paper end recognition
- Continuous paper, printer setting at least 66 lines**/**page

An AUTO VIEW function is recommended for a better reading of the last printed lines.

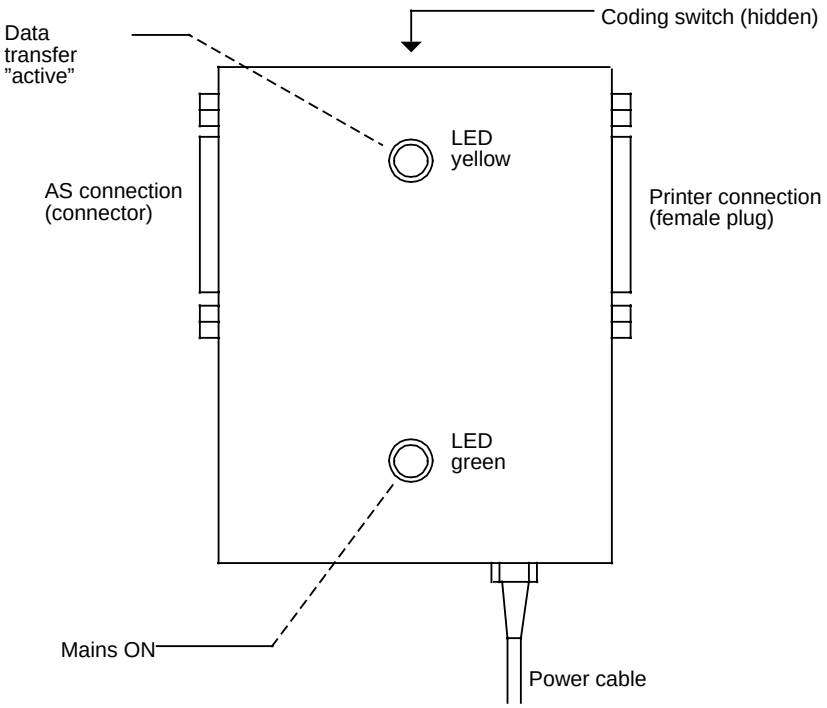
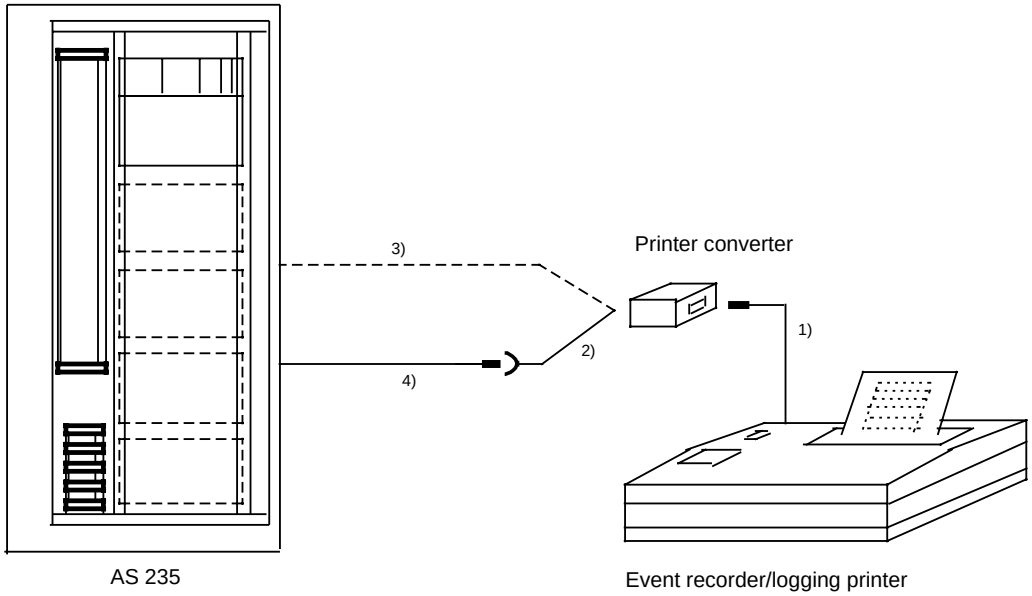


Fig. 4.59 Printer converter (top view)

- Connection

Link the printer converter to the mains (AC 230 V, 50/60 Hz) with a power cable (Fig. 4.60). A green LED indicates the readiness for service. The transfer of the operating condition settings (coding switches, see Fig. 4.62 occurs simultaneously. The links to the AS or to the printer are shown in Fig. 4.60. A yellow blinking LED indicates the data transfer.



1) Connecting cable to link the event recorder/logging printer to the printer converter;
Standard Centronics connecting cable (parallel)

2) Adapter connecting cable 6DS8317-8AC between the system specific connecting cable (4)) and the printer converter

3) System specific connecting cable 6DS8316-8xx between AS 235 and printer converter for the printer connection of new systems

4) System pecific connecting cables for the printer connection of already delivered systems
AS 220 S/K/H, AS 230/230 K: 6DS8126-8xx
AS 235/235 K/H: 6XV2167-8Axxx or 6XV2155-8Axxx

Fig. 4.60 Connection of a printer converter

- Coding switch meaning

The coding switches are disposed on the printer converter and appear after removing a cover. They allow setting the printer converter operating conditions.

Meaning	Switch S1									
	1	2	3	4	5	6	7	8	9	10
TTY (20 mA)	●									
V.24	○									
BUSY		●								
XON/XOFF		○								
BUSY no current			●							
BUSY current			○							
BUSY at pin 25				●						
BUSY at pin 2				○						
Data width 8 bits					●					
Data width 7 bits					○					
No parity						○	○			
Odd parity						○	●			
Even parity						●	○			
300 bauds								○	○	●
600 bauds								○	●	○
1200 bauds								○	●	●
2400 bauds								●	○	○
4800 bauds								●	○	●
9600 bauds								●	●	○
19200 bauds								●	●	●
Maintenance This selection must **not be set.** werIt is only used for test and maintenance.						●	●	○	○	○

● ON
○ OFF
▭ Required setting (state upon delivery)

Fig. 4.61 Setting coding switch S1

Meaning	Switch S2							
	1	2	3	4	5	6	7	8
Receive RX active	●	●	○	○				
Receive RX passive, without protective resistor	○	○	●	○				
Receive RX passive, with protective resistor	○	○	○	●				
Transmit TX active					●	●	○	○
Transmit TX passiv, ohne Schutzwiderstand					○	○	●	○
Transmit TX passive, with protective resistor					○	○	○	●

● ON
○ OFF
Required setting (state upon delivery)

Fig. 4.62 Setting coding switch S2

- Coding switch setting for AS 235

When the printer converter is delivered the coding switches are already set for use with an AS 235.

Caution:

Only modify the coding switch position in de-energized state.

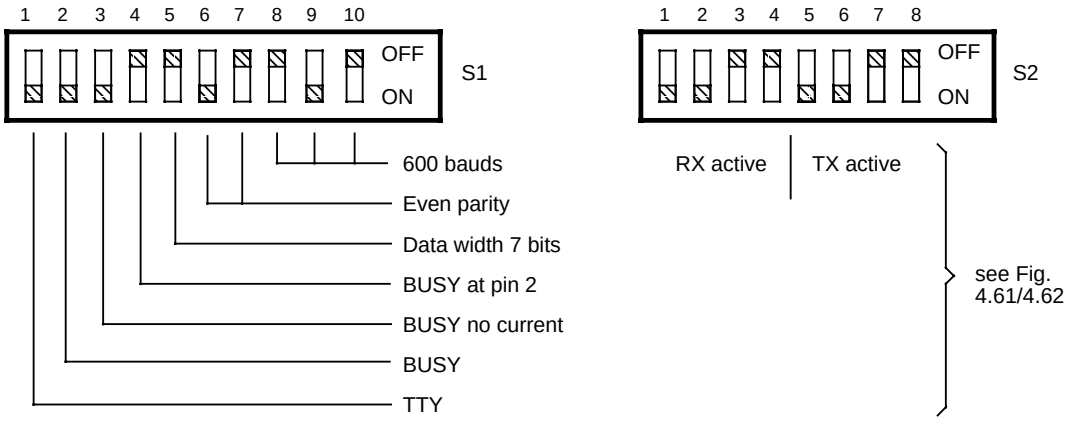
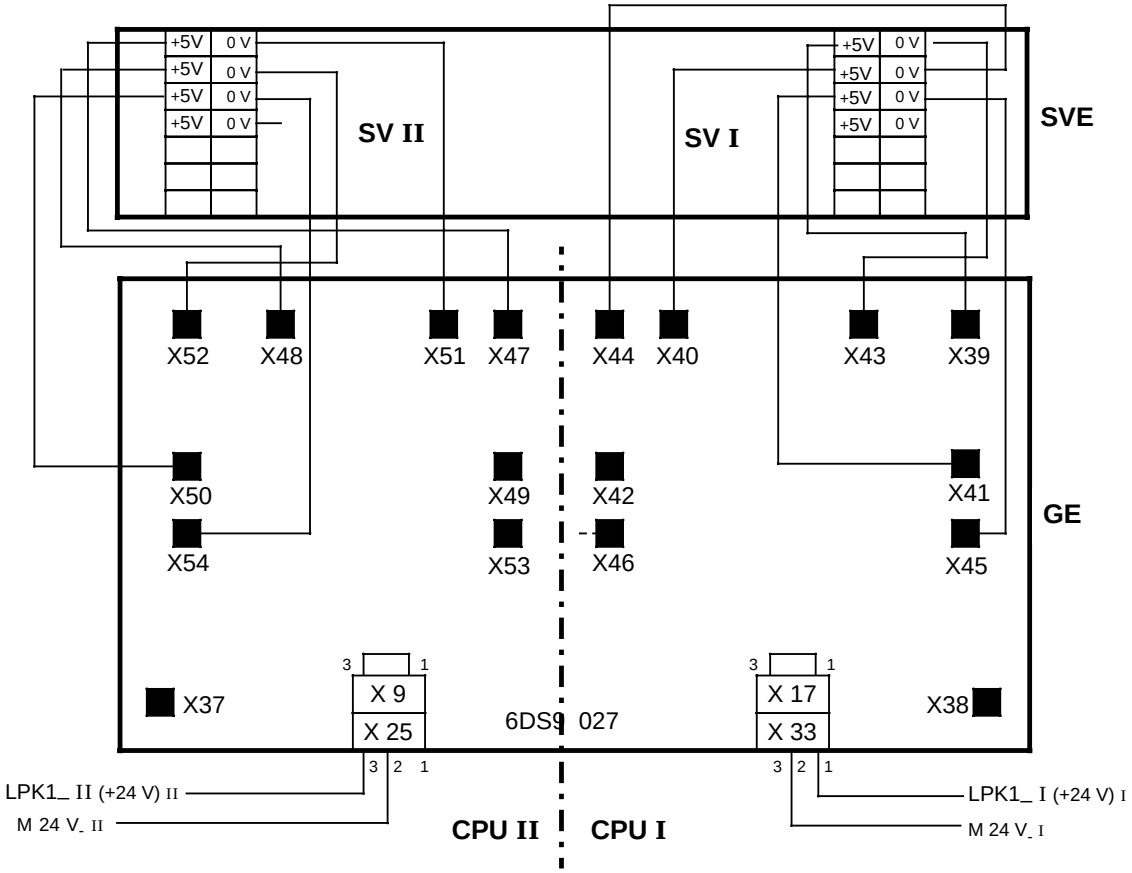


Fig. 4.63 Setting the coding switches with AS 235

4.8 Basic Unit and I/O Bus Cabling

4.8.1 Central Unit Power Supply Connections



Subrack, rear view

LPK1 I/II
LPK2 I/II
M24V I/II
SVE Power supply assembly
SV Power supply unit
GE Basic unit

Fig. 4.64 Power supply lines between SV and GE

4.8.2 Ribbon Cables between Basic Unit and Extension Unit

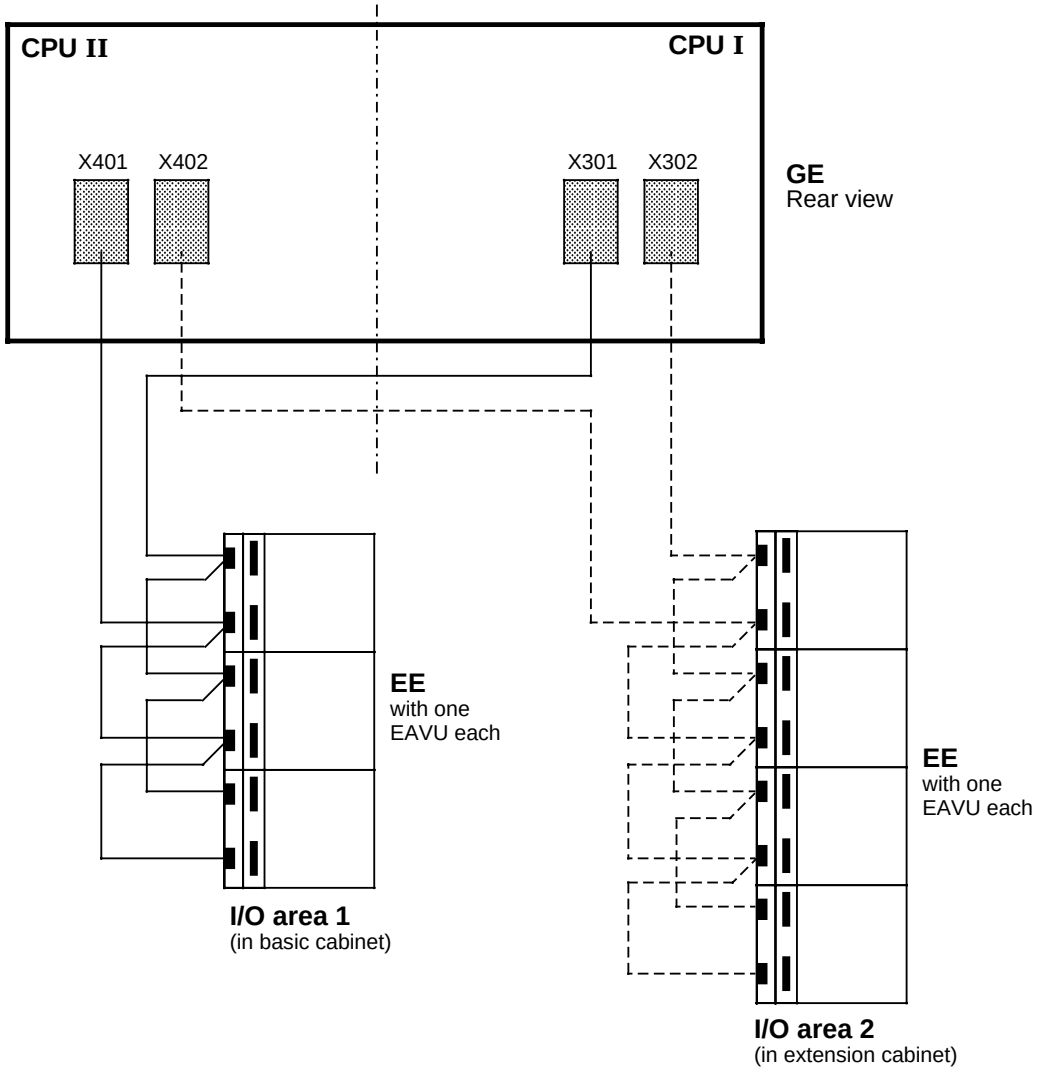


Fig. 4.65 Connecting diagram of the I/O bus ribbon cables

5 Commissioning

Check the cabinet installation before commissioning.

– Are all components available that are necessary for operation?
(Visual check of the subracks)

– Have both central processing units the same configuration?
(The configuration planned for operation)

– Has the power supply unit been connected?
(Cabinet power supply unit operational?)

- Has the N-AS**/**N8-H local bus interface been installed?
(Correct setting of the S11/S12 switches?)

- Are the operator input units connected and operational?
(Check connections)

- Have the EAVUs been installed?
(Has the connection of the X2 backplane connector been established at the rear of the extension units in accordance with the I/O configuration?)

• Initial system loading

The two central processing units can either be booted from one mini floppy disk unit (MDE) in succession or from two MDEs in parallel.

The system software must be loaded separately into each CPU.
Initial state:

– MDE connected, system disk not inserted.
– Backup battery on RAM module not inserted.
– Switch on RAM module in position "RUN" or "BOOT".

Putting system into operation:

1. Switch on the two CPUs by their protective switches F1 and F2.

   CPU assumes STOP mode (red LED ON).
   The red LED on the RAM module goes ON.
   The red fault LED on the SB is ON.

2. Insert system disk into MDE and press ZRS pushbutton on CPU module.

   Red LEDs on CPU and RAM modules go OFF.
   Green LED (BOOT) on RAM module goes ON.
   The system software is booted from the MDE. The following message texts are displayed on the monitor **1)**:

   URLADER: ANLAUF VERS. 01 . . . . . Pos. 1
   (Initial loader: startup of Vers. 01)
   SYSTEMDISKETTE IN LAUFWERK EINLEGEN: OK . . . . . Pos. 2
   (Insert system diskette into drive: OK)
   PRÜFUNG SYSTEMDISKETTE: OK . . . . . Pos. 3
   (Checking system diskette: OK)
   SYSTEM-DISKETTE: AS 235 H VERS. XXX SYSTEMSOFTWARE . . . . Pos. 4
   (System diskette: AS 235 H, version XXX system software)
   SYSTEM-DISKETTE WIRD GELADEN: . . . . . Pos. 5
   (System diskette is being loaded)

1) Initial loading is only displayed for CPU II. CPU II should therefore be loaded first if only one MDE is available.

This display disappears after approximately 5 minutes and system message S300 appears. Initial loading for the respective CPU is terminated.

The first CPU to have been loaded automatically transitions from failure mode to master mode; the second CPU remains in failure mode until the system software has been loaded, then assumes passive mode. This means that the two CPUs are still in asynchronous operation.

Synchronization may now be started by pressing the backup pushbutton on the comparator coupler module (VKB) for approximately one second.

The transition into backup mode is indicated by the standby LED which lights up in addition to the passive LED. Synchronization may also be controlled via the keyboard (cf. the AS 235 H Description C79000-T8076-C416 in the Manual C79000-G8076-C416).

Pressing the backup pushbutton remains without effect for approximately 15 seconds after the CPU has been started.

The synchronization module in the master CPU defines the "meeting point" of the two synchronization modules and initiates a hardware stop of the second CPU. The passive CPU then transitions into backup mode. Both synchronization modules and the comparator coupler module (which had no function in asynchronous operation) now initiate synchronous operation of the two CPUs.

The comparator coupler module (VKB) routes all read data from the master CPU via the bus to the second CPU. The synchronous operation causes all register contents to be verified.

The second CPU cannot assume mastership during updating.

Passive and standby LED are both on during loading. Both CPUs are operating synchronously when the passive LED is extinguished.

Synchronization is only possible in master**/**passive or passive**/**master mode if both CPUs have the same module configuration, the same memory configuration, and the same system software level (cf. the AS 235 H Description C79000-T8076-C416 in the Manual C79000-G8076-C416).

- Activating and de-activating the system or the CPU in battery-backed operation

The standby CPU assumes mastership after a maximum of 50 ms after the master CPU has been switched off. The N-AS**/**N8-H is re-parametrized when mastership is changed.
De-activating the backup CPU does not affect the master CPU.
CPU I always remains master if both CPUs are switched on at the same time (t < 2 s).
The first CPU to have been switched on becomes master if the time difference is more than 2 seconds.

- Possible error messages

- SYS-RAM DEFEKT (Pos. 2):	- Defective memory module
- FLOPPY-ANSCHALTUNG DEFEKT (Pos. 2):	- Mini floppy disk interface module is defective or incorrect jumper setting on mini floppy disk interface
- LAUFWERK NICHT BEREIT (Pos. 2): . . .	- Mini floppy disk unit is defective or has not been connected
- DATEI 1 DEFEKT (Pos. 3):	- Parts of the system floppy disk are defective [1)]
- BACKUP-DATEI DEFEKT (Pos. 3):	- Parts of the system floppy disk are defective [1)]
- DISKETTE DEFEKT (Pos. 3):	- System floppy disk is completely defective or no system floppy disk is in drive.
- NICHT LESBAR, ERNEUTEN VERSUCH STARTEN (Pos. 3):	- No AS floppy disk is in drive or system Floppy disk is completely defective.
- LESEFEHLER (Pos. 4):	- System floppy disk label is defective or switch on MDA is in special mode position.
- KEINE SYSTEMDISKETTE (Pos. 4):	- Inserted floppy disk is a user floppy disk, not a system floppy disk.
- PRÜFSUMME FALSCH (Pos. 5):	- Transmission error from MDA to RAM or system floppy disk is defective.
- UMSCHALTUNG AUF BACKUP-DATEI .	- Read error in master file.
- BEIDE DATEIEN NICHT LESBAR. . . . . NEUE SYSTEMDISKETTE ERFORDERLICH (Pos. 5):	- Defect on floppy disk which has not been detected during previous checks.
- SCHREIBFEHLER SYS-RAM (Pos. 5): . .	- Fault on memory module which has not been detected during memory test.

If neither of the above messages appears at position 1, the initial program loader cannot be activated at all (i.e. a fatal hardware defect has occurred).

[1)] A new system disk should be obtained in these cases so as not to lose the advantage of file redundancy.

Notes

6 Maintenance

6.1 Qualified Personnel

Persons who are **not qualified** should not be allowed to handle the equipment/system. Non-compliance with the warnings contained in this manual or appearing on the equipment itself can result in severe personal injury or damage to property.

Only **qualified personnel** should be allowed to work on this equipment**/**system.

Qualified personnel as referred to in the safety guidelines in this manual as well as on the product itself are defined as follows:

- System planning and design engineers who are familiar with the safety concepts of automation equipment;
- Operating personnel who have been trained to work with automation equipment and are conversant with the contents of the manual in as far as it is connected with the actual operation of the plant;
- Commissioning and service personnel who are trained to repair such automation equipment and who are authorized to energize, deenergize, clear, ground and tag circuits, equipment and systems in accordance with established safety practices.

We refer again to the ”Safety-related Guidelines for the User”. You find these Guidelines in this Manual before Section 1.

6.2 Fault Elimination

The service personnel is guided by fault messages from the system or system components to the cause of the fault.

The AS 235 H Description (C79000-T8076-C484 in the Manual C79000-G8076-C416) contains explanations regarding fault indications. The defect is shown in the fault screen display, provided that it has been located by the software.
In any other case, interpretation of the values displayed in the same screen display using the VKB Operating Instructions (C79000-T8076-C345) helps isolating the fault.

The screen display "EAVU registers" and the EAVU Description (C79000-T8076-C343) may be used for further analysis if the fault has occurred during I/O access.

A fault must be eliminated by modifications if it has been caused by configuration errors.

The following procedure is recommended if a fault is due to a hardware failure:

Replace the printed circuit boards one by one until the faulty module has been located.

Return the defective module and a fault description (using the form provided for products to be returned) to the factory for repair or ask ANL A 434 ED, Erlangen for a replacement.

Caution

Switch off the module supply voltage (switch off the power supply unit or remove the module fuse, for example) before removing or inserting a module.
Switch off the system power supply unit before performing any wiring (modification or repair work) on the backplane or in the SAE area.
Verify that the system is in an orderly state (e.g. no short-circuits by bent wrap pins or wire bits in the subrack backplane) before the voltage is switched on.

Note

A buffer module may be removed or installed during operation. Since the high charging current may cause a breakdown of the power supply unit, the capacitors on the replacement module must be charged via a 1-K ohm resistor up to approximately DC 24 V before the module is installed. Ensure that the polarity is correct during charging.

6.3 Backup Battery

A lithium battery (AA type) on the memory module 6DS1 837-8.. or 6DS1 844-8.. is used for buffering the memory contents.

The battery is supplied as a separate item together with the module, and is not installed. It may be installed or replaced during operation.

The battery voltage is monitored every 60 s. The fault LED lights up and a system message (S357) is issued if the voltage drops below 2.8 V.

The message only disappears after the battery has been replaced. In operation this I&C message means that the battery is discharged. In this case replace the battery.

This system message only indicates low battery voltage during running operation. Since it cannot be guaranteed that the memory contents have been maintained when the battery voltage drops below the tolerance value during buffer mode.

Battery failure mode (BAU) is assumed when AS operation is continued after voltage recovery.

Logic interpretation of the BAU state is only performed during system start-up. The system reacts as follows:

– The system requests a new initial loading during start-up and clears the user memory if the BAU signal is active (logic "0"), even if the switch on the memory module is in RUN position. The system issues S300.

– The system starts without request for a new initial loading if the BAU signal is logic "1" (the battery has not failed in the meantime). A failure in between (e.g. by battery replacement) cannot be detected by the module 6DS1 837-8..

  However the module 6DS1 844-8.. recognizes a battery change in backup mode and reacts automatically with a BOOT requirement at the next system startup.

Caution

When the memory module has been removed during the backup mode, the stored data cannot be guaranteed.

Use only replacement batteries of the same type. The batteries should be replaced at least once a year as a preventive measure.

Depending on the memory configuration, the capacity of a lithium battery lasts for:
1 MB at least 500 hours with module 6DS1 837-8..
2 MB at least 300 hours with module 6DS1 837-8..
3 MBat least 200 hours with module 6DS1 837-8..
4 MBat least 480 hours with module 6DS1 844-8..

The backup battery can be tested using a suitable voltmeter (digital voltmeter).
A new battery must have a no-load voltage of 3.6 V.

- Replacing the battery

- Memory module 6DS1 837-8..

  First remove the cover from the battery case on the front panel of the memory module. The battery may now be removed or installed.

- Memory module 6DS1 844-8..

  Pull out the battery drawer up to the stop, remove the old battery, insert the new battery with the right polarity. push the drawer till the snap position.

  The battery drawer may also be completely removed when the lateral locating springs are pressed (see following Fig. 6.1).

  Now the battery can be inserted or removed.

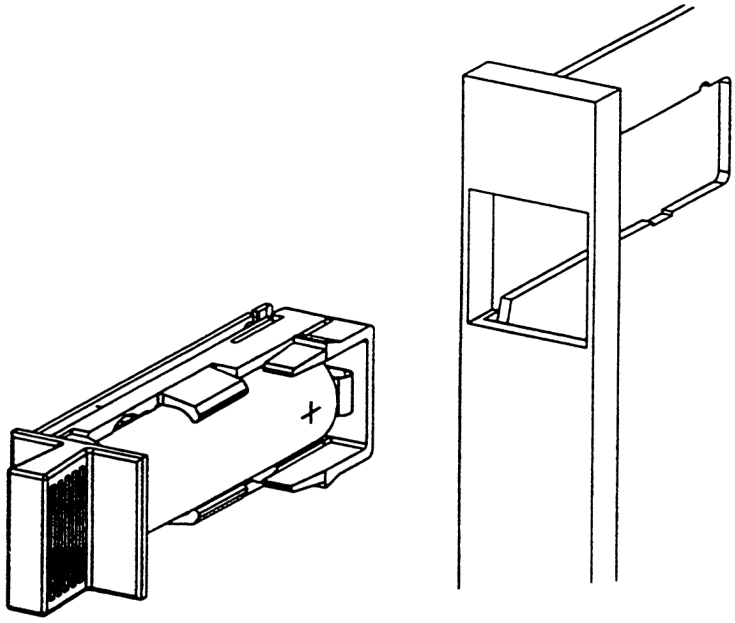


Fig. 6.1 Battery drawer of the memory module 6DS1 844-8··

Clean the surfaces in order to guarantee proper contact.

Warning

Never open a battery, it contains strongly corrosive agents. Do not throw batteries into an open fire.
Protect your environment: Do not include old or used batteries in the normal garbage. Oberserve the local regulations for discarding special and toxic waste.

Caution

Observe the polarity during installation.
6DS1 837-8..: ”POSITIVE POLE must point upwards.”
6DS1 844-8..: ”NEGATIVE POLE must point to grip side.”
Observe the ”ESD Guidelines”.
(discharge static charges before inserting)

6.4 Circuit Diagrams

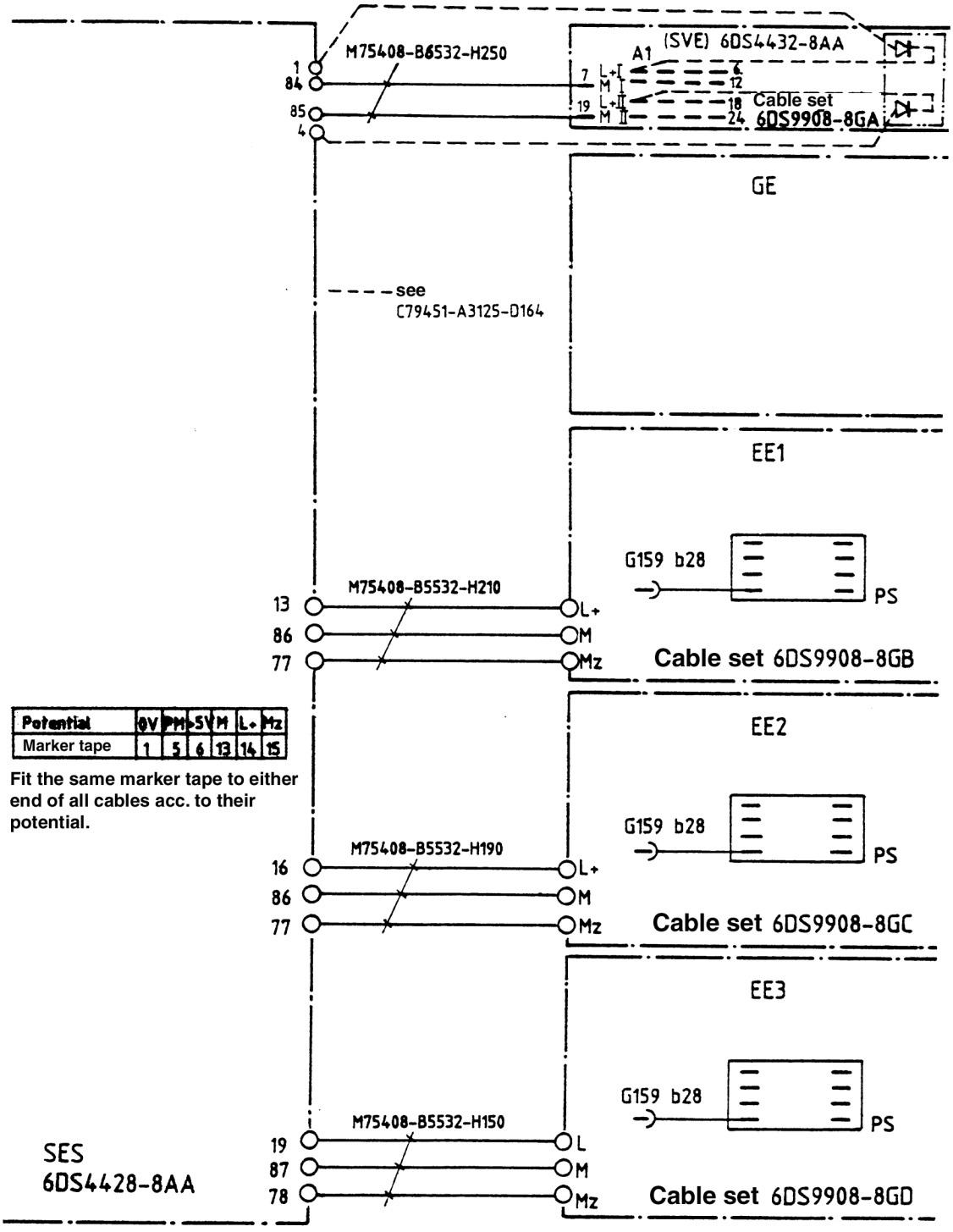


Fig. 6.2 Basic cabinet, connections L+, M, MZ

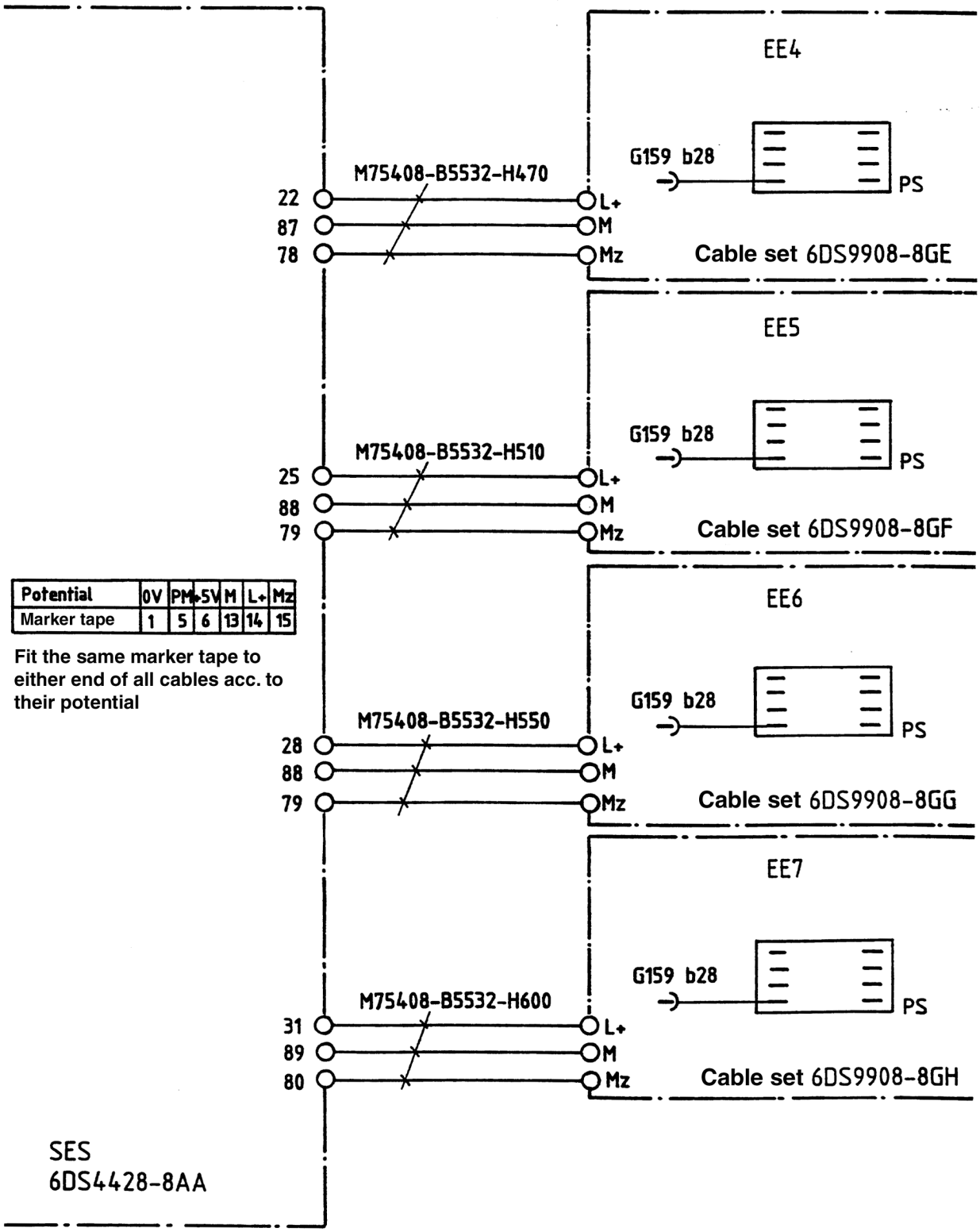


Fig. 6.3 Extension cabinet, connections L+, M, MZ

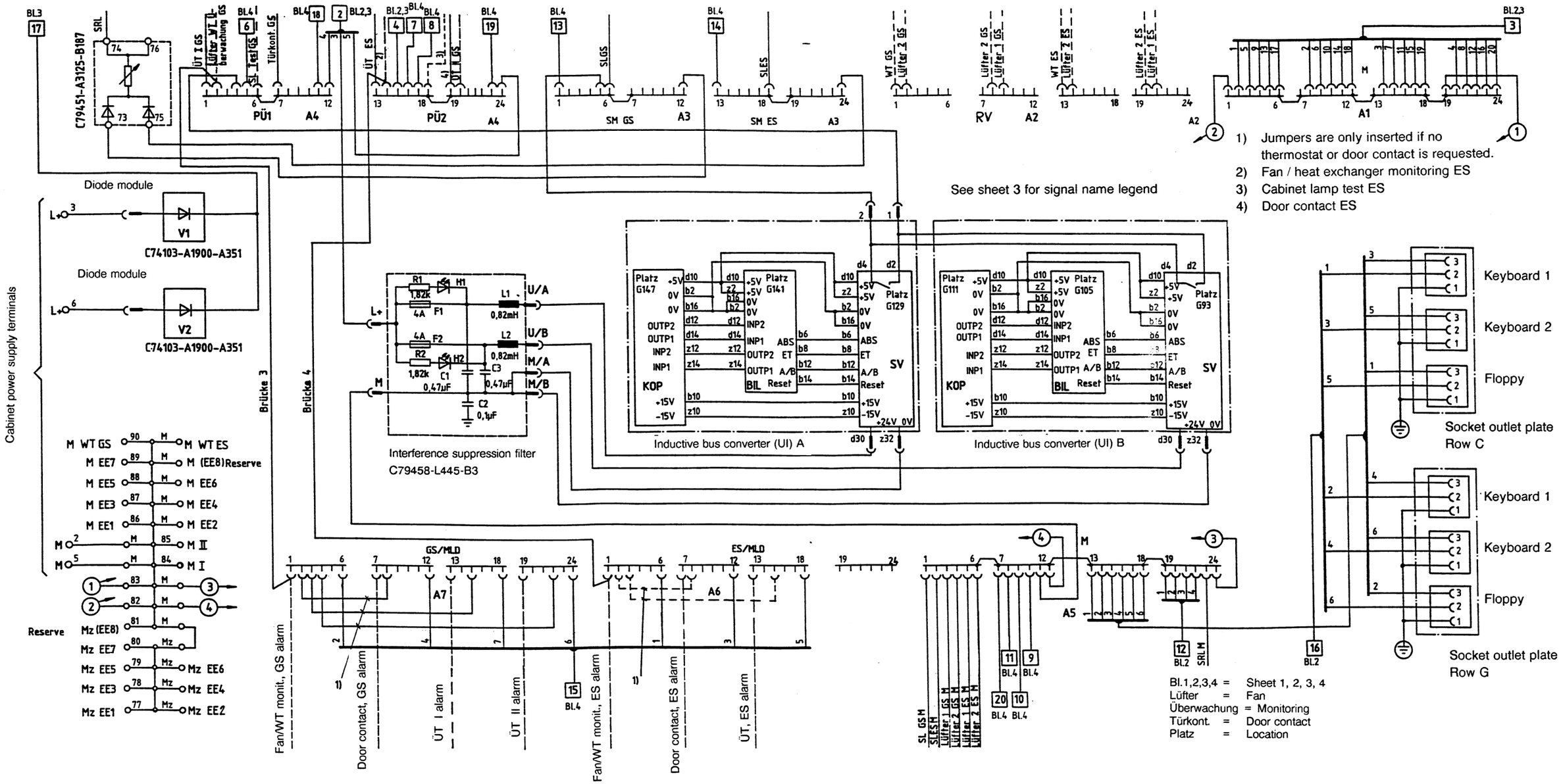


Fig. 6.4.1 AS 235 H cabinet power supply unit, sheet 1

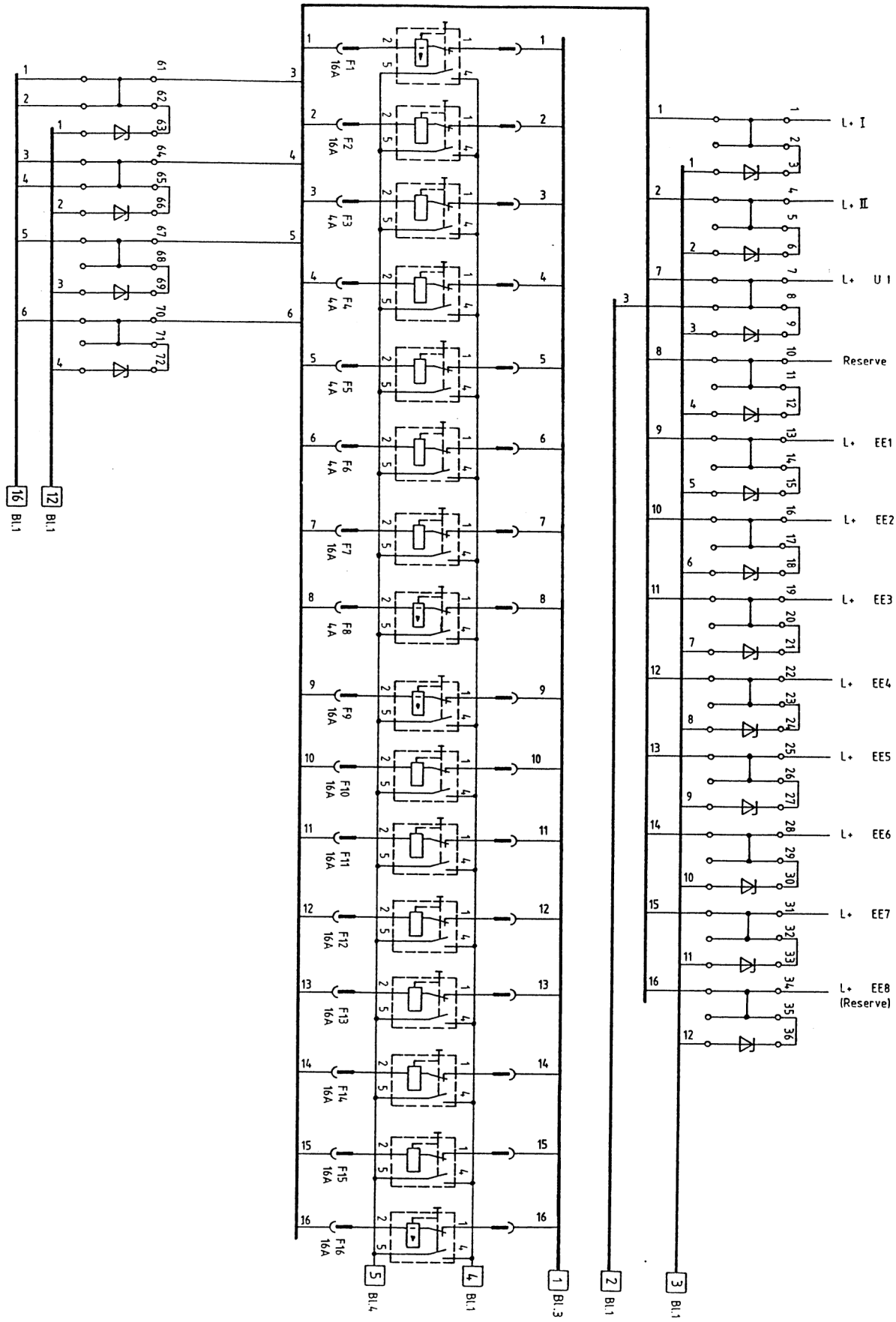


Fig. 6.4.2 AS 235 H cabinet power supply unit (SES), sheet 2

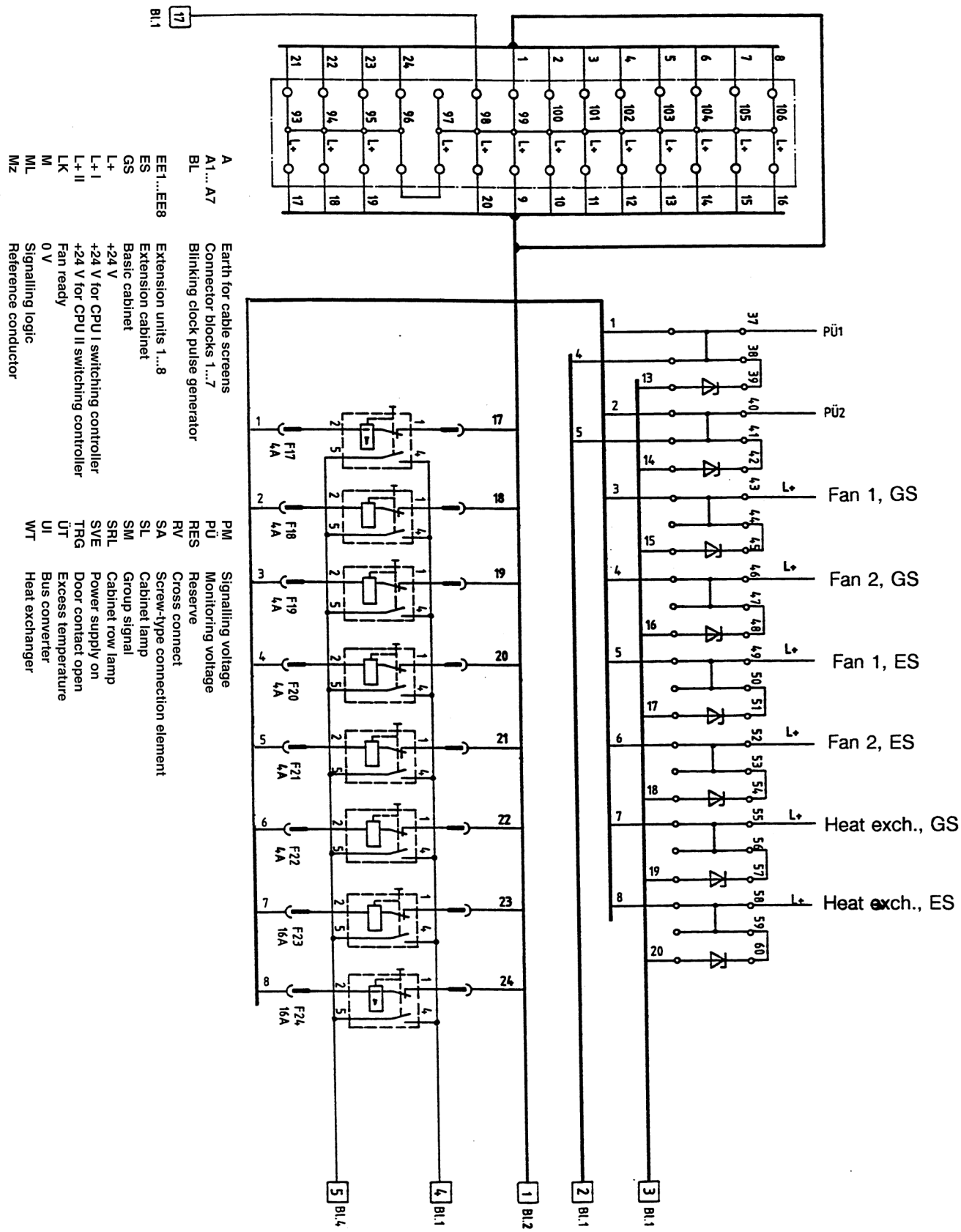


Fig. 6.4.3 AS 235 H cabinet power supply unit (SES), sheet 3

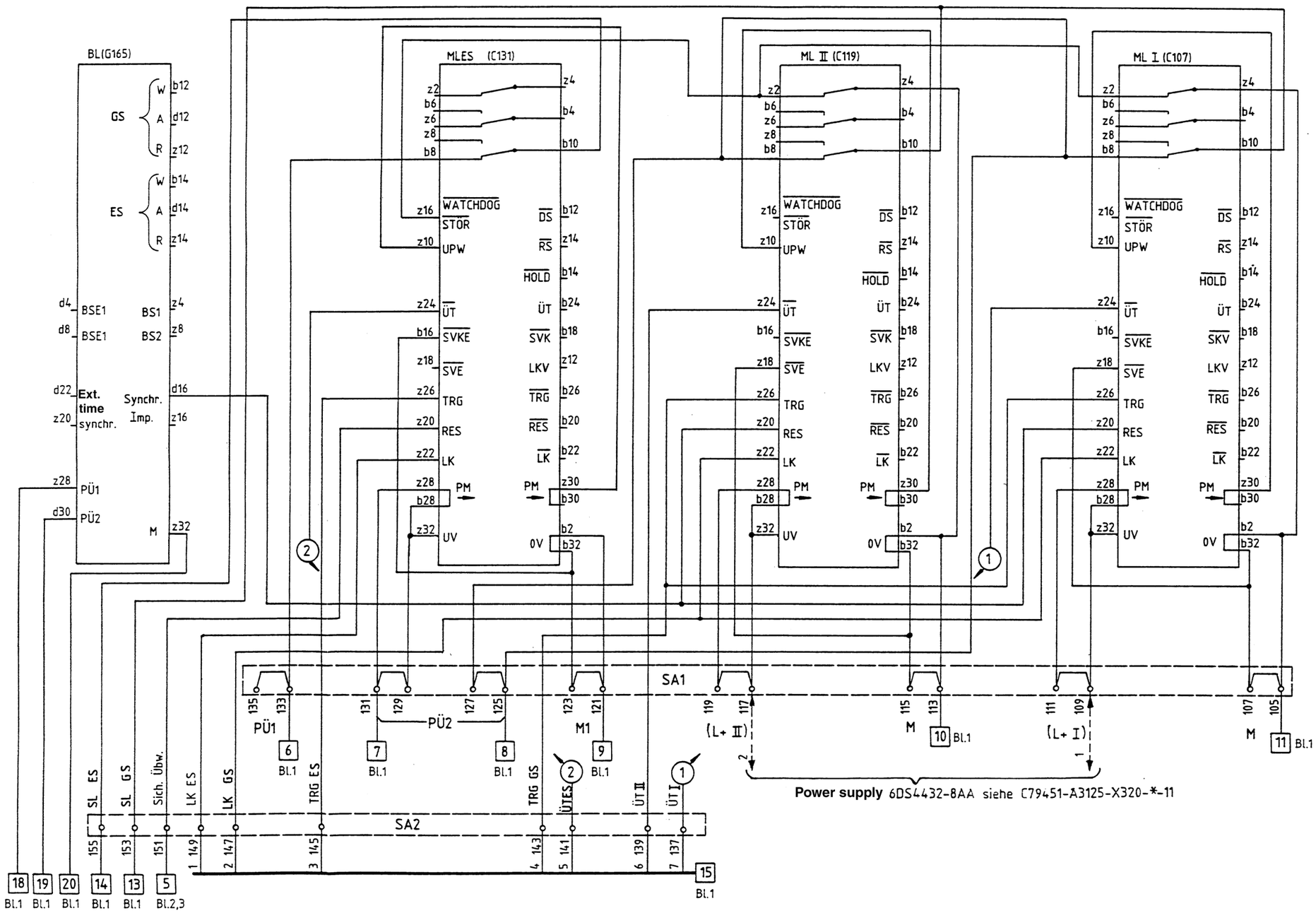


Fig. 6.3.4 AS 235 H cabinet power supply unit (SES), sheet 4

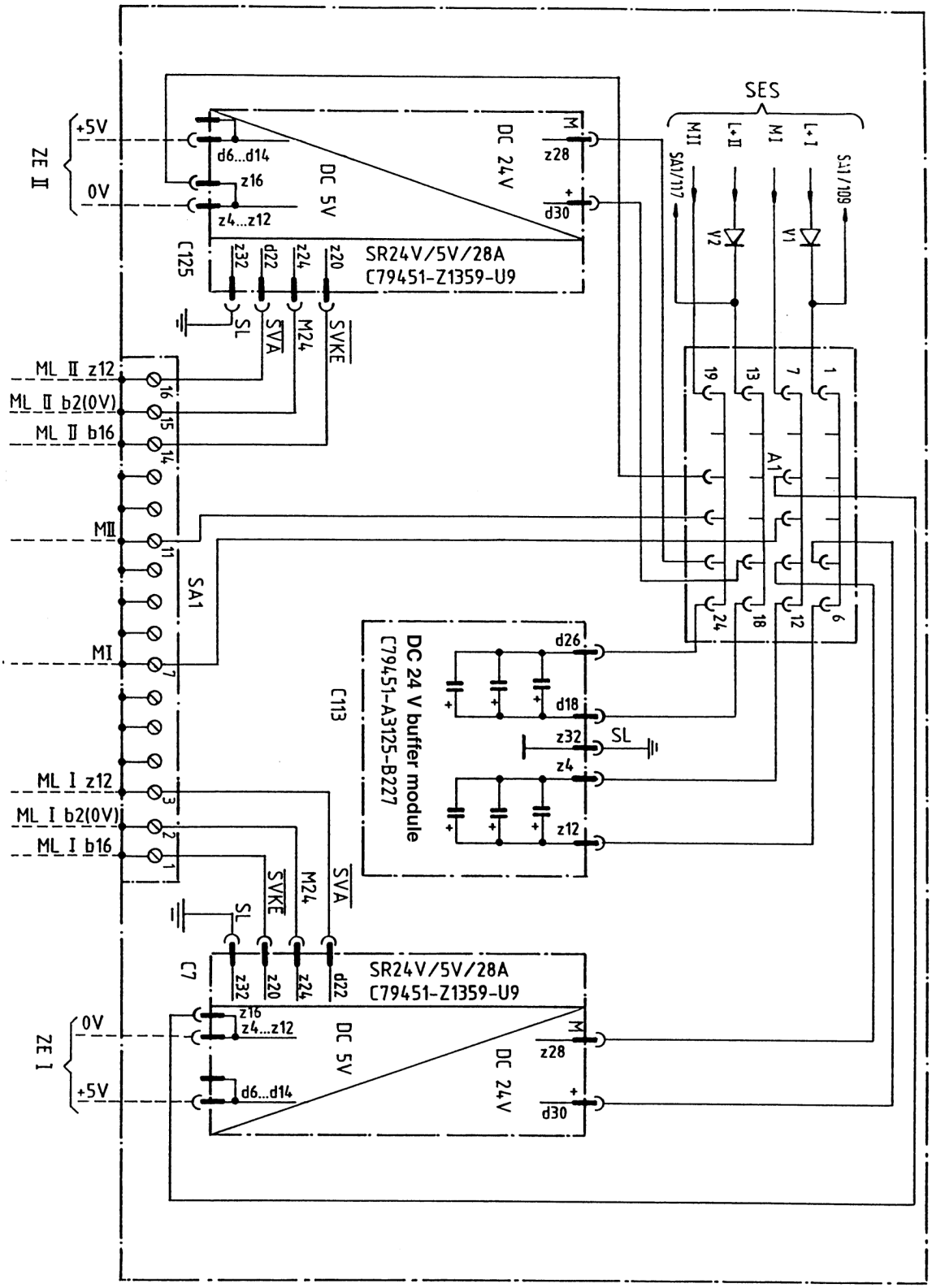


Fig. 6.5 Power supply tier (SV), DC 24 V / DC 5 V

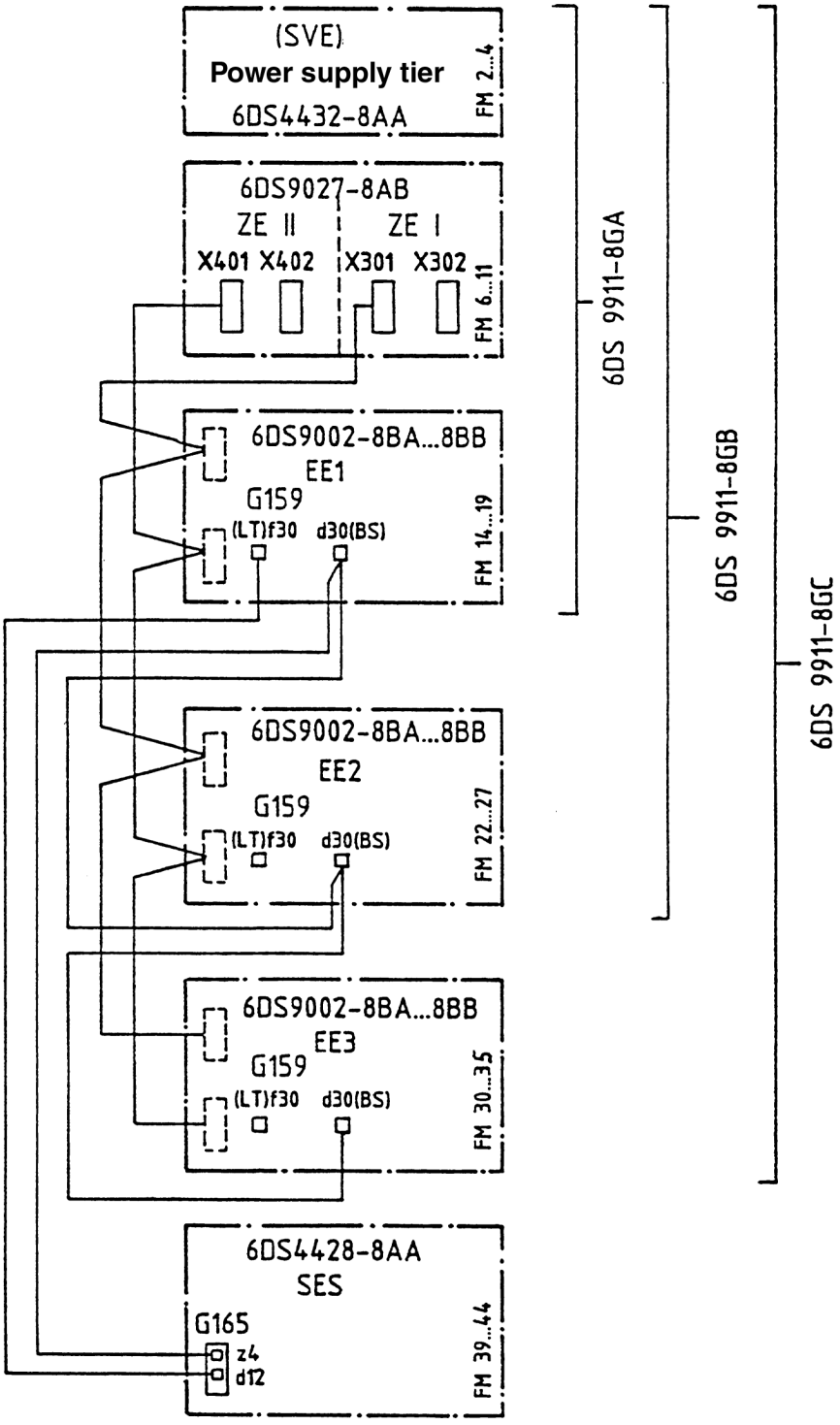


Fig. 6.6.1 I/O bus, basic cabinet

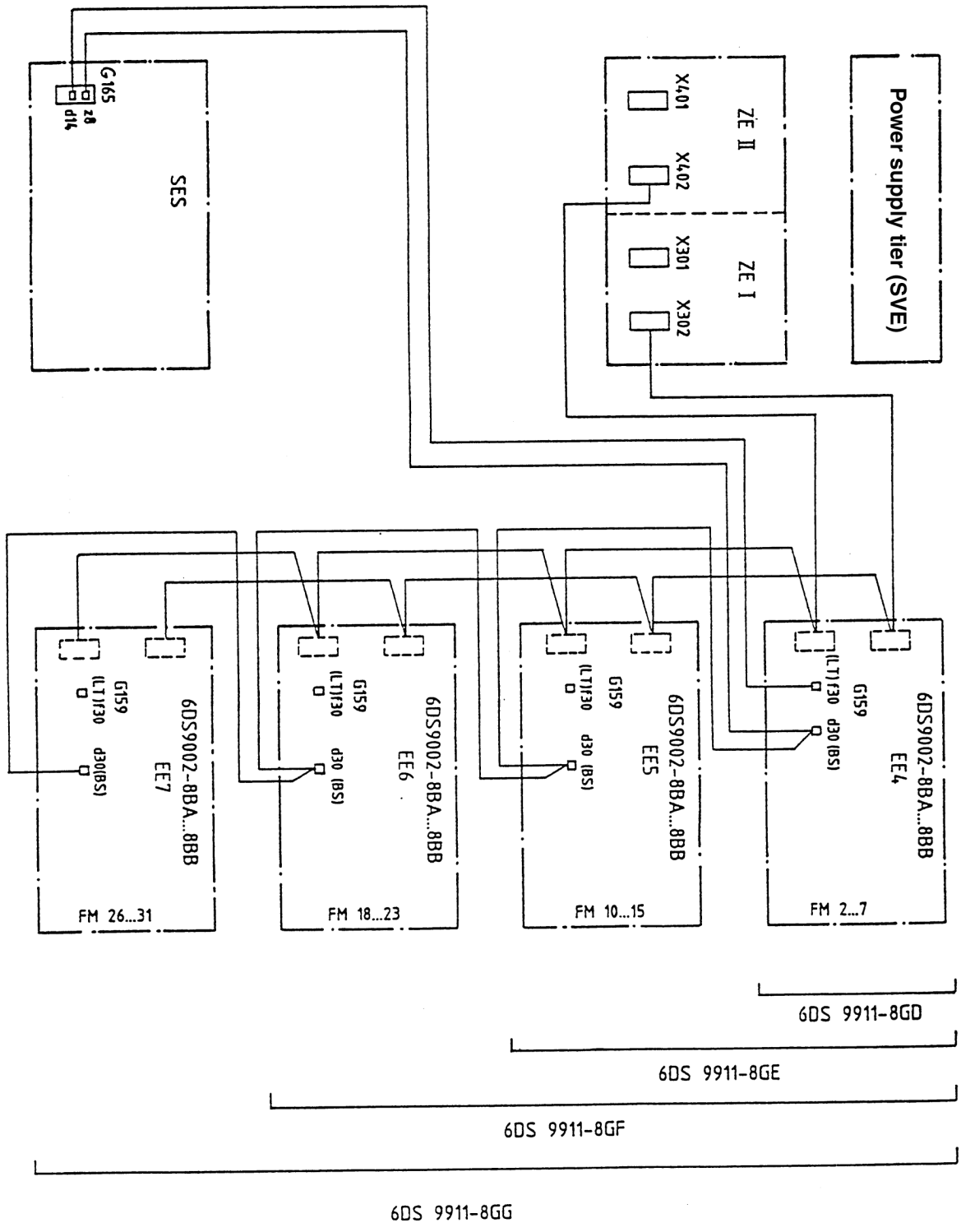
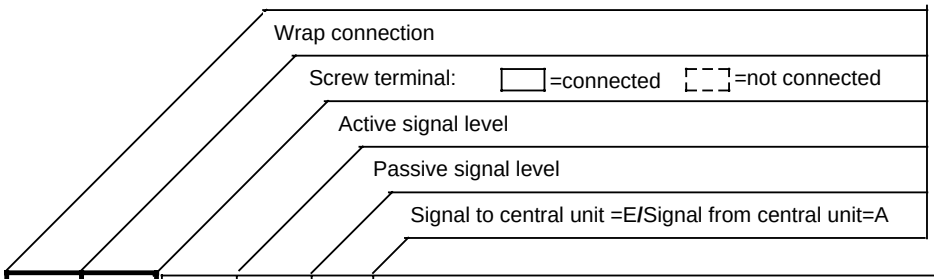
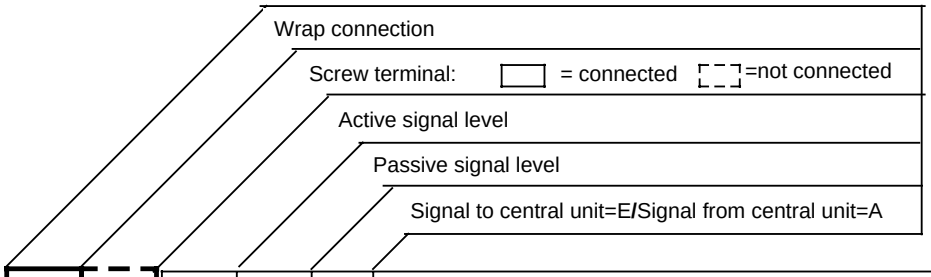


Fig. 6.6.2 I/O bus, extension cabinet



X13 / X29	1 / 2 / 3	+5 V	0 V	E	Overtemperature extension cabinet, 5-V signal	**MELD8I**
		0 V	+24 V	E	Door contact extension cabinet, 24-V signal	**TK2I**
		+5 V	0 V	E	Door contact extension cabinet, 5-V signal	**MELD7I**
X14 / X30	1 / 2	+5 V	0 V	E	Fan contact basic cabinet	**MELD2I**
				E	0-V reference potential for +5 V	**0 V**
X15 / X31	1 / 2	+5 V	0 V	E	Overtemperature basic cabinet	**MELD3I**
		+5 V	0 V	E	Door contact basic cabinet	**MELD4I**
X16 / X32	1 / 2	+24 V	0 V	A	Video relay control signal	**RGBI**
				E	M-reference potential for+24 V	**M24I**
X17 / X33	1 / 2 / 3			E	+24 V for BED.2 in CPU I	**LPK2I**
				E	M-reference potential for +24 V	**M24I**
				E	+24 V for SB and BED.1 in CPU I	**LPK1I**
X18 / X34	1 / 2 / 3	0 V	+5 V	A	Common alarm from CPU I	**WD_NI**
		+5 V	0 V	E	Time pulse	**MELD1I**
		0 V	+24 V	E	Reserve input (24 V)	**RES2I**
X19 / X35	1 / 2 / 3	0 V	+5 V	E	Central reset from power supply unit I	**ZRS_NI**
		0 V	+5 V	E	Data project signal from power supply unit I	**DS_NI**
		0 V	+5 V	E	Power failure alarm from power supply unit I	**NAU_NI**
X20 / X36	1 / 2 / 3	+5 V	0 V	E	Fan contact extension cabinet, 5-V signal	**MELD6I**
		0 V	+24 V	E	Overtemperature extension cabinet, 24-V signal	**UET2I**
		0 V	+24 V	E	Fan contact extension cabinet, 24-V signal	**LKM2I**
X98 / X88	1 / 2 / 3	+5 V	0 V	E	Blown-fuse alarm	**MELD5I**
						– –
						– –

Fig. 6.7 Connections to CPU I (the same sequence as in the rack)



1 ●	1 ○	+5 V	0 V	E	Blown-fuse alarm	**MELD 5II**
2 **X99** ●	2 **X89** ○					**— —**
3 ●	3 ○					**— —**
1 ●	1 ○	+5 V	0 V	E	Fan contact extension cabinet, 5-V signal	**MELD6II**
2 **X12** ●	2 **X28** ○	0 V	+24 V	E	Overtemperature extension cabinet, 24-V signal	**UET2II**
3 ●	3 ○	0 V	+24 V	E	Fan contact extension cabinet, 24-V signal	**LKM2II**
1 ●	1 ○	0 V	+5 V	E	Central reset from power supply unit II	**ZRS_NII**
2 **X11** ●	2 **X27** ○	0 V	+5 V	A	Data project signal from power supply unit II	**DS_NII**
3 ●	3 ○	0 V	+5 V	E	Power failure alarm from power supply unit II	**NAU_NII**
1 ●	1 ○	0 V	+5 V	A	Common alarm from CPU II	**WD_NII**
2 **X10** ●	2 **X26** ○	+5 V	0 V	E	Time pulse	**MELD1II**
3 ●	3 ○	0 V	+24 V	E	Reserve input (24 V)	**RES2II**
1 ●	1 ○			E	+24 V for BED.2 in CPU II	**LPK2II**
2 **X9** ●	2 **X25** ○			E	M-reference potential for+24 V	**M24II**
3 ●	3 ○			E	+24 V for SB und BED.1 in CPU II	**LPK1II**
1 ●	1 ○	+24 V	0 V	A	Video relay control signal II	**RGBII**
X8	**X24**					
2 ●	2 ○			E	M-reference potential for +24 V	**M24II**
1 ●	1 ○	+5 V	0 V	E	Overtemperature basic cabinet	**MELD3I**
X7	**X23**					
2 ●	2 ○	+5 V	0 V	E	Door contact basic cabinet	**MELD4II**
1 ●	1 ○	+5 V	0 V	E	Fan contact basic cabinet	**MELD2II**
X6	**X22**					
2 ●	2 ○			E	0-V reference potential for+5 V	**0 V**
1 ●	1 ○	+5 V	0 V	E	Overtemperature extension cabinet 5-V signal	**MELD8II**
2 **X5** ●	2 **X21** ○	0 V	+24 V	E	Door contact extension cabinet, 24-V signal	**TK2II**
3 ●	3 ○	+5 V	0 V	E	Door contact extension cabinet, 5-V signal	**MELD7II**

Fig. 6.8 Connections to CPU II (the same sequence as in the rack)

7 Technical Data

- System configuration

- Redundant system
- Two independent terminals are possible.
- Integrated programming functions for user programs and user function blocks.
- 2 I/O areas
- I/O area 1 1 EE 1 to EE 3 in the basic cabinet and up to two ES 100 K
- I/O area 2 EE 4 to EE 6 in the extension cabinet and up to two ES 100 K
  or EE 4 to EE 7 in the extension cabinet and up to one ES 100 K
- The AS 235 H can be used as a stand-alone system or as a distributed component.

  The TELEPERM CS 275 bus system is used for communication with other automation systems.

- System functions

Function blocks for:	Open and closed-loop control, monitoring, operator input, visualization (processing and standardized representation)
Analog**/**digital processing	Arithmetic functions, timers
Binary processing and	Logic operations and open-loop control functions
STEP M control language	
Higher programming language (TML)	Creation of user function blocks, image and log blocks
Signal input/output, bus communication	Analog/binary**/**BCD input/output, including reading/writing of binary signals/analog values
Output on color monitor/printer	Image/log/alarm output on two printers possible
Data transfer	Link to other bus devices, such as AS, OS, PR
Extension unit subracks	Subracks for extension units which permit installation of certain TELEPERM ME power plant modules
Loadable system software	The software is loaded into a special write-protected system RAM
Data protection	7 code bits for variables (see AS 235 H Description C79000-T8076-C416 in the Manual AS 235 H, C79000-G8076-C416).

- Central function control via bus

Central configuring, loading, and filing of an AS 235 H system (target device) from another AS 230**/**235**/**235 H (configuring device).

Using an AS 230/235 configuring device for any AS 230/235 that is connected to the same CS 275 bus system (also via bus coupling units).

AS 235 configuring devices:	Operator terminal 1 = central position Operator terminal 2 = local position Normal process output may be continued. Process control and target device monitoring are not permitted.
Target device:	Local input possible
Loading/filing:	From STRUK device to/from drive of STRUK device

- Local function control from AS 235 H

Distributed configuring, operator control and monitoring of an AS 235 H system (target device) via local operation channel and BKA configuring from a PC (AT-compatible) using PROGRAF PC.

- Central unit

Central processor	microprogrammed 16**/**32-bit slice processor, CMOS
Processing width of CPU	2×16 bits or 1×32 bits
Execution time (average)	2 µs to 6 µs for instructions with a binary operand 5 µs to 30 µs for instructions with an analog operand
Computing accuracy	10^{-4} for single-precision analog values 10^{-9} for double-precision analog values
Priority levels	16
User-accessible priority levels	5
Time required for changing a program level	
after an interrupt	Approx.. 19.5 µs
Time generation (smallest unit)	4 ms
Fixed basic cycles	125 ms or 1 s
Registers	16 processing levels with 24 registers + 32 arithmetic registers
• Memory	Stat. CMOS-RAM
Interface to central processor	16-bit data bus
Addressable units	Byte, word (1 byte = 8 bits, 1 word = 16 bits
Data protection	Parity, byte-by-byte

Main memory (user-RAM)	
6DS1 837-8··:	1536 K words (16 bits each)
6DS1 844-8··:	2000 K words (16 bits each)
System memory	
6DS1 837-8··:	256 K (16 bits each), write-protection
6DS1 844-8··:	512 K (16 bits each), write-protection
Data buffer	Lithium battery (Type AA)
Memory buffer time	
with 6DS1 837-8AA/-8DA	At least 500 h
with 6DS1 837-8BA/-8EA	At least 300 h
with 6DS1 837-8CA/-8FA	At least 520 h
with 6DS1 844-8··	At least 500 h

Battery must be replaced once a year.

Data protection, hardware monitoring	RAM parity check and watchdog function, battery monitoring

- Filing/loading the user memory contents

80-track HD floppy disks with 1 MB net capacity in connection with a 6DS3 900-8AD mini floppy disk unit (from version 4 onwards)

Loading time	Approx. 2 min per 1 MB
Filing time	Approx. 8 min per 1 MB
Formatting	Without operator terminal inhibition

- I/O devices

Two independent operator inputs units

Number of operator input units that may be used simultaneously	2
Operator input unit	1 monitor, 1 process communication keyboard, 1 configuring keyboard
Monitor types	RGB color monitor, D series monitor
Representation	Color, 32 lines with 64 characters each
Alarm line	1
Working area	28 lines/64 characters
Input line	1 line for input via configuring or process communication keyboard
Image frequency	50 Hz (non-interlaced)
Number of alphanumeric characters	64; 7-bit code to DIN 66003 Table 1 or ISO 646 or CCITT-V3, international alphabet No. 5
Symbols, icons	256, according to standard symbol coding set
Blinking frequency on monitor	2 Hz

Configuring unit	Configuring keyboard, mini floppy disk unit, connecting cables
Logging printer	80 characters/line or 132 characters/line, page log
Event recorder	Event recorder only for single line output, due to the AS 235 software
Print speed	600 bits/s for logging printer and event recorder

- Serial interface modes

- TTY, 20-mA current loop, isolated, passive
- Asynchronous transmission with start/stop bit
- Even parity
- 1200 bits/s for process communication keyboard and configuring keyboard
- 600 bits/s for printer
- 4800 bits/s for PROGRAF AS and KOPAS

- Process interface, I/O modules, function modules

Number of I/O modules per extension unit (total)	13
in basic unit	39
in basic unit + extension unit	91
with ES100K	122
Number of extension units	Up to 7
with ES100 K	Up to 10
Number of cabinets	1 or 2

- I/O modules

Signal modules	Binary and analog
Function modules	Stand-alone open and closed-loop control modules with integrated microprocessors and directly connectable control stations; can be configured from PG/PC
Interface and arithmetic modules	Interface to SIMATIC, ES100K analog/binary arithmetic modules, others

- Blinking clock-pulse generator

Blinking signal outputs z4, z8	U = L+ –3 V typ. I = max. 350 mA per output; this corresponds to approx. 55 modules
Time synchronization inputs potentialfrei	U = 12 to 42 V I = 10 to40 mA Pulse width >2ms; perm. pulse bouncing time max. 6 ms minute pulse
Lamp test outputs	U = L+ from system
Alarm inputRES 1 (floating)	U = 12 to42 V I = 10 to40 mA I <10 mA alarm

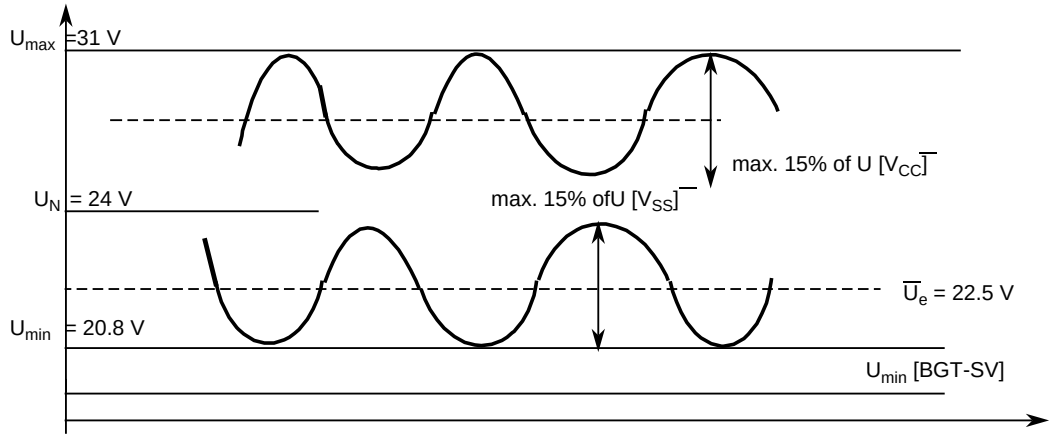
b12, d12, z12, b14, d14, z14 als as signal outputs	I = 1 A
Lampe test outputs as relay outputs	U = max. 40 V I = max. 2.5 A

- AS 235 H DC 24 V

Supply voltage U_V	+24 V
Permissible area of DC 24 V	$\overline{+}$22.5 V to+28.7 V
Permissible ripple	15 % of DC mean value [V_{CC}] in the permissible area

(Ue=22.5 V; min. U_V with max.ripple)

Supply voltage L+:



Limit conditions of operation	35 V 500 ms, recovery time 50 s 45 V 10 ms
Voltage dip with U_N=DC 24 V	0 V, 5 ms, recovery time 10 s
Current consumption, DC 24 V incl. all interface modules	<8.5 A from 24 V (without I/O modules) power supply of extension units via 6DS1 006-8AA U=5 V I=max. 5 A, fuse on DC 24 V side 2. 5 A
External fusing (to be carried out by user)	max. 80 A (with I/O modules)
Signal level of ÜT, LK, TK, UZSYN	DC 24 V - no alarm, 0V - I&C alarm
Voltage switch-off after occurence of ÜT or ÜT	1 min following ÜT or ÜT , the 5-V voltage of the central unit concerned is switched off
Current rating of the lamp contact of the alarm logic module	max. 1 A
Insulation to protection class	VDE 0160

Insulation of modules, air and creepage clearances between pins or conductors to VDE 0110.

- Design

Potential difference of all neutral earth points in distributed systems 7 V

- Mechanical stress ..... (AS 235 H, cabinet)

Stress during operation (full subrack in housing) ..... 10 Hz to150 Hz with 0.15 mmdisplacement 150 Hz to 500 Hz with 2 g

Transport ..... Air-suspended lorry required

- Environmental conditions

Permissible ambient temperature of the modules during operation ..... T= 0 °C to55 °C
T/h ..... 10 K
T/min ..... 0.5 K
for storage ..... T= – 40 °C to+70 °C
T/h ..... 20 K

Ventilation ..... Self-ventilation for basic unit and extension units, provided that the permissible thermal load for the individual cabinets is not exceeded

Permissible cabinet entry temperature: ..... 0 °C to40 °C

Permissible humidity
during operation ..... 65 %
for storage ..... 75 %
Condensation ..... not permissible

Standard cabinet, cabinet power loss P_S

Cabinet entry temp.	25 °C	30 °C 35 °C	40 °C
P_{Smax} without LBG	450 W	420 W 380 W	350 W
P_{Smax} with LBG	700 W		
P_{Smax} with WT, without LBG	450 W	420 W 380 W	350 W
P_{Smax} with WT, with 1 LBG	700 W		
P_{Smax} with WT, with 2 LBG	1000 W		

LBG=fan module, WT=heat exchanger

- EMC

EN 50081-2 (Update 93) ..... class A
EN 50082-2 (Update 93) ..... criterion A

- Type of protection

AS 235 H, system cabinet	IP 10
System cabinet with heat exchanger	IP 54
Gases	Industrial atmosphere is permitted in accessible rooms

- Fan module (LBG)

Order No.	6DS9 943-8AA ·
Number of fans	3
Air flow, free-air operation	3×170 m^3/h
Fan service life	approx. 40,000 h
Fan motor MTBF ambient temperature 55 ° C and U=DC 30 V	85,000 h
Monitoring circuit MTBF	1.16×10^6 h
Power supply	to be generated as safety extra-low voltage (SELV)
Rated value	DC 24 V
Upper limit incl. ripple	DC 30 V
Lower limit incl. ripple	DC 19 V
Ripple	up to AC 3.6 V_{pp}
Internal fusing in SES	6.3 A
External fuse required	4 A
Power consumption	16 W
Contact rating of alarm contact	< DC 30 V/100 mA
Permissible ambient temperature during operation	0 °C to+55 °C
Permissible temperature for transport and storage	– 40 °C to+70 °C, high temperature for a short time
Protection class to VDE 0106, p.1 and IEC 536	I
Protection type to IEC 529 and EN 60529	
open	IP 00
built-in with perforated sheet underneath	IP20
Radio interference level to VDE 0871	B
Noise level	45 dBA
Length of flying cable	25 cm
Fan module connecting cable	
Length 2.20 m	C79195-A3732-H220
Dimensions (w x h x d) with brackets	483mm×43.5mm×174mm
Weight	2.32 kg

The fan module is maintenance-free.
Based on a service life of 40,000 h specified by the manufacturer, it is recommended to replace the fan or the fan module every 4 years.

Adjustment after the fan has been replaced	Jumper settings for alarm signals

AS 235 H, Standard Configuration with Order Numbers (without I/O modules)

AF	Remote bus connector board	6DS9 203-8DA
BKA	Operator input channel interface module	6DS1 330-8CA
BL	Blinking clock-pulse generator module	6DS1 922-8AA
CPU 235 H	Central processing unit)	6DS1 141-8AA
EABA	I/O bus interface module	6DS1 312-8BB
EAVU	I/O comparator and switchover module	6DS1 144-8AA
EE	Extension unit for maxi-termi-point	6DS9 002-8BA
EE	Extension unit for wire-wrap	6DS9 002-8BB
GE	Basic unit (subrack for CPU I and CPU II)	6DS9 027-8AB
M	(Color) monitor for AC 110/230 V	6DS3 401-8BK
	for DC 24 V	6DS3 401-8BL
MDA	Mini floppy disk interface module	6DS1 326-8BB
MDE	Mini floppy disk unit	6DS3 900-8AD
ML	Alarm logic module	6DS1 901-8AA
N-AS	Local bus interface module	6DS1 223-8AA
PBT	Process communication keyboard	6DS3 305-8BA
PUM	Buffer module	C79451-A3125-B227
SB	Synchronization module	6DS1 143-8AA
SED	Cabinet power supply diode	C74103-A1900-A351
SES	Cabinet power supply unit	6DS4 428-8AA
SP	Memory module	6DS1 837-8DA/-8EA/-8FA
SP	Memory module	6DS1 844-8CA/DA
ST	Configuring keyboard	6DS3 303-8AA
SV	Power supply module	C79451-Z1359-U9
SVE	Power supply unit	6DS4 432-8AA
SVM	Power supply module	C79451-A3117-D29
SVME	Power supply unit for extension unit	6DS1 006-8AA
UI	Inductive bus converter for CS 275	6DS4 400-8AB
VKB	Comparator coupler module	6DS1 142-8AA
VR	Video relay	C79451-Z1399-U910

Note: Each CPU contains one or two EABA and BKA modules.
They are identified by the index 1 or 2.

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Page

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

Siemens Aktiengesellschaft

Order No. C79000–B8076–C293
Printed in the Federal Republic of Germany

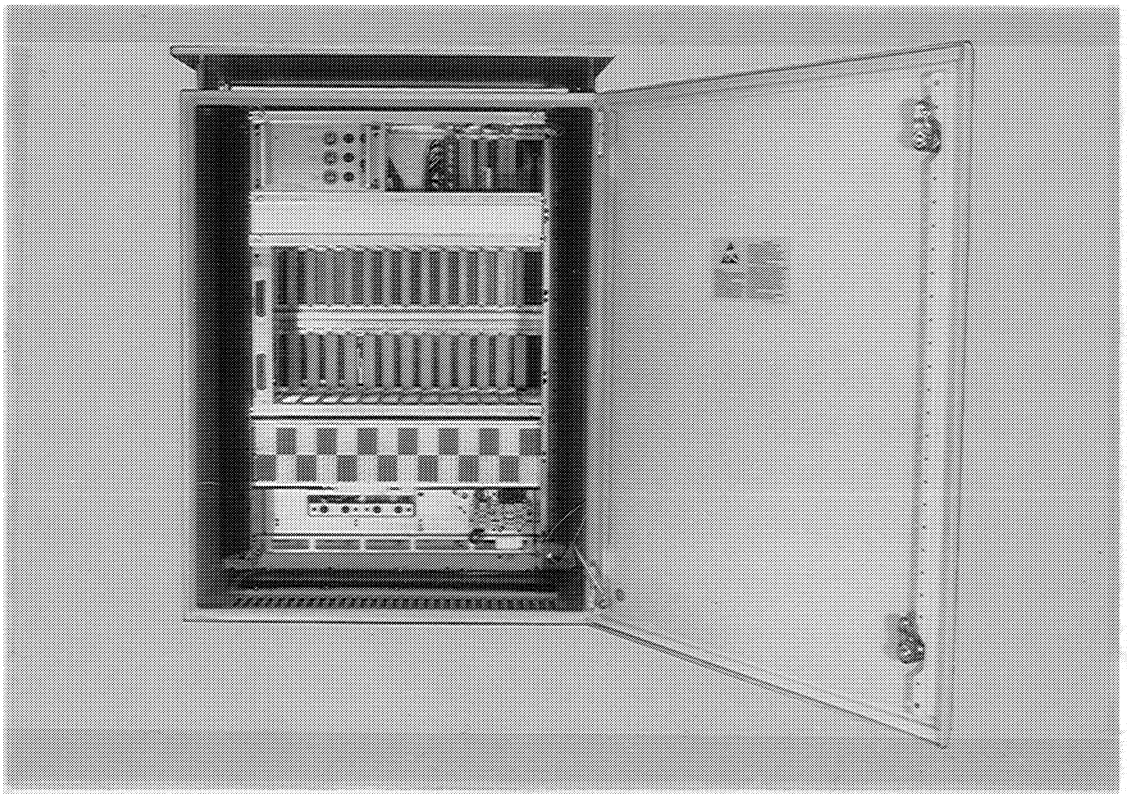
SIEMENS

TELEPERM M

ES 100 K Extension System

6DS2103-8..

Instructions C79000-B8076-C124-04



Contents

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1 Description

1.1 Application

The TELEPERM M ES 100 K extension system supplements the number of I/O bus slots of the AS 220, AS 230, AS 235 and AS 235 H automation systems, especially those of the compact versions AS 220 K, AS 230 K and AS 235 K.

More input/output modules can therefore be used than in the corresponding basic units.
In addition, all interface modules can also be operated in the ES 100 K which are permissible for the I/O bus used of the automation system extended by the ES 100 K.

> **N O T E**
>
> The CS 275, N-V.24 and CP581-TM bus components are not permitted in the ES 100 K.
> Permitted I/O modules are given in the configuration list "Variable Equipment".

Linking of the ES 100 K to a SIMATIC S5 programmable controller also enables TELEPERM M I/O modules to be used in the SIMATIC S5 system.

The ES 100 K extension system is particularly suitable for TELEPERM M automation systems and SIMATIC S5 programmable controllers for the connection of peripheral units with a highly distributed structure since the ES 100 K can be operated up to a distance of 500 m from the basic system/central controller.

> **Warning:**
>
> The ES 100 K extension system is **not** safety-oriented system. It must **not** be used in installations in that an error in the ES or AS could led to dangerous operating states and so be dangerous for men, machines or environment.
> Such safety-relevant automation tasks have to use either a safety-oriented AS (e.g. an F or HF system tested by the German Inspectorate TÜV) or an ES 100 K with correspondent locking circuits or protection systems avoiding the appearance of dangerous operating states.

1.2 Design

The ES 100 K is available in AC 220 V and DC 24 V versions.
The subrack contains a slot in the single-height power supply tier for the power supply module AC 220 V/DC 24 V, 18 A or DC 24 V/24 V.
The double-height tier underneath is the actual extension for I/O modules.
The first slot is provided for the interface module for ES 100 K 6DS1322-8AA (slot not essential).
The +5-V voltage for the I/O bus in the ES 100 K is generated by this module.
The remaining 13 slots can be equipped with I/O modules.

The module slots with the built-in backplane connectors as well as the outer subrack dimensions have the dimensions of the ES 902 packaging system.

The backplane connectors X1 of the 14 slots of the ES 100 K are connected together via a bus board.

1.2.1 Subrack Assignment

Subrack C79451-A3260-A3 (ES 100 K, AC 230 V)
Subrack C79451-A3260-A4 (ES 100 K, DC 24 V)

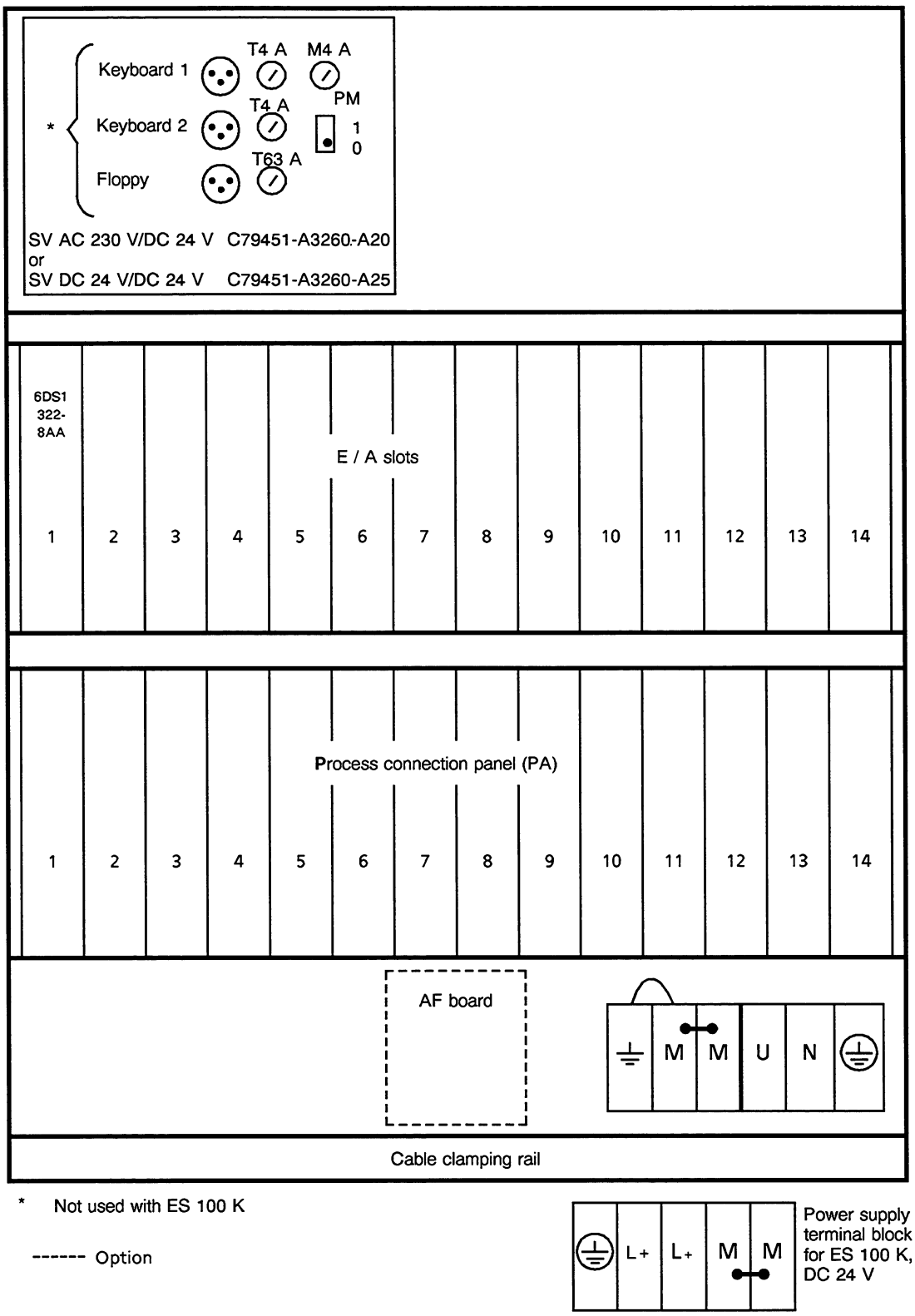


Fig. 1/1 Subrack assignment in ES 100 K, AC 220 V and ES 100 K, DC 24 V

1.2.2 Connection of Process Signals

The backplane connectors X2 of the I/O slots of an ES 100 K are connected as follows to the process connection panel (PA) underneath:

- I/O slots 1 to 4 — Process connection panel locations 1 to 4

- I/O slots 5 to 14 — Process connection panel locations 5 to 14

PM or M is additionally present at the following locations:
- Process connection panel locations 1 and 2
  z32 connected to PM
- Process connection panel locations 5 to 14
  z32 to f32 connected to M

Cabinet alarms can be connected to the remaining pins of the process connection panels (see Fig. 1/5). The process connection panel is only accessible from the front. The signal lines are connected using the Maxi-Termi-Point system.
The cable screens are connected to the cable clamping rail which is connected in turn to the subrack in a conducting manner (not insulated design).
All cables are connected via the cable clam-ping rail.

1.2.3 Power Supply

The ES 100 K systems have their own power supplies and are not supplied from the automation system. The 0 V of all power supplies in the AC 220 V versions must be connected together using the power supply terminal block via terminal M (conductor cross-section 10 mm^2). The power supply is identical to that of the AS 230 K/235 K.
A mains filter is used to suppress interferences.
A redundant supply of L_+ is provided in the ES 100 K, DC 24 V. A transorb diode protects against overvoltages.
The earthing concept is shown in Figs. 1/3 to 1/10. The permissible difference in potential between all ground star points of the systems is $\leq$ 7 V.

1.2.4 Housing/Cabinet

The subrack is fitted in a sheet-steel housing.
Installation is possible in standard TELEPERM M cabinets if the design guidelines are observed. The conditions listed in Section 1.5 apply if delivery is without a housing.

1.2.5 Couplings

- **Coupling in TELEPERM M system, a)**

The I/O bus in the ES 100 K is coupled to the I/O bus of the basic unit of a TELEPERM M automation system via the interface module for ES 100 K 6DS1322-8AA and the cable connector 6ES5721-....
One of these modules is inserted in the ES 100 K, e.g. at slot 1, the second in a TELEPERM M AS system. Up to four ES 100 K systems can be connected in series.

- **Coupling of SIMATIC S5 expansion units to TELEPERM M automation systems via ES 100 K, b)**

Coupling is possible with the interface module for S5 expansion units 6DS1321-8AA in the ES 100 K via the non-multiplexed SIMATIC I/O remote bus and the CC/EU interface module 310 6ES5310-3AB11 in the SIMATIC S5 expansion unit (6ES5 183 or 6ES5 186 for I/O modules in compact version, ER 701-2 for I/O modules in block design).

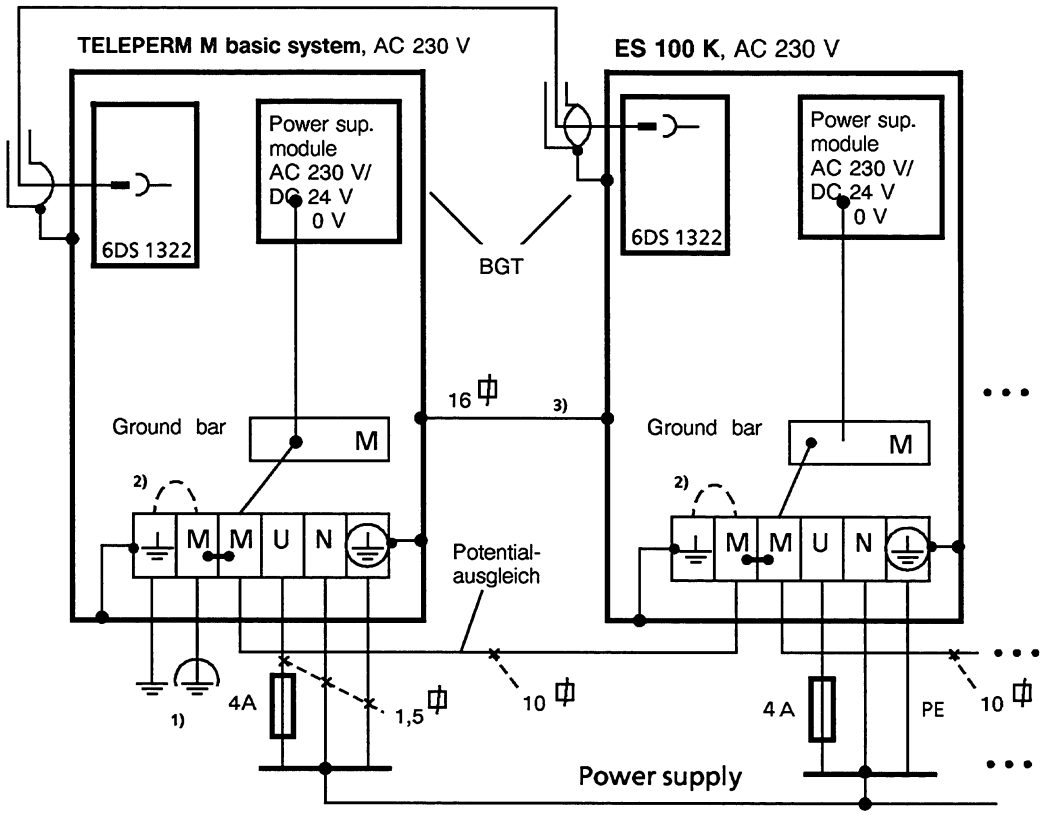
- **Coupling of ES 100 K to SIMATIC S5 programmable controllers, c)**

When coupling to a SIMATIC S5 programmable controller, one module 6DS1322-8AA is present in the ES 100 K and one module 6ES5304-3UA11 in the SIMATIC S5 central controller. Operation of TELEPERM M I/O modules in the SIMATIC S5 system via the multiplexed SIMATIC remote bus is possible via these two modules. ES 100 K systems can also be connected in series in this case.

The cable connectors of the I/O remote bus must be connected in configurations a) and c) to the last interface module in each case using the cable terminating plug 6ES5760-1AA11, in configuration b) using the cable terminating plug 6ES5760-0AA11.

1.2.6 Earthing Conditions

- **Coupling in TELEPERM M system**



Earth symbols

Low-noise earth, electronic earth

Local earth (building earth)

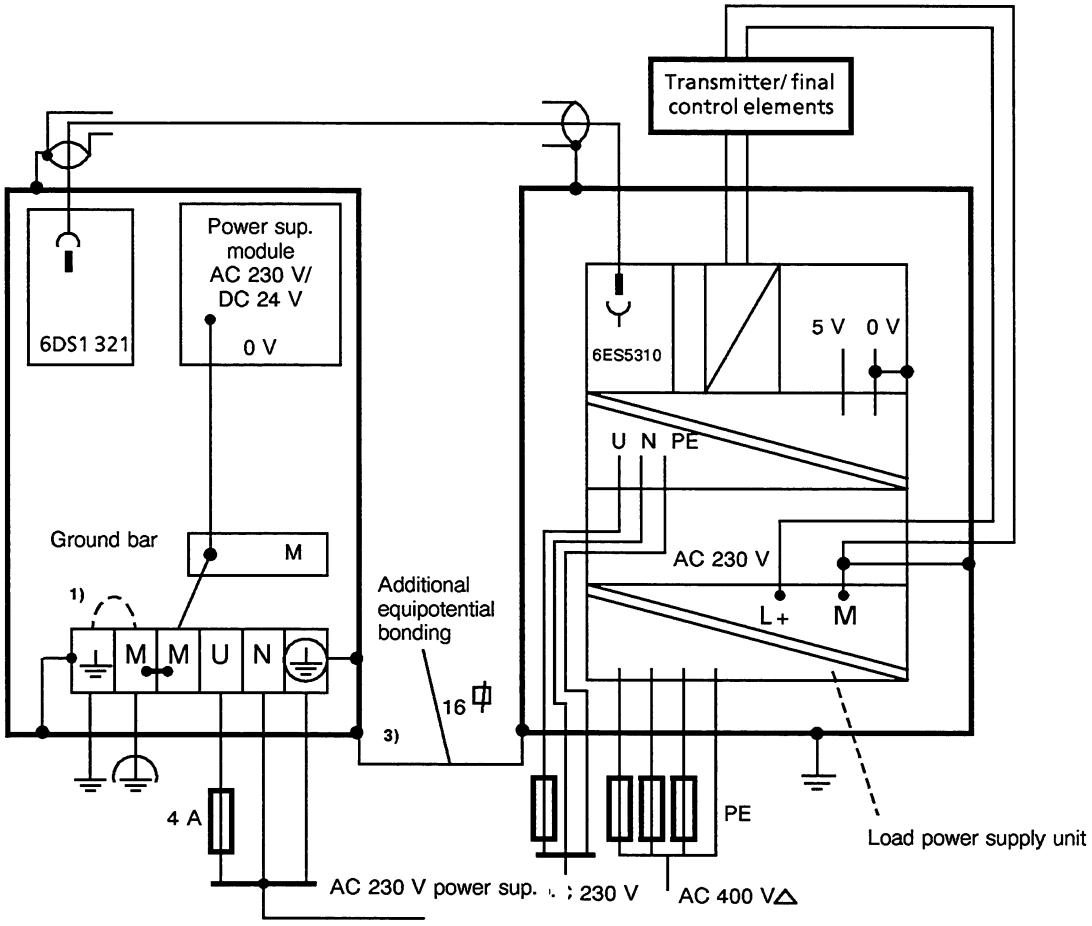
Local earth or PE

PE

1) Only contact one device (e.g. between AS 235 K) to electronics earth or separately to building earth
2) Remove jumper
3) Additional equipotential bonding if necessary, see Instructions 6DS1322-8AA

Fig. 1/2 Earthing of AS 235 K, AC 230 V with ES 100 K, AC 230 V

- **Coupling of SIMATIC S5 expansion units to TELEPERM M automation systems via ES 100 K**



TELEPERM M basic or extension system AC 230 V

SIMATIC expansion unit
6ES5 183-3 UA 12 (AC 230 V)
Use of floating and non-floating I/O modules possible

1) Remove jumper, connect M to electronics earth orseparately to building earth

3) Additional equipotential bonding if necessary (see Instructions for 6DS1 321-8AA)

Earth symbols

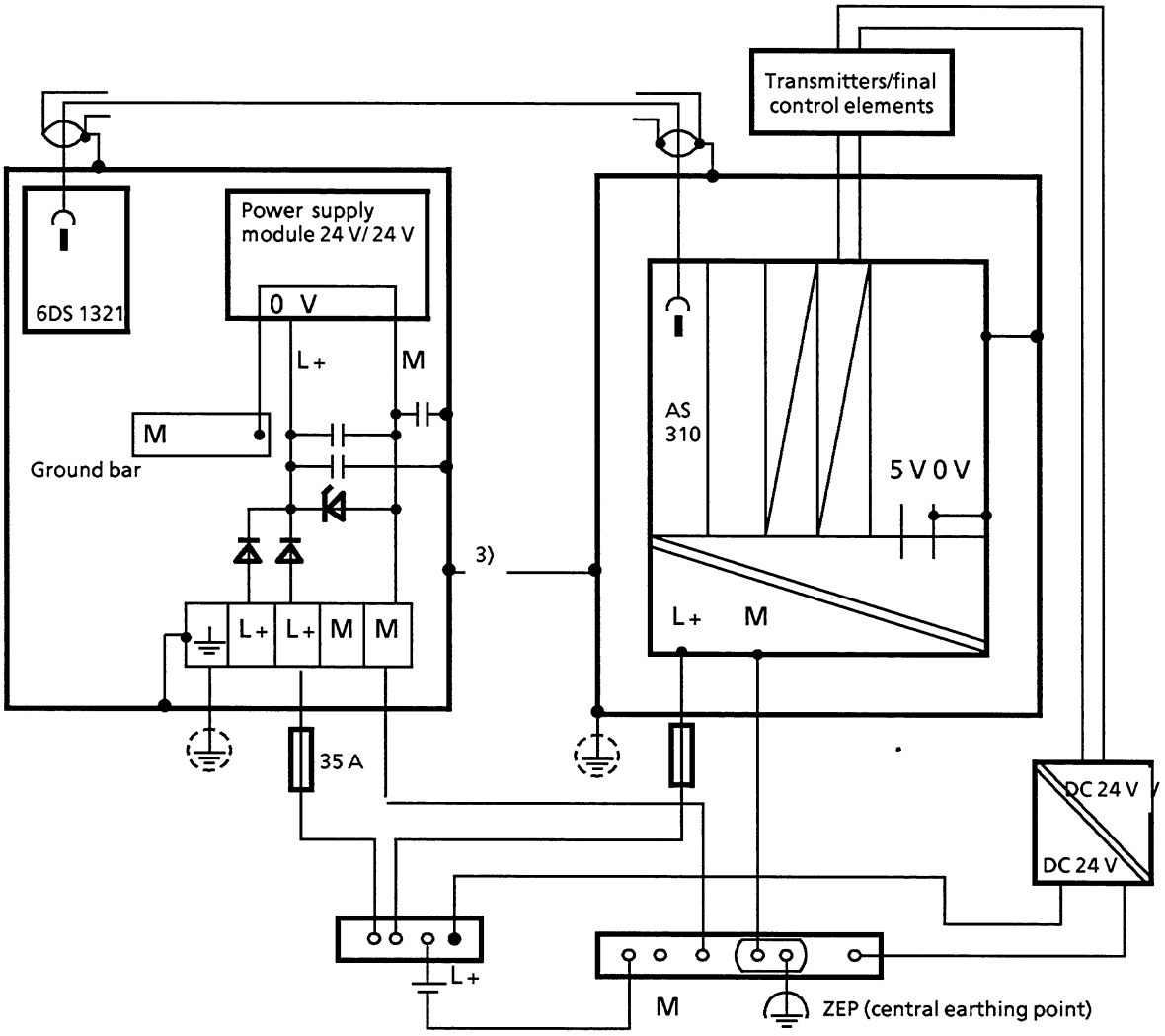
Low-noise earth, electronic earth

Local earth (building earth)

Local earth or PE

PE

Fig. 1/3 TELEPERM M earthing concept, AS or ES system AC 230 V, with SIMATIC expansion unit AC 230 V

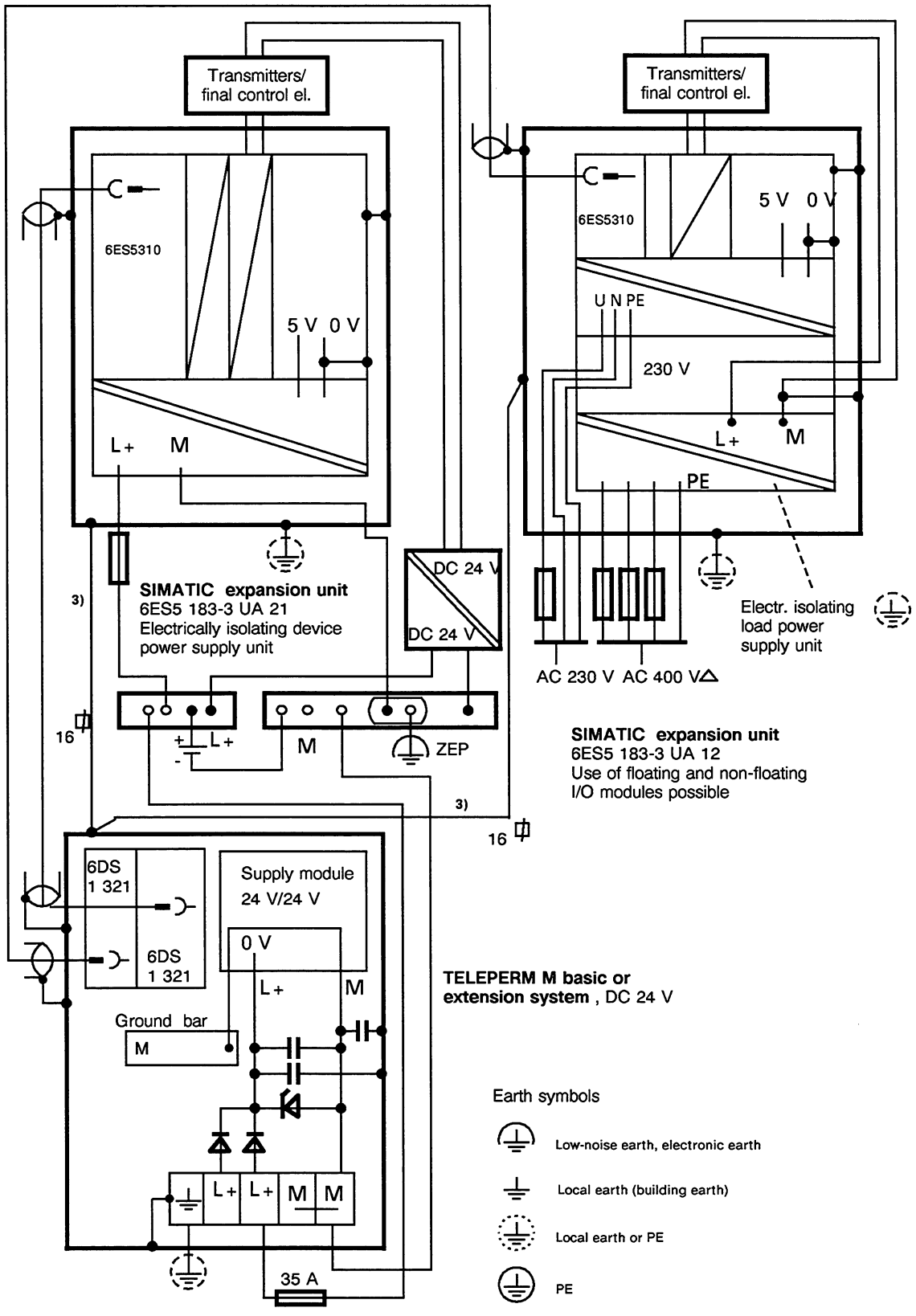


TELEPERM M basic or extension system DC 24 V

SIMATIC expansion unit
6ES5183-3UA21 (DC 24 V)
Only use electrically isolating device / load power supply unit

3) Additional equipotential bonding if necessary,
see instructions for 6DS1321-8AA, interface module for SIMATIC S5 expansion unit DC 24 V and central earthing point

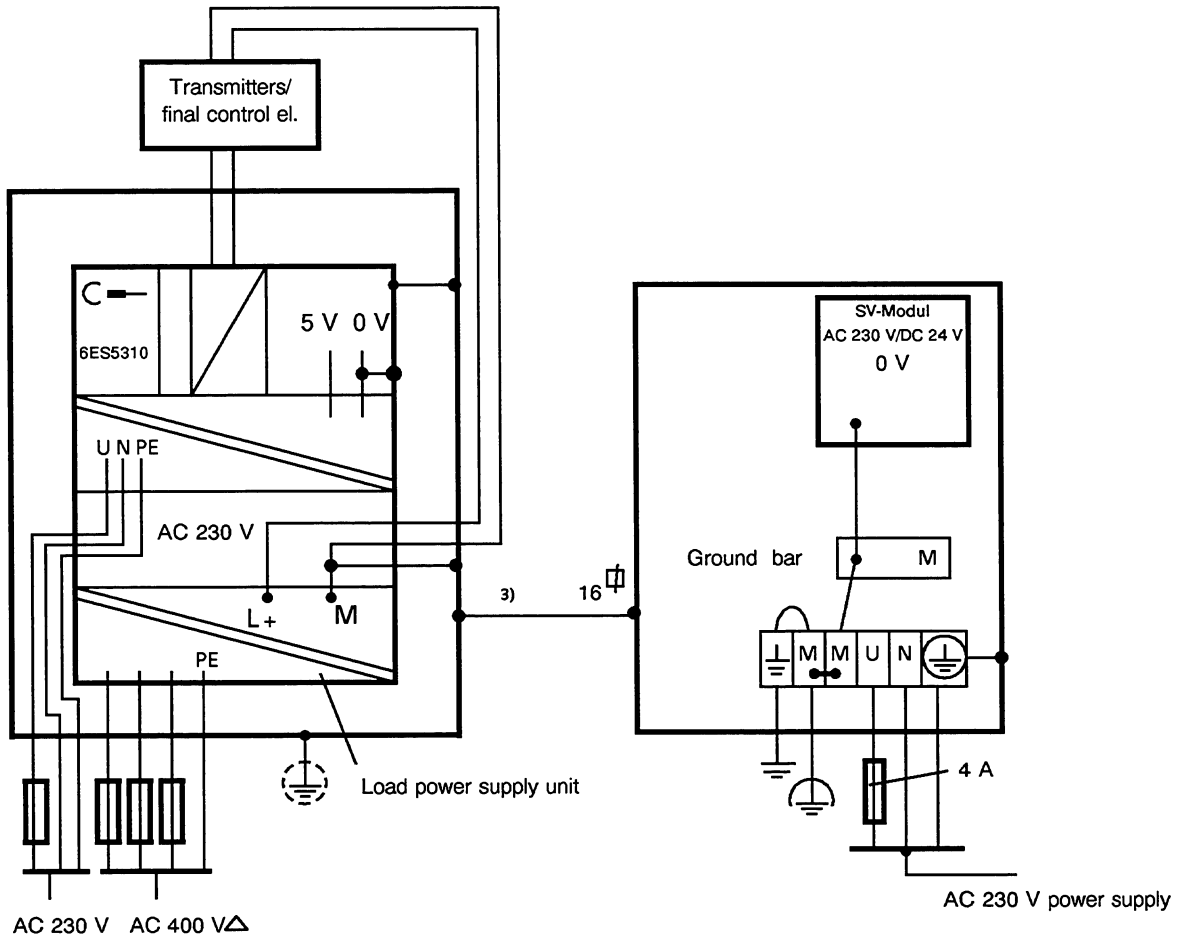
Fig. 1/4 TELEPERM M earthing concept, AS or ES system DC 24 V, with SIMATIC expansion unit DC 24 V and central earthing point



3) Additional equipotential bonding if necessary

Fig. 1/5 TELEPERM M earthing concept, AS or ES system DC 24 V, with SIMATIC S5 expansion units DC 24 V/AC 230 V and central earthing point (ZEP)

- **Coupling of ES 100 K to SIMATIC S5 programmable controllers**



SIMATIC basic unit **TELEPERM M extension unit** (AC 230 V)

3) Additional equipotential bonding if necessary

Earth symbols

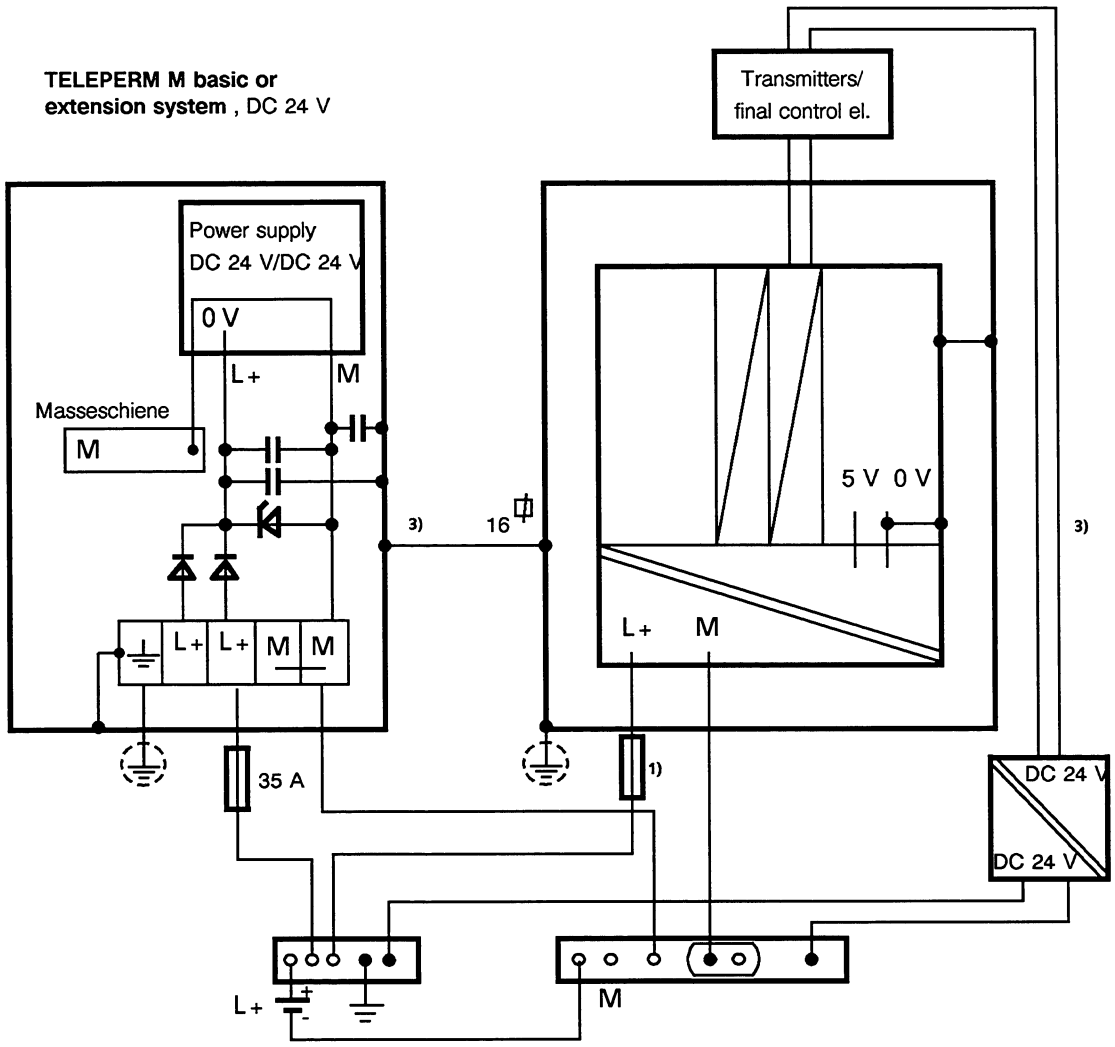
Low-noise earth, electronic earth

Local earth (building earth)

Local earth or PE

PE

Fig. 1.6 Earthing concept of TELEPERM M extension unit (AC 230 V) with SIMATIC basic unit (AC 230 V)



1) See corresp. SIMATIC description

3) Additional equipotential bonding if necessary

Earth symbols

Low-noise earth, electronic earth

Local earth (building earth)

Local earth or PE

PE

Fig. 1/7 Earthing concept of TELEPERM M extension unit (DC 24 V) with SIMATIC basic unit (DC 24 V) and central earthing point

1.3 Mode of Operation

1.3.1 Power Supply

The ES 100 K, AC 220 V is powered by the AC 230 V mains voltage. A power supply module (C79451-A3260-A20) generates DC 24 V from this.

The ES 100 K, DC 24 V is powered by a redundant L_+ supply and the power supply module DC 24 V/DC 24 V.

The interface module for ES 100 K 6DS1322-8AA provides the 5-V supply for the I/O bus in the ES 100 K (see jumper assignments).

1.3.2 Coupling of ES 100 K in TELEPERM M System

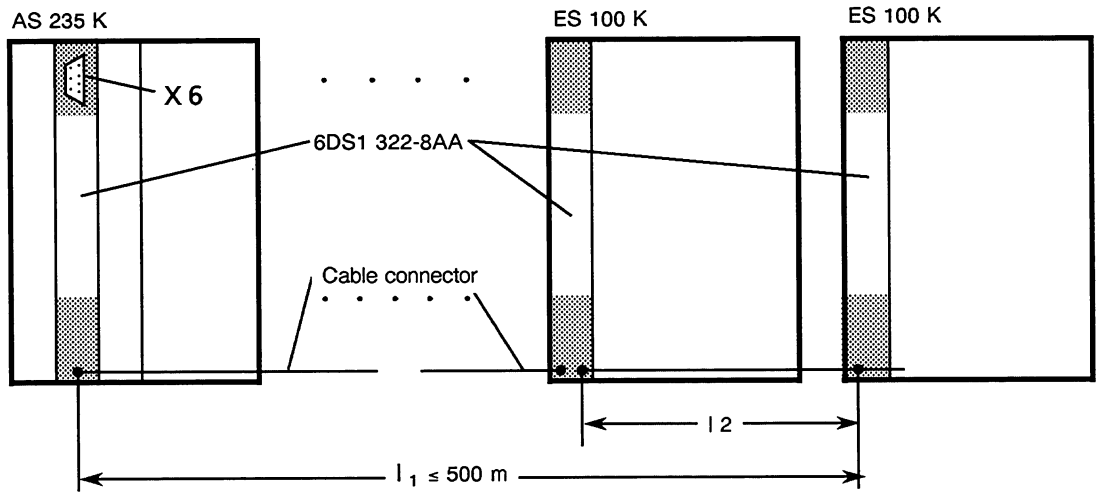
The coupling of the I/O bus of an ES 100 K with the I/O bus of a TELEPERM M automation system is a parallel bus coupling using two interface modules for ES 100 K 6DS1322-8AA (cable connector 6ES5721-0....) with a multiplexed parallel bus (multiplex operation between addresses and data).

Up to four ES 100 K systems can be connected in series to an interface module for ES 100 K. The incoming cable is connected in each case to connector X3, the outgoing cable to connector X4 on the interface module. The end of the cable must be terminated by a cable terminating plug on connector X4.

The bus drivers permit a maximum coupling length of 500 m.

- **Double addressing check (1-out-of-n check, EANK)**

Depending on the cable length **between two ES 100 K interface modules**, the cycle time for access to I/O modules can be increased using a jumper on the interface module in the AS in order to detect and signal double addressing (see Fig. 1/8).



$l_2 \leq 200$ m → jumper X6 (11, 12) inserted → Double addressing is detected, cycle time for I/O access ≤ 26.5 µs

$l_2 \leq 500$ m → jumper X6 (11, 12) open → Double addressing is detected, but cycle time for I/O access extended to ≤ 38 µs

Fig. 1.8 Coupling of ES 100 K in TELEPERM M system

Caution

Double addressing of an I/O module in an AS 235. AS 235 K or AS 235 H and an I/O module in an ES 100 K is not detected.

A power failure in an ES 100 K or on an interface module 6DS1322-8AA (L_+ or +5 V I/O bus) leads to a READY delay with all I/O modules in the associated ES 100 K as well as in the following ES 100 K systems of this branch.

See Section 2.3 for the jumper settings of the interface module for ES 100 K 6DS1322-8AA. Also refer to the instructions "Interface module for ES 100 K extension systems", Order No. C79000-B8076-C125, for pin assignments and further information.

1.3.3 Coupling of ES 100 K to SIMATIC S5 Programmable Controllers

The coupling partners are the module 6ES5304-UA11 in the SIMATIC central controller and the interface module for ES 100 K 6DS1322-8AA in the ES 100 K.

Transmission in the range up to ... m is the same as with a coupling in the TELEPERM M system via a multiplexed parallel bus (multiplex mode between addresses and data, RS 422 interface conditions).

Caution

Double addressing is not detected in the SIMATIC system (EANK is not evaluated).

See Section 2.3 for the jumper settings of the interface module for ES 100 K 6DS1322-8AA.
Also refer to the instructions "Interface module for ES 100 K extension system", Order No. C79000-B8076-C125, for pin assignments and further information.

1.4 Technical Data

Installation in a TELEPERM M standard cabinet is permissible if the design guidelines for these cabinets are observed.
The conditions in Section 1.5 apply if delivered without a housing.

- **System structure**

Extension of the peripherals of the TELEPERM M AS 235, AS 235 K and AS 235 H automation systems, mainly AS 235 K.
Use of TELEPERM M I/O modules in the SIMATIC S5 system.
This structure enables the automation of distributed plants.

- **Process interface**

Number of I/O modules:

I/O slots per ES 100 K	13
Together with AS 230 (max. 6 x ES 100 K)	Max. 88
Together with AS 230 K (max. 8 x ES 100 K)	Max. 105
Together with AS 235 K (max. 8 x ES 100 K)	Max. 108
Distance from basic unit	Max. 500 m

- **Supply voltages**

- ES 100 K, AC 230 V

Supply voltage U_V	AC 230 V, ± 10 %
Current consumption	Dependent on configuration
External fuse	4 A slow-blow
Permissible thermal loading in IP 21 housing	200 W
Voltage dip with U_N = AC 230 V	≤ 10 ms

- ES 100 K, DC 24 V

Supply voltage U_V	U_N = +24 V
Permissible range	DC = +21 V to +33 V including ripple
Permissible ripple	15 % of mean DC voltage
Limiting range of use	DC = +35 V ≤ 500 ms DC = +45 V ≤ 10 ms
Voltage dip with U_N = 24 V	0 V, ≤ 5 ms, recovery time 10 s
Current consumption	Depending on configuration
External fusing	25 to 35 A in each case (to be provided by user)
Permissible thermal loading in IP 21 housing	200 W

- **Delay times on I/O bus for distributed coupling**

100-m cable	t_{delay} = 2.5 µs
Conversion from TELEPERM M I/O bus to TELEPERM M I/O remote bus and vice versa	t_{delay} = 2.5 µs
Conversion from TELEPERM M I/O bus to RS 422 interface	t_{delay} = 2.5 µs

- **Insulation**

Insulation	To VDE 0160
Protection class	I

Insulation of modules with respect to clearance and creepage distances from pin to pin or from conductor to conductor according to VDE 0110.

- **Design**

Potential difference of all ground star points of distributed systems	≤ 7 V

- **Weight**

ES 100 K, AC 230 V (without I/O modules, in housing)	68 kg
ES 100 K, DC 24 V (without I/O modules, in housing)	60 kg
IP 21 housing	39 kg

- **Mechanical stress**

Operational stress (subrack fitted in housing)	10 Hz to 150 Hz with 0.15 mm excursion 150 Hz to 500 Hz with 2 g
Transport	Using lorry with air suspension

- **Ambient conditions**

Permissible ambient temperature of modules

- Operation	T = 0 °C to 55 °C
Change in temperature/h	≤ 10 K
Change in temperature/min	≤ 0.5 K
- Storage	T = -40 °C to +70 °C
Change in temperature/h	≤ 20 K
Ventilation	Self-ventilation

Sheet-steel housing/standard cabinet

Permissible cabinet inlet temperature	0 °C to 40 °C
Permissible humidity	
- Operation	≤ 75 %
- Storage	≤ 65 %

Condensation not permissible

- EMC

to EN 50081/2 (release 93)	Limit class A
to EN 50082/2 (release 95)	Criterion A

- Low voltage guideline
  EN 60950 (release 96)
- **Degree of protection**

ES 100 K (with I/O modules) in:	
- Subrack	IP 00
- Sheet-steel housing	IP 21

Impairment of function by gases	Industrial atmospheres in occupied rooms are permissible

- Subrack

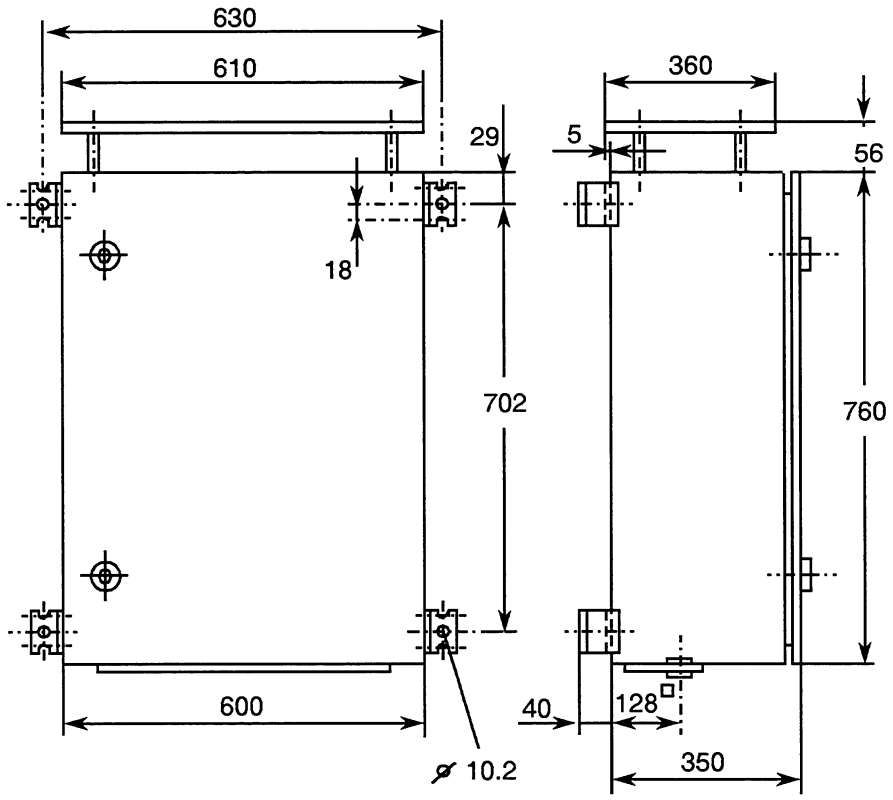


Fig. 1.9 Subrack - IP 21 sheet-steel housing

1.5 Planning and Installing the Subracks when Delivered without Compact Housings

Preliminary Remark

These installation instructions for compact systems without housings take into consideration the specific properties of TELEPERM M and are an extension of the existing guidelines. A deterioration in the electromagnetic compatibility (EMC) and improper operation of the system can be expected if deviations from the installation instructions are made or if individual measures are not observed.

Before installing and operating the automation or extension system, examine the subrack with the circuit boards for transport damage.

Regulations for electrostatically sensitive devices must always be observed when handling electronic modules.

1.5.1 Installation Instructions for Compact Systems in other Housing/Cabinet

- **Dimensions and weights of the compact systems**

The subracks of the compact systems must always be installed in a closed metal housing or cabinet; degree of protection at least IP 10 to VDE 0100; protection against foreign matter must be provided if applicable.

Subracks must not be installed in an open housing or frame.

- Minimum dimensions of metal housing/cabinet:

  Width : at least 600 mm
  Height : at least 760 mm
  Depth : at least 350 mm

The bending radii "R" of the remote bus cable and routing in the cabinet according to TELEPERM M design guidelines must be observed during planning (R ≥ 300 mm with standard remote bus cable).

- Weight of ES 100 K subrack (AC 220 V) **without** I/O modules:

  ES 100 K : 28 kg

  8 kg less with DC 24 V supply.

- **Ambient conditions**

Permissible ambient temperature of metal housing/cabinet:
0 °C to 40 °C with 75 % relative humidity.

Permissible ambient temperature of modules in metal housing/cabinet:
0 °C to 55 °C, condensation not permissible.

The metal housing/cabinet must be ventilated from the bottom to the top; the subrack must only be installed vertically.

Removal of dissipated heat from the individual systems must be guaranteed.

Power dissipation **without** I/O modules:

ES 100 K AC 230 V : 20 W
ES 100 K DC 24 V : 20 W

The power dissipation of the I/O modules used must be taken into account to obtain the total power dissipation of the systems.

- **EMC conditions**

The EMC conditions and the installation guidelines must be observed (see C79000-G8076-C417).

Peripheral and power supply cables must be routed to the subrack from below.
The cable screens must be connected to the cable clamping rails using clips (e.g. PUK clips).

Caution

When installing more than one compact system in a suitable metal housing/cabinet, the systems must have the same connection voltage. Connection of the mains voltage must be made using screened cables. In the case of a DC 24 V supply, an interference suppressor must be connected to the supply line on entry into the cabinet (such as interference suppression unit C79165-A3012-B41 in the standard cabinet).

No components which do not belong to the system must be located in the metal housing/cabinet (e.g. lines/cables, contactors, thyristors, electronic modules etc.).

- **VDE regulations**

The VDE safety regulations VDE 0100, VDE 0106 Part 100, VDE 0110, VDE 0160 must be observed in the design and during operation.
The protection class of the subrack is I according to IEC 536/VDE 0106, Part 1.

An earth connection must be made between the subrack and the metal housing/cabinet (Cu 6 mm^2).

- **Earthing**

The metal housing/cabinet with the compact systems must be provided with a local earth/central earthing point/equipotential bonding conductor according to the examples shown in these instructions and in the design regulations.

2 Installation and Commissioning

Before installing the ES 100 K extension system, check the housing and subrack with modules for damage during transport

Caution

When using electrical systems, devices and components observe the prescriptions and guidelines for handling electrostatically sensitive devices. For this see the "Guidelines for handling electrostatically sensitive devices ESD" before Register 1 of this Manual. Damages could occur in case of non-observance.

Note

When you do not already know the safety user notes and the guidelines for handling electrostatically sensitive devices, shortly called ESD you should read these notes before beginning this section.
The strict reading and observance of these guidelines and notes protects you and the system from possible damages, before and during operation.

2.1 Mounting and Installation

- Wall mounting of ES 100 K in sheet-steel housing

If the ES 100 K extension system is fitted in a sheet-steel housing (IP 21), the housing can be fitted to a wall using a mounting set.
The mounting set is delivered together with the housing.

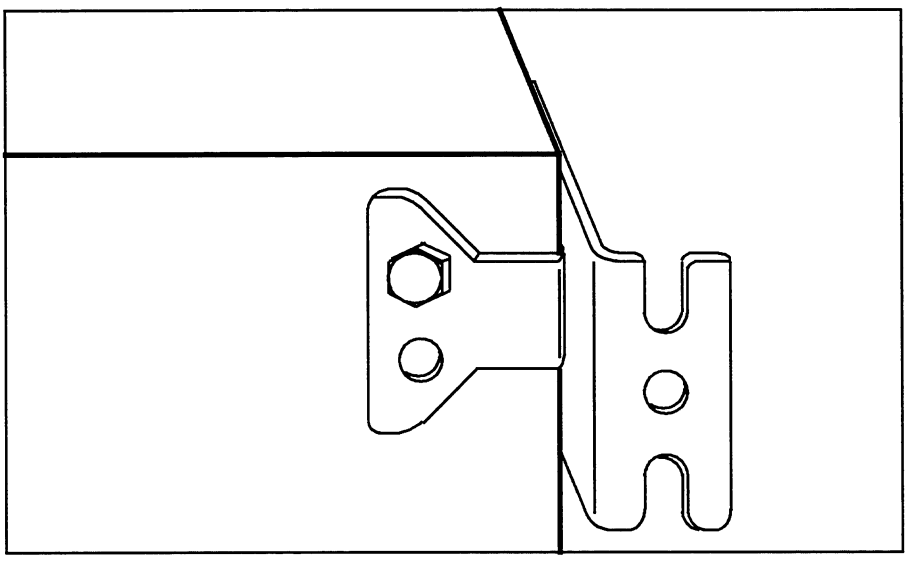
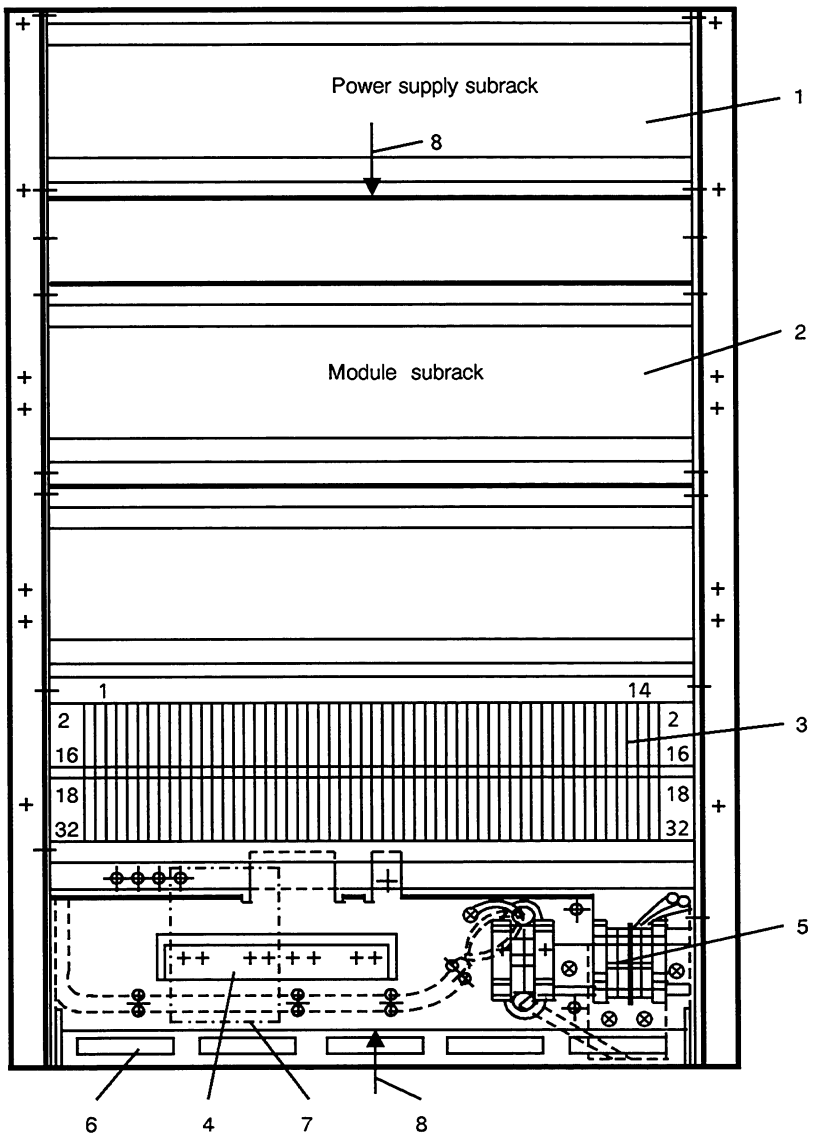


Fig. 2.1 Installation of mounting set for IP 21 housing

- Installation of ES 100 K subrack in a standard cabinet

The basic system of the ES 100 K, consisting of subracks and modules, can also be installed in standard TELEPERM M cabinets. The basic system subracks differ depending on the power supply.

ES 100 K/AC230 V subrack: Order No. : C79451-A3260-A3
ES 100 K/DC 24 V subrack: Order No. : C79451-A3260-A4



1 Power supply tier
2 I/O modules
3 Process connection panel PA
4 Connector board for remote bus (AF)
5 Connection for power supply
6 Cable clamping rails
7 Mounting location for remote bus connector
8 Holding point

Fig. 2.2 Installation of ES 100 K subrack in standard TELEPERM M cabinet

Caution

The subrack should be lifted by two persons. **Do not** rest it on its rear panel, the wrap pins would be bent.

Caution

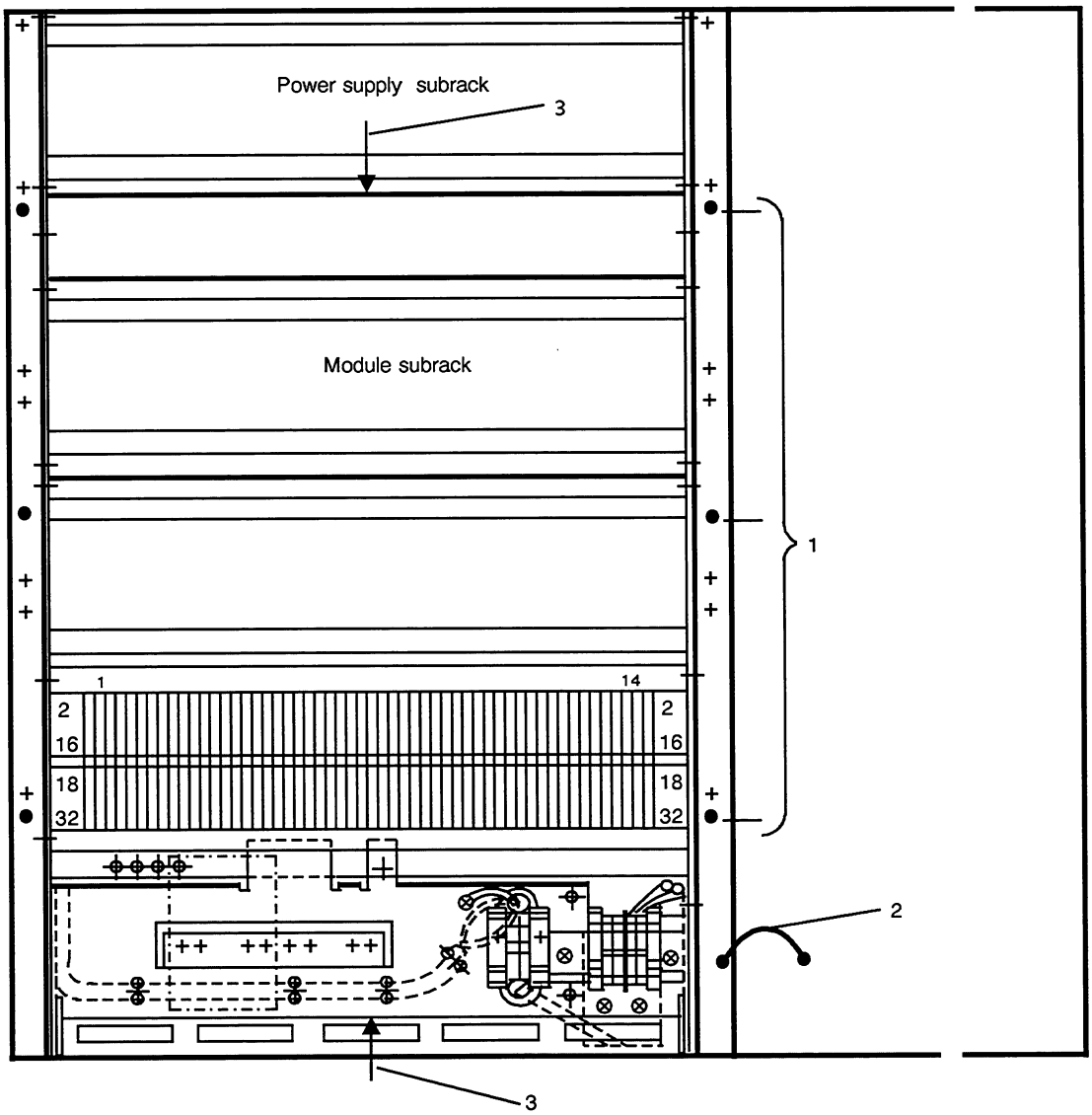
A screened mains cable must be used if the ES 100 K/AC 230 V subrack is installed in a standard cabinet, and the screen must be connected to the standard cabinet

- Removal/installation of ES 100 K subrack in sheet-steel housing

To remove an ES 100 K from a sheet-steel housing (IP 21/IP 54), proceed as follows:

- Place housing with subrack on rear panel of housing.
- Loosen earthing cable between subrack and housing.
- Loosen screws connecting subrack to housing (see Fig. 2/3).
- The subrack can now be removed by two persons. Put down vertically.

Installation in a sheet-steel housing (IP 21/IP 54) is carried out in the reverse order..



1 Securing screws
2 Earthing cable
3 Holding point

Fig. 2.3 Installation/removal of ES 100 K subrack into/from sheet-steel housing IP 21

2.2 Connection of Process Signal Cables

Caution

Process signals must always be connected using screened cables and routed separately from circuits with voltages > 60 V. The cables must consist of twisted pairs of conductors. Each signal circuit must be routed through one pair. Analog and binary signals must only be routed in separate cables because of the danger of crosstalk. Analog position feedbacks and limit switches of final control elements are combined in one cable.
Note that binary signals from contacts may have to be connected to a 47-kohm resistor as a check for line breakages.

The process cables are inserted into the ES 100 K housing from below. The screens must be connected to the cable clamping rails. A differentiation must be made between a braided screen (Fig. 2/5) and a foil screen (Fig. 2/6). The process cables are connected to the process connection panel PA using the Maxi-Termi-Point system (MTP).

- Types of cable

Suitable cables for process signals are installation cables for industrial electronics (SIMATIC cables) with color-coded conductors twisted in pairs and combined into bundles. The cables with stranded or solid conductors (cross-section 0.5 mm^2, diameter 0.8 mm) have a static screen.

Cable designation	for
A-Y(ST)YY n×2×0,8/1,4 BdSi	Burying in earth *)
J-Y(ST)Y n×2×0,8/1,4 BdSi	Normal use
J-LiYY n×2×0,5/1,6 BdSi	Mini control panels
J-LiYCY n×2×0,5/1,6 BdSi	Vibration and stress, plug connection

A Outer cable
Bd Twisted in bundles
C Screen braiding
J Installation cable
Li Stranded conductor
Si SIMATIC colors
(ST) Static screen
Y PVC insulation

*) Burying in earth is not recommended. If absolutely essential, ensure that the transmitted signals are not falsified.

Table 2/1 Installation cables for industrial electronics

- Conductor coding

The conductors twisted in pairs are identified by eight basic colors of the insulating covering (Table 2/2).

Conductor	1 2	3 4	5 6	7 8
Pair	1	2	3	4
Color	bl rd	gy ye	gn br	wh bk

bl blue
rd red
gy gray
ye yellow
gn green
br brown
wh white
bk black

Table 2/2 Basic colors of the insulating coverings of a bundle

Four pairs of conductors belong to a color group and are twisted together into a bundle. The individual conductors of a bundle also have a ring code so that mixing up of conductors with the same colors from different bundles is prevented. When counting the bundles, start with the innermost position.

- Routing the process cables

The process cables must be routed in earthed cable racks separately from power cables. The distance between these two types of cables must be at least 200 mm. Cables outside buildings must be routed in cable ducts and provided with an additional earthed screen (armoring). On entry into buildings, all conductors must be provided with suitable overvoltage arresters for lightning protection (see "General lightning protection regulations ABB" and the corresponding VDE guidelines "Requirements placed on transmitters and output devices").

Caution

Devices connected via process cables must not generate interfering voltages. For example, relays or solenoid valves driven by binary outputs must be interference-suppressed directly on the instrument terminals by suitable protection circuits (quenching diodes, voltage-dependent resistors).

Bundle No.	Ring color	Ring group/code	Bundle spiral
1 2 3 4	pink	I II III IV	—
5 6 7 8	orange	I II III IV	—
9 10 11 12	violet	I II III IV	—
13 14 15 16	pink	I II III IV	blue
17 18 19 20	orange	I II III IV	red

Table 2.3 Conductor bundle coding

- Connection to process connection panel or via signal distribution cabinet

The process cables can be connected directly to the process connection panel PA without intermediate wiring (female connectors with pins 0.8 x 2.4 mm for solderless Maxi-Termi-Point system).
Special signal distribution cabinets are available to provide a clear interface between the process and electronics cabinets in the plant. The individual conductors can be cross-connected here and arranged using appropriate marshalling connections such that a destination-oriented combination of conductors is possible for the respective cabinets. Signal distribution cabinets are uneconomical in the case of smaller plants and single cabinets.

- Connection of cables with braided screen

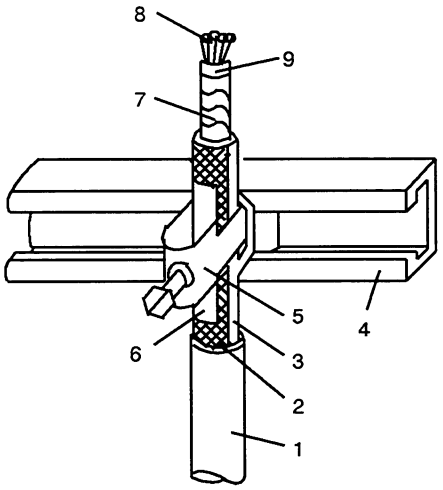
Approx. 50 mm of the outer cable sheath must be removed at the screen connection clamp.

The cable is hooked into the clamping rail using the cable clamp and two trough assemblies and screwed tight. Two thin cables can also be secured using one clamp. The insulation should be retained if possible up to the process connection panel PA and the individual conductors fanned out there.

In order to guarantee a large-area contact, upper and lower trough assemblies should be used as the cable clamps (e.g. Messrs. PUK, Köln Werke KG, cable clamp model H, type K12 (12 mm diam.) to K20 (20 mm diam.) and trough assembly type LW12 (12 mm diam.) to LW20 (20 mm diam.)).

One set of cable clamps with associated trough assemblies is enclosed. Additionally required clamps must be ordered depending on the number of cables.

Plastic parts in the clamps must be removed.



1 Signal cable with braided screen
2 Approx. 50 mm braided screen exposed
3 Trough assembly (e.g. PUK model H, type LW12 to LW20), 40 mm long
4 Cable clamping rail
5 Cable clamp (e.g. PUK model H, type K12 to K20)
6 Top part of clamp, adjustable using screw
7 Cable sheath
8 Pairs of conductors to MTP connections
9 Adhesive tape or sleeve

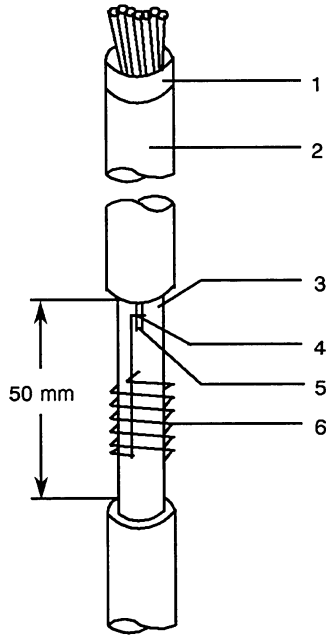
Fig. 2.4 Connection of cables with braided screen

- Connection of cables with foil screen

Carefully remove 50 mm of cable sheath (do not damage foil screen). Expose supplementary earth wire on one side and solder to tin-plated wire (0.8 mm diam.).

Wind the wire around the exposed foil as in Fig. 2.6.

Clamp the foil cable as in Fig. 2.5. Do not tighten the screw of the cable clamp too tight as the foil screen would otherwise be damaged.



1 Adhesive tape or sleeve
2 Cable sheath
3 Foil screen
4 Solder point
5 Supplementary earth wire exposed
6 Wire wrapping (e.g. tin-plated wire, 0.8 mm diam.)

Fig. 2.5 Connection of cables with foil screen

2.3 Jumper Settings

Interface Module for ES 100 K 6DS1322-8AA

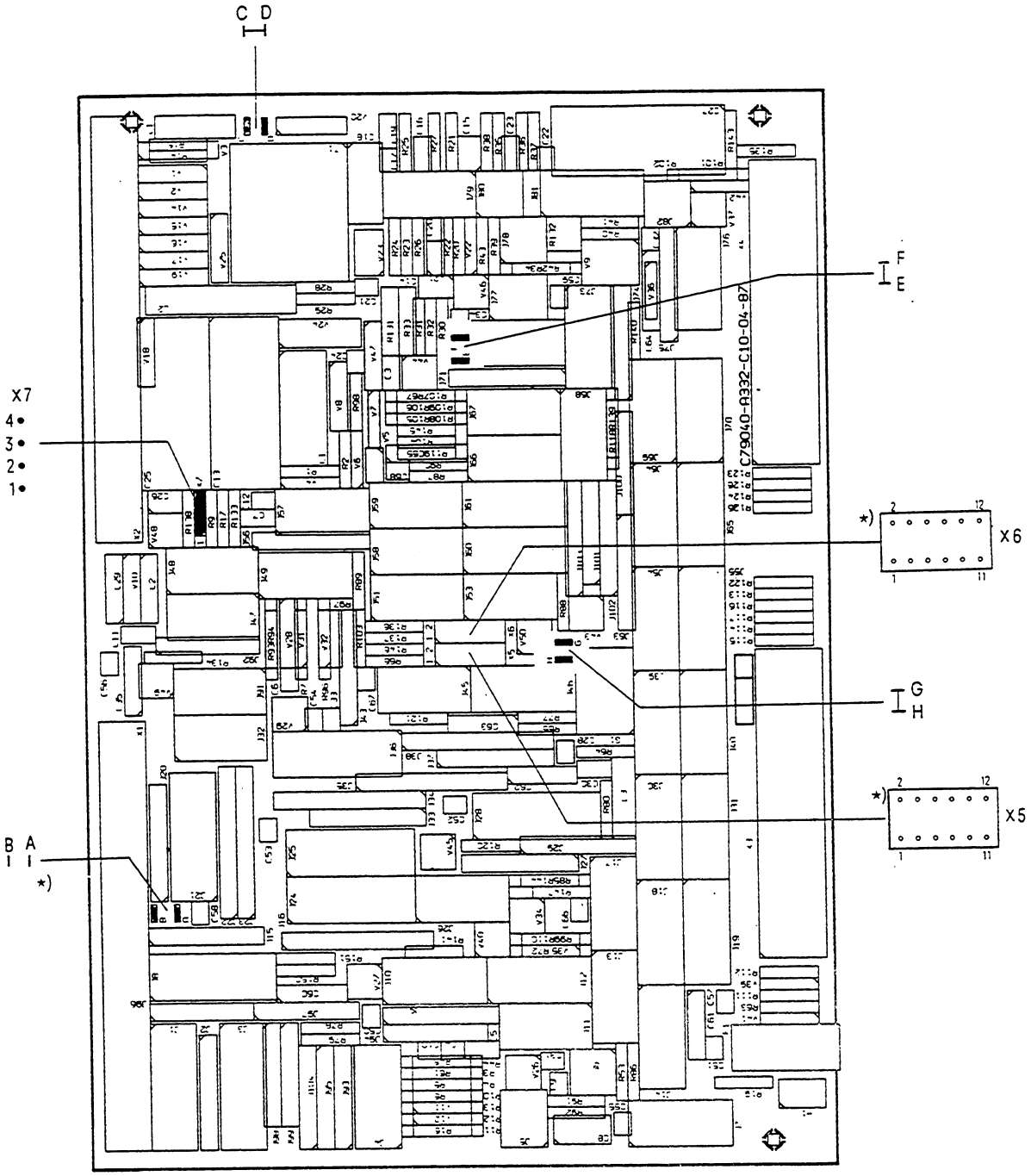


Fig. 2/12 Interface module for ES 100 K 6DS1322-8AA

- Interface module for ES 100 K in the TELEPERM M basic unit

			Observations:
X5:	1,2	EG/GG	(X)
	3,4	TM/S5	( ) not relevant in GG
	5,6	internal/external flashing	( )
	7,8	2.5 MHz	( ) 1)
	9,10	5 MHz	( ) 1)
	11,12	10 MHz	( ) 1)
X6:	1,2	EANK	( )
	3,4	PRDY	( )
	5,6	LAST ELEMENT	( ) irrelevant
	7,8	TEST	( )
	9,10	LOCK	( )
	11,12	Delay off	( ) 2)
X7:	1,2	Frame address	( )
	3,4		( )
Soldered jumper A – B			( ) 5 V I/O bus from basic unit Jumper must be removed!

1) Cable connector lengths (total) between basic unit and last extension unit

1 ≤ 100 m → jumper **X5:**	7,8	( )
	9,10	( )
	11,12	(X)
1 ≤ 300 m → jumper **X5:**	7,8	( )
	9,10	(X)
	11,12	( )
1 ≤ 500 m → jumper **X5:**	7,8	(X)
	9,10	( )
	11,12	( )

(X) Jumper inserted
( ) Jumper not inserted

2) Detection of double addressing ES 100 K ↔ ES 100 K

	Jumper X6 (11,12)	
	inserted	open
Cable length between two ES 100 K	≤ 200 m Double addressing detected	≤ 500 m Double addressing detected
Cycle time for I/O access	≤ 26.5 µs	≤ 38 µs

- Interface module for ES 100 K in TELEPERM M extension unit (for coupling to TM basic unit)

				Observations:
X5:	1, 2	EG/GG	( )	
	3, 4	TM/S5	( )	
	5, 6	internal/external flashing	( )	
	7, 8	2.5 MHz	( )	1)
	9, 10	5 MHz	( )	1)
	11, 12	10 MHz	( )	1)
X6:	1, 2	EANK	(X)	
	3, 4	PRDY	(X)	
	5, 6	LAST ELEMENT	( )	irrelevant
	7, 8	TEST	( )	irrelevant
	9, 10	LOCK	( )	
	11, 12	Delay off	( )	
X7:	1,2	Frame address	( )	3)
	3,4		( )	
A	B		(X)	5V I/O bus from 6DS1322-8AA
C	D		(X)	
E	F	Test jumpers	(X)	
G	H		(X)	

- Interface module for ES 100 K in ES 100 K (for coupling to SIMATIC central controller)

				Observations:
X5:	1, 2	EG/GG	( )	
	3, 4	TM/S5	(X)	
	5, 6	internal/external flashing	(X)	
	7, 8	2.5 MHz	( )	1)
	9, 10	5 MHz	( )	1)
	11, 12	10 MHz	( )	1)
X6:	1, 2	EANK	(X)	
	3, 4	PRDY	(X)	
	5, 6	LAST ELEMENT	(X)	if last element !
	7, 8	TEST	( )	irrelevant
	9, 10	LOCK	( )	
	11, 12	Delay off	( )	
X7:	1, 2	Frame address	( )	3)
	3, 4		( )	

Soldered jumpers A B (X) 5 V I/O bus from 6DS1 322-8AA

(X) Jumper inserted
( ) Jumper not inserted

1) Cable connector lengths (total) between basic unit and last extension unit (siehe Seite 2-9)

3) Frame address

Jumper	1-2	3-4	Slot address
1st EU	x	x	0-13
2nd EU	-	x	16-29
3rd EU	x	-	32-45
4th EU	-	-	48-61

Jumper meaning

X5: 1,2 EG/GG Mode selection
open: Operation in extension unit (EU)
inserted: Operation in basic unit (BU)

X5: 3,4 TM/S5 Only relevant in EU mode, selection of used basic unit.
open: TELEPERM basic unit (AS 235, AS 235H, AS 235K)
inserted: SIMATIC basic unit (AG 135, ...)

X5: 5,6 Int./ext. flashing, flashing voltage source for common error LED.
offen: internal clock generator, i.e. on the interface board
gesteckt: external clock generator, i.e. flashing voltage via pin 2d30 (BSE) from central processor.

X5: Clock Clock frequency selection of the control logic
7,8 inserted: 2.5 MHz for coupling cable lengths < 500 m
9,10 inserted: 5 MHz for coupling cable lengths < 300 m
11,12 inserted: 10 MHz for coupling cable lengths < 100 m
Insert always only one of the jumpers X5 7,8 9,10 11,12!

X6: 1,2 PRDY Switch on/off the resistance of the signals PRDY and
3,4 EANK EANK.

open: Only in BU mode: The resistors are present on the I/O interface board.
inserted: Only in EU mode: The resistors of the remote bus interface board are used..

X6: 5,6 Last EU Only relevant in EU mode with SIMATIC BU, connects the PEU input to LOW (peripherie ready).
open: In all EUs that are connected to further EUs via connector 4
inserted: Only in the EU in that no other EU is connected.

X6: 7,8 Test Connects the "TEST" signal of the control logic to pin 1b8.
open: No allocation without further bus master in the system.
inserted: HIGH signal at pin 1b8 prevents this module to access on the I/O bus.

X6: 9,10 LOCK Connects the "LOCK" signal of the control logic to pin 1z6.
open: No allocation without further bus master in the system.
inserted: HIGH signal at pin 1z6 prevents this module to access on the I/O bus.

X6: 11,12 Verzögerung Switching on the prolongation of the peripheral access time.
open: Delay switched on
inserted: Normal read/write cycle time

X7:

Jumper	1-2 PLAD 10	3-4 PLAD 11	Slot addresses for S mod.	for E mod.
Extension unit				
1. EG	x	x	0-13	1-14
2. EG	-	x	16-29	17-30
3. EG	x	-	32-45	33-46
4. EG	-	-	48-61	49-62

x = Jumper inserted

Soldering jumper A-B for external or internal 5-V bus supply, source determination for the 5-V bus voltage.

When the interface module is inserted in the basic unit, the **jumper A-B must be open** because the 5-V bus voltage has to come from the central unit.

Caution

If the jumper A-B is inserted, the 5-V source voltage of the module can be overloaded when the basic unit supply is switched off.

When the interface module is inserted in an extension unit (ES 100 K), the **jumper A-B must be open** because the 5-V voltage has to be delivered from the interface module.

3 Maintenance

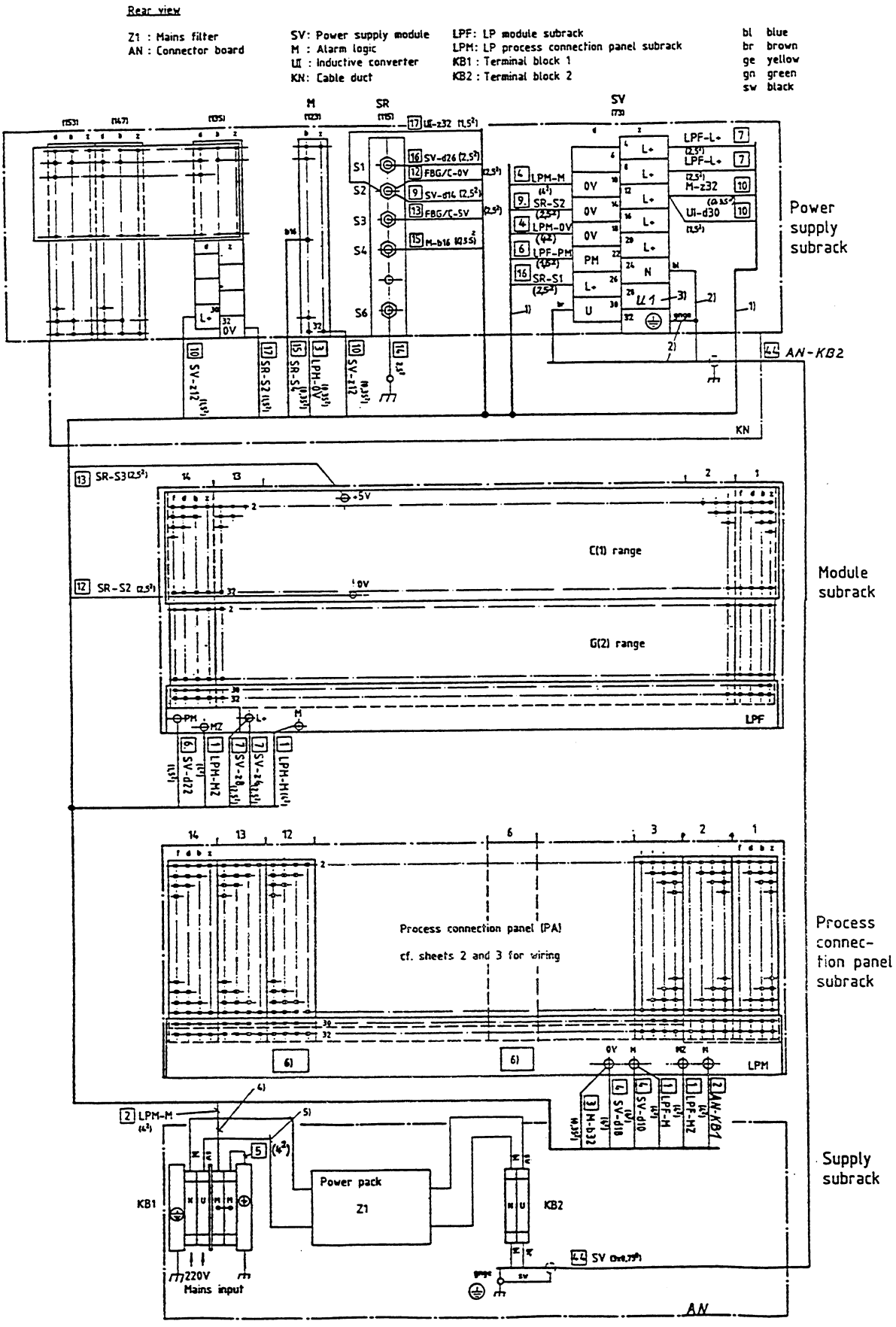


Fig. 3.1 Connection diagram ES 100 K, AC 230 V

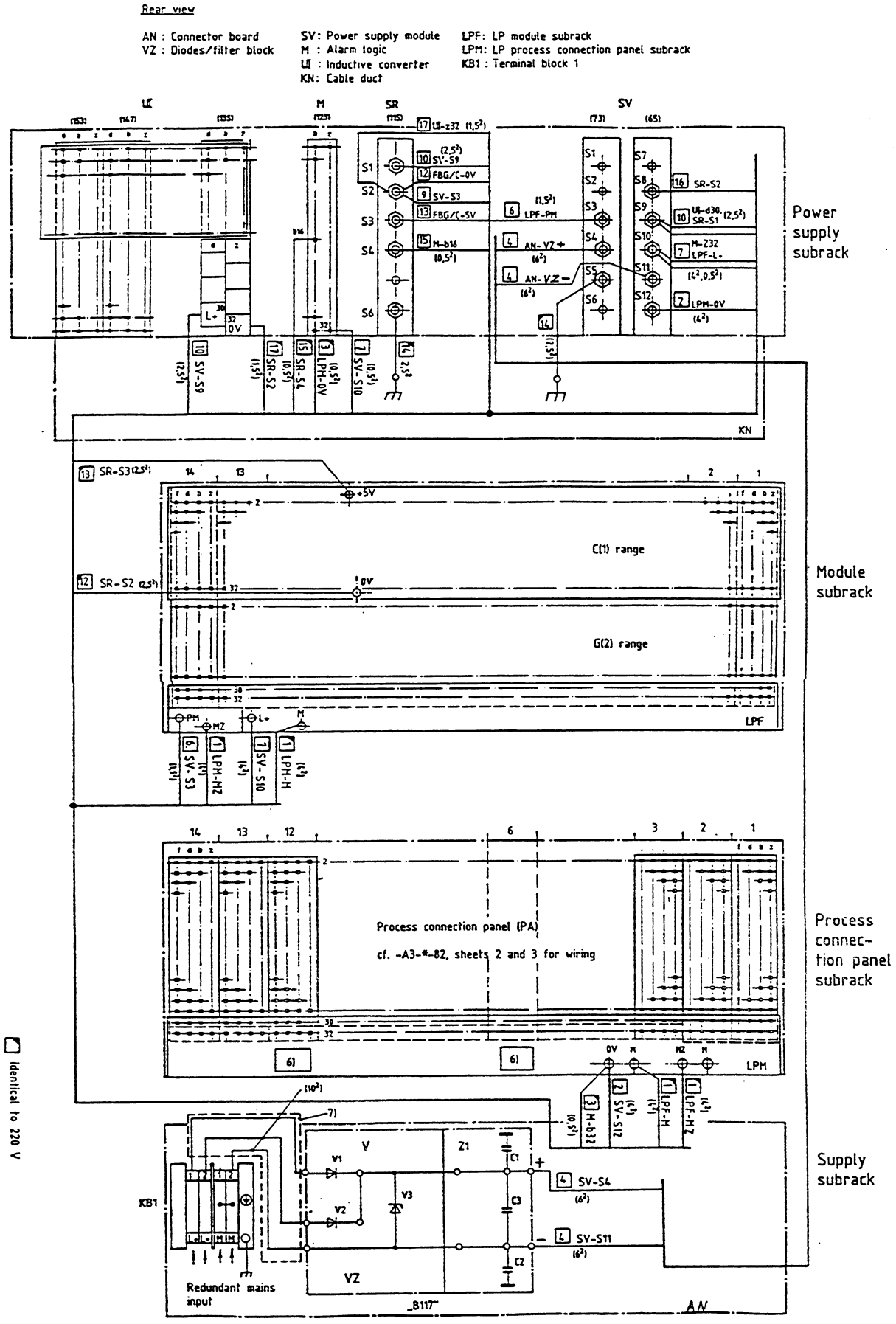


Fig. 3.2 Connection diagram ES 100 K, DC 24 V

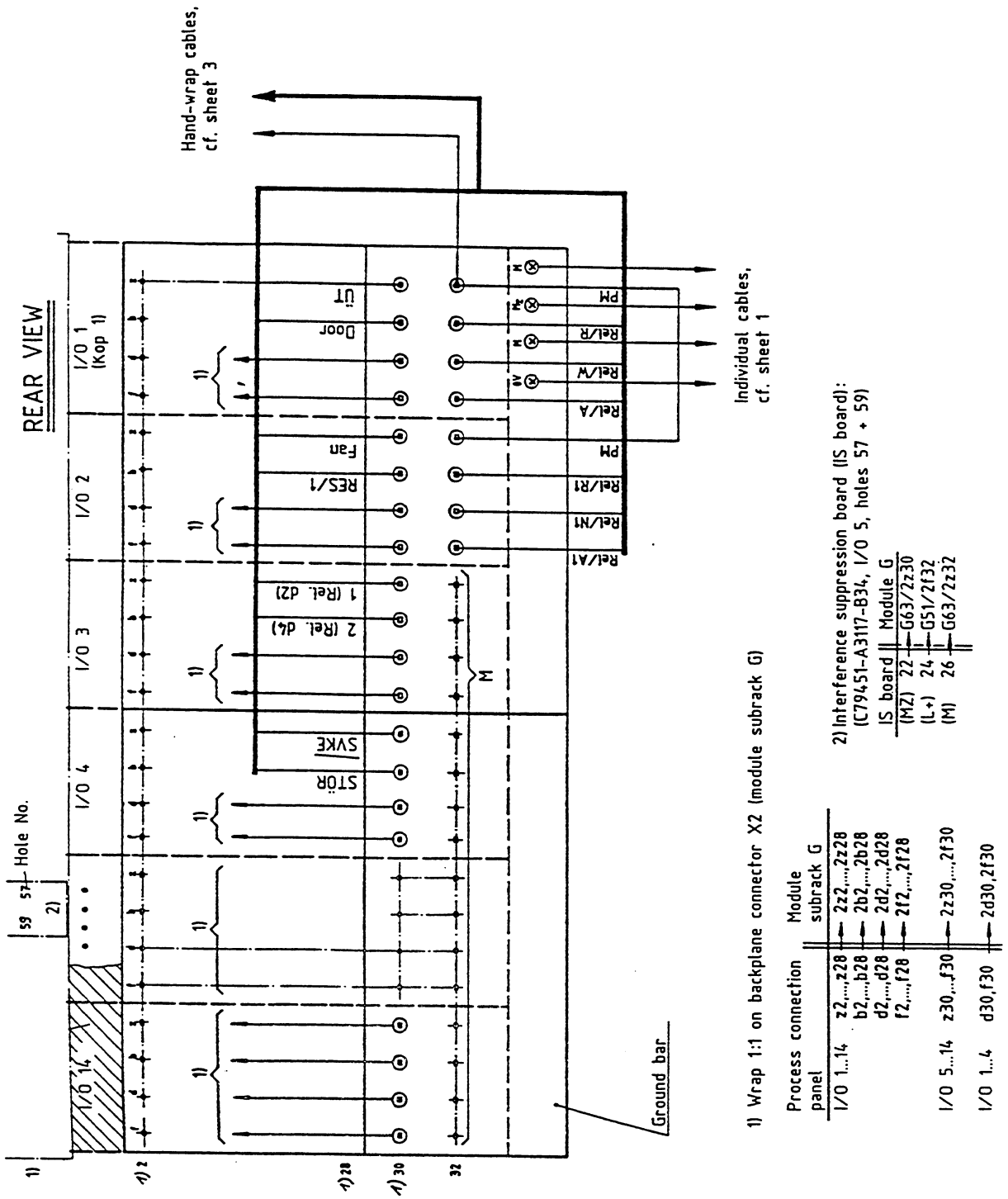


Fig. 3.3 Wrap connections ES 100 K

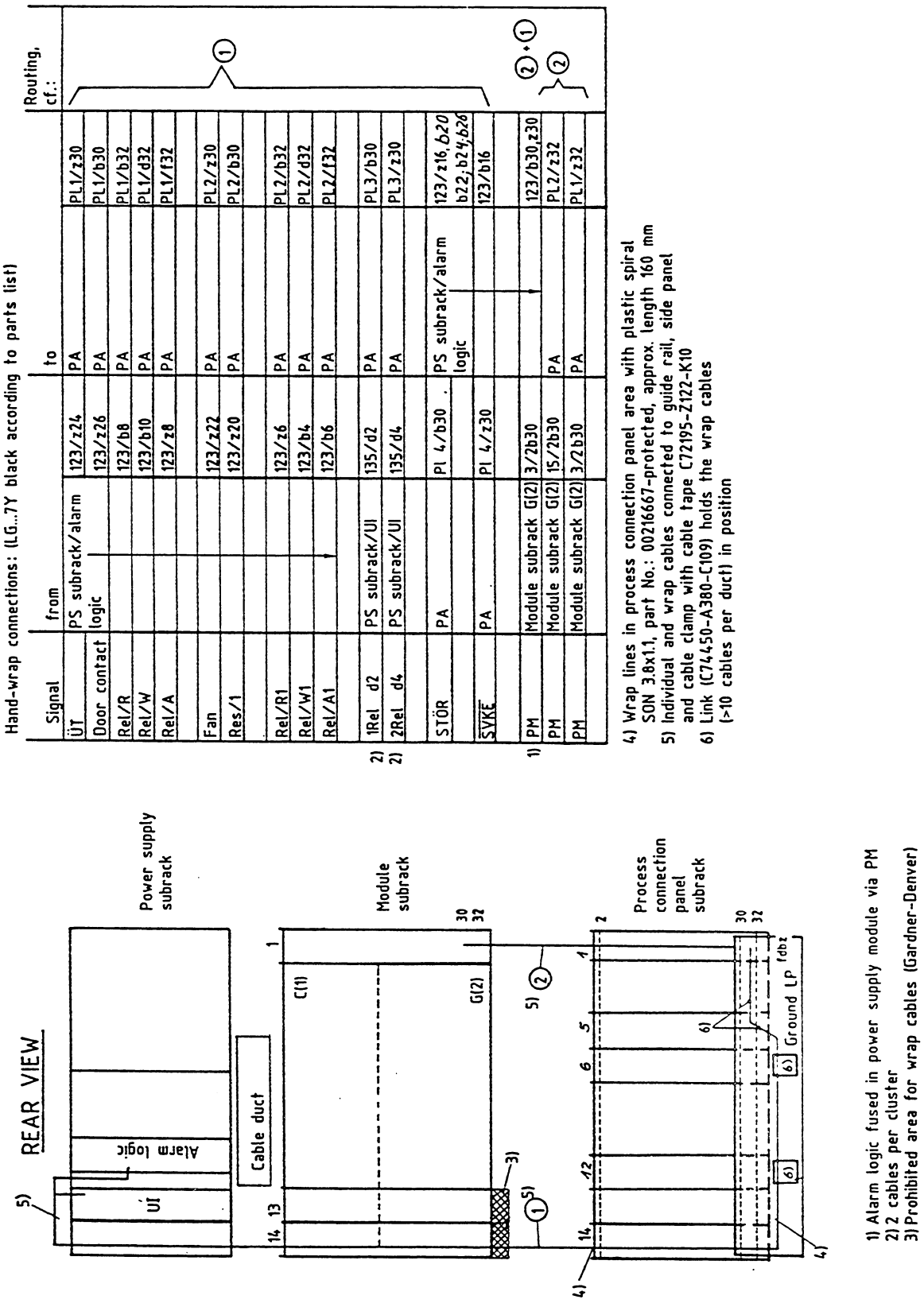


Fig. 3.4 Hand-wrap connections ES 100 K

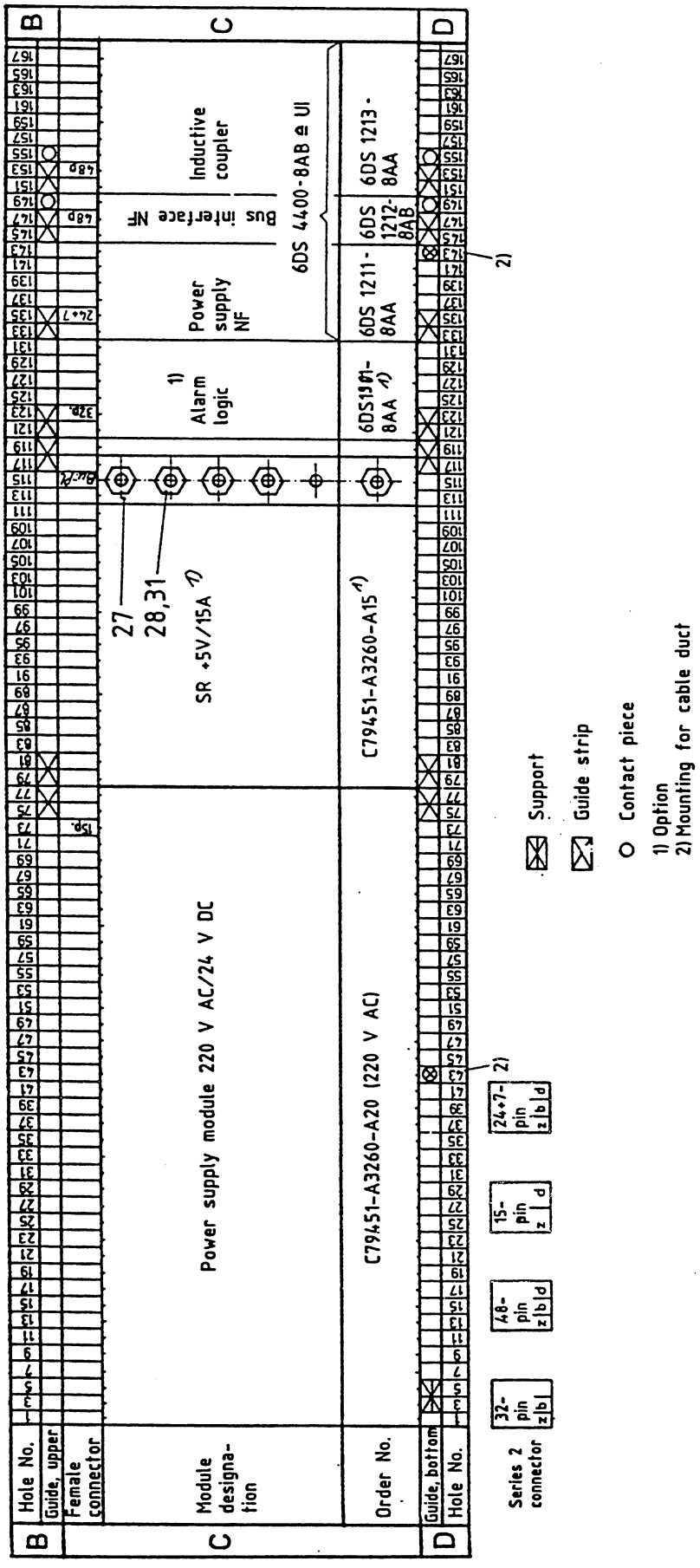


Fig. 3.5 Slots in power supply subrack ES 100 K, AC 230 V

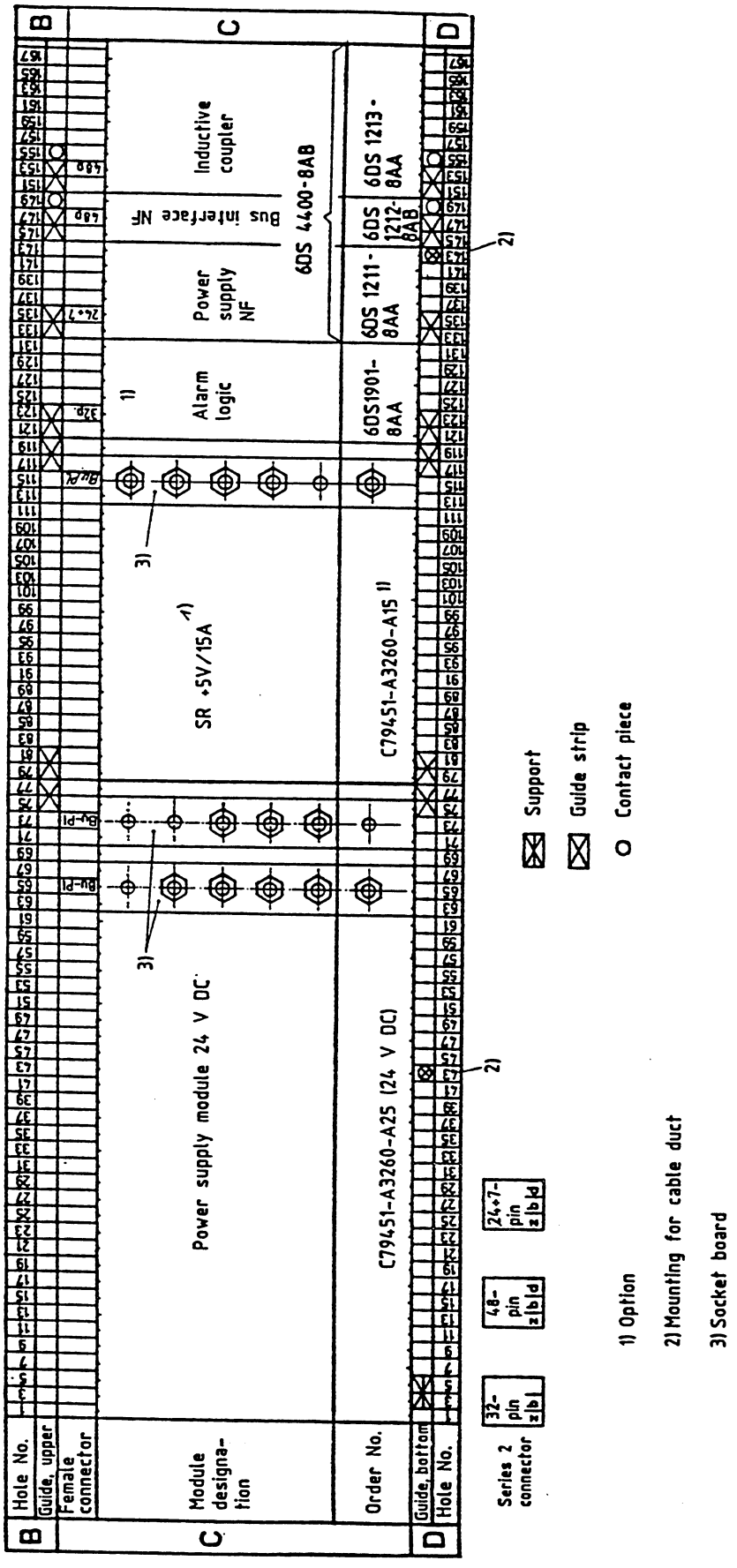


Fig. 3.6 Slots in power supply subrack ES 100 K, DC 24 V

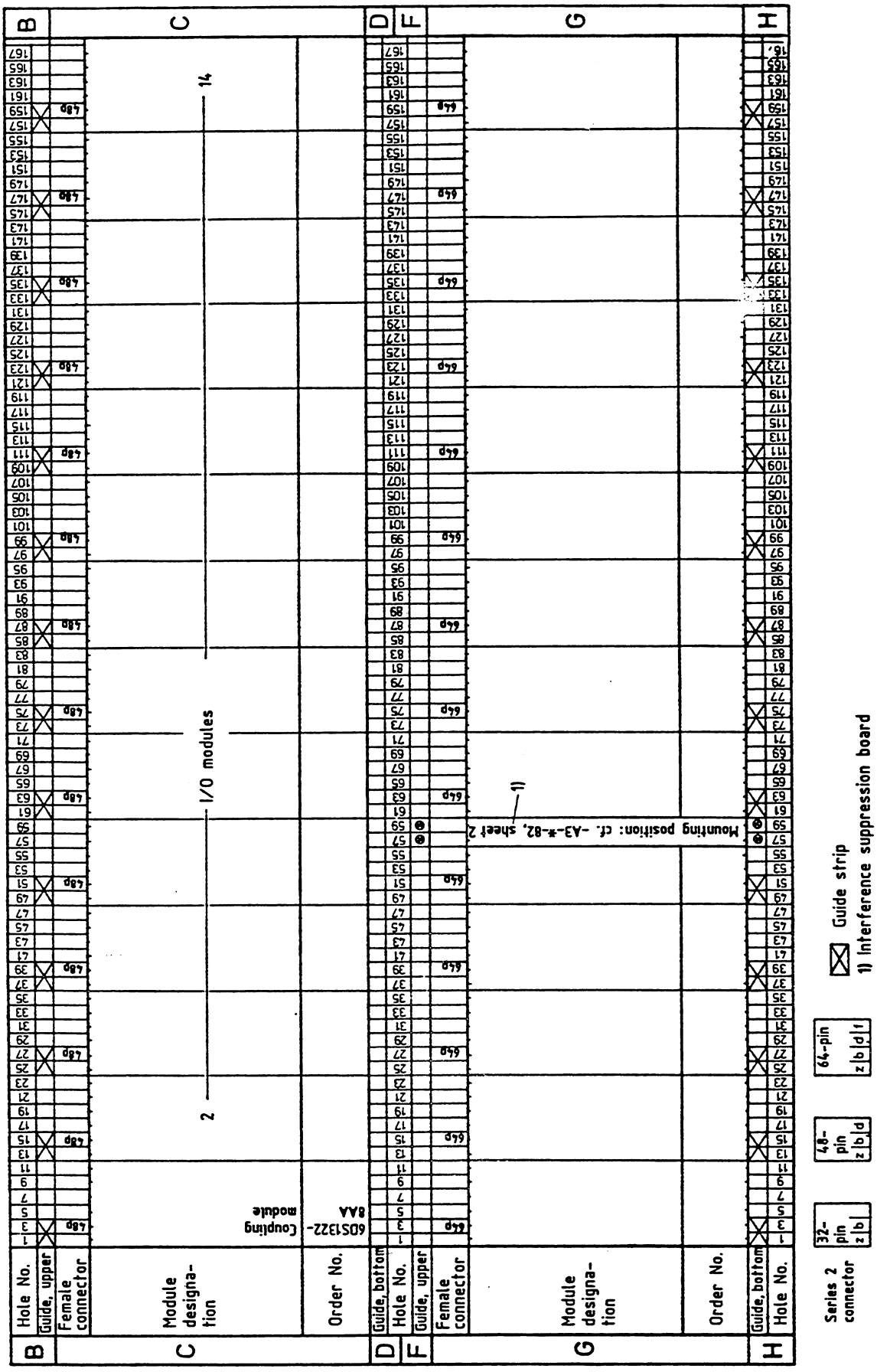


Fig. 3.7 Slots in module subrack ES 100 K

SIEMENS

Siemens Aktiengesellschaft

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Order from: Gerätewerk Karlsruhe

Printed in the Federal Republic of Germany

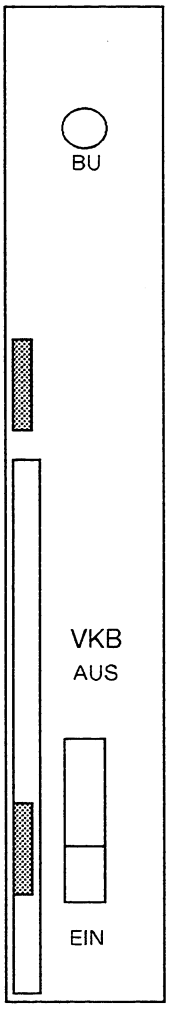
SIEMENS

TELEPERM M

Comparator Coupler Module

6DS1 142-8AA

Technical Description C79000-T8076-C345-02



0 Abbreviations

AS 235	TELEPERM M AS 235 automation system
AS 235 H	Fault-tolerant 1-out-of-2 TELEPERM M AS 235 automation system
BE	Binary input module
BKA1	Operator input channel interface module 1
BKA2	Operator input channel interface module 2
CPU	Central processing unit (the module)
DMA	Direct memory access
DG	Diagnostic unit
DGA	Diagnostic unit interface module
E/A	Input and output (I/O)
EABA1	I/O bus interface module 1
EABA2	I/O bus interface module 2
I II	Identification numbers (Roman numerals) of the redundant subsystems (redundancies) within a multi-redundant system.
EAVU	I/O comparator and switchover module
INT-BE	Interrupt-generating binary input module (group interrupt module, SF61)
MDA	Mini floppy disk interface module
MEMR-N	Peripheral bus read signal
MEMW-N	Peripheral bus write signal
N8-H	Local bus interface module
PESPA	Peripheral memory area A
PESPB	Peripheral memory area B
RDY-N	Acknowledgement signal from an addressed unit (module)
RR-N	Memory bus read signal
SAR	Memory address
SB	Synchronization module
SEP	Standard plug-in station
SP	Memory module
VKB	Comparator coupler module
WR-N	Memory bus write signal
ZE	Central processing unit
ZT	Central unit (CPU I and CPU II)

1 Application

The comparator coupler module (VKB) is used in the fault-tolerant TELEPERM M AS 235 H "1-out-of-2 automation system".
It performs special tasks which enable the two central processing units to operate in independent and synchronous mode.

The VKB module
- compares the address, data and control signals of both CPUs in order to facilitate swift fault detection, and issues an error message to the CPU when a malfunction has been detected;
- transfers, during a backup operation [1], all read data from memories and registers to the memories and registers of the second central processing unit;
- supports software-controlled troubleshooting
- routes any access from N8-H and MDA from the master CPU to the standby CPU.

[1] "Backup" describes the process in which the internal states (memory contents, interrupt and timer values, etc.) of the master CPU are transferred to the passive CPU after both CPUs have been synchronized. The internal states of both CPUs are identical after this process has been terminated.

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2 Design

The VKB module is a printed circuit board of double-height Euroformat (233 x 160 mm) with a 15-mm wide front panel (1 standard plug-in station).
The central unit consists of two central processing units (CPU I and CPU II); the VKB module is installed between these two CPUs (Fig. 1).

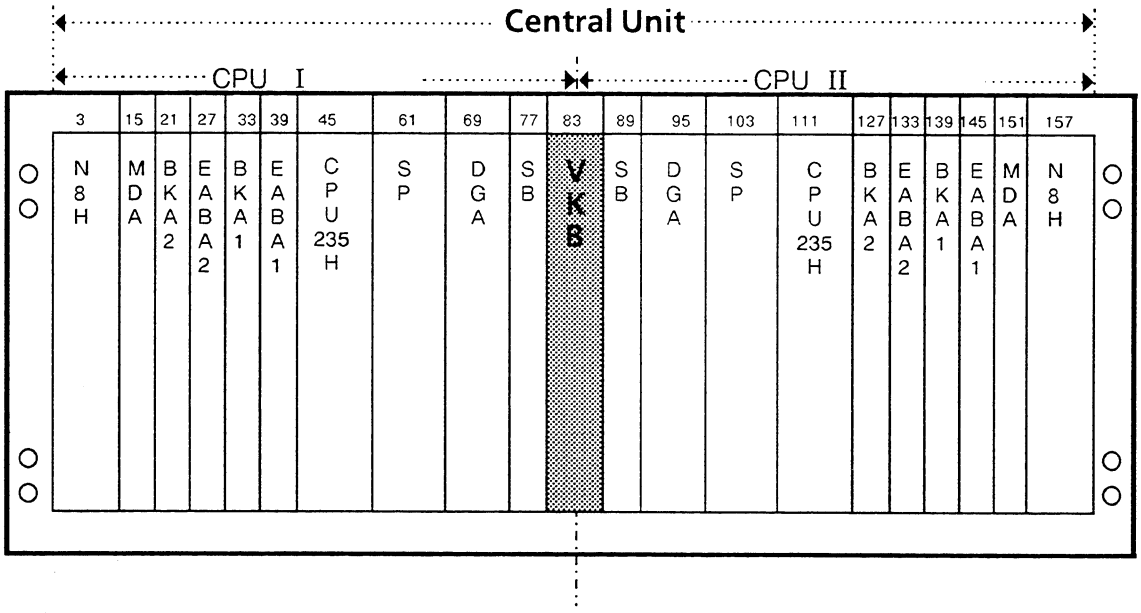


Fig.1 Central unit structure

The module is installed in slot 83 of the central unit subrack. It is connected to the backplane and the other modules via two male edge connectors:
- 96-way X1 backplane connector (upper edge connector)
- 96-way X2 backplane connector (lower edge connector)

The comparator and coupling function of the VKB necessitate special connections to both central processing units.
The following main signal groups are connected to the VKB module (cf. Fig. 3):

- peripheral address bus from CPU I and CPU II, for coupling and comparison;
- peripheral data bus from CPU I and CPU II, for coupling and comparison;
- memory data bus from CPU I and CPU II, for coupling and comparison;
- bus control signals from CPU I and CPU II, for coupling, comparison, and bus driver control;
- private lines to the synchronization modules (SB) of both CPUs.

Only one VKB is used in each central unit. The module features two internal channels in order to guarantee independence of the CPUs connected. All functions exist twice on the VKB module and are allocated to the CPUs accordingly.

The front panel contains

- one switch (VKB ON/OFF)
- one pushbutton (BU)

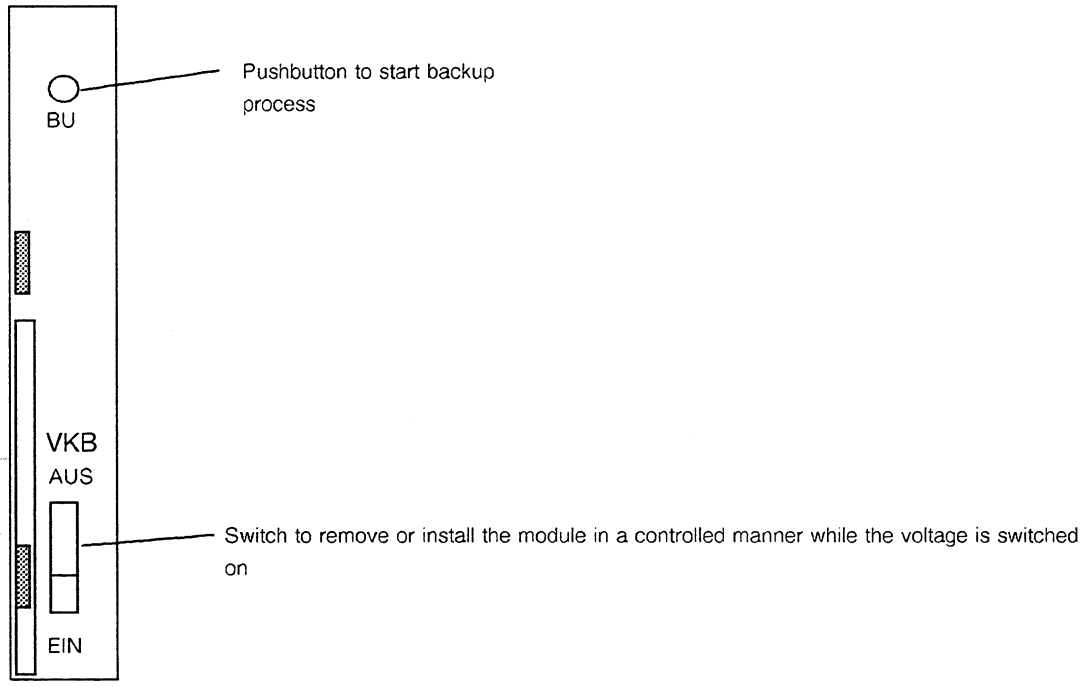
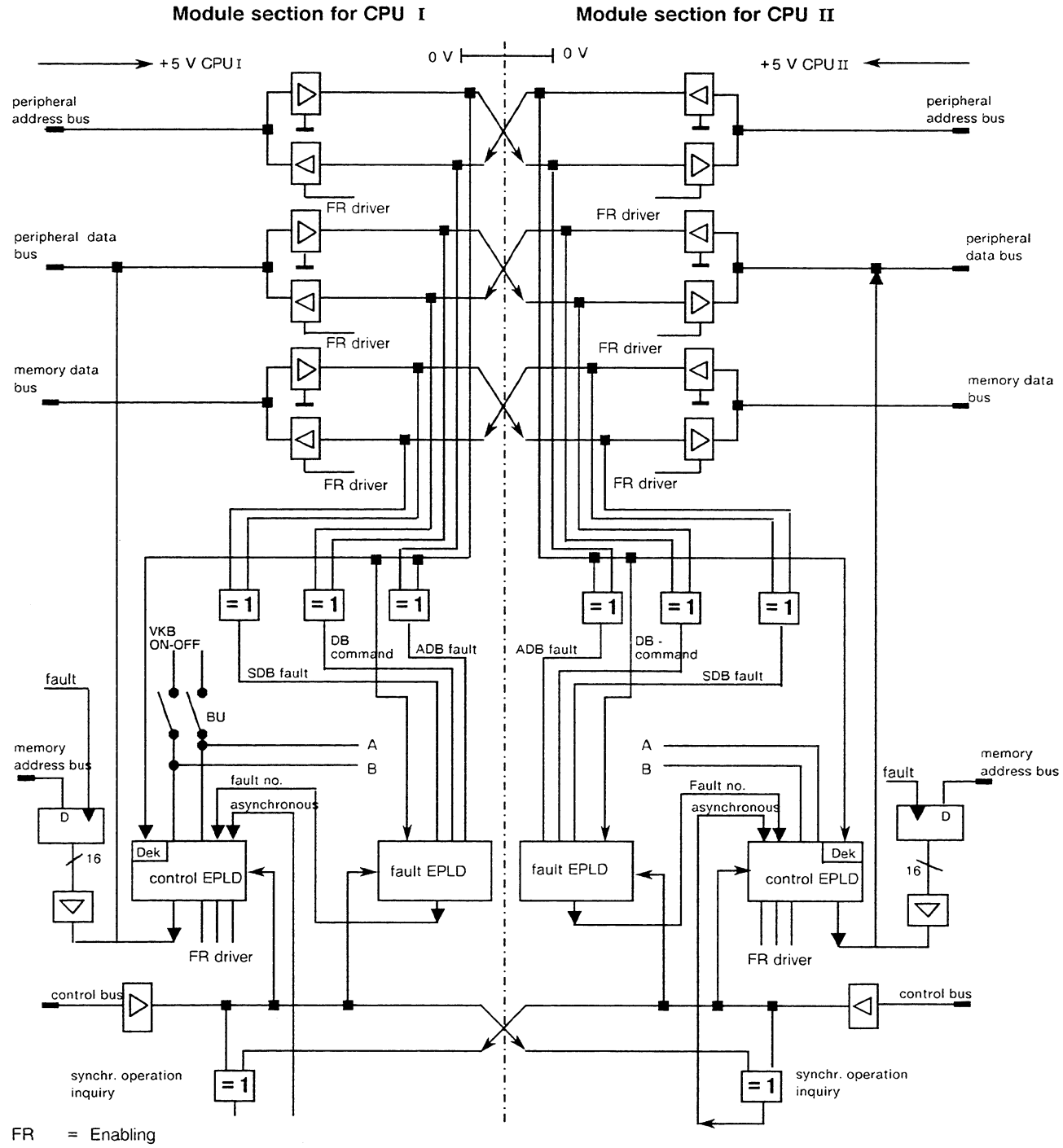


Fig. 2 VKB front panel

3 Method of Operation



FR = Enabling

= 1 = Comparator

EPLD = Erasable Programmable Logic Device

ADB = Address bit

DB = Data bit

SDB = Memory data bit

Fig. 3 Block diagram of the comparator coupling module (VKB)

3.1 Peripheral Bus Link

The peripheral bus consists of:

- address bits 0 to 15,
- data bits 0 to 7, and
- control signals (MEMR-N, MEMW-N, RDY-N, ...)

The peripheral bus is routed to CPU I or CPU II, depending on the central unit status [1]. Routing of control signals is performed by the synchronization module, not by the VKB. The buses are only enabled if both CPUs are operating synchronously and only in the cases mentioned below [1]. All VBK links are disabled in asynchronous operation.

The peripheral address bus is enabled:

- between master and standby CPU during DMA [2].

The peripheral data bus is enabled:

- from the master to the standby CPU during DMA write operation
- from CPU I to CPU II during operator input channel 1 read operation (address 9F8XH)
- from CPU II to CPU I during operator input channel 2 read operation (address AF8XH)
- from CPU I to CPU II during I/O bus interfaces 1 and 2 read operation (addresses 4FDDH, 8FDDH, 4FDAH)
- from the master to the standby CPU during N8-H read operation (address 8FDEH)
- from the master to the standby CPU during MDA read operation (addresses 8FE0H...8FE9H and 8FF0H...8FF2H)

Each CPU reads the register contents of its own modules if the CPUs are operating in asynchronous mode.

All functions of the AS 235 system are available in a passive CPU, apart from communication via the CS 275 bus system (N8-H has been de-parameterized). The passive CPU cannot access the extension units.

3.2 Memory Data Bus Link

The memory data bus is only enabled during a read-memory operation in backup mode in order to update the memory of the passive CPU. Both CPUs operate synchronously (enabling is only possible in synchronous operation). The drivers are automatically disabled once backup has been terminated.

[1] see Chapter 3.1 in the Operating Instructions C79000-B8076-C293-02
[2] DMA = direct memory access
Data exchange between peripheral units (here N8-H and MDA) and main memory (SP).

3.3 Comparator Functions

The VKB compares address, data and control signals of the central processing units in order to ensure swift fault detection.

The following signals are compared:

1. Peripheral address bus (ADB 0...15), valid with the positive edge of MEMR-N or MEMW-N.

2. Peripheral data bus (DB 0...7), valid with the positive edge of MEMR-N or MEMW-N.

3. Memory data bus (SBD 0...SDB 15), valid with the positive edge of RR-N or WR-N

4. MEMR-N and MEMW-N of both CPUs for deviations of more than 30 ns.

5. RR-N and WR-N of both CPUs for deviations of more than 30 ns.

3.4 Fault Finding Support

The VKB contains functions which accelerate and facilitate fault finding after fault detection. The module produces a snapshot of the bus states at the moment of fault detection which contains the following facts:

1. The fault was detected during a memory bus read or write operation.
2. States of the memory bus address bits 9...24 at the moment when the fault occurred.
3. Access to the modules SB, VKB, EABA1, EABA2, BED1, BED2, EAVUs, group interrupt module, I/O modules in the I/O area 1 (PESPA) and I/O modules in the I/O area 2 (PESPB) at the moment when the fault occurred (coded information is available, see Fig. 4).
4. The fault was detected during a peripheral bus read or write operation.
5. Memory data bus not identical.
6. Peripheral data bus not identical.
7. Peripheral address bus not identical.
8. Fault reported from I/O area 1.
9. Fault reported from I/O area 2.
10. N8-H fault.

This information can be retrieved from the VKB registers (see Chapter 3.5).

3.5 Data Transfer

Data transfer from CPU to VKB is performed via registers which are in the address range of the peripheral bus:

4FD0H...4FD3H and 4FD7H (4...H means that the addresses are within the PESPB range).

Register 1: Reading the fault type (MEMR)

Address	Bit (1-active)	Meaning
4FD0H	0	Asynchronous memory bus
	1	Asynchronous peripheral bus
	2	Faulty memory data bus
	3	Faulty peripheral address bus
	4	Faulty peripheral data bus
	5	Fault in I/O area 1
	6	Fault in I/O area 2
	7	Backup request (corresponds to register 2: bit 7)

Register 2: Reading the fault source (module)

Address	Bit (1-active)	Meaning			
4FD1H	0 1 2 3 4	The table in Fig. 5 shows the codes of 18 modules or areas			
		N8-H fault	Fault during reading1)	Fault during writing 1)	
	5	0	1	0	
	6	1	1	0	0
	7	Backup request (corresponds to register 1: bit 7)			

1) Write or read refers to the faulty peripheral or memory data bus.

The contents of registers 1 and 2 are loaded at the moment when the fault occurred (the PU5-N interrupt signal transitions from "1" to "0"). The VKB reset signal resets the contents to "0".

Register 3: Reading the memory address bus in the event of a fault

More significant memory address bits

Address	Bit	Meaning
4FD2H	0	SAR 17-N
	1	SAR 18-N
	2	SAR 19-N
	3	SAR 20-N
	4	SAR 21-N
	5	0
	6	0
	7	SAR 24-N

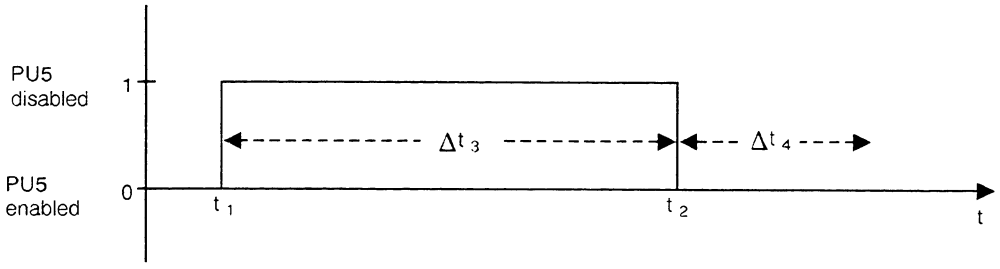
Register 5: Reading the memory address bus in the event of a fault

Less significant memory address bits

Address	Bit	Meaning
4FD7H	0	SAR 9-N
	1	SAR 10-N
	2	SAR 11-N
	3	SAR 12-N
	4	SAR 13-N
	5	SAR 14-N
	6	SAR 15-N
	7	SAR 16-N

Registers 3 and 5 are set to an undefined state at the end of the backup operation (identical for CPU I and CPU II).
Their contents is overwritten by a CPU-specific current value when PU5-N is triggered (signal transition from "1" to "0").

Register 4: Setting or resetting the fault message reset signal
Address 4FD3H



t_1 The reset signal is set by a write access to 4FD3H (data = XXH)

t_2 The reset signal is reset by a read access to 4FD3H (data = FFH)

Δt_3 Fault message output is disabled between t_1 and t_2 and the fault registers are reset. All fault indicators in the registers 1 and 2 are set to 0, i.e. the registers 4FD0 and 4FD1H contain 00H during this time.

Δt_4 Fault message output is possible from moment t_2 onwards.

Fig. 4 Setting or resetting the fault message reset signal

Module	Mo.type dec. ↓	Register 2: Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hexadecimal addresses	Remarks
	0	0	0	0	0	0		No module addressed
EABA1	1	0	0	0	0	1	PESPA#FDD,	Module was addressed at fault time
EABA2	2	0	0	0	1	0	PESPB#FDD,	Module was addressed at fault time
BKA 1	3	0	0	0	1	1	PESPA#FCX & ADB13 = 0, PESPA#F8X&ADB13 = 0,	Module was addressed at fault time
BKA 2	4	0	0	1	0	0	PESPB#FCX, PESPA#F8X & ADB13 = 1,	Module was addressed at fault time
VKB	5	0	0	1	0	1	PESPB#FD#00XX, PESPB#FD(0111)7,	Module was addressed at fault time
SB	6	0	0	1	1	0	PESPB#FD#00XX, PESPA#FD7,	Module was addressed at fault time
EAVU-1-0	7	0	0	1	1	1	PESPA#F7X,	Module was addressed at fault time
EAVU-1-1	8	0	1	0	0	0	PESPA#F6X,	Module was addressed at fault time
EAVU-1-2	9	0	1	0	0	1	PESPA#F5X,	Module was addressed at fault time
EAVU-1-3	10	0	1	0	1	0	PESPA#F4X,	Module was addressed at fault time
EAVU-2-0	11	0	1	0	1	1	PESPB#F7X,	Module was addressed at fault time
EAVU-2-1	12	0	1	1	0	0	PESPB#F6X,	Module was addressed at fault time
EAVU-2-2	13	0	1	1	0	1	PESPB#F5X,	Module was addressed at fault time
	14	0	1	1	1	0		VKB defective
EAVU-2-3	15	0	1	1	1	1	PESPB#F4X,	Module was addressed at fault time
INT-BE	16	1	0	0	0	0	PESPA#F4#0XXX,	Module was addressed at fault time
	17	1	0	0	0	1		VKB defective
	18	1	0	0	1	0		VKB defective
	19	1	0	0	1	1		VKB defective
EA-1 = I/O area 1	20	1	0	1	0	0	PESPA#F_NXX, PESPA#F#00XX#X,	Module of area was addressed at fault time
	21	1	0	1	0	1		VKB defective
	22	1	0	1	1	0		VKB defective
	23	1	0	1	1	1		VKB defective
EA-2 = I/O area 2	24	1	1	0	0	0	PESPB#F_NXX, PESPB#F#00XX#X,	Module of area was addressed at fault time
	25	1	1	0	0	1		VKB defective
	26	1	1	0	1	0		VKB defective
	27	1	1	0	1	1		VKB defective

= Delimiter

Fig. 5 Module addressed at the moment when the fault occurred

Module	Mo.Type dec. ↓	Register 2: Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hexadecimal addresses	Remarks
	28	1	1	1	0	0		VKB defective
	29	1	1	1	0	1		VKB defective
DMA-MDA/N8-H	30	1	1	1	1	0	PESPA#FDE,PESPA#FE#0XXX, PESPAFE#100X, PESPA#PESPAFE#100X, PESPA#FF000X,PESPA#FF001X,	VKB defective
	31	1	1	1	1	1		VKB defective or missing

= Delimiter

Fig. 5 Module addressed at the moment when the fault occurred (continued)

4 Operation

The following requirements must be satisfied before backup operation can be started:

- set switch to VKB ON
- the CPU to be updated must be in a passive state.

Press the "BU" pushbutton on the front panel, and start the backup procedure. Once backup has been terminated, the passive central processing unit assumes standby status (R) without disturbing the on-line process of the master CPU (see Chapter 3.1 in the Operating Instructions C79000-B8076-C293-02).

The module may be replaced while supply voltage is on without disturbing the master CPU processing. The VKB switch must first be set to OFF. This switch may only be operated when the central unit is not in M/R or R/M mode. If this is not observed, data inconsistency in the passive CPU will require CPU bootstrapping.

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5 Installation

The module contains electrostatically sensitive components. Please observe the "Guidelines for Handling Electrostatically Sensitive Devices and Modules" (contained in this manual before Section 1) during installation, commissioning and maintenance of the module.

Caution

The switch must be in "VKB-AUS" [OFF] position before the module can be removed or installed while the supply voltage is switched on.

Select M/P or P/M mode before removing the module if the central unit is in M/R or R/M mode. Press the ZRS pushbutton on a CPU or switch off the circuit breaker in a CPU rack for this purpose. It is recommended to bring the standby CPU into a passive state.

The VKB has no display. The messages and states stored by the VKB are directly routed to the VDUs.

Jumper settings are not required.

5.1 Connector Pin Assignments

Pin	c	b	a
1	2P 5 V	2P 5 V	1P 5 V
2	2P5V	M	1P 5 V
3	MEMR_NII	1P 5 V	MEMRL_NI
4	MEMW_NII		MEMW_NI
5	PESPA_II	M	PESPA_I
6	ADB0_II	SAR15NI	ADB0_I
7	PESPB_II	SAR14NI	PESPB_I
8	ADB1_II	M	ADB1_I
9	ADB2_II	SAR13NI	ADB2_I
10		ZRS_N_II	SAR19NI
11	ADB3_II	M	ADB3_I
12	SAR18NII	SAR12NI	SAR18NI
13	ADB4_II		ADB4_I
14	ADB5_II	M	ADB5_I
15	SAR19NII	ZRS_N_I	SAR20NI
16	ADB6_II	SAR15NI	ADB6_I
17	ADB7_II	M	ADB7_I
18	SAR20NII	SAR14NII	DB0_I
19	ADB8_II	DB0_II	ADB8_I
20	ADB9_II	M	ADB9_I
21	DB1_II	SAR21NI	DB1_I
22	ADB10_II	DB2_II	ADB10_I
23	ADB11_II	M	ADB11_I
24	DB3_II	SAR21NII	DB3_I
25	ADB12_II	DB4_II	ADB12_I
26	ADB13_II	DB6_II	ADB13_I
27	DB5_II	DB4_I	DB5_I
28	ADB14_II	DB2_	ADB14_I
29	ADB15_II	SAR13NII	ADB15_I
30	2P 5 V	SAR12NI	1P 5 V
31	DB7_II		DB7_I
32	DB6_II	M	

Fig. 6 VKB, X1 backplane connector, pin assignments

Pin	c	b	a
1	2P 5 V	2P 5 V	1P 5 V
2	WR_N_II	M	WR_N_I
3	M	1P 5 V	M
4	RR_N_II	FN8_N_I	RR_N_I
5	2P 5 V	M	1P 5 V
6	BUI_N_II	FN8_N_II	BUI_N_I
7	DG1_N_I	SAR9NI	DG1_N_II
8	DG2_N_I	M	DG2_N_II
9	SYNC_NII	SAR24NI	SYNC_NI
10	KOPP_NII	SAR12NI	KOPP_NI
11	SYEA1NII	M	SYEA1NI
12	SYEA2NII	PU5S_NII	SYEA2NI
13	M	SAR9NII	M
14	D15_N_II	M	D15_N_I
15	D14_N_II	PU5S_NI	D14_N_I
16	D13_N_II	SAR24NII	D13_N_I
17	D12_N_II	M	D12_N_I
18	D11_N_II	SAR10NI	D11_N_I
19	D10_N_II	HLDA_NII	D10_N_I
20	D9_N_II	M	D9_N_I
21	D8_N_II	HLDA_NI	D8_N_I
22	D7_N_II	SAR11NII	D7_N_I
23	D6_N_II	M	D6_N_I
24	D5_N_II	FSIG1NI	D5_N_I
25	D4_N_II	FSIG2NI	D4_N_I
26	D3_N_II	SAR16NI	D3_N_I
27	D2_N_II	M	D2_N_I
28	D1_N_II	FSIG1NII	D1_N_I
29	D0_N_II	FSIG2NII	D0_N_I
30	2P 5 V	SAR16NII	1P 5 V
31	MAST-NII	SAR10NII	MAST-NI
32	SAR17NII	M	SAR17NI

Fig. 7 VKB, X2 backplane connector, pin assignments

6 Technical Data

Supply voltage:	+5 V from CPU I +/-0.25 V +5 V from CPU II +/-0.25 V
Max. current consumption:	500 mA on CPU I side 500 mA on CPU II side

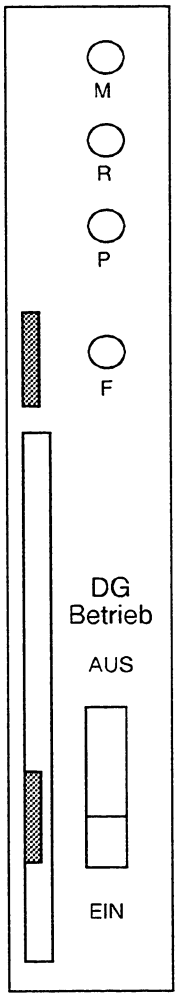
SIEMENS

TELEPERM M

Synchronization Module

6DS1 143-8AA

Technical Description C79000-T8076-C344-02



0 Abbreviations

AS 235	TELEPERM M AS 235 automation system
AS 235 H	Fault-tolerant 1-out-of-2 TELEPERM M AS 235 automation system
BKA 1	Operator input channel interface module 1
BKA 2	Operator input channel interface module 2
CPU	Central processing unit (the module)
DG	Diagnostic unit
DGA	Diagnostic unit interface module
E/A	Input and output (I/O)
EABA1	I/O bus interface module 1
EABA2	I/O bus interface module 2
EAVU	I/O comparator and switchover module
HW	Hardware
I II	Identification numbers (Roman numerals) of the redundant subsystems (redundancies) within a multi-redundant system.
LED	Light emitting diode
MDA	Mini floppy disk interface module
MUA-N	Memory unit available (control signal)
N8-H	Local bus interface module
OS	Operator control and monitoring system
PUn	Interrupt signal: process interruption n
PU5	Standard: free PU no. 5; exclusively used for redundancy-related purposes in the 235 product family
RDY	Ready signal
RMS-N	Return signal from memory or peripherals
SB	Synchronization module
SP	Memory module
SV	Power supply unit
SW	Software
VKB	Comparator coupler module
ZE	Central processing unit
ZRS	Central reset signal from the power supply unit
ZT	Central unit (CPU I and CPU II)

1 Application

The synchronization module (SB) is used in the fault-tolerant TELEPERM M AS 235 H "1-out-of-2 automation system".
It performs all synchronization tasks that are required to establish or maintain synchronous operation.

The SB
- guarantees synchronous operation of the CPUs
- generates the processor and system clock pulses
- synchronizes the basic clock pulses of the CPU
- synchronizes read and write data
- synchronizes interrupt signals
- supplies CPU status messages
- controls initial synchronization.

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2 Design

The SB module is a printed circuit board of double-height Euroformat (233 x 160 mm) with a 15-mm wide front panel (1 standard plug-in station).
The central unit consists of two central processing units (CPU I and CPU II) with two SB modules installed between these two CPUs (Fig. 1).

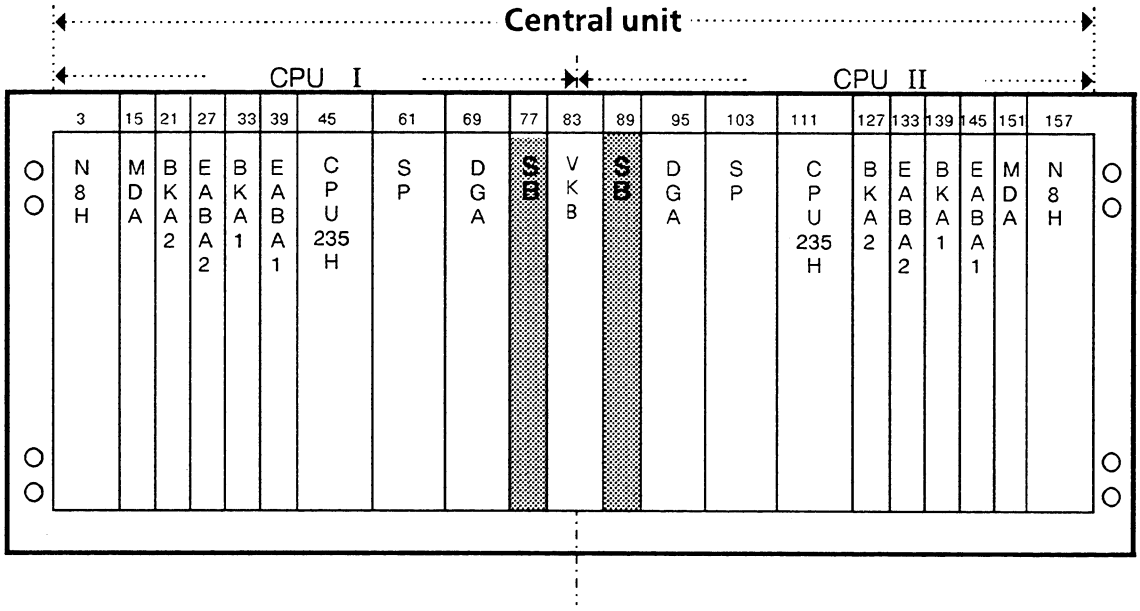


Fig. 1 Central unit structure

The modules are installed in slots 77 and 89 of the central unit subrack.
They are connected to the backplane and the other modules via two male edge connectors:
- 96-way X1 backplane connector (upper edge connector)
- 96-way X2 backplane connector (lower edge connector)

In addition, there are direct connections between the two SB modules for synchronization purposes.

The following main signal groups are connected to the SB module:
- peripheral address bus from the associated CPU, for address decoding;
- peripheral data bus from the associated CPU, for data transfer;
- control signals from and to the associated CPU;
- interrupts PU0...PU8, for synchronization;
- DMA[1] control signals from N8-H and MDA, for synchronization;
- signal exchange with the SB module of the other CPU (status, general information and synchronization signals).

[1] DMA = direct memory access
Information exchange between peripheral units (here N8-H and MDA) and main memory (SP).

The front panel contains :

- four LEDs
- one switch

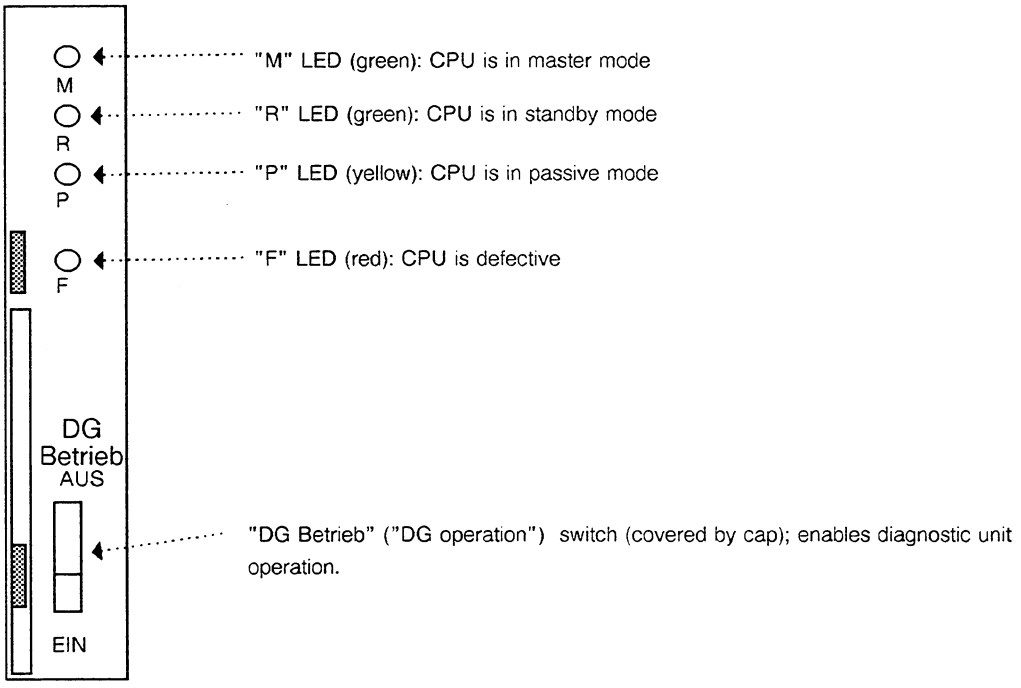
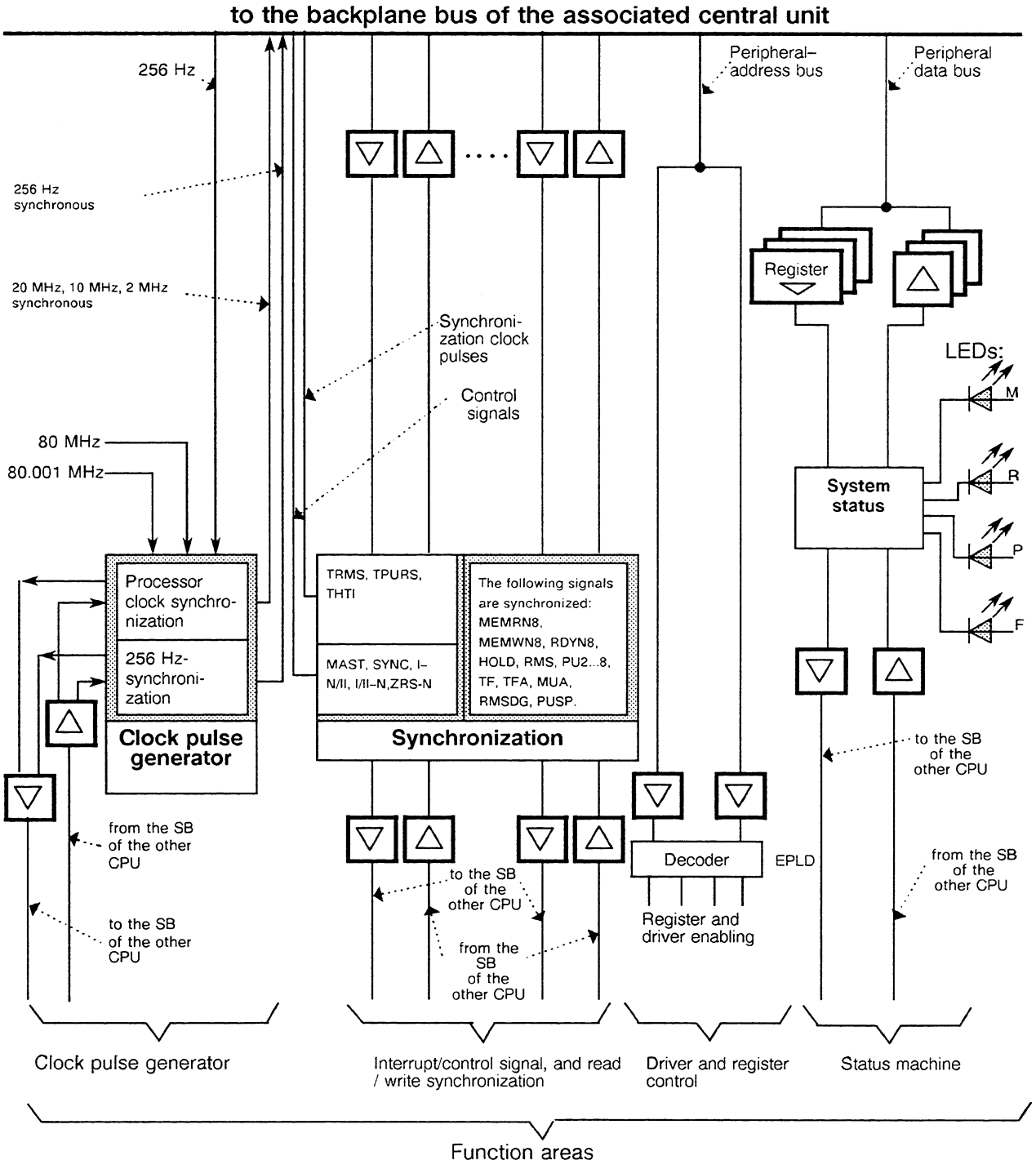


Fig. 2 SB Front panel

3 Method of Operation

The SB tasks are subdivided into five function areas (see Fig. 3):

1. Clock pulse generator function area
2. Read/write synchronization function area
3. Interrupt and control signal synchronization function area
4. Status machine function area
5. Driver and register control function area



EPLD = Erasable programmable logic device

Fig. 3 Block diagram of the synchronization module (SB)

3.1 Clock Pulse Generator Function Area

This function area is subdivided into three different parts:

1. Generation of the two synchronous 20/10-MHz processor clock pulses.
2. Generation of the two synchronous 2-MHz system clock pulses.
3. Synchronization of the two 256-Hz basic clock pulses (PU1) of the CPU.

3.1.1 Generation of the Two Synchronous 20/10-MHz Processor Clock Pulses

A special clock pulse generator circuit receives two basic clock pulses (80.0 MHz and 80.001 MHz). The 80.0-MHz basic clock pulse is activated in CPU I, the 80.001-MHz basic clock pulse in CPU II. Both basic clock pulses are divided to yield 20 MHz. The faster basic clock pulse also yields exactly 20 MHz due to synchronization. Dividing the 20-MHz clock pulse by 2 yields the 10-MHz clock pulse. The 10/20-MHz processor clock pulses are issued to the processor modules. They are exactly identical in terms of phase and frequency.

3.1.2 Generation of the Two Synchronous 2-MHz System Clock Pulses

The synchronous 2-MHz system clock pulses are gained by dividing the two 10-MHz processor clock pulses (5:1).

3.1.3 Synchronization of the Two 256-Hz CPU Basic Clock Pulses (PU1)

The 256-Hz CPU basic clock pulses are synchronized by special synchronization circuits on the SB module. These clock pulses are kept synchronous by monitoring the 256-Hz CPU output clock pulses and synchronizing the internal CPU divider stages according to this result. The 256-Hz clock pulses are phased with the processor clock pulses and fed back to the CPUs as a time alarm PU1. Both CPUs then react in the same way (and synchronously).

3.2 Read/Write Synchronization Function Area

The following signals are synchronized by the SB module in order to maintain synchronous CPU operation:

- RDY-N
- MUA-N
- RMS-N.

The acknowledgement signal RDY-N of an access via the peripheral bus is phased with the processor clock pulse and synchronized by waiting for the RDY-N from both CPUs. Once both signals are active and pending, synchronous RDY-N signals are transferred to the processor modules. The CPUs become asynchronous if RDY-N from one CPU is missing. The CPU with the missing RDY-N issues a corresponding error message while the faultless CPU continues its normal operation.
Mutual synchronization is not required for the acknowledgement signals MUA-N and RMS-N (access via the memory bus). The SB module guarantees that synchronous CPU operation is maintained by acknowledgement signal synchronization with the processor clock pulses.

3.3 Interrupt and Control Signal Synchronization Function Area

All interrupt signals that are significant for synchronous CPU operation (PUs, processor interruptions) are synchronized on the SB module. These are:

Interrupt signal	Meaning	Comment
PU1	256 Hz time impulse	see Chap. 3.1.3
PU2	Interrupt of the serial interfaces from operator input channel 1	1)
PU3	Interrupt of the serial interfaces from operator input channel 2	2)
PU4	Process alarm	3)
PU6	Time synchronization impulse from master clock	4)
PU7	Interrupt from N8-H	5)
PU8	Interrupt from MDA	6)
HOLD	DMA request from N8-H or MDA	7)

1) PU2 is phased with the TPURS processor clock pulse. In synchronous mode, the phased PU2 is coupled from CPU I to CPU II and fed to the processor by both SB modules. The CPUs react synchronously. Coupling is not performed in asynchronous operation; the PU2 of the local operator input channel is enabled.

2) PU3 responds basically in the same manner as PU2; the difference is that PU3 is coupled from CPU II to CPU I in synchronous mode.

3) PU4 is phased with the TEAINT clock pulse before it is output and branched by the EAVUs. The SB also utilizes this clock pulse for phasing PU4. This eliminates propagation delays and the PU4 signals are synchronous when they are fed to the CPUs.

4) PU6 is phased with the TPURS clock pulse. The SB module in CPU I couples PU6 in synchronous CPU mode to the CPU module in CPU II, from where it is issued to the CPUs. PU6 of the local operator input channel is enabled in asynchronous operation.

5) As PU4, with PU7 and TPURS as clock pulse.

6) As PU4, with PU8 and TPURS as clock pulse.

7) PU5 is phased with the THTi clock pulse and, in synchronous operation, coupled by the SB in the master CPU to the SB in the standby CPU, so that it is issued synchronously by both CPUs. PU5 is only fed to the own CPU if the CPUs are not in synchronous operation.

The following additional DG signals are synchronized on the SB module in order to be able to utilize the diagnostic unit in synchronous operation:
- TFS-N
- TFAS-N
- PUSPS-N
- RMS-N (from DG).

The diagnostic unit interface (DGA) first transfers the unsynchronized signals to the corresponding SB module where they are phased with the THTi or TPURS clock pulses and the processor clock pulse. The SB in CPU I sends its signals to the SB in CPU II in order to enable both SBs to feed synchronous signals to the CPUs. This means that the DG must always be connected to CPU I if it is to be utilized in the synchronous central unit. All activities start here. A second DG connected to CPU II cannot become active in the synchronous central unit. Both DGs service their associated CPUs in asynchronous mode.

3.4 Status Machine Function Area

The status machine in the SB module supports the system software in computing the ZT status. ZT status describes the status of the two CPUs with respect to the application program execution. ZT status can be, for example:
CPU I/CPU II = master/standby (M/R), master/passive (M/P), ...,

A CPU can assume the following states:

Master	-	(M);	only this CPU can access process outputs;
Standby	-	(R);	this CPU is synchronous with the master CPU;
Passive	-	(P);	this CPU is completely disconnected from the process;
Fault	-	(F);	this CPU is defective or starting.

Each CPU computes these states for both CPUs and transfers them via registers to the SB hardware. The software reads the current states of both CPUs from a register and issues appropriate messages.

Four LEDs on the front panel indicate the different states. Backup status is indicated by the R and P LEDs lighting up simultaneously.

3.5 Driver and Register Control Function Area

The SB register addresses are decoded in this function area on the basis of the address on the peripheral bus and the MEMR-N and MEMW-N control signals (see Chapter 3.6).
Backup is controlled by addressing specific locations (data is irrelevant). Once backup [1] has started, register 5 in the CPU that is to be updated disables the RDY-N acknowledgement signal until the address of register 5 is in the master CPU too (moment of hardware synchronization). Due to RDY-N synchronization, both CPUs can continue their operation synchronously.

Furthermore, addresses are decoded in which data must be coupled from CPU I to CPU II or vice versa. This is necessary in case of a backup in order to branch specific single-channel data. The SB modules disable the output of the control signals MEM-R (peripheral bus) and RR-N (memory bus) in the CPU if data from the other CPU is transferred.

[1] "Backup" describes the process in which the internal states (memory contents, interrupt and timer values, etc.) of the master CPU are transferred to the passive CPU after both CPUs have been synchronized. The internal states of both CPUs are identical after this process has been terminated.

3.6 Data Transfer

Data transfer from CPU to SB is performed via registers which are in the address range of the peripheral bus:

8FD0H...8FD3H and 8FD7H (8...H means that the addresses are within the PESPA range).

Register 1: read ZT status

Address	Bit (1-active)	Meaning	Comment
8FD0H	0	CPU I is master CPU	0, if CPU I is de-energized
	1	CPU I is standby CPU	0, if CPU I is de-energized
	2	CPU I is passive	0, if CPU I is de-energized
	3	CPU I is starting up	0, if CPU I is de-energized
	4	CPU II is master CPU	0, if CPU II is de-energized
	5	CPU II is standby CPU	0, if CPU II is de-energized
	6	CPU II is passive	0, if CPU II is de-energized
	7	CPU II is starting up	0, if CPU II is de-energized

Register 2: write ZT status

Address	Bit (1-active)	Meaning
8FD0H	0	CPU I becomes master
	1	CPU I becomes standby
	2	CPU I becomes passive
	3	CPU I is starting up
	4	CPU II is master
	5	CPU II is standby
	6	CPU II is passive
	7	CPU II is starting up

Register 3: read mailbox (information comes from the SB of the other CPU)

Address	Bit (1-active:)	Mean-ing	Comment
8FD1H	0	M0;	Bit 0 = 0 if the other CPU is de-energized
	1	M1;	Bit 1 = 0 if the other CPU is de-energized
	2	M2;	Bit 2 = 0 if the other CPU is de-energized
	3	M3;	Bit 3 = 0 if the other CPU is de-energized
	4	M4;	Bit 4 = 0 if the other CPU is de-energized
	5	M5;	Bit 5 = 0 if the other CPU is de-energized
	0-active:		
	6	0	
	7	0	

M0... M5 = alarm bits 0...5

Register 4: write mailbox (information goes to the SB of the other CPU)

Address	Bit (1-active:)	Meaning
8FD1H	0	M0
	1	M1
	2	M2
	3	M3
	4	M4
	5	M5
	6	-----
	0-active:	
	7	Fault in own CPU, fault LED is set by writing a binary "0".

Register 5: start backup

Address	Meaning
8FD2H	Write data: XXH; the access has only a control function.

Register 6: terminate backup

Address	Meaning
8FD3H	Write data: XXH; the access has only a control function.

Register 7: read CPU identification

Address	Bit	Meaning	
		CPU I	CPU II
4FD1H	0	1	0
	1	0	1
	2	1	
	3	1	
	4	1	
	5	1	
	6	1	
	7	0 = CPUs run synchronously	

The VBK responds to a discrepancy if this register is read, and the CPUs run asynchronously afterwards.

4 Operation

Caution

If the diagnostic unit (DG) is to be used for analyzing a CPU of the AS 235 H system, the "DG-BETRIEB" [DG mode] switch on the SB must be in position "EIN" [ON]. The switches on both SB modules must always have the same position in synchronous operation. Asynchronous operation in DG mode results if the switches are set to different positions. For synchronous operation, the DGA must always be installed in CPU I; both SB switches must be in position "EIN". The DGA in CPU I can then communicate with the central unit. All DG functions are available in synchronous CPU operation, except ZRS. ZRS only acts upon one CPU, even if the switch on the SB is in "AUS" [OFF] position.
Always press the pushbutton on the DGA front panel to reset the DGA before changing the switch position on an SB module (this clears pending jobs from the DG to the CPU).

In order to avoid disturbances of the redundant operation by a fault from "one" source (due to branching/synchronizing the DG control signals), the DGA switches on the SB module should be in "AUS" [OFF] position if DG mode is not absolutely necessary.

Please note the instructions in the DGA description when the DGA is to be installed or removed while the voltage is switched on (possible in synchronous operation).

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5 Installation

The module contains electrostatically sensitive components. Please observe the "Guidelines for Handling Electrostatically Sensitive Devices and Modules" (contained in this manual before Section 1) during installation, commissioning and maintenance of the module.

Caution

The module may only be removed or installed after the power supply of the corresponding CPU has been switched off.

5.1 Connector Pin Assignments

Pin	c	b	a
1	1P 5 V	M	TTLE02I
2	1P5V	PESPA_I	M
3	MEMR_NI	PESPB_I	M10_I
4	MEMW_NI	ADB13_I	MI_Q
5	1P5V	PU1S_NI	M
6	ADB0_I	M	RI_Q
7	PU3S_NI	PU2S_NI	PI_Q
8	1P5V	MR220NI	MRN8_NI
9	ADB1_I	M	AI_Q
10	LPK1_I	PU4S_NI	MWN8_NI
11	1P5V	RGB_I	M
12	TPAB_Q	M	RDY_N_I
13	ADB2_I	RDYS_NI	DB0_I
14	1P5V	RMSDGANQ	RMSDGZNQ
15	ADB3_I	M	PU6S_NI
16	PU2_N_I	PU7S_NI	PU6_N_I
17	ADB4_I	DB1_I	M
18	PU3_N_I	DB2_I	PU8S_NI
19	ADB5_I	PUSPA_NQ	PUSPZ_NQ
20	1P5V	PU8_N_I	DB3_I
21	ADB6_I	M	TFAS_NI
22	PU4_N_I	TPZU_Q	TFS_N_I
23	ADB7_I	DB4_I	M
24	ADB8_I	MWA_N_Q	MWZ_N_Q
25	RMSM_NI	MRA_N_Q	MRZ_N_Q
26	1P5V	RA_N_Q	RZ_N_Q
27	ADB9_I	M	DB5_I
28	ADB10_I	DB6_I	TFA_N_I
29	ADB11_I	PU6AB_NQ	PU6ZU_NQ
30	DB7_I	RRM_N_I	TF_N_I
31	1P5V	HLDS_NI	M
32	M20_I	M	ZRS_N_I

Fig. 4 SB, X1 backplane connector, pin assignments

Pin	c	b	a
1	1P5V	M	ES2_NI
2	1P5V	WR_N_I	M
3	BUI_N_I	MUAM_NI	
4	RR_N_I	MUA_N_I	
5	1P5V	M	M
6	PU7_N_I	TSAB_Q	PUSP_NI
7	TJAB_Q	RMS_N_I	PUSPSNI
8	1P5V	PU2AB_NQ	PU2ZU_NQ
9	SYNC_NI	M	M
10	KOPP_NI	ZU1_Q	AB1_Q
11	TJZU_Q	ZU2_Q	AB2_Q
12	TJZU_Q	ZU3_Q	AB3_Q
13	1P5V	ZU4_Q	AB4_Q
14	IZII_NI	ZU5_Q	AB5_Q
15	TPURS-I	M	M
16	INZII_I	ZU6_Q	AB6_Q
17	HT_N_I	TFAB_N_I	TFZU_N_Q
18	1P5V	TFAAB_NQ	TFAZU_N_Q
19		PU3AB_NQ	PU3ZU_NQ
20	HLDA_NI	HLDAZNI	ES1_NI
21	MI_Q	HOLDA_NQ	HOLDZ_NQ
22	1P5V	N8AB_N_Q	N8ZU_N_Q
23	RI_Q	MFAAB_NQ	MFAZU_NQ
24	PI_Q	M	M
25	AI_Q	DIV4ZUI	DIV4ABI
26	MII_Q	TTAB_Q	TTZU_Q
27	RII_Q	MUAAB_NQ	MUAZU_NQ
28	1P5V	PU1_N_II	TEAVI1I
29	PII_Q	SQVZ_NI	TEAVI2I
30	AII_Q	M	M
31	1P5V	MAST_NI	MAST1NI
32	PU1_N_I	HLD_NI	MAST2NI

Fig. 5 SB, X2 backplane connector, pin assignments

6 Technical Data

Supply voltage:	+5 V +/-0.25 V
Max. current consumption:	1 A

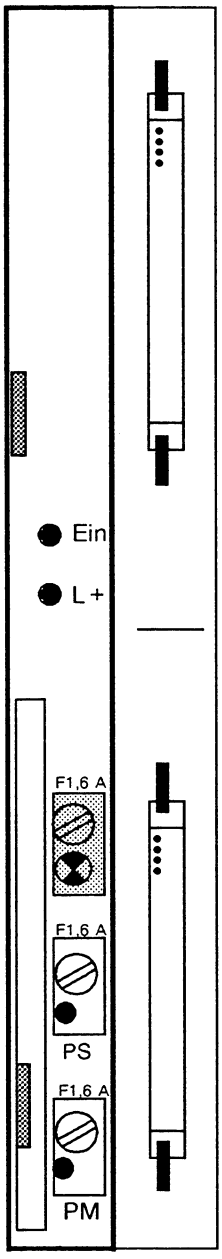
SIEMENS

TELEPERM M

I/O Comparator and Switchover Module (EAVU)

6DS1 144-8AA

Technical Description C79000-T8076-C343-02



Contents

0 Abbreviations

I II Identification numbers (Roman numerals) of the redundant subsystems (redundancies) within a multi-redundant system.

AA	Analog output module
AE	Analog input module
AF	Remote bus connector board
AS	Automation system
AZR	Flag register of the CPU 235 H
B	Backup (CPU status = synchronization and updating)
BA	Binary output module
B&B	Operator control and monitoring
BE	Binary input module
BGT	Subrack
BKA	Operator input channel interface module
BKU	Operator input channel switchover (for AS 235 H: video relay and adapter cable)
BL	Blinking clock-pulse generator module
BS	Blinking voltage (24-V signal, 0 V = ON)
CS275	LAN for linking TELEPERM M systems
CPKL	CPU operational (CPKL = 1 means reset)
CPU235H	Central processing unit 235 H
DF	Dynamic group error output (24-V impulse)
DG	Diagnostic unit
DGA	Diagnostic unit interface module
DMA	Direct memory access
E...	Signal names beginning with an E often refer to the I/O bus
E/A	Input and output (I/O)
EABA	I/O bus interface module
EANK	One-out-of-n code; TELEPERM M procedure for detecting I/O addresses with no or multiple assignments
EAVU	I/O comparator and switchover module
EE	Extension unit
EPDL	Ultraviolet erasable programmable logic circuit
EPROM	Ultraviolet erasable programmable read-only memory
ES	Extension cabinet
F	Fail-safe (by redundancy)
FDC	Floppy-disk controller
FIFO	First in first out (queuing hierarchy)
FMD	Dynamic error message
FMS	Static error message
GE	Basic unit (subrack for CPU I or CPU II)
GS	Basic cabinet
H	Fault-tolerant (by redundancy)
HC	High-speed CMOS
HF	Both fail-safe and fault-tolerant
HW	Hardware

INT1-INT4	TELEPERM M I/O interrupts 1 to 4 (AS 235 only utilizes interrupt INT1 which may only be raised by an SF61 group interrupt module)
LAN	Local area network; mid-range communications bus
Latch	Buffer
L +	Positive supply voltage, 24 V rated value
LED	Light emitting diode
LOES	Clearing the user memory by entering "LOES;"
LS	Low-power Schottky
LTM	I&C alarm
M	Earth, negative pole
MDA	Mini floppy disk interface module
MDE	Mini floppy disk unit
MDT	Mean downtime (mean time between the occurrence of a failure and operation restart)
ML	Alarm logic module
MTBF	Mean time between failures (mean time between two failure occurrences, i.e. faultless interval)
MZ	Off-load earth, reference potential for analog inputs
N8	TELEPERM M local bus interface, 8 bits on CS 275 bus system
N8-H	N8 in a fault-tolerant 1-out-of-2 master reserve configuration of a redundant automation system
NAU	Power failure
NV	Local bus distributor
OC	Open collector driver or line (normally for wired-AND or, in negative logic, wired-OR (low active) connections)
OS	Operator control and monitoring system
P	Passive (asynchronous CPU status; no N8-H accesses etc.)
P..__I P..II	Signal names beginning with a P often refer to the I/O buses between EABA modules and an EAVU module
PBE	Testable binary input module
PBT	Process communication keyboard (TELEPERM M AS accessory)
PE	Protective earth, cabinet potential
PESP	Peripheral memory area (TELEPERM M signal for memory-mapped I/O)
PESPA	PESP area which includes SF0...SF61 of EABA1
PESPB	PESP area which includes SF100...SF160 of EABA2
PLAD	Location address in the I/O range (address bits 11 to 6)
PUM	Buffer module
PRA	Testable relay output module
PROM	Programmable read-only memory
PM	L + for alarm purposes
PS	L + for logic "1" of 24-V inputs
PÜ	L + for monitoring purposes
PU	Process interrupt
PU5	Standard: unassigned process interrupt No. 5 (PU5) which is exclusively used for redundancy-related purposes in the 235 product family
QVZ	Time-out during memory or peripheral access

RaAd	Rack address (address bits 11 and 10)
RAM	Random access memory
RD	Read
RDY	Ready
RDY_RCK	Ready read from the I/O buses
ROM	Read-only memory
RSOF	Software reset
SAE	Cabinet connection element
SB	Synchronization module
/(_N)	"/" before a signal name indicates negation; _N or _IN/_IIN after a signal name is used instead in a circuit diagram
SED 31	Cabinet power supply diode
SEP	Standard plug-in station in a subrack, 15.24 mm wide
SES	Cabinet power supply unit
SE	Signal interface module
SimI	One-bit EAVU output signal (24-V permanent or impulse signal, chiefly used for simulating interrupts for SF61 test)
SYNC	Synchronization signal from the CPUs
SF61	Signal interface module in slot address 61 (mnemonic name for a group interrupt module in this slot; 48-bit binary input module)
STA	Starting block processing by entering "STA;"
STO	Halting block processing by entering "STO;"
SV	Power supply
SVE	Power supply unit
SW	Software
TEAVI	Clock pulse from the CPU to the EAVU, used for interrupt synchronization
TM	TELEPERM M
UI	Inductive bus converter unit for CS275
VD 11	Logic diode module for messages
VKB	Comparator coupler module
VLSI	Very large scale integrated circuit
VR	Video relay
WR	Write
ZE	Central processing unit
ZEP	Central earthing point
ZRS	Central reset
ZT	Central unit (CPU I and CPU II)

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1 Application

The I/O comparator and switchover module (EAVU) is used in the fault-tolerant AS 235 H automation system.
It forms the link between the central unit (which consists of two central processing units in an AS 235 H system) and the I/O modules.

The EAVU

- converts redundant I/O bus signals from the central units into single-channel I/O bus signals of the extension unit (EE);
- distributes single-channel signals to the two CPUs;
- routes signals from the master CPU to the individual modules;
- verifies the identity of redundant address, data and control signals from and to the central processing units;
- generates an error signal if it detects a discrepancy;
- determines the range concerned by a given I/O command;
- provides information regarding
  - jumper setting
  - last I/O access
  - last register access
  - comparator and status information

  via internal registers;
- influences
  - the actual mastership
  - check of the local extension unit
  - clearing the error registers
  - interrupt inhibit

  via internal registers;
- provides fault finding utilities
- monitors process alarms
- monitors that the supply voltages (24 V and 5 V) are within the tolerance limits
- generates alarm and signal voltages for the local extension unit range (both voltage circuits are provided with a 1.6-A fuse).

One EAVU can be installed in each extension unit. Up to seven EAVU modules are therefore possible in a fully configured AS 235 H system that consists of basic and extension cabinets (cf. Chapter 2.1 of the Operating Instructions; Order No. C79000-B8076-C293). 91 I/O modules may be addressed in normal configuration, including up to three group interrupt modules (SF61) in the basic cabinet.

The EAVU module is installed in the slot at the extreme right-hand side (seen from the front) of a 14-slot extension unit (addresses 0 to 13).

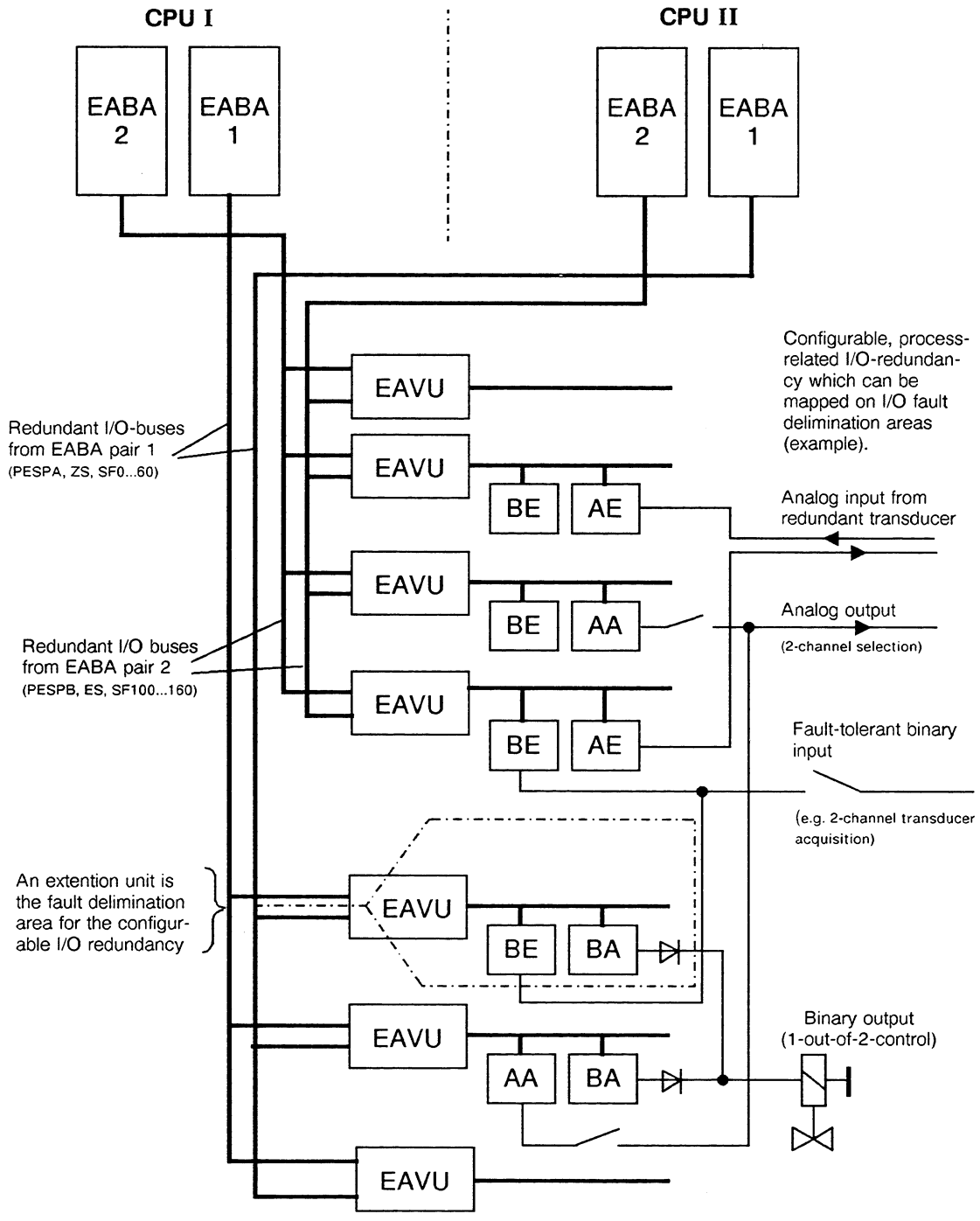

Fig. 1.1 The EAVU in the process I/O structure of an AS 235 H (example)

2 Design

The EAVU module consists of a basic and an extension board, which are screwed together.Two front-panel connectors (for ribbon cables) on the extension board provide the connections between the EAVU module and the two redundant I/O buses.

Two backplane connectors provide the connections to the extension unit I/O bus (X1) and the 24-V supply voltage (X2).

Rack-related jumper settings are also performed in the X2 backplane connector.

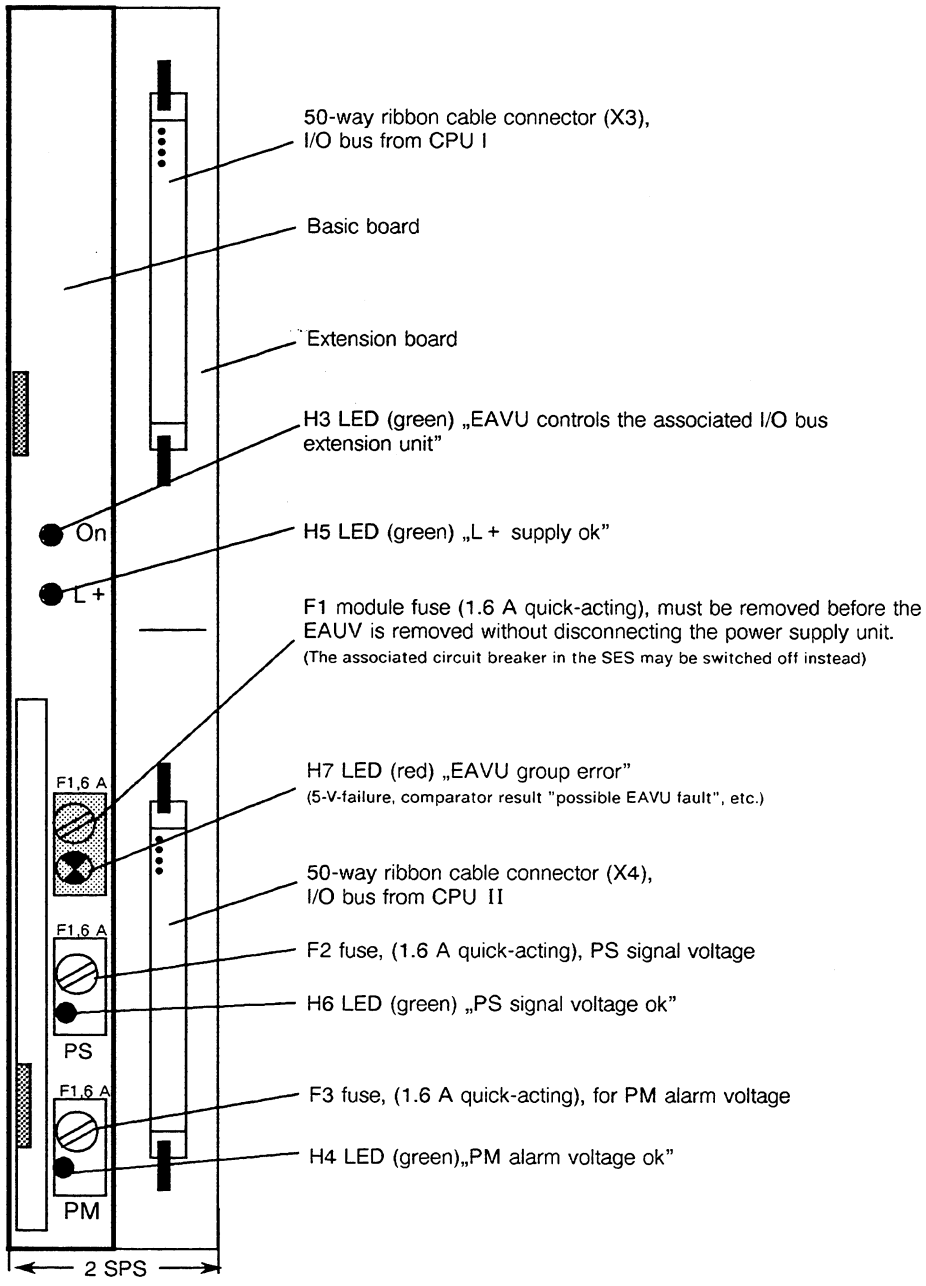

Fig. 2.1 EAVU front panel

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3 Method of Operation

3.1 Function

The EAVU maintains a direct connection with the two central processing units via the two ribbon cables that are connected to the front-panel connectors. Data and signal exchange with CPU I takes place via the upper connector (X3), the lower connector (X4) is used for data and signal exchange with CPU II.
The extension units in the basic cabinet (EABA1) and the extension cabinet (EABA2) are connected via one pair of I/O bus interface modules each.

In normal operation, the EAVU is supplied via this connection with two synchronous sets of data and signals. It checks whether the two sets are identical, determines the addressee (e.g. I/O module y) and transfers data and signals from the master CPU to the single-channel bus of the extension unit.

Signals and data from the I/O modules are transferred to the EAVU, and branched to the two central processing unit connections.

The EAVU sends a fault signal to each CPU if it detects a discrepancy between CPU I and CPU II. It also checks the signals on the single-channel I/O bus (by feedback reading).

Signal processing and utilization of the internal registers is discussed in the following chapters.

3.2 Signal Processing

3.2.1 Address Signal Processing

During each I/O and EAVU register access, the I/O bus interface modules (EABA) transmit 12 address bits (PADB0 to PADB11) and a 1-active select signal (PESP) to the EAVU modules. The areas discussed below exist twice since each CPU has two EABA modules. The CPU generates a separate PESP (PESPA and PESPB) which depends on the most significant address bits. Add 100 to the slot and EAVU numbers in order to address the PESPB area.

The following areas have been defined:

ADB0 . . ADB5	Selects one byte out of max. 64 (0..63) within a slot address.
ADB6 . . ADB9	Selects one out of max. 12 (0...11) or 16 (0...15) possible slot addresses within an extension unit. Depending on the extension unit configuration (EAVU and group interrupt module), the slot addresses available in the extension unit end modulo-16 with 11, 12 or 13.
ADB10 ADB11	Selects one out of four areas (PE0...PE3) with 16 slot addresses each (i.e. one extension unit).

ADB0 ... ADB5 are the byte addresses and ADB6...ADB11 the I/O module addresses for an I/O access.

ADB0 . ADB2	Selects one out of 8 control and status registers of an EAVU (0...7) or one byte (0...5) of a group interrupt module.
ADB3 . ADB5	Selects the register area of an EAVU, a special register area or the group interrupt module.
ADB6 . . ADB11	These have the binary value 111101 (61 decimal) and mean: SF61 signal interface area for EABA1 (PESP-A, GS); SF161 area for EABA2 (PESP-B, ES)

Double-redundant address decoupling and decoding provides 16 double-redundant signals (ADB8...ADB11, ADB0...ADB7, four select signals). The signals of the current EAVU master are selected from these signals.

The 12 single-channel address bits and the newly generated PESP (extension unit or rack PESP) are then sent to the I/O bus of the extension unit. The three least significant address bits and the associated select signals are used for controlling EAVU-internal registers and the control logic.

Address bits 4 to 11 are read from the extension unit I/O bus (backplane bus) and transferred to the extension board. The address bits 0...3 and the four select signals are also transferred via drivers to the extension board. All 16 feedback signals are branched into two channels on the extension board and compared with the corresponding signals before the branch-off point. The signal path (Fig. 3.1) shows that one single response of the comparators on the backup side (comparing returned master signals with backup signals) indicates asynchronous operation of the CPUs or a hardware failure in one of the EAVU CPU interfaces. A fault in the single-channel EAVU section or (with address bits 4...11) in the extension unit backplane is indicated if only comparators on the master side or (more likely) two redundant comparators have responded. Combinations indicating asynchronous operation are interpreted and transferred as a fault signal (PU5) to the CPUs. The comparator signals from the non-master side prevent a fault signal (PU5) from being generated in asynchronous operation.

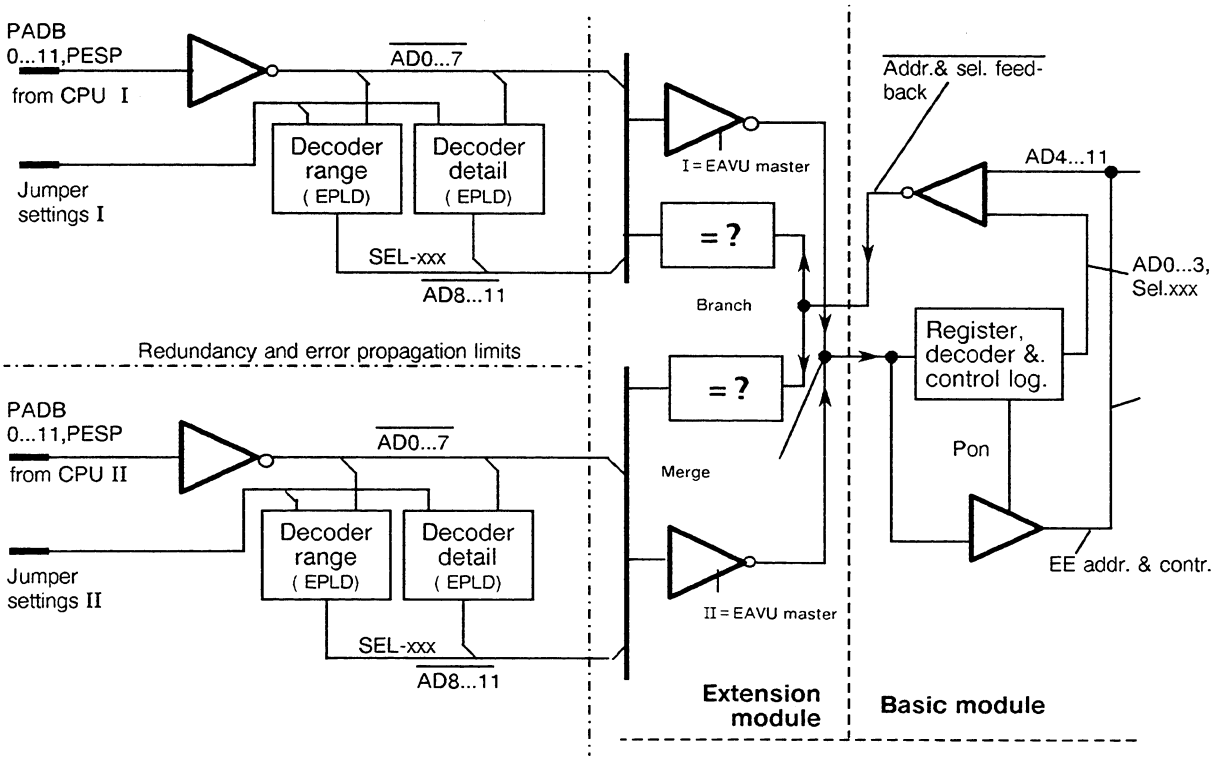

Fig. 3.1 Address path structure

Comparison interpretation for address bits 4...11 is only active if the EAVU controls the connected extension unit. If this is not the case, the extension unit interface is set to a high impedance, and a useful feedback signal is not available.

The signals from the comparators on the extension board are stored during the majority of register accessing activities, and all I/O accessing activities. Storage is performed towards the end of the access after the ready signal has been activated and before the control signal has disappeared. In the event of a ready signal time-out, storage is performed approximately 94 microseconds after access has been started. The comparison results stored with other access data can thus be accessed via four access status or fault registers, and interpreted by software. Access data storage is inhibited when these registers are read.

3.2.2 Control Signal Processing

Each I/O bus interface unit (EABA) of the central processing units transmits the following control signals:

/PMEMW /PMEMR /PCPKL	0 = Write access 0 = Read access 0 = CPU operational 1 = Reset I/O modules

The synchronizing modules (SB) transmit the following signals:

/SYNC /MAST TEAVI	0 = The two CPUs are synchronous 0 = The CPU is N8-H master A clock pulse whose positive edge is used for synchronizing interrupts to the CPUs. It is also used on the EAVU module for clocking status machines. Since this clock pulse is generated on the synchronization modules and derived from the CPU read and write signals, there are no edges during I/O or EAVU access.

These signals are transmitted in redundant mode via the two I/O buses I and II to the EAVU module. The mutually redundant /MAST signals must be different (only one CPU can be N8-H master) and all other signals must be equal in faultless synchronous operation.

Read and Write

The signals from the EAVU master are selected from the valid read and write signals via a signal switch on the EAVU basic board, and processed in single-channel mode. The generated single-channel signals are inactive if an EAVU master does not exist. Signals which are used for controlling the write/read sequence and internal EAVU registers are transferred as write/read signals to the I/O bus of the extension unit if the EAVU controls its extension unit.

TEAVI clock

Brief pulses of approximately 90 ns duration are derived from the redundant TEAVI clock signals on the EAVU basic board and ORed to form a clock pulse. This single-channel clock pulse is used for clocking various sequence controllers in order to achieve synchronous integration and release of the module in accordance with the CPU clock pulse. The same clock pulse is used for synchronizing interrupts.

The single-channel clock pulse is monitored by a watchdog circuit (700 microseconds). Time-out of this watchdog

- clears the synchronized interrupts,
- sets a clock error flip-flop that can be read and reset by the software,
- forces dynamic mode of the single-channel clock pulse.

Dynamisation prevents certain sequence controllers from being frozen. Forced dynamisation only works after a TEAVI clock from (at least) one CPU has occurred. This means that an EAVU cannot exit reset status without at least one previous clock pulse from the CPUs.

PCPKL, SYNC, MAST

These signals influence EAVU mastership control, resetting of the EAVU and connected I/O modules, and generation of the fault signal (PU5) to the CPUs.

An EAVU mastership enabling signal and an EAVU mastership disabling signal for each CPU are generated in redundant fashion in the redundant section of the EAVU extension board.

SP1/SP2 disabling signals:

SP1 SP2	The CPU concerned sets /PCPKL = 1 A specific value is written into the mastership control register

Removing an I/O bus ribbon cable from the front panel has the same effect as the SP1 condition.

The influence of the SYNC and MAST signals from the CPU on the EAVU mastership enabling signal can be controlled by a mastership control register:

Fg1	Enabling with local /MAST = 0 or other /MAST = 1 and local EAVU mastership. I.e. N8-H master (remains) enabled.
Fg2 Fg3	Unconditionally enabled. Transition to Fg1 if /SYNC = 1; i.e. N8-H master is (again) enabled provided that the CPUs become asynchronous.

Enabling and disabling conditions are both ORed, disabling has the higher priority, however. A master signal (/MAST = 0) from the CPU initiates mastership enabling once the EAVU has been reset (i.e. during reset state of the master control registers). This means that, in synchronous operation, the N8-H master also becomes EAVU master. CPU I is preferred if both enabling signals are issued at the same time. The second CPU can assume EAVU mastership after an enabling signal has disappeared, provided that this is permitted by the mastership control registers and the CPU signals CPKL, master and SYNC. Mastership transfer to the basic board is inhibited as long as there is a pending access from the accepting CPU.

The CPU mastership signals are not monitored since generation of the EAVU mastership signals I and II is mutually interlocked. The basic board monitors, however, whether there is an EAVU master at all. This monitoring function may respond for a few microseconds during a controlled N8-H mastership change or for up to 20 ms after certain faults during software faultfinding. A longer response can be caused by a permanent (bilateral) /CPKL = 1 or if both EAVU master enabling signals are missing for any other reason (see above). This "EAVU master missing" causes the EAVU to be reset after approximately 50 ms until /EE-CPKL = 1 has been sent to the I/O modules or the access watchdog has elapsed for the first time (3.5 to 4 seconds). The start-up flag is set after reset, and prevents further resets caused by the watchdog timer.

Resetting the I/O modules connected to the EAVU by /EE-CPKL = 1 can be initiated by the following conditions:

- both masters are missing (bilateral /PCPKL = 1);
- both masters are missing due to mastership control register access;
- the EAVU has been reset by an elapsed access watchdog and a cleared start-up flag;
- the EAVU has been reset by a power supply failure or by software via the CPKL control register without any further effect on the EAVU.

The signal "CPUs operational and synchronous" is generated on the basic board by ANDing the redundant SYNC signals and the redundant CPKL signals. A PU5 fault interrupt is initiated when this common signal disappears. This interrupt only reaches the CPU which still has an active SYNC signal. This PU5 does not set the CPU fault bit. The common synchronous operation signal clears all fault registers when it appears (after a delay of approximately 50 microseconds); the delete signal is pending for approximately 150 microseconds. Fault registers are also cleared by EAVU reset and special software access procedures.

3.2.3 Data Signal Processing

During I/O and EAVU register write and read operations, the I/O bus interface modules transmit and/or expect eight data bits (PDB0...PDB7) via bidirectional lines to or from the EAVUs. Identical data sets must be transmitted from the EAVUs to the central processing units during a read operation.

Fig. 3.2 shows the EAVU data signal path. The incoming data signals are routed via the front-panel connector to an eight-bit comparator (HC688) and a signal splitter which select the signals for the EAVU master from these redundant signals as a single-channel write data bus (/WR-DB). A single-channel read data bus (RD-DB) is branched via a driver in a redundant fashion. These branch drivers are only inhibited if a read data "zero" is to be forced for certain access operations to redundant group interrupt modules or during an access to a redundant jumper register. The (two-channel) read data is transferred to the CPUs if this is permitted by address and control signals. The above-mentioned comparator is fed to the second input. The specified part of the data signal path exists twice on the extension board, with separate artwork design.

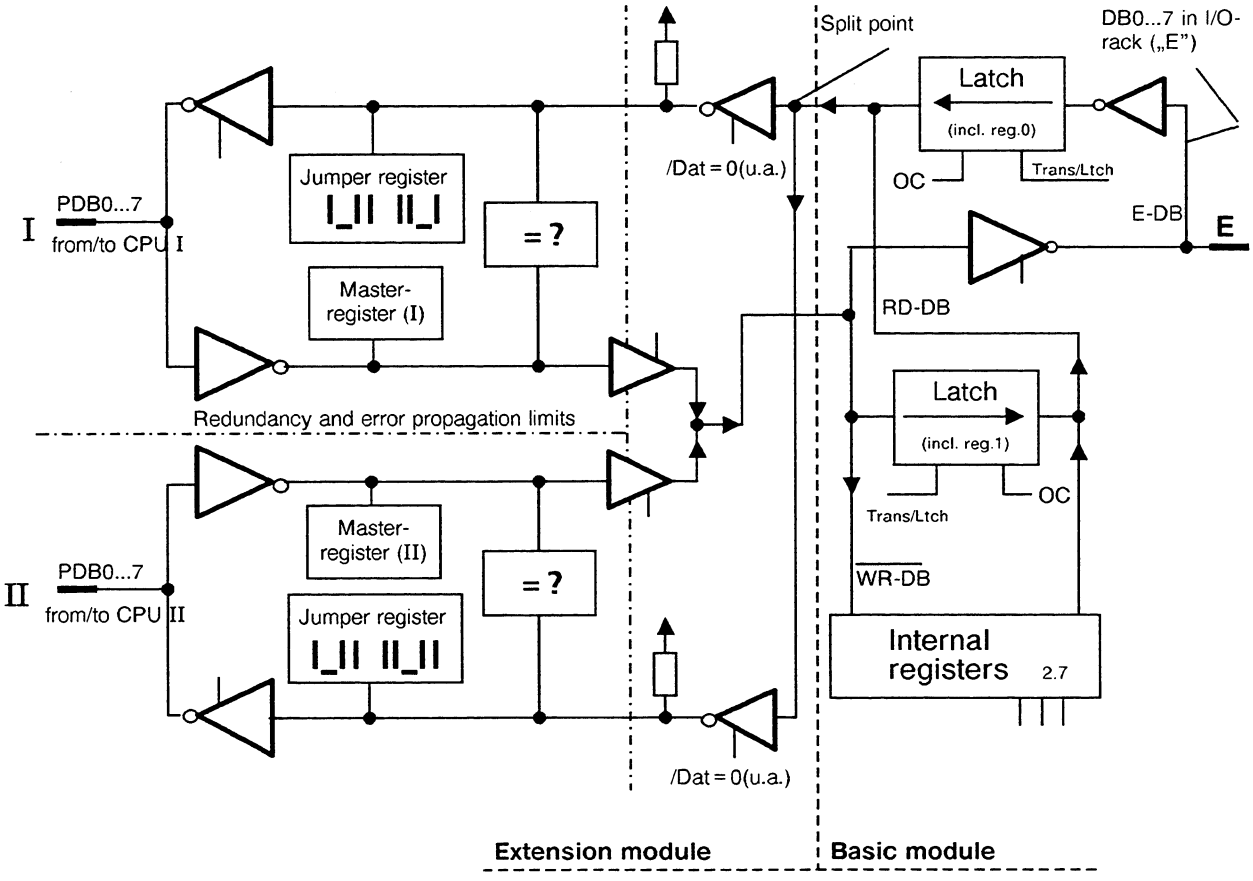

Fig. 3.2 EAVU data path structure

A check (feedback) data item is applied to the single-channel read data bus (RD-DB) during a write access to EAVU registers or the connected I/O modules. The redundant data comparators thus provide a useful signal after each access to the EAVU or a connected I/O module. The comparator signals obtained by a write access must be interpreted in the same fashion as for the address path (see above). The response of a comparator during a read access indicates a defect in the ribbon cable or in the single-channel part of one of the connected EAVUs or of the EABA concerned. These conditions which are also interpreted by the hardware set the read error flip-flops I or II. These flip-flops can be read by software. An error message (PU5) is always issued when the backup comparator responds (as described for the addresses), irrespective of a read or write access.

All non-redundant EAVU write registers are connected to the single-channel write data bus (/WR-DB); all non-redundant EAVU read registers are connected to the single-channel read data bus (RD-DB). The redundant jumper registers and the redundant mastership control register are accommodated on the extension board, and are directly connected to the corresponding redundant buses.

A transparent eight-bit latch (HC563) between the single-channel data buses (/WR-DB and RD-DB) provides the following functions:

- It is made conductive during a write operation into the registers 1...7 (i.e. all EAVU registers except jumper registers and I/O data path control registers). This also retains the current register write data item at the end of the write operation.
- The output is enabled during write operations to the EAVU registers 1...7. This provides the above-mentioned feedback data item required by the data comparators during a register write operation.
- This latch can be addressed as a write register (reg. no.1) without influencing any other EAVU register. This register can also be used as a multicast register, i.e. it can simultaneously be written to in all EAVUs connected to an EABA. This effect can be used for initiating one of the two possible EANK faults (EANK = 0: no module addressed) for test purposes.
- The latch contents, i.e. the last register write data item, can be read from a register address (reg. no. 1). Together with the above-mentioned possible write operations, suitable (six) test patterns can be used for a complete check of the register data paths to and from the EAVUs on possible stuck-at faults and transverse short-circuits.

A data item from the single-channel write data bus /WR-DB is sent to the extension unit data bus if

- the EAVU controls the connected I/O modules, and
- no I/O read access for the EAVU I/O area exists.

Data on the extension unit data bus is decoupled via series resistances and a Schmitt trigger, and read. The latch (HC563) between the decoupled data signals and the single-channel read data bus RD-DB has the following functions:

- It is set during each I/O write operation and when data is written into the I/O data path register (register no. 0). The current data item is retained at the end of an access.
- The output is enabled during such a write operation. This provides the above-mentioned feedback data item for the data comparators during the I/O write operation.
- The latch is made conductive during each I/O read operation. This enables the signal path from the I/O modules to the CPUs. The data item in the latch is frozen a short time after the ready signal from the I/O module has arrived. This ensures that both CPUs accept the same data at the end of a read operation, even after a possible signal transition at the process inputs. If the ready signal from the I/O modules is delayed, the data is frozen approximately 94 microseconds after access has been started. Freezing also retains the (last) current I/O bus data item.
- The last extension unit data bus data item can be read from a register address (reg. no. 0). Together with the above-mentioned write operation under the same EAVU register address on the extension data bus (i.e. without addressing connected I/O modules), suitable (six) test patterns can be used for a complete check of the data paths from the CPUs via the EAVUs, including the extension unit (backplane) data bus, on possible stuck-at faults and transverse short-circuits. This register can also be used as a multicast register, i.e. it can simultaneously be written to in all EAVUs connected to an EABA. This can be used for initiating the EANK fault "Multiple addressing" (EANK >1: more than one module is addressed) for test purposes.

3.2.4 Ready Signal Processing

A ready signal is generated by an I/O module during read or write operations or by the EAVU during EAVU register access. The ready signal from the I/O modules, which is qualified by an enabling signal, runs via the X1 backplane connector. The ready signal from the extension unit backplane bus is accepted 700 ns after access has begun if

- an I/O module in the EAVU range has been accessed
- no EE ready signal was pending when access was started.

This means that an incorrect ready signal on the EE cannot affect access to the EAVU registers; a permanently applied ready signal on the EE bus acts as a ready time-out rather than as a shortened access with unpredictable reaction. Once a ready signal has occurred, it is retained until access is terminated. This prevents asynchronous operation of the CPUs if the ready signal from an I/O module is removed prematurely (due to a malfunction).

The overall ready signal is delayed by 700 ns and branched to the extension board when a read access to the I/O modules is performed. There it is ORed with the ready signal for redundant registers and transmitted in redundant mode via the ribbon cables to the I/O bus interface modules (EABA). The utilized OC drivers are enabled by the redundant address decoding circuitry if:

- a read or write operation is pending
  and
- a register or I/O access in the EAVU range is performed
  or
- a group interrupt module access in the EAVU range and in the time window concerned is performed.

The result is that an incorrect single-channel permanent ready signal from the EAVU modules is blocked. A combination with a read or write operation avoids unnecessary execution time required by the transfer of the ready signal to the CPUs at the end of an I/O access.

The redundant ready signal of the I/O buses I and II is fed back and read. This read-back ready signal from the master side is selected on the basic board. Any access by or to the EAVU (except to a redundant register) is completely blocked if an incorrect signal is pending. (The EABA reacts in the same manner if it detects a permanent ready signal on the I/O bus.)

An additional access end signal is generated on the basic board. This signal is influenced by:

- the select signals (register, I/O, SF61),
- the ready signal generated on the basic board,
- the read-back ready signal during an SF61 access,
- access time measuring signals indicating an access exceeding 94 microseconds.

The access end signal stores the read data in a buffer in order to enable the CPUs to continue their synchronous operation even if the read data of the extension unit changes while the access is being performed.
The access end signal also triggers, after a delay, the three access status registers and the hardware-controlled comparator signal interpretation.

Access status register triggering is inhibited after
- an attempt has been made to perform read access to exactly this register or to the fault register.

Triggering of the access status register **and** the hardware-controlled comparator signal interpretation is inhibited by
- a central unit error bit which is set by the EAVU itself after incorrect synchronous operation has been detected.

The result of the first inhibition is that the values stored for a single access are supplied at once when the access status register is read. The second inhibition freezes the values that were stored for the access in which the synchronization fault was detected by the EAVU hardware.

3.2.5 EANK Signal Processing

The one-out-of-n check (EANK) is a peculiarity of the I/O modules in a TELEPERM M system which enables two faults in the I/O area to be detected:

1. An I/O module does not respond to a valid I/O address. The reason can be that either the application software erroneously assumes I/O modules that have not been configured or I/O modules that are normally available have been installed incorrectly or not at all. This problem, which may occur in any system, can be detected by a ready signal delay. Interpretation of this fault is normally inhibited by the EANK circuits (jumper setting) on the I/O bus interface modules of the AS 235 H system.
   This fault is also known as "addressing error".

2. The second possible problem occurs if several modules are addressed simultaneously by the same address. This problem, which is caused by incorrect jumper setting on I/O modules or racks, does not cause a ready signal delay and thus no effect can be reliably detected by software means.
   This fault is also known as "insertion error".

Either fault can be detected by the EANK circuitry.

A line taken to all I/O modules is fed by a voltage source with U_0 = 5 V and R_i = 562 ohms. Each module which responds to an address connects a 562-ohm resistance between the line and earth (OC driver). The resulting voltage is measured by two comparators which sense whether no module (full voltage value), exactly one module (half the voltage value) or more than one module (a third or less of the voltage value) has responded to the address. These analog signals can easily be decoupled in a redundant system and converted from single-channel to multi-channel mode.

The comparator signals generated on the basic board ("one", "two", or "more" I/O modules have been addressed) are branched to the extension board. There they are qualified by select signals (and time windows during a group interrupt module access) which are generated on the extension board. The EANK signals for EAVU register access are also generated on the extension board. An EANK signal is generated during normal register access. One multicast register, however, supplies two EANK signals (i.e. "insertion error"), the other multicast registers supply no EANK signal (i.e. "addressing error"). Since these errors are retained if several EAVU modules respond simultaneously, the EANK circuitry on the I/O bus interface modules can be tested.

The generated digital EANK signals are converted into loads on the EANK line in the I/O ribbon cables to the I/O bus interface modules. The corresponding OC-controlled (two times two) LS125 drivers with a series resistance of 562 ohms are triggered by the redundant address decoding function. Individual faults can therefore not affect both CPUs and a fault in the single-channel EAVU section cannot affect more than one I/O fault delimitation area.

3.2.6 Interrupt Processing

Four different interrupts (INT1...INT4) are provided in the TELEPERM M I/O area which enable acyclic reaction to process events. Various I/O modules can create process alarms according to different criteria. These alarms are connected by jumper selection to one of the OC interrupt lines of the EE-I/O bus (and thus, in standard configuration, directly to the CPU). In order to guarantee synchronous CPU reaction in the AS 235 H system, the interrupts are synchronized by the TEAVI clock pulse before they are branched to the EAVU module. An EAVU module only forwards an interrupt if it controls the connected I/O modules and if additional criteria, which can be selected by jumper setting and in the software, have been satisfied.

Different from the above-mentioned general utilization of the four interrupts, the 230/235 product family only uses INT1 with one additional restriction: the interrupt proper may only be raised by a single group interrupt module, the 48-bit binary input module 6DS1 601-8BA (or 6DS1615-8AA), under address SF61. All process alarms must be fed to this module as a 24-V signal whose positive edge is interpreted. This means that alarm outputs (group alarms) from other I/O modules must also be interconnected with SF61 inputs. The SF61 input signals are delayed in analog input filters by 1.5 to 3 ms. After an INT1 has occurred, the 230/235 system software reads all six SF61 bytes in order to determine the interrupt source. The 48-bit binary input module removes its INT1 interrupt when it reads byte 0 and delays subsequent interrupts by an off-state interval of approximately 1 ms.

Although all four interrupts are synchronized and fanned out on the EAVU according to these interrupt rules (in order to obtain the same extension possibilities as the standard configuration), additional functions have only been implemented for INT1:

- correct disappearance and disabled condition of INT1 are monitored;
- frequency and disabled condition of INT1 are monitored;
- INT1 is digitally filtered with 1.63 ms delay (option);
- software-transparent double- or triple-redundant mode of the group interrupt module is possible. The software recognizes only one group interrupt module under SF61.

It is a CPU hardware and microprogram feature that excessive or permanent occurrence of INT1 retains CPU processing in one software level. Process execution is thus inhibited. The first two of the above functions prevent a single fault from causing this reaction in an AS 235 H system. Any EAVU which is not responsible for SF61 (by jumper assignment) will block INT1. The (EE) interrupt must disappear when byte 0 of an SF61 is read. This response towards the CPU is forced and controlled by a forced dynamic reaction. The next INT1 interrupt will only be enabled at least 1.63 ms after SF61 byte 0 has been read and INT1 disappeared for at least 100 microseconds. A permanent INT1 interrupt is passed on once only. A limit of 160 or 32 interrupts per 3.2 seconds can be selected for INT1 frequency blockage. The 3.2-second time interval can be shortened by (cyclic) software accesses.

Blocking permanent or excessively frequent INT1 signals can be selected for each individual EAVU and redundant group interrupt module. The total values from all redundant group interrupt modules must be taken into account if interrupt blockage after excessively frequent interrupts is used for protecting against cycle overload. According to configuration, a maximum number between 3*32 and 3*160 interrupts per time interval is permitted and passed on. Redundant alarms are recognized by the central unit as **one** single interrupt but counted individually by each EAVU concerned if alarms are connected in a redundant fashion and the filter has been activated.

The **third** above-mentioned function compensates for the skew of the analog filters on the group interrupt modules. The method of creating a redundant status for group interrupt modules which is discussed below makes it possible that the same interrupt source can be connected in a redundant fashion to redundant group interrupt modules. The skew of the analog filters may cause multiple interrupts that are initiated by the same event. This effect, which might take some program execution time, can be avoided by applying an optional digital filter to the INT1 signal. All alarms which become effective during the filter time of the first alarm are then acquired during one single scan.

The **fourth** function removes the redundancy bottleneck caused by the group interrupt module conception.

The 48 inputs of the group interrupt module (i.e. the 48 possible process alarms) are interrogated via six bytes.

These are subdivided into the groups I0, I1 and I2:

Group	SF61-bytes	Proces alarms	AD2	AD1	AD0
I0	0 and 1	1 to 16	0	0	X
I1	2 and 3	17 to 32	0	1	X
I2	4 and 5	33 to 48	1	0	X

Jumper settings for each EAVU (PESPA, GS) allocated to EABA1 specify the primary responsibility of the EAVU for one of the three alarm or interrupt groups, and whether an SF61 has been allocated. Primary responsibility automatically assigns secondary and tertiary responsibility for the other groups.

Jumper for I0	I1	I2	Causes... I0 (1...16)	Responsibility I2 (17 ... 32)	Responsibility I3 (32 ... 48)
o	o	o	none	none	none
B	o	o	primary	secondary	tertiary
o	B	o	tertiary	primary	secondary
o	o	B	secondary	tertiary	primary
o	B	B	secondary	primary	primary
B	B	o	primary	primary	secondary
B	o	B	primary	secondary	primary
B	B	B	primary	primary	primary

B Jumper inserted
o Jumper not inserted

Any EAVU responsible for SF61 transfers addresses and control signals to its SF61 module. This is performed simultaneously for all redundant group interrupt modules. Data signals and ready signals to the CPU are immediately transferred if the module has primary responsibility. (A correct EANK signal is an additional condition for immediate transfer if SF61 redundancy has been selected.) EE data or data = 0, EANK, and the ready signal are transferred after 6 microseconds if the module has secondary responsibility (after 12 microseconds in the case of tertiary responsibility). The primary responsible EAVU supplies data = 0, EE-EANK and a forced ready signal after 18 microseconds as a last action to be taken. This can only happen after SF61 has completely lost redundancy and additional faults have occurred. These four time windows are created such that they do not overlap, even if several EAVUs with group interrupt modules are involved. The window for the ready signal is always slightly smaller than the window for the read data.

Under normal circumstances, all SF61 modules can terminate access within a few microseconds without any extra delay. The SF61 modules that are primarily responsible for an interrupt module can supply their read data (including correct EANK and RDY) via the allocated EAVU. The second or third module takes over if the first module fails and configuration has been set up accordingly. Jumper setting permits configuring the modules such that a "SF61 replacement" EAVU can either transfer data to the CPUs that corresponds to the input signals of the SF61 module or data = 0. The first possibility requires all (interrupt) inputs of all SF61 modules to be allocated sensibly. The second possibility only requires (interrupt) inputs with primary responsibility of the EAVU to be connected. Sensible connections for the first case include redundant connections of the alarm source either directly or via redundant interrupt-generating binary input modules, constant zero (M) or one (PS). Fig. 3.3 shows various possible interrupt configuration and interconnection structures.

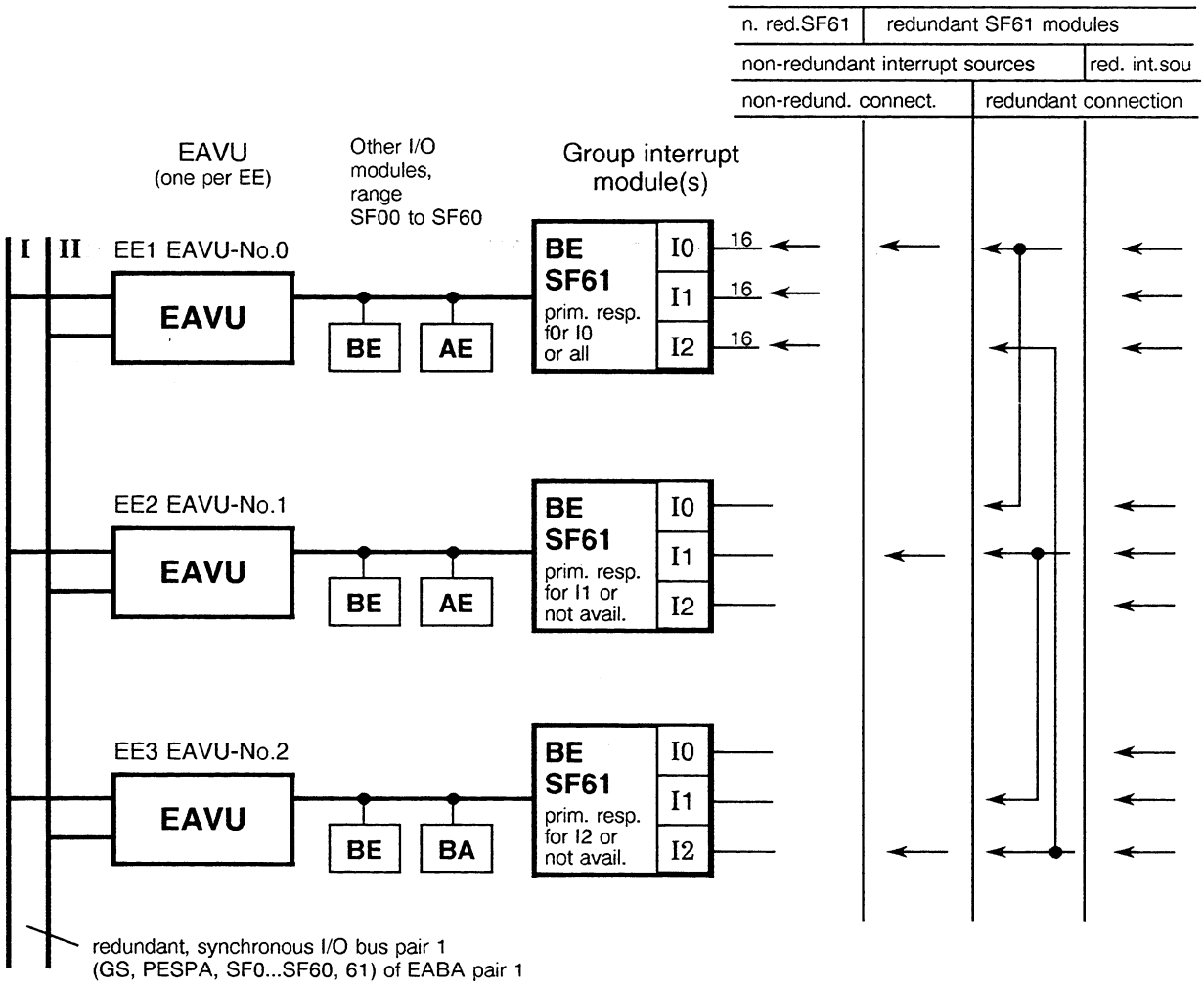

Fig. 3.3 Utilization of the SF 61 group interrupt module

In the second case (i.e. unconnected inputs of non-primary responsibility), interrupt generation can be suppressed by appropriate jumper setting on the group interrupt module

The system software perceives only one single SF61 in this SF61 redundancy scheme; any access is recognized by all redundant SF61 modules. When reading SF61 modules, the system software therefore neither detects a redundant structure of the SF61 nor the actual access procedure which is merely extended if an SF61 or one of several EAVUs with redundant SF61 is lost. This becomes obvious from the stored access bit when the EAVU access status register is read subsequently. Group interrupt module redundancy losses are thus discovered and indicated by the system software. Connecting constant zero (M) to an input that is not used for process alarms, and connecting constant one (PS) to the same input of the two other SF61 modules causes the corresponding alarm bit to be set after a process alarm if "replacement SF61 modules" have taken over. This status can be directly interpreted by the application program.

3.3 Register

Exactly one EAVU is responsible (per jumper setting) for user or system software access to I/O and group interrupt modules. The system software checks the jumper settings on possible collisions. The EAVU responsible connects address, control and data signals to its I/O bus and provides the required acknowledgement and, during read operations, data signals as a result of the access immediately and synchronously to the CPUs.

Internal information and control features of the EAVU itself provide 10 EAVU write registers and 10 EAVU read registers in the SF61 area of the EAVUs (PESPA, GS) allocated to the EABA1 pair and in the SF161 area of the EAVUs (PESPB, GS) allocated to the EABA2 pair. These SF addresses and thus the EAVU registers are only partly user-accessible via an EAVU function block and therefore protected against unauthorized access.

The ten EAVU registers consist of the jumper registers (I and II) and eight status and control registers (0...7). All registers can be accessed in synchronous mode for both CPUs and in asynchronous mode for the EAVU master CPU. The redundant jumper registers and (with restricted functions) the redundant master control register are also accessible for the non-master CPU in asynchronous mode.

The lower three control registers (see write registers 0...2) can be written to as "multicast registers" in a special address range. One write operation in the multicast register range has simultaneous effect on all EAVUs of an EABA pair.

Figs. 3.4 and 3.5 show the address schedule and a summary of all EAVU registers. Some registers with the same number have completely different functions and meanings during write or read operations. Read and write registers are discussed in separate chapters.

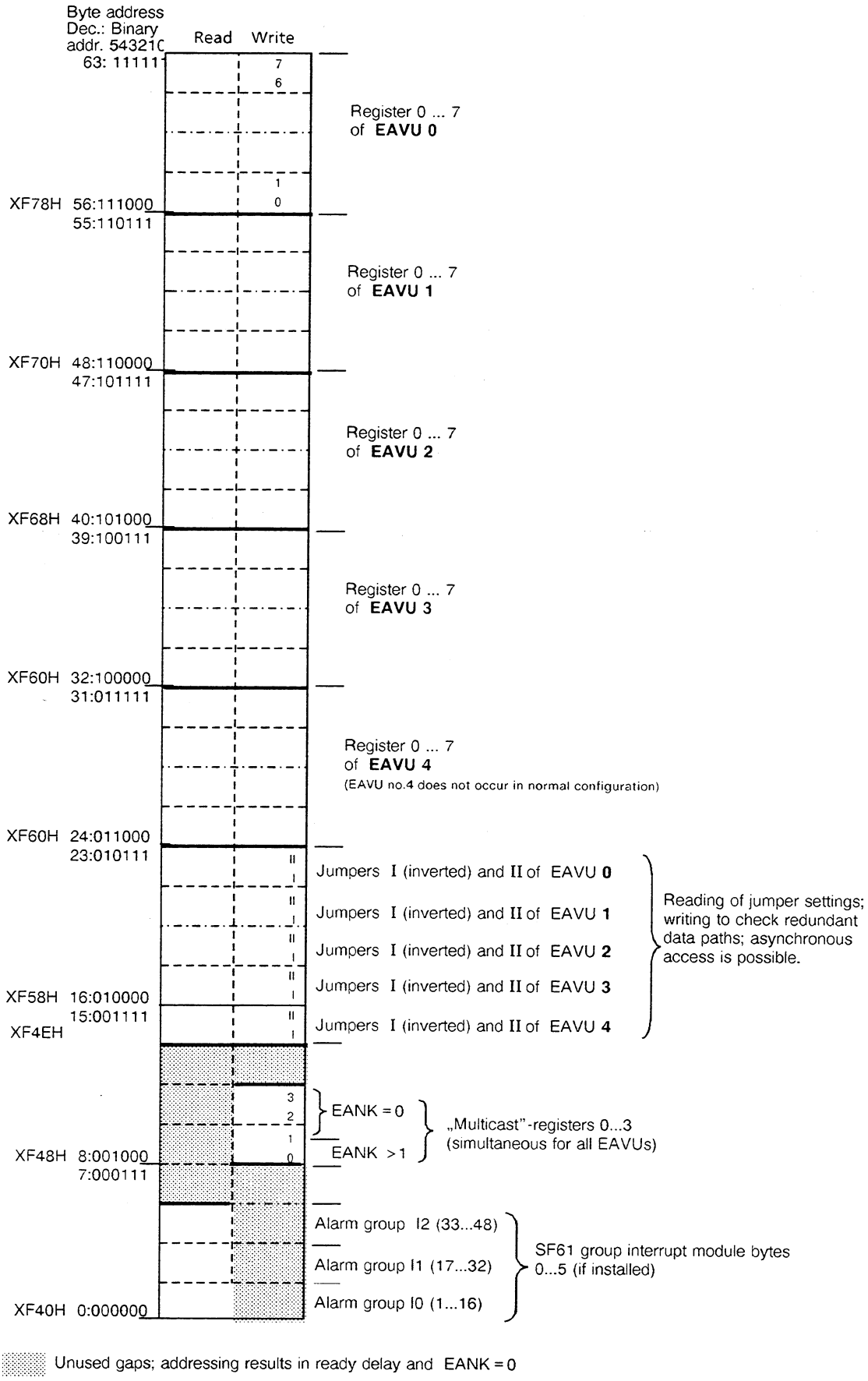

Fig. 3.4 EAVU register address schedule

Register No/Des.	Read Register		Write Register	
/Brück_I	Inverted jumper assignment I		1-channel data path and access verification	1)
Brück_II	Jumper assignment II		1-channel data path and access verification	
00	Last I/O access data		Data path verification (I/O bus)	2)
01	Last register write data		Data path verification (register)	
02	Interrupt status		EAVU control user program	
03	EAVU status		I/O master-(I – II) and ON control	
04	Last access status (common)	No comparator and status latch during reading	CPKL and periph. control (POn) OFF	
05	Last access status _I		CPKL and periph. control (POn) ON	
06	Last access status _II		Only CPKL of I/O bus ON	
07	Error status		EAVU control system software	

1) These two registers may also be addressed by the passive CPU in asynchronous operation. Status information is not stored when these registers are accessed.
2) These four write registers can be addressed together as multicast (MC) registers for all EAVUs of a PESP area.

Fig. 3.5 EAVU register overview

3.3.1 Read Register

Read registers "jumpers I inverted" and "jumpers II"

The bits in this register mirror the corresponding jumper settings which define address decoding for I/O and SF61 access. Reading these jumper settings enables the system to determine the I/O configuration during start-up and to check whether mandatory and recommended configuration instructions have been complied with. Jumper settings must be redundant; that is why two jumper registers exists. Apart from being inverted, the bits of jumper register I have the same meaning as those of jumper register II.

Jumper register II assignment

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MitLue	I2Fg	I1Fg	I0Fg	Pe3Fg	Pe2Fg	Pe1Fg	Pe0Fg

Bits 0 to 3 and 7 specify the I/O module or process interface module address range for which the EAVU is responsible:

set bits					The EAVU is responsible for address range	and thus in normal configuration for	
7 MitLue	3 Pe3Fg	2 Pe2Fg	1 Pe1Fg	0 Pe0Fg		GS (PESPA)	GS (PESPB)
1	X	X	X	1	SF×00...SF×15	EE No. 1	EE No. 4
0	X	X	X	1	SF×00...SF×11	EE No. 1	EE No. 4
1	X	X	1	X	SF×16...SF×31	EE No. 2	EE No. 5
0	X	X	1	X	SF×16...SF×27	EE No. 2	EE No. 5
1	X	1	X	X	SF×32...SF×47	EE No. 3	EE No. 6
0	X	1	X	X	SF×32...SF×43	EE No. 3	EE No. 6
X	1	X	X	X	SF×48...SF×60	-	EE No. 7
1	X	0	0	0	Gaps translated[1)]	-	EE No. 7a

[1)] The code of the address bits ADB11...ADB8 can be changed
from ADB11...8 = XY11 to ADB11...8 = 00XY
if such a jumper setting has been selected.
The gaps caused by the modulo-16 slot addressing scheme (12...15, 28...31, 44...47) are translated into existing slot addresses (0...3, 4...7, 8...1) of a further extension unit with rack address 0. This means that the gaps between the I/O slot addresses are removed whilst the slot addresses in unchanged standard extension units are retained (the standard AS 235 fills some of the gaps with its I/O slots in the basic unit).

The remaining bits mirror the jumper settings which define the responsibilities for an SF61 group interrupt module.

Bit 4 = 1 The EAVU is primarily responsible for SF61 bytes 0 and 1 (I0)
Bit 5 = 1 The EAVU is primarily responsible for SF61 bytes 2 and 3 (I1)
Bit 6 = 1 The EAVU is primarily responsible for SF61 bytes 4 and 5 (I2)

The system software checks the identity of jumper settings I and II. The interface between the EAVU concerned and the EE-I/O bus is inhibited and a message issued if the system software detects any discrepancy in the jumper settings. Subsequent I/O or SF61 access would cause asynchronous operation (PU5) of the two CPUs if the jumper settings differ.

Read register 0 „last I/O access data item"

The data item of the last I/O access or register 0 write operation has been stored in a latch and is supplied. Provided that this EAVU controls the I/O modules connected, this function is used by the self-test software together with a possible write access to the write register 0 for performing a complete check of the data paths between CPUs and EE data bus. The fault finding software uses this EAVU for determining the data item that was valid during the faulty access to the I/O modules. Thus, in addition to the data read from the access status registers, it obtains further information regarding the access operation during which a fault has been detected.

Read register 1 „last register write data item"

The data item of the last write access to the write registers 1 to 7 has been stored in a latch and is supplied. This information can be used by the self-test software together with a possible write access to the write register 1 for performing a complete check of the data paths between CPUs and EAVU registers on all stuck-at faults and transverse short-circuits.

Read register 2 „interrupt status"

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IntZV	DynSp	SWSp	Dat0Sub_N	INT3	INT2	INT1	INTFg

Bit 0 = 1 INT1 is enabled, no fault, no inhibition

Bit 0 = 0 INT1 is inhibited due to a set error message (duration or frequency), forced dynamic activities (read SF61 byte 0), filter function, I/O check disabled or explicit software inhibition.

This inhibition is the OR combination of all interrupt inhibiting signals generated on the basic boards. Completely independent of this function is the inhibition of INT1 on the (redundant) extension board if the backplane jumper settings do not indicate any SF61 responsibility.

Bit 1 to Bit 3 The three interrupt bits indicate the line status on the extension unit. This information is independent of whether these interrupts have been enabled or disabled by jumper settings on the EAVU. This enables polling of up to three different alarms per extension unit.
The EAVU issues INT1 if bit 0 (enabled) and bit 1 (EE-INT1) are both 1 and the jumpers have been set accordingly.

Bit 4 = 0 Irrespective of the input values, data item 0 is supplied in an alternative secondary or tertiary read operation from a group interrupt module.

Bit 5 = 1 Software inhibition for INT1 has been set.

Bit 6 = 1 INT1 is inhibited after SF61 byte 0 has been read. The signal may not be active for more than 250 microseconds or together with INT1 (the latter causes an I&C alarm).

Bit 7 = 1 INT1 occurred too frequently, fault inhibition, I&C alarm.

"Too frequently" within an unsynchronized time interval of 3.2 seconds or within a shorter time interval defined by regular software access operations is, in reset status, defined as more than 160 interrupts per interval and EAVU.

Read register 3 „EAVU status"

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ResBr2	/ResBr1	/Filter	DefOn_N	POn_N	ECPKL	PLAD11	PLAD10

Bit 1,0 Slot address bits 11 and 10, i.e. the rack address (its value should be identical to the EAVU number modulo-4).
Bit 2 = 1 The CPKL line of the extension unit is low (no I/O reset)
Bit 3 = 0 The EAVU interface to the EE-I/O bus is active
Bit 4 = 0 The EAVU assumes control over EE after reset.
Bit 5 = 0 The filter jumper is inserted; INT1 is filtered by the EAVU with T = 1.5 ms
Bit 6 = 1 Backup jumper 1 (X2 backplane connector) has been inserted.
Bit 7 = 0 Backup jumper 2 (X2 backplane connector) has been inserted.

Read register 4 to 7

Read registers 4 to 6 and, to a certain extent, 7 mirror the status of the previous access via this EAVU to I/O modules and EAVU registers. They reflect the status of other access operations further in the past if one of the "comparator and status latch inhibitions" has been set.

Access status register triggering (and thus any modification of the read registers 4 to 6) is inhibited
- during read access to registers 4...7 and any jumper register access;
- by the central unit fault bit which is set by the EAVU when asynchronous operation is detected, and may be cleared by the system software.

Triggering the hardware comparator interpretation and thus any modification of bits 7, 6, 3, and 2 of register 7 is inhibited
- as long as the central unit fault bit is set;
- when register 7 is read.

Read register 4 „last common access status"

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/EANK	Z77	Z12	Z6	RegS	IntS	PvISel	/P0n

Bit 0 = 0 The EAVU had control over the connected extension unit.
Bit 1 = 1 I/O or SF61 were selected.
Bit 2 = 1 SF61 was selected.
Bit 3 = 1 An EAVU register was selected.

Bit 1 must be 1 if bit 2 = 1 (not vice versa). Bit 3 and bit 1 cannot be 1 at the same time. Any deviation from these rules indicates an address decoding error on the EAVU master side.

Bit 4 = 1 Access time exceeded 6 µs
Bit 5 = 1 Access time exceeded 12 µs
Bit 6 = 1 Access time exceeded 77 µs

		Access time in µs was approx. between			
Z12	Z6	(withZ 77 = 0)	or (with Z77 = 0)		or (with Z77 = 1)
0	0	1...6 (a)	26...32	51...58	77...83
0	1	6...13 (b)	32...38	58...64	83...90
1	0	13...19 (c)	38...45	64...70	90...96
1	1	19...26 (d)	45...51	70...77	96...102

Remark : The values 1 to 20 µs always apply for SF61.

Bits 4 to 6 show whether an SF61 read access was direct (a), via the alternatively secondary (b) or tertiary (c) responsible EAVU or incorrect, i.e. with forced ready signal after 19 microseconds (d). If all bits 4 to 6 are set, access with ready delay (QVZ) is very likely (cf. registers 5 and 6, bit 0). Due to the time sequence, status data and read data item are frozen approximately 94 microseconds after I/O access has been started. This cannot happen during an EAVU register access (swift internally generated ready signal) or an SF61 access (possibly earlier forced ready signal). Contradictory time measurement bits after such an access indicate an EAVU fault in the single-channel section.

Bit 7 = 0 None of the two possible EANK faults during I/O or SF61 access.
Bit 7 = 1 Addressing or insertion error during I/O, SF61 or register access. This bit must be 1 after a register access. Any discrepancy indicates a fault in the single-channel EANK circuitry of the EAVU or on an I/O module in the extension unit.

Read register 5 „last access status I"

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/RD	/WR	MAST	On	/DG1	/AdG1	/AdSG1	RDYRck

Bit 0 = 1 Ready was active on I/O bus I (to the EABA).
Bit 1 = 0 Addresses 8 to 11 and four select signals from I were identical with the corresponding single-channel signals.
Bit 2 = 0 Addresses 0...7 of I and the EE-I/O bus (read-back) were identical.
Bit 3 = 0 Data bus I and common single-channel data bus had the same value.
Bit 4 = 1 The interface to the I/O bus (to EABA) was active.
Bit 5 = 1 CPU I was EAVU master.
Bit 6 = 0 It was a write access.
Bit 7 = 0 It was a read access.

Read register 6 „last access status II"

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/RD	/WR	/MAST	On	/DG1	/AdG1	/AdSG1	RDYRck

Like register 5, apart from the inverted master bit 5.

Bit 5 = 0 CPU II was EAVU master.

Remarks on registers 5 und 6:

Bits 1 (AdSG1) = 1 are only to be interpreted as a discrepancy if the EAVU had control over its extension unit. Further interpretation of the comparisons can be found in the description of address and data paths, Chapters 3.2.1 and 3.2.3.

Bits 5 (/Mast I and Mast II) must be identical in both registers. Any discrepancy indicates a hardware fault in the single-channel part of the EAVU. The two remaining bits in both registers are also identical after an access in synchronous operation without hardware fault. Any discrepancy indicates a fault in the corresponding redundant EAVU part, the related I/O bus ribbon cable, the CPU or the EABA.

I/O access with ready delay (QVZ) is very likely if both bits 0 (RdyRck) in both registers 5 and 6 are 0. This should also manifest as an addressing error register 4 bit 7 = 1. Discrepancy indicates that an I/O module address supplies correct EANK but no ready signal (incorrect byte address of an existing module) or that a fault has occurred in the corresponding single-channel EAVU part.

Read register 7 „fault status"

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZF	EF	TF	F24	LF _ I	LF _ II	AnlMk	SaFe

This register indicates faults that can be detected by the hardware and diagnoses that have been determined by the hardware from stored access status data (cf. read registers 4 to 6).

Bit 0 = 1 "Common alarm" has been set; the red LED is blinking. The hardware interpretation of an access status indicates an EAVU fault in the single-channel section (bit 6 set), or the software-controlled "common alarm" bit has been set. (No register can be read after other faults which causes the EAVU to be reset and the common alarm LED to be activated.)

Bit 1 = 1 The EAVU had been reset. This start-up flag inhibits the access watchdog. It is reset by the software.

Bit 2 = 1 Read error II (data comparator II during read access)

Bit 3 = 1 Read error I (data comparator I during read access)

Bit 4 = 1 Low voltage (< 19 V) of the 24-V voltages L+, PM or PS or overvoltage of L+ (and thus also PM and PS if the fuses are ok).

Bit 5 = 1 Clock error; both clock pulses TEAVI-I and TEAVI-II have failed for more than 700 microseconds.

Bit 6 = 1 Probably EAVU fault (EAVU master comparator).

Bit 7 = 1 Probably central unit fault (EAVU backup comparator, not master comparator). A PU5 has been raised if this bit is set.

3.3.2 Write Register

Write register I and II „single-channel data path check"

These two registers have the same address as the above-mentioned jumper registers. Access to these registers is also possible in asynchronous mode from the non-EAVU-master side, and does not cause the access status registers to be triggered.

Any data may be written to these registers without influencing the EAVU (in particular its single-channel part). A ready signal is only issued if the data path comparator finds that there is no difference between the written pattern and the contents of the corresponding jumper register. The two jumper registers contain mutually inverted patterns if jumper setting is correct. This fact enables the read and write access to the EAVUs to be checked with inverted data patterns in asynchronous mode and from both CPUs. The jumper registers are read and this read pattern is written into these registers. This EAVU accessibility test is the basis of the fault finding procedure in the I/O section after asynchronous CPU operation has begun.

Ready delay is provoked by writing an "incorrect" pattern. This enables the data comparator to be tested (bit by bit) and demonstrates correct recognition of a ready time-out.

Write register 0 to 2

Writing to these registers is possible for each individual EAVU. In addition, these registers can be used as multicast registers in a special address range. All EAVUs of a PESP area or an EABA pair can write the same data simultaneously to these multicast registers. Multicast register access has a different effect on the EANK signal (cf. Chapter 3.2.5) than writing to the corresponding individual EAVU registers.

Writing to multicast register 0 causes "addressing error" or "insertion error" to be signalled for each EAVU on the redundant I/O buses to the CPUs or EABAs. This is detected by the EABAs and causes corresponding reactions.

Writing to the multicast registers 1 or 2 does not cause any fault reaction (due to the jumper setting in the AS 235 H).

This feature may be used for accelerating the data path test for all EAVUs of a PESP area and for performing common re-triggering of all EAVU watchdogs (simultaneously and without time-consuming checking in configuration and fault tables).

Write register 0 „data path check for I/O"

Any data can be written into this register and read back under the same address. The EE data bus is used as a signal path here. Hardware checking and monitoring operations are performed in the same manner as for any other I/O access.

Since writing data to these registers has no side-effects on the EAVU or the I/O modules connected, six suitable test patterns and the read-back feature can be used for performing a complete check of the data path between CPUs and EE-I/O data bus on all stuck-at faults and short-circuits between data bits.

Write register 1 „data path check for registers"

Any data can be written into this register and read back under the same address. Hardware checking and monitoring operations are performed in the same manner as for any other EAVU register access.

Since writing data to these registers has no side-effects on the EAVU or the I/O modules connected, six suitable test patterns and the read-back feature can be used for performing a complete check of the data path between CPUs and EE-I/O data bus on all stuck-at faults and short-circuits between data bits.

Write register 2 „EAVU control - user"

Bits 6 to 3 are irrelevant when data is written to this register; their value is merely reflected in read register 1 (register data latch). This register controls the 24-V SimI output (X2 z28) of the EAVU and some EAVU interrupt functions. An EAVU function block can be used for writing to this register; the following control functions may also be initiated by the application program. Values with bits 6...3 not equal 0 are rejected when the function block input is parameterized. Most of the remaining control functions (write registers 3, 6 and 7) are reserved for the system software.

Value written into register 1)					causes	Explanation
Bit 7	Bit 2	Bit 1	Bit 0	Dec		
0	0	0	0	0	Nothing	1)
0	0	0	1	1	SimI OFF (0 V)	2)
0	0	1	0	2	SimI ON (24 V)	2)
0	0	1	1	3	SimI-ON impulse	2, 3)
0	1	0	0	4	SimI-inverted	2)
1	0	0	0	128	SW-Int1-inhibited	4, B)
1	0	0	1	129	SW-Int1-enabled	4)
1	1	0	0	132	Reset interrupt inhibition	5)
1	1	1	0	134	ditto. & INT1 frequency limit = 32	6)
1	1	1	1	135	ditto. & INT1 frequency limit = 160	6)

See page 3-29 for explanations.

Explanations of the table on page 3-28:

B) This access can be initiated by operator input in the EAVU screen form of the FBS SYST.HBED.

1) The "Dec" column specifies the decimal value which must be used for parameterizing the EAVU-FBS input in order to initiate one of the listed functions. Using 0 for parameterization does not initiate any FBS action or write access. The values 5 to 7, 130, 131, and 133 are reserved and should not be used.

2) The functions 1 to 4 control the 24-V Siml output via the bottom backplane connector X2 (z28). Reset status is OFF (0 V).

3) The duration of the impulse is between 75 and 130 microseconds. The falling edge (and thus the effective impulse duration) is very load-dependent since the 24-V output can only drive in positive direction.

4) These calls set and clear the software interrupt inhibition.
The set call (128 = 80H) also sets the limit for the INT1 frequency monitoring function to a reset value of 160.

5) While calls 128 and 129 only refer to software-controlled interrupt inhibition, call 132 resets all interrupt inhibitions (by interrupt faults and software). The time interval for the frequency monitoring function is restarted. In contrast to 133 to 135, such an access should not be performed by EAVU-FBS in cyclic mode. It is absolutely forbidden for an EAVU-FBS that is installed in an alarm cycle.

6) These access operations reset the counter for the interrupt frequency monitoring function, provided that no interrupt frequency fault has been detected. The time interval for the interrupt frequency monitoring function is restarted after such an access. Cyclic calls of such an access enable the user to define monitoring intervals that are shorter than the 3.2 s implemented in the hardware. These access operations are also used for setting the limits for the INT1 frequency monitoring function. The recommended default value (and reset status) is 160 interrupts per time interval. The maximum interrupt frequency can be limited to 160 interrupts per second, for example, if such a call has been installed by EAVU-FBS in the corresponding cycle.

Write register 3 „master control"

The non-master CPU may also write in asynchronous mode into this redundant register which is used by the system software for controlling the EAVU mastership, i.e. selecting the CPU that has access to the I/O modules and non-redundant EAVU registers and defining the related criteria (cf. Chapters 3.2.1 and 3.2.3).

Value	Function
32H	CPU II becomes EAVU master (during synchronous operation)
22H	CPU II becomes EAVU master
44H	CPU I becomes EAVU master (during synchronous operation)
54H	CPU I becomes EAVU master
07H	N8-H master becomes EAVU master (reset status), normal mode
86H	No EAVU master, EE-/CPKL = 1, reset start-up flag
06H	No EAVU master, EE-/CPKL = 1

The registers are redundant (on the extension board); data can also be written to these registers in asynchronous mode. Each individual CPU acts upon its own enabling processes in asynchronous mode. Both CPUs must only agree on unconditional enabling of CPU II. CPU I can therefore have a decisive role during a "flying master change" in asynchronous mode.

Writing a value 06H or 86H disables both CPUs as EAVU masters and initiates a preliminary INT1 and PU5 inhibition on the basic board (which is released by any other register write operation or by EAVU reset). Disabling both CPUs as EAVU master causes (after 39 to 54 ms) EE-/CPKL = 1. Further access is only possible to the (redundant) jumper registers; such an access does not re-trigger the access watchdog. Watchdog time-out (3.5 to 4 s) resets the EAVU. EAVU reset is extended to approximately 200 ms, after this time it is started from the reset status. The watchdog function is not effective if the start-up flag is (still) set.

Write register 4 "EE-CPKL and EAVU I/O control OFF"
Write register 5 "EE-CPKL and EAVU I/O control ON"
Write register 6 "EE-CPKL ON"

Access will be ineffective if bits 0 to 2 of the write data item for these three registers have not been set to register number 4, 5 or 6. The other bits are irrelevant, their value is only reflected in the read-back data item (read register 1).

These access operations enable the system software to remove I/O module control and responsibility for jumper-selected I/O address ranges from the EAVU or to enable these functions.

Switching the EE-CPKL ON or OFF refers to the OC control of these lines by the EAVU. The software-controlled CPKL = 1 is not extended by the hardware; time restrictions for resetting I/O modules must be controlled by the software. This software control of the EE-CPKL signal also enables the user program to use the EAVU-FBS for resetting the I/O modules.

Write register 7 „EAVU system control"

Bits 6 to 3 are irrelevant when data is written into this register; their value is only reflected in read register 1.

Value written into the register					causes	Explanation
Bit 7	Bit 2	Bit 1	Bit 0	Dez.		
0	0	0	0	0	Nothing	1)
0	1	1	0	6	Reset start-up flag	2)
0	1	1	1	7	Set start-up flag	
1	0	1	0	130	Set common fault	
1	0	1	1	131	Reset fault	3)
1	1	0	0	132	Reset interrupt inhibitions	4)
1	1	0	1	133	Interrupt filter ON	5)
1	1	1	0	134	Interrupt filter OFF	5)

1) Writing 0 to this register has no effect.

2) These calls reset (6) or set (7) the start-up flag. The status after a hardware reset of the EAVU has been set. The EAVU access watchdog is de-activated if the start-up flag is set.

3) All fault flip-flops including the software-controlled common fault are reset. Interrupt inhibitions and counters are not influenced by this call. Resetting the software-controlled common fault is delayed by 50...100 microseconds in order to avoid impulses on the static and dynamic 24-V common fault line if the fault re-appears immediately.

4) All INT1 inhibitions are reset, including the ones for a permanent INT1. If a permanent INT1 is pending due to a fault, this access results in a (single) INT1 before permanent INT1 inhibition is set again. This access operation can be controlled by the FBS SYST-HBED.

5) The additional INT1 filter has been activated or de-activated. The state after start-up depends on the X2 filter jumper.

3.4 Monitoring and Error Indications

The following list contains the EAVU monitoring functions (-) with their indications and reactions (*):

-	Undervoltage of 24-V voltages	* Register bit transitions
-	Overvoltage of 24-V L + voltage	* Register bit transitions
-	Over- or undervoltage on 5-V bus	* EAVU reset, FMS, FMD
-	Total failure of L + < 12 V	* EAVU reset, FMS, FMD
-	L + failure	* Green LED OFF
-	PM failure	* Green LED OFF
-	L + failure	* Green LED OFF
-	Correct disappearance of INT1 (permanent)	* Register bit, INT inhibition
-	INT1 frequency	* Register bit, INT inhibition
-	Comparison of data, addresses and selects in the EAVU standby branch	* Register bits, PU5, FMS, FMD
-	Comparison of data, addresses and selects in the EAVU master branch	* Register bit transitions
-	Var. internal control signal discrepancies	* Register bit transitions
-	Watchdog for access to/via EAVU	* EAVU reset
-	Watchdog for external TEAVI clock	* Register bit transition, INT inhibit
-	Watchdog for internal clock pulse	* EAVU reset

Synchronization monitoring and PU5 are only possible in synchronous operation.

The access watchdog expires after approximately three seconds. It is re-triggered by each read or write access to a register (except jumper register) of the EAVU or an I/O module within the EAVU responsibility, and is only supposed to detect complete I/O access cessation due to hardware or software faults. The access watchdog is triggered by cyclic EAVU register access operations from the system software. EAVU reset caused by an expired watchdog is extended to at least 200 ms.

Once the EAVU has been reset, the access monitoring function that checks on too long a pause between two successive access operations only becomes active after the start-up flag has been reset by the system software. An EAVU that has been added in on-line mode is thus not permanently reset but can be successfully addressed and recognized by the software any time after it has been activated (for the first time).

3.4.1 Controls and Displays on the Front Panel

The following elements are arranged from top to bottom on the EAVU front panel: a green LED "ON", a green LED "L +", the module fuse, a larger red fault LED, a fuse and a green LED for PS, and a fuse and a green LED for PM. The fault LED and the module fuse are in the grey "fault bar" in the lower third of the front panel according to the usual front panel layout of TELEPERM M I/O modules.

The individual elements have the following meanings:

LED "ON" (green)

The green LED indicates that the EAVU has control over the I/O bus of the connected extension unit(s). The status after a reset depends on the jumper setting. The system software can activate and de-activate EAVU control over the associated extension unit(s). The EAVU interface to the EE-I/O bus is completely de-activated when control has been de-activated.

LED „fault" (red, blinking)

This blinking LED, which can be synchronized with the cabinet clock pulse (BS), is triggered if

- the 5-V bus supply voltage is out of tolerance
- the L + supply voltage is out of tolerance
- the module fuse has been removed
- the hardware interpretation of an access status indicates an EAVU fault in the single-channel part
- the common fault bit has been set.

The last possibility is used by the system software for indicating a fault on an EAVU or a related extension unit. The fault LED does not indicate if both L + and PM fail (e.g. after the circuit breaker in the SES has tripped or both front panel fuses have blown). The two green LEDs "L + " and "PM" are off in these cases. The blinking clock pulse in the cabinet has failed if, in these cases, the red fault LED lights permanently.

Provided that L + and PM are within their tolerances, a fault indication (including the ones set by the software) issues a static and a dynamic 24-V signal (FMS and FMD) which may be included in the hardware alarm concept (cabinet lamp, control room).

LED (green) and module fuse (F 1.6 A) „L + "

The module fuse protects the **L +** supply voltage of the EAVU. Removing the fuse resets the EAVU and enables the EAVU to be separated from the EE and CPU buses in a controlled manner.

Caution:

If L + has not been switched off at the SES circuit breaker, the module fuse must be removed before the EAVU can be removed or the front panel cables can be disconnected or connected. The fuse may only be re-inserted after the module has been installed.

The green LED is fed by the EAVU L + supply after the module fuse. The module fuse has blown or the L + supply voltage of the EE failed if this LED is extinguished.

LED (green) and fuse (F 1.6 A) „PS"

The EAVU supplies the 24-V signal voltage via this fuse and an X2 pin (b28) to certain I/O modules. This voltage also feeds the green LED. The signal voltage for the extension unit has failed if this LED is extinguished. This means in general that the PS fuse on the EAVU module or the extension unit L + supply from the SES has failed.

LED (green) and fuse (F 1.6 A) „PM":

The EAVU supplies the 24-V alarm voltage via this fuse and an EE bus line to the I/O modules. This voltage also feeds the green LED. The alarm voltage for the extension unit has failed if this LED is extinguished. This means that the PM fuse on the EAVU module or the extension unit L + supply from the SES has failed.

3.4.2 Power Supply Unit

The 5-V bus voltage is fed to the EAVU via the X1 top backplane connector, and the 24 V (L+) voltage via the bottom backplane connector. The following voltages are derived from L+, each decoupled via inductors, 1.6-A front panel fuses (quick-acting) and Schottky diodes:

- The internal L+ supply of the EAVU module. Total failure (<7 V) or removing the related fuse resets the EAVU.
- The PM alarm voltage for the EAVU and the I/O modules connected. This voltage is applied via the bottom backplane connector X2 to the PM bus line of the extension unit.
- The PS signal voltage. This voltage is routed via the bottom backplane connector X2 to the PS stripline of the extension unit (wrapped or connected by maxi-termi-points).

All three 24-V voltages are monitored for undervoltage conditions (<19.5 V). Undervoltage or overvoltage of the internal L+ (>33.5 V) appears as bit 4 = 1 in the fault register (7). The existence of these voltages is also indicated by green LEDs on the front panel. (These are fed by the same voltages; only a significant drop below the monitoring threshold will cause the LED to extinguish.)

The 5-V bus voltage is monitored for undervoltage or overvoltage conditions, the limits are 4.5 V and 6 V respectively. The EAVU is reset if this monitoring function responds.

Maximum generation with diodes provides a fault-tolerant 24 V voltage which is derived from the internal 24-V supply voltages L+ and PM (after the front panel fuses). This voltage feeds the blinking fault LED and the drivers for the 24-V signals FMS, FMD and Siml. Diode OR combinations and resistance-zener-diode dividers generate 5 V out of all three 24-V supply voltages (internal, PM and PS). A fault-tolerant 5-V supply for fault signal control (FMS, FMD) and voltage monitoring is generated from these voltages and the 5-V bus. The EE-PCKL pull-up resistor is also fed by a diode OR combination of all 5-V sources. This 1-active reset signal therefore only disappears together with the last extension unit supply voltage.

Faults in the 24-V supply become obvious to the system software via an EAVU register bit. Faults in the 5-V supply are indicated as a malfunction (FMS = LED, FMD) and reset the EAVU. 5-V undervoltage is simulated and EAVU reset triggered if the front panel fuse has been removed or L+ dropped below approximately 6 V (e.g. after the corresponding circuit breaker in the SES has tripped). The module fuse **must be** removed **or** the extension unit supply switched off before the EAVU or a front panel ribbon cable can be removed.

3.4.3 Error Considerations

Due to internal redundancies, comparators and monitoring functions, most of the faults are self-signalling in normal operation or can easily be detected and located by the system software.

Passive (i.e. without effect) failure of the INT1 monitoring and decoding function is completely irrelevant if the EAVU is not associated to an SF61 module. Since the INT1 monitoring function of an EAVU with SF61 module should not respond during normal process operation and without I/O module faults, only few defects of these circuit parts remain hidden. Occasional repetition tests are recommended. If, for example, the /INT1 line of the extension unit is manually connected with earth, the monitoring function should respond to a permanent INT1 signal. The software can test the entire INT1 signal path, even outside normal operation, irrespective of the occurrence of real process alarms if the software-controlled 24-V EAVU output Siml is connected to an alarm input of its SF61 (either directly or via an interrupt-generating binary input module). Using special test software makes it also possible to initiate interrupts in quick succession such that the frequency monitoring function must respond and is tested. The frequency monitoring function can also be tested by connecting a non-earthed square-wave generator with TTl-OC output to the EE-/INT1 line.

Faults on the double-redundant I/O bus lines are immediately detected in synchronous mode during the first access operation affected and signalled in redundant manner to the CPUs (PU5). The majority of these faults is also detected by the comparators on the VKB. The system software then interrupts process execution and locates the fault in the central unit. The system then continues with the faultless CPU as N8-H and EAVU master. Such a CPU-I/O bus fault can be caused by faults on the lines, the EABAs or one of the EAVUs connected. Its effect on the I/O or EAVU registers depends on the fact whether or not the faulty CPU was EAVU master during the last access. Only an EAVU register or an I/O output byte can be incorrectly set if the fault has occurred in the EAVU master CPU and during a write access. The former can be corrected by the system software overwriting all significant EAVU registers after fault finding has been terminated and before on-line operation is resumed. The latter is corrected by the user program in the next cycle. Since such a brief malfunction caused by an incorrect access operation after a CPU fault can only affect one I/O fault delimitation area, a possibly configured I/O redundancy proves also useful in this case.

Faults in the single-channel part of the EAVU and in particular in the interface to the I/O bus can disturb access to the extension unit in the same way as certain I/O module faults. Standard configuration with a high number of I/O fault delimination areas and a suitable redundancy image of I/O modules is a good method to prevent such a loss of an I/O delimination area which also proves effective against a large class of malfunctions.

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4 Installation and Commissioning

4.1 EAVU Connection

The EAVU module is installed in slot no. 14 of the extension unit (the slot at the extreme right-hand side, seen from the front).

The upper backplane connector X1 connects to the power supply module of the extension unit and, via the bus board of the extension unit, to the I/O modules in the extension unit (5-V bus, EE-I/O bus).

The lower backplane connector X2 connects to the cabinet power supply unit (24-V supply used for generating 24-V signals). The necessary jumpering must also be made at this connector (see Chapter 4.4).

The ribbon cable from CPU I (cable duct) is plugged into the upper front connector X3; the ribbon cable from CPU II is plugged into the lower front connector X4.

The topmost fuse in the front panel protects the module power supply, the two other fuses protect the PS signal voltage (centre) and the PM alarm voltage (bottom).

Caution

The module fuse may not be installed before the module has been inserted, and must be removed when the module is removed without the module power supply being switched off.

Four of the five LEDs on the front panel are on during faultless operation. The fifth LED (below the module fuse) lights up in the event of a failure.

4.2 I/O Module Address Ranges

Figs. 4.1 and 4.2 give an overview of the I/O address ranges and the possible jumper settings. Some of the represented responsibilities can be enabled for an EAVU. The system software ensures that only one single EAVU with activated I/O bus interface is responsible for an I/O address range.

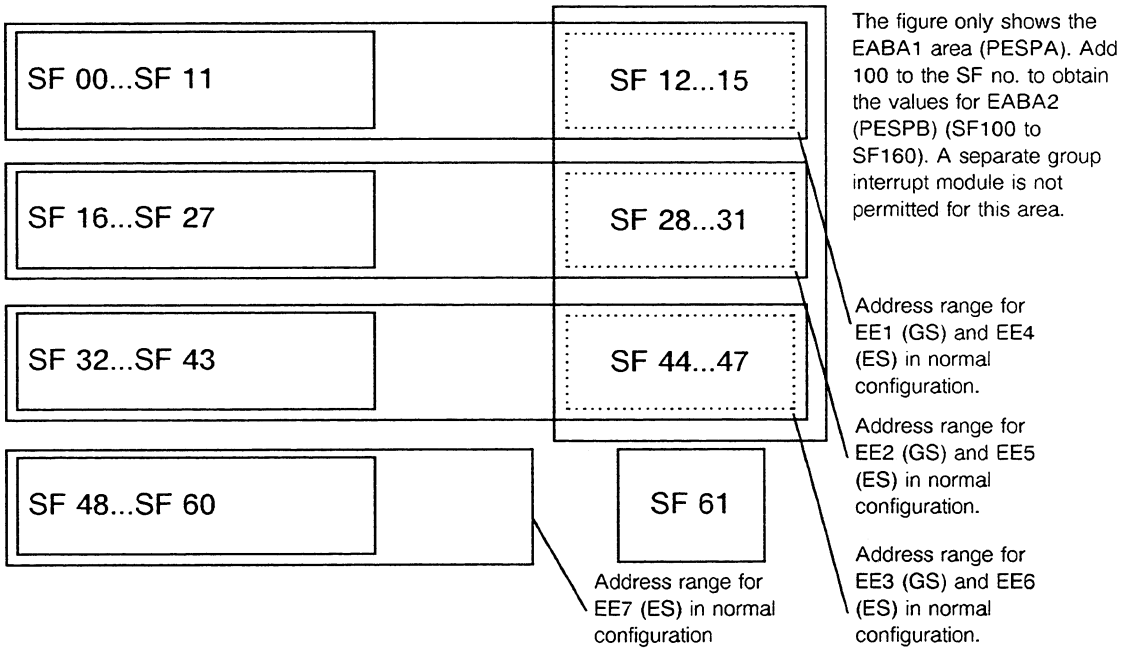


Fig. 4.1 Peripheral address range for PESPA

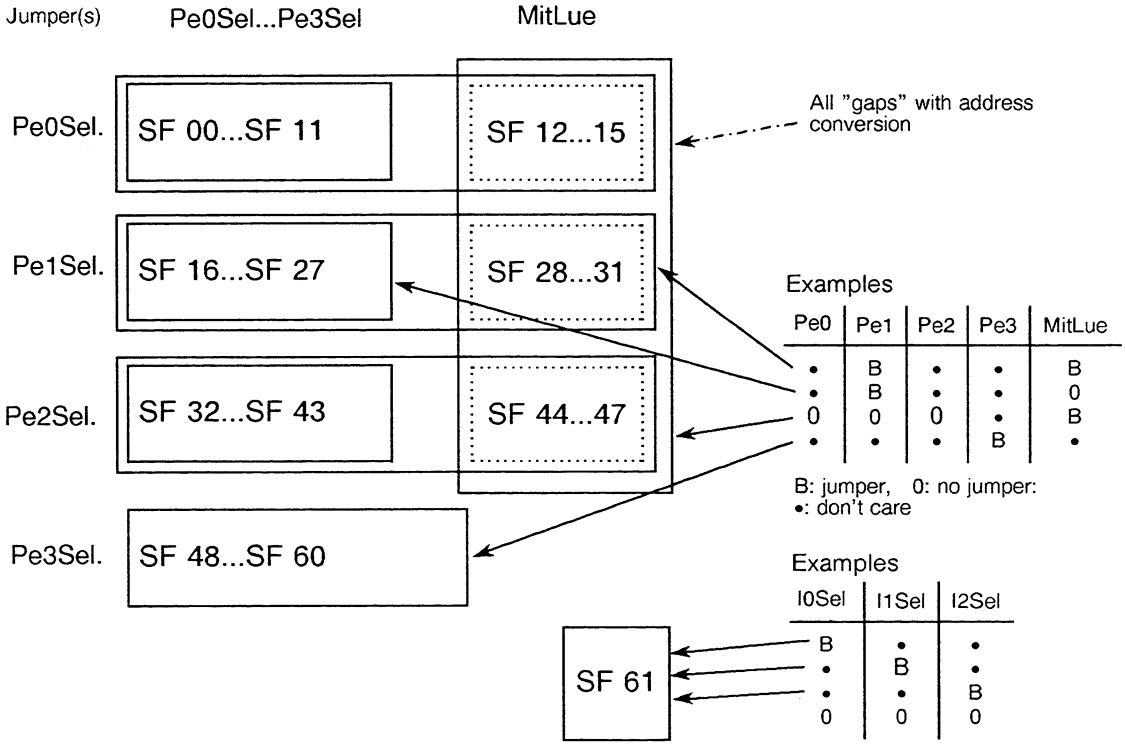


Fig. 4.2 Jumper settings to peripheral address ranges

Basic cabinet, EABA 1 (PESPA)

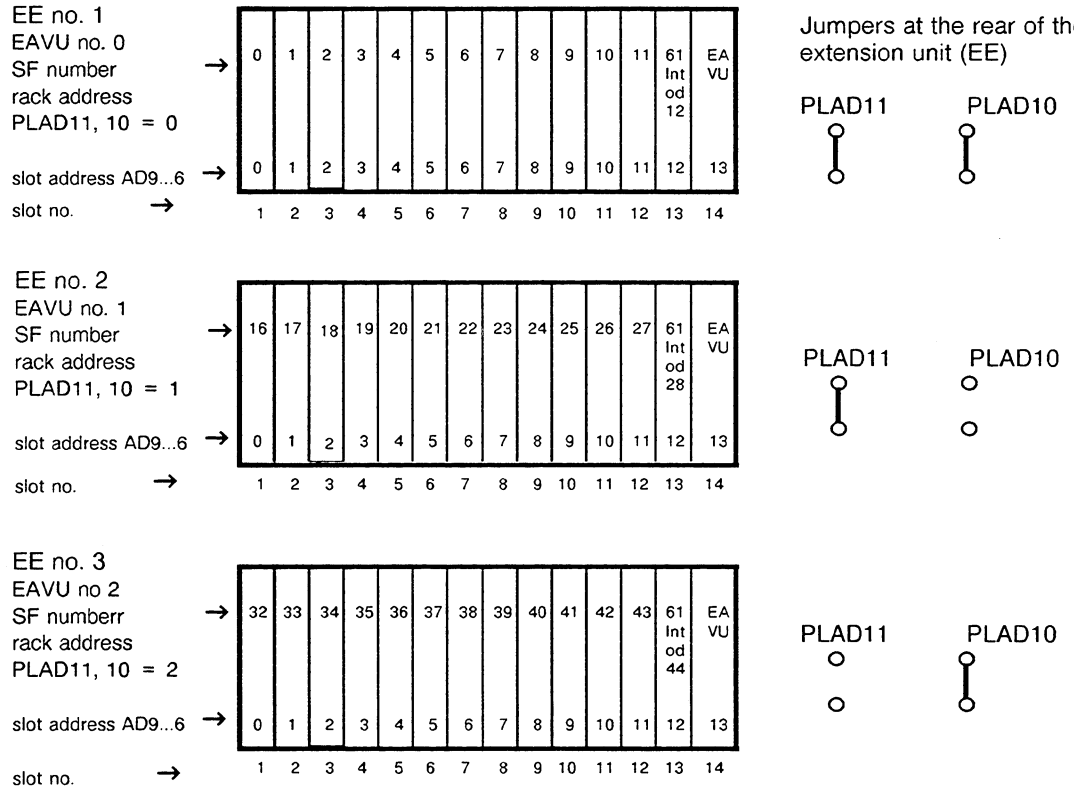


Fig. 4.3 Peripheral slot addresses in the basic cabinet

Extension cabinet EABA 2 (PESPB)

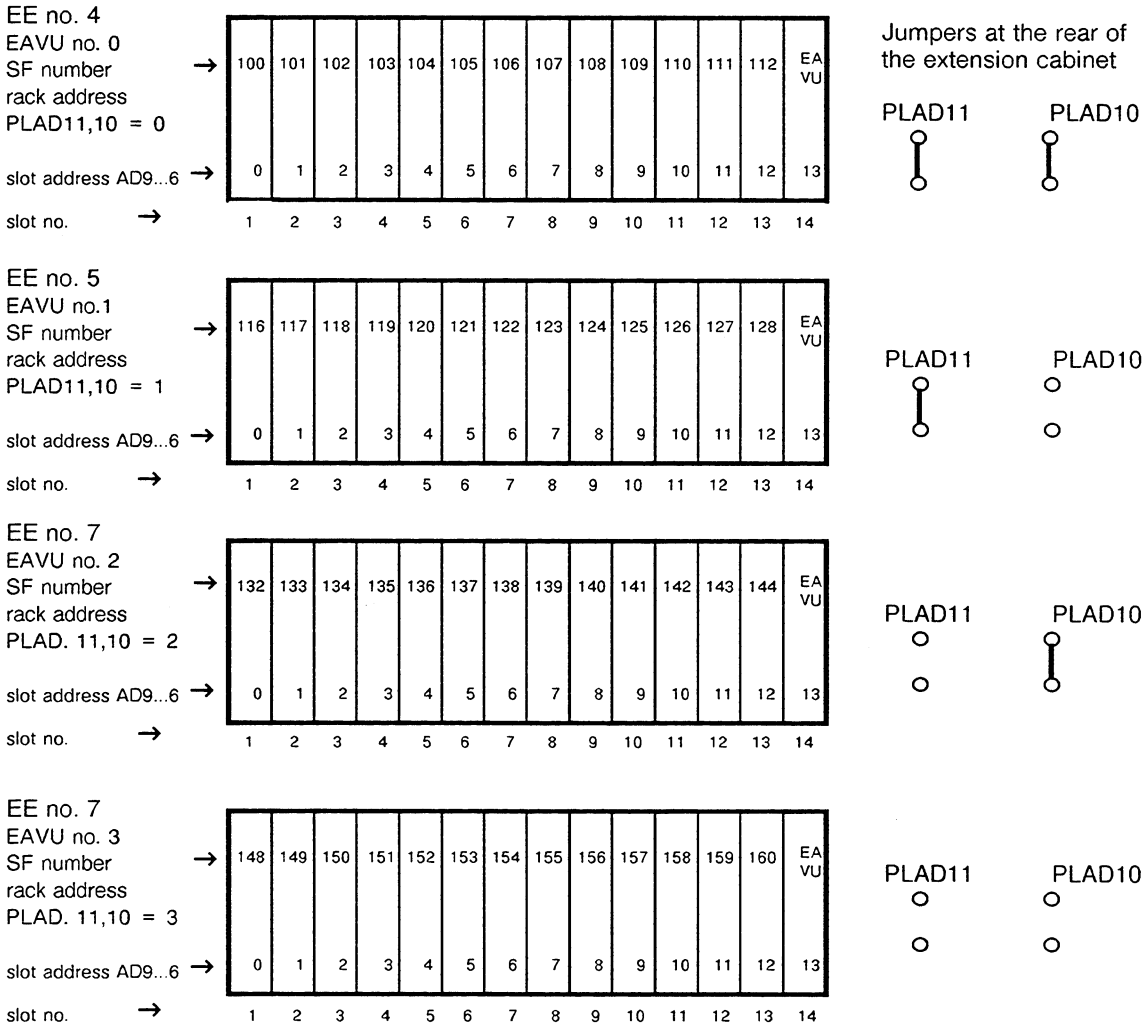


Fig. 4.4 Peripheral slot addresses in the extension cabinet

4.3 Connector Pin Assignments

The following figure shows the connector pin assignments of the individual EAVU connectors.

X1

Pin No.	d	b	z
2		0 V ■	+5 V ■
4	/PMEMW	/PMEMR	+5 V
6	0 V	/PRDY	
8	/PCPKL		PPESP
10	0 V	/INT2	/INT1
12	EANK	/INT4	/INT3
14	0 V	PDB1	PDB0
16	PDB4	PDB3	PDB2
18	PDB7	PDB6	PDB5
20	0 V	PADB1	PADB0
22	PADB4	PADB3	PADB2
24	PADB7	PADB6	PADB5
26	PADB10	PADB9	PADB8
28	PLAD7 [1)]	0 V	PADB11
30	PLAD10	PLAD9 [1)]	PLAD8 [1)]
32	PLAD6 [1)]	0 V ■	PALD11

1) = not assigned with EAVU ■ = protruding pin

Fig. 4.5 X1 backplane connector

All X1 backplane connectors of an extension unit are interconnected.

X2

	Pin No.	f	d	b	z	
1)	2	RESBR 1	DTI0SUB	0 V	0 V	_ I
	4	/Pe0Fg	0 V	/Pe1Fg	/FILTER	
	6	/Pe2Fg	0 V	/Pe3Fg	0 V	
	8	/I0Fg	0 V	/I1Fg	/I2Fg	
	10	NRMSB	0 V	/MITL	0 V	
	12	NRLSB	0 V	/I2B4	MSPA	
	14	RESBR2	DTI0SUB	0 V		_ II
	16	/PE0Fg	0 V	/PE1Fg	MSPE	
	18	/PE2Fg	0 V	/PE3Fg	0 V	
	20	/I0Fg	0 V	/I1Fg	/I2Fg	
	22	NRMSB	0 V	/MITL	0 V	
	24	NRLSB	0 V	/I2B4	DEFON	
	26	0 V			0 V	
	28	FMS (24V common fault)	FMD (SF dynamic)	PS (24 V after fuse)	SIML	
2)	30	LT (lamp test) not used	BS (blinking voltage	PM (24V alarm)		
	32	L + (24 V)	L + (24 V)	M	M	

■ = protruding pin

1) Wrap pins or maxi-termi-point
2) Bus board
_ I CPU I area
_ II CPU II area

Fig. 4.6 X2 backplane connector

X3 /X4

Pin No.			
1	**0 V**	**0 V**	2
3	SYNC_ N		4
5	TEAVI	**0 V**	6
7			8
9	PMR _N	PMW_ N	10
11	**0 V**	**0 V**	12
13	/PRDY_N	PPESP 1	14
15		PCPKL_N	16
17	**0 V**	INT1_N	18
19	INT2_N	INT3_N	20
21	INT4_N	PEANK	22
23	**0 V**	PDB6	24
25	PDB7	PDB2	26
27	PDB3	PDB4	28
29	PDB5	PDB0	30
31	PDB1	**0 V**	32
33	**0 V**	PADB9	34
35	PADB10	PADB11	36
37	PADB3	PADB4	38
39	PADB5	PADB6	40
41	PADB7	PADB8	42
43	PADB0	PADB1	44
45	PADB2	**0 V**	46
47	MAST_N	**0 V**	48
49	FSIG_N	**0 V**	50

Fig. 4.7 X3 and X4 front connectors

X3 Pin assignment to CPU I Signal names have the suffix _I
X4 Pin assignment to CPU II Signal names have the suffix _II

4.4 Jumper Settings

Significant jumper settings on the EAVU must be double-redundant and identical in order to be able to limit and locate faults. Different settings of such jumpers normally result in an asynchronous operation (PU5) of the CPUs. All jumper settings required for AS 235 operation must be wrapped at the rack part of the lower backplane connector X2 or established by maxi-termi-point connections. There is only one single jumper installed on the EAVU module itself which is used for the module self-test, all other jumper connections on the EAVU are open. This means that there are no application-, system- or EE-specific jumper settings on the EAVU module which could cause problems when the module is replaced.

- Jumpers on the basic board

X30/ 1 – 2: Module test jumper, always inserted. This jumper may **not** be removed.

- Jumpers on the extension board

The two 32-way double-row male edge connectors X11 and X12 on the upper and lower edge of the extension board are redundant to one another. X11 at the upper edge is responsible for area I, X12 for area II. Fig. 4.8 shows the pin assignments and possible jumper settings. The brought-out signals are test signals, the possible jumpers are only relevant for service purposes and special modes. All X11 and X12 jumpers are open in normal AS 235 mode.

X11 / X12

0 V	1	2	0 V
SS N	3	4	MS N
P5V	5	6	P5V
P5V	7	8	NMM
	9	10	PON
PVI	10	12	PESEL
INTS N	13	14	/REGS
MC	15	16	BRRG N
SF61 EPLD-Tst	17	18	SF62 EPLD-Tst
SF62_BER not connected EPLD-Tst	19	20	TRLAT ELPD-Tst
IntSot	21	22	RWQU
RD from CPU	23	24	WR from CPU
RDY_N prior to driver to CPU	25	26	PESP N from CPU
FSIGF	27	28	DETV N to EPLD
0 V	29	30	0 V
	31	32	

Jumpers:
1 – 3 Sync signal is forced
2 – 4 Master signal is forced
3 – 5 Sync signal is inhibited
4 – 6 Master signal is inhibited
7 – 8 The interface to the EABA I/O bus is only enabled for the EAVU master
27 – 29 PU5 fault signal is inhibited
28 – 30 Alternative address decoding is activated

X11 Signal names with suffix –I (CPU I)
X12 Signal names with suffix –II (CPU II)

All jumpers are open in normal operation.

Fig. 4.8 X11/X12 test and jumper connectors

- Jumper settings at the X2 backplane connector of the extension unit

X2 / z12 – z16
The EAVU cannot exit reset status if this jumper has not been installed. A missing jumper has a similar effect as a removed module fuse. This jumper requirement makes it impossible for an EAVU to be started in an unprepared slot without any X2 jumpers.
The tables below utilize the following symbols: "**B**" for a jumper to 0 V, "**o**" for open and "• " (no entry) means that this jumper is irrelevant here. The following pins of the X2 backplane connector are connected with 0 V: b2, d4, d6, d8, d10, d12, z6, z10 (for jumpers I and spare jumper 2), z2 (for the filter jumper), z26 (for DefOn), f26, and z26. These 0-V pins make it possible to establish any necessary jumper setting to a neighbouring 0-V pin using wrap or maxi-termi-point connections. Never interconnect pins of double-redundant jumpers and establish a common wrap connection to 0 V. A single fault (broken wire, poor pin contact) could impair both redundant EAVU parts and thus both CPUs.

Name Pin I Pin II	ENMSB f10 f22	ENLSB f12 f24		Normal assignment EE no. in		with RaAd
				GS	ES	
	B	B	EAVU no. = 0	1	4	0
	B	o	EAVU no. = 1	2	5	1
	o	B	EAVU no. = 2	3	6	2
	o	o	EAVU no. = 3		7, 7a	3

The EAVU number is defined by these 2x2 jumpers to f10, f12 and f22, f24. Each EAVU pair must have EAVU numbers; the same EAVU number may not be assigned to two different EAVUs within a PESP area. The EAVU number specifies the address range of the EAVU registers within the 64 bytes of the address range SF61 (EABA1, PESPA) and SF61 (EABA2, PESPB).
Configuration recommendation: wrap the EAVU number bits according to the rack address bits PLAD10 and PLAD11 (see last column "RaAd" in the table above). The rack address bits are set by soldering jumpers on the extension unit backplane.
Up to three EAVU modules with the numbers 0 to 2 that are assigned to the EABA1 modules can be accommodated in the basic cabinet. Up to four EAVU modules with the numbers 0 to 3 that are assigned to the EABA2 modules can be accommodated in the extension cabinet. These specifications and the three columns at the right-hand side of the table above refer to the recommended normal configuration.

Name Pin I Pin II	MitL b10 b22	/Pe3Fg b6 b18	/Pe2Fg f6 f18	/Pe1Fg b4 b16	/Pe0Fg f4 f16	EAVU is responsible for address range
	B	•	•	•	B	SF×00...SF×15
	o	•	•	•	B	SF×00...SF×11
	B	•	•	B	•	SF×16...SF×31
	o	•	•	B	•	SF×16...SF×27
	B	•	B	•	•	SF×32...SF×47
	o	•	B	•	•	SF×32...SF×43
	B	•	o	o	o	gaps translated
	•	B	•	•	•	SF×48...SF×60

(× is 0 for PESPA and 1 for PESPB)

These 2x5 jumpers to f4, b4, f6, b6, b10 and f16, b16, f18, b18, b22 specify for which I/O module and signal interface module ranges (SF00 to SF60 for EABA1, i.e. basic cabinet, PESPA, and SF100 to SF160 for EABA2, i.e. extension cabinet, PESPB) the EAVU is responsible (**B**) or not responsible (**o**). Each existing extension unit (i.e. its slot range) must have exactly one responsible EAVU.Exactly one jumper pair (out of the first four) must be inserted for one EAVU per extension unit. This is the one which corresponds to the rack address (PLAD11, PLAD10) and the EAVU number.

The MitL jumper must be inserted in normal configuration if at least one of the jumper pairs Pe0, Pe1 or Pe2 has been inserted. Two or more of the above-mentioned address ranges may be contiguously enabled for an EAVU if three or less extension units and EAVU modules per PESP area or special modules with an address range exceeding 64 bytes (i.e. special communication modules) are used. These jumper settings can be read via registers; this enables the system software to check I/O configuration and validity of configuration during initialization.

Name Pin	ResBr1 f2	ResBr1 f14	DefOn z24	After reset, the EAVU has
	• •	• •	o B	control over EE no control over EE

The first two of these three non-redundant jumpers to f2, f14 and z24 are irrelevant spare jumpers. The DefOn jumper to z24 specifies whether (o) or not (B) the EAVU has control over its extension unit after a reset has been performed. If the DefOn jumper is not inserted (normal state), the EAVU assumes control over the connected I/O modules after a hardware reset has been performed. No further system software activities ar required, and the application program can perform the necessary I/O access operations via the EAVU. The system software can read the status of these three jumpers from the EAVU status register.

Name Pin	/Filter z4	An INT1 interrupt signal is (with T = 1.5 ms digital) additionally
	B o	filtered not filtered

The non-redundant jumper to z4 specifies whether the INT1 signals (apart from synchronization with the TEAVI clock pulse) are passed without delay or whether the additional INT1 filter function on the EAVU is enabled. The effect of this filter is that two or three interrupts from redundant SF61 modules which occur within a time window whose width is specified by the filter time are processed by the central unit as **one single** interrupt (not as two or three different interrupts). Such interrupts in quick succession from redundant SF61 modules are caused by the tolerances of the analog input filters (T = 1.5...3 ms) if redundant or fanned-out alarm signals are (directly or indirectly) connected to redundant SF61 modules in a redundant manner. The same event without EAVU filter could trigger multiple interrupts. There is no disturbance from these multiple interrupts apart from increased cycle load. Redundant interrupt connection therefore requires the choice between a slightly increased cycle load and a slightly delayed interrupt signal. The filter function should be enabled for all EAVU modules concerned if it is considered expedient in a redundant SF61 configuration.

Name Pin I Pin II	/I0Fg f8 f20	/I1Fg b8 b20	/I2Fg z8 z20	EAVU resp. for INT1 group primary	 secondary	 tertiary	Filter
	o	o	o	none	none	none	
	B	o	o	I0	I1	I2	*
	o	B	o	I1	I2	I0	*
	o	o	B	I2	I0	I1	*
	B	B	o	I0, 1	I2	none	*
	B	o	B	I0,2	I3	none	*
	o	B	B	I1,2	I0	none	*
	B	B	B	I0, 1, 2	none	none	

Enabling the filter function is recommended for configurations marked by *; using the DatI0Sub jumper is relevant.

These 2x3 jumpers to f8, b8, z8 and f20, b20, z20 specify whether (any B) or not (ooo) the EAVU is responsible for an SF61 group interrupt module. Primary, secondary or tertiary responsibility of the EAVU for the three groups of 16 interrupts can also be specified within the possible software-transparent interrupt redundancies.

Configuration rules: These jumpers may only be inserted in EAVU modules associated to EABA1 (PESPA, basic cabinet) whose extension units contain exactly one SF61 group interrupt module in EE slot number 13. None of the three jumper pairs may be inserted more than once in all EABA1-EAVUs; any one pair should be inserted either exactly once or not at all. In other words: there is either no interrupt or exactly one EAVU has primary responsibility for each interrupt area. The jumper settings can be read via registers; these rules can therefore be verified by the system software.

Name Pin I Pin II	DtI0Subst d2 d14	If this EAVU is used as secondary or tertiary replacement for reading SF61 bytes from an interrupt module
	B o	SF61 data is read 0 data is supplied

This redundant jumper setting to d2 and d14 is only relevant if the EAVU is responsible for an SF61 group interrupt module and if the redundancy function is used for the group interrupt module. Either the input data of the redundant SF61 module can be read or zero data can be permanently issued (this means for the system software that no interrupt is pending) if, due to a failure of the primarily responsible SF61 or EAVU module, another module must take over for reading the SF61 bytes. The process alarms must be connected in redundant fashion to the corresponding inputs of the SF61 module if the first case is selected. (The system software can solely detect the jumper settings for I; both redundant jumpers must always be in the same position.)

Connection of ES 100 K systems

If there is an empty extension unit (EE) in either the basic cabinet (GS) or the extension cabinet (ES) it is possible to connect an ES 100 K system instead. The interface module required in such a case (i.e. 6DS1322-8BA) has to be installed in one of the existing extension units.

Even if the basic cabinet and the extension cabinet are fully equipped with three or four EEs respectively, another two ES 100 K systems can be connected to the basic cabinet and one more ES 100 K to the extension cabinet.

In order to ensure that the additional I/O modules installed in an ES 100 K are addressable the slot addresses (SF number) used in the ES 100 K must be enabled for the EAVU concerned by additional jumpers on the EAVU backplane connector (X2).

The jumper settings to be made on the backplane connector X2 of the EAVU in respect of ES 100 K systems are described in Chapter 4.7.6 of the AS 235 H Instructions (Order No. C79000-B8076-C293).

- Summary of the possible jumper assignments

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z
2	RESBR 1	DtI0Sub	0 V	0 V
4	/Pe0Fg	0 V	/Pe1Fg	/FILTER
6	/Pe2Fg	0 V	/Pe3Fg	0 V
8	/I0Fg	0 V	/I1Fg	/I2Fg
10	NRMSB	0 V	/MITL	0 V
12	NRLSB	0 V	/I2B4	MSPA
14	RESBR2	Dt0Sub	0 V	1)
16	/Pe0Fg	0 V	/Pe1Fg	MSPE
18	/Pe2Fg	0 V	/Pe3Fg	0 V
20	/I0Fg	0 V	/I1Fg	/I2Fg
22	NRMSB	0 V	/MITL	0 V
24	NRLSB	0 V	/I2B4	DEFON
26	0 V			0 V
28	FMS 2)	FMD 2)	PS 3)	SIMI 4)
30		BS	PM (24 V alarm)	
32	L+ (24 V)	L+ (24 V)	M	M

5) wraps pins 2 to 28; 6) bus board (pins 30, 32)

_I
_II

●···● Jumper possible
●—● Jumper necessary
●↘ Connection possible
■ Protruding pin
_I for CPU I
_II for CPU II

1) Jumper z12-z16 must always be inserted; otherwise the EAVU remains in a reset state.
2) Static and dynamic 24-V fault alarm signals; may be connected to a conventional signalling system.
3) 24-V signal voltage PS; must be connected to the EE stripline if required.
4) 24-V test signal output; may be connected to a binary input.
5) Wrap pins or maxi-termi-point pins.
6) Bus board

Fig. 4.9 Summary of all jumpers on the X2 backplane connector

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub	0 V	0 V	
4	/Pe0Fg ●—●	0 V	/Pe1Fg	/FILTER	
6	/Pe2Fg	0 V	/Pe3Fg	0 V	_I
8	/I0Fg	0 V	/I1Fg	/I2Fg	
10	NRMSB ●—●	0 V	/MITL ●···● 4)	0 V	
12	NRLSB ●—●	0 V	/I2B4	MSPA ●	
14	RESBR2	Dt0Sub	0 V		5)
16	/Pe0Fg ●—●	0 V	/Pe1Fg	MSPE ●	
18	/Pe2Fg	0 V	/Pe3Fg	0 V	
20	/I0Fg	0 V	/I1Fg	/I2Fg	_II
22	NRMSB ●—●	0 V	/MITL ●···● 4)	0 V	
24	NRLSB ●—●	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	
30		BS	PM (24V alarm)		6)
32	L+ (24 V)	L+ (24 V)	M ■	M	

●···● = Jumper possible

●—● = Jumper necessary

●↘ = Connection possible

■ = Protruding pin

_I for CPU I

_II for CPU II

For EE	:	1 in GS or 4 in ES
EAVU no.	:	0 (or 100 for ES)
I/O module range	:	SFx0...SFx15
or		SFx0...SFx11

4) The smaller I/O module address range results if the MitL jumper pair has not been inserted.
5) Wrap pins or maxi-termi-point pins.
6) Bus board

Fig. 4.10 X2 backplane connector: jumpers for EE 1 and EE 4

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub	0 V	0 V	
4	/Pe0Fg	0 V	/Pe1Fg	/FILTER	
6	/Pe2Fg	0 V	/Pe3Fg	0 V	_I
8	/I0Fg	0 V	/I1Fg	/I2Fg	
10	NRMSB	0 V	/MITL	4) 0 V	
12	NRLSB	0 V	/I2B4	MSPA	
14	RESBR2	Dt0Sub	0 V		5)
16	/Pe0Fg	0 V	/Pe1Fg	MSPE	
18	/Pe2Fg	0 V	/Pe3Fg	0 V	
20	/I0Fg	0 V	/I1Fg	/I2Fg	_II
22	NRMSB	0 V	/MITL	4) 0 V	
24	NRLSB	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	
30		BS	PM (24V alarm)		6)
32	L+ (24 V)	L+ (24 V)	M	M	

●···● Jumper possible

●—● Jumper necessary

●↘ Connection possible

■ Protruding pin

_I for CPU I

_II for CPU II

for EE : 2 in GS or 5 in ES
EAVU no. : 1 (or 101 for ES)
I/O module range : SFx16...SFx31
or SFx16...SFx27

4) The smaller I/O module address range results if the /MitL jumper pair has not been inserted.
5) Wrap pins or maxi-termi-point pins.
6) Bus board

Fig. 4.11 X2 backplane connector: jumpers for EE 2 and EE 5

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub	0 V	0 V	
4	/Pe0Fg	0 V	/Pe1Fg	/FILTER	
6	/Pe2Fg ●—●	0 V	/Pe3Fg	0 V	
8	/I0Fg	0 V	/I1Fg	/I2Fg	_I
10	NRMSB	0 V	/MITL ●···●	4) 0 V	
12	NRLSB ●—●	0 V	/I2B4	MSPA ●	
14	RESBR2	Dt0Sub	0 V		
16	/Pe0Fg	0 V	/Pe2Fg	MSPE ●	
18	/Pe2Fg ●—●	0 V	/Pe3Fg	0 V	
20	/I0Fg	0 V	/I1Fg	/I2Fg	_II
22	NRMSB	0 V	/MITL ●···●	4) 0 V	
24	NRLSB ●—●	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	
30		BS	PM (24V alarm)		
32	L + (24 V)	L + (24 V)	M ■	M	

5) wraps pins 2–28; 6) bus board

●···● Jumper possible

●—● Jumper necessary

■ Protruding pin

_I for I/O bus I

_II for I/O bus II

for EE	:	3 in GS or 6 in ES
EAVU no.	:	2 (or 102 for ES)
I/O module range	:	SFx32...SFx47
or		SFx32...SFx43

4) The smaller I/O module address range results if the /MitL jumper pair has not been inserted.

5) Wrap pins or maxi-termi-point pins.

6) Bus board

Fig. 4.12 X2 backplane connector: jumpers for EE 3 and EE 6

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub	0 V	0 V	
4	/Pe0Fg	0 V	/Pe1Fg	/FILTER	
6	/Pe2Fg	0 V	/Pe3Fg	0 V	
8	/I0Fg	0 V	/I1Fg	/I2Fg	_I
10	NRMSB	0 V	/MITL	0 V	
12	NRLSB	0 V	/I2B4	MSPA	
14	RESBR2	Dt0Sub	0 V		
16	/Pe0Fg	0 V	/Pe1Fg	MSPE	
18	/Pe2Fg	0 V	/Pe3Fg	0 V	
20	/I0Fg	0 V	/I1Fg	/I2Fg	_II
22	NRMSB	0 V	/MITL	0 V	
24	NRLSB	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	5)
30		BS	PM (24V alarm)		6)
32	L+ (24 V)	L+ (24 V)	M	M	

●—● Jumper necessary

■ Protruding pin

_I for CPU I

_II for CPU II

for EE	:	7 in ES
EAVU no.	:	103
I/O module range	:	SF148...SF160

5) Wrap pins or maxi-termi-point pins

6) Bus board

Fig. 4.13 X2 backplane connector: jumpers for EE 7

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub	0 V	0 V	_I
4	/Pe0Fg	0 V	/Pe1Fg	/FILTER	
6	/Pe2Fg	0 V	/Pe3Fg	0 V	
8	/I0Fg	0 V	/I1Fg	/I2Fg	
10	NRMSB	0 V	/MITL ●—● 4)	0 V	
12	NRLSB	0 V	/I2B4	MSPA	
14	RESBR2	Dt0Sub	0 V		_II
16	/Pe0Fg	0 V	/Pe2Fg	MSPE	
18	/Pe2Fg	0 V	/Pe3Fg	0 V	
20	/I0Fg	0 V	/I1Fg	/I2Fg	
22	NRMSB	0 V	/MITL ●—● 4)	0 V	
24	NRLSB	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	
30		BS	PM (24V alarm)		
32	L+ (24 V)	L+ (24 V)	M	M	

5) 6)

●—● Jumper necessary

■ Protruding pin

_I for CPU I

_II for CPU II

for EE : 7a (alternative assignment) in ES
EAVU no. : 103
I/O module range : SF112...115, 128...131, 144...147
Translated into SF100...103, 104...107, 108...111

4) The MITL jumper pair may not be inserted on any other EAVU if this jumper setting has been selected.
5) Wrap pins or maxi-termi-point.
6) Bus board

Fig. 4.14 X2 backplane connector : alternative jumper assignment for EE 7

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub ●···● 3)	0 V	● 2)	0 V
4	/Pe0Fg	0 V	/Pe1Fg	● /FILTER	
6	/Pe2Fg	0 V	/Pe3F	0 V	
8	/I0Fg ●—●	0 V	/I1Fg	/I2Fg	_I
10	NRMSB	0 V	/MITL	0 V	
12	NRLSB	0 V	/I2B4	MSPA	
14	RESBR2	Dt0Sub ●···● 3)	0 V		
16	/Pe0Fg	0 V	/Pe1Fg	MSPE	
18	/Pe2Fg	0 V	/Pe3Fg	0 V	
20	/I0Fg ●—●	0 V	/I1Fg	/I2Fg	_II
22	NRMSB	0 V	/MITL	0 V	
24	NRLSB	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	
30		BS	PM (24V alarm)		
32	L+ (24 V)	L+ (24 V)	M	M	

5) 6)

●—● Jumper necessary

●···● Jumper possible

■ Protruding pin

_I für I/O bus I

_I für I/O bus II

Primarily responsible for : I0 alarms 1 to 6

2) Filter jumpers recommended.
3) Jumper pair required if the other alarms have also been connected in redundant fashion.
5) Wrap pins or maxi-termi-point pins.
6) Bus board

Fig. 4.15 X2 backplane connector: jumpers for the first redundant group interrupt module

These jumper settings are to be performed in addition to the ones shown in Figs. 4.10 to 4.14.

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub ●···●	● 3) 0 V	● 2) 0 V	
4	/Pe0Fg	0 V	/Pe1Fg	● /FILTER	
6	/Pe2Fg	0 V	/Pe3Fg	0 V	
8	/I0Fg	0 V ●—●	/I1Fg	/I2Fg	_I
10	NRMSB	0 V	/MITL	2) 0 V	
12	NRLSB	0 V	/I2B4	MSPA ●	
14	RESBR2	Dt0Sub ●···●	3) 0 V		5)
16	/Pe0Fg	0 V	/Pe1Fg	MSPE ●	
18	/Pe2Fg	0 V	/Pe3Fg	0 V	
20	/I0Fg	0 V ●—●	/I1Fg	/I2Fg	_II
22	NRMSB	0 V	/MITL	0 V	
24	NRLSB	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	
30		BS	PM (24V alarm)		6)
32	L+ (24 V)	L+ (24 V)	M	M	

●—● Jumper necessary

●···● Jumper possible

■ Protruding pin

_I for I/O bus I

_II for I/O bus II

Primarily responsible for : I1 alarms 17 to 32

2) Filter jumpers recommended.
3) Jumper pair required if the other alarms have also been connected in redundant fashion.
5) Wrap pins or maxi-termi-point pins.
6) Bus board

Fig. 4.16 X2 backplane connector: jumpers for the second redundant group interrupt module

These jumper settings are to be performed in addition to the ones shown in Figs. 4.10 to 4.14.

X2 Seen from behind, lower left-hand female backplane connector in the extension

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub ●···●	3) 0 V	● 1) 0 V	
4	/Pe0Fg	0 V	/Pe1Fg	● /FILTER	
6	/Pe2Fg	0 V	/Pe3Fg	0 V	_I
8	/I0Fg	0 V	/I1Fg	● /I2Fg	_I
10	NRMSB	0 V	/MITL	0 V	_I
12	NRLSB	0 V	/I2B4	MSPA	_I
14	RESBR2	Dt0Sub ●···●	3) 0 V		_II
16	/Pe0Fg	0 V	/Pe1Fg	MSPE	_II
18	/Pe2Fg	0 V	/Pe3Fg	0 V	_II
20	/I0Fg	0 V	/I1Fg	● /I2Fg	_II
22	NRMSB	0 V	/MITL	0 V	_II
24	NRLSB	0 V	/I2B4	DEFON	_II
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	5)
30		BS	PM (24V alarm)		6)
32	L+ (24 V)	L+ (24 V)	M	M	6)

●—● Jumper necessary

●···● Jumper possible

■ Protruding pin

_I for CPU I

_II for CPU II

Primarily responsible for : I2 alarms 33 to 48

2) Filter jumpers recommended.
3) Jumper pair required if the other alarms have also been connected in redundant fashion.
5) Wrap pins or maxi-termi-point pins.
6) Bus board

Fig. 4.17 X2 backplane connector: jumpers for the third redundant group interrupt module

These jumper settings are to be performed in addition to the ones shown in Figs. 4.10 to 4.14.

X2 Seen from behind, lower left-hand female backplane connector in the extension unit

Pin no.	f	d	b	z	
2	RESBR 1	DtI0Sub	0 V	2) 0 V	
4	/Pe0Fg	0 V	/Pe1Fg	/FILTER	
6	/Pe2Fg	0 V	/Pe3Fg	0 V	
8	/I0Fg	0 V	/I1Fg	/I2Fg	_I
10	NRMSB	0 V	/MITL	0 V	
12	NRLSB	0 V	/I2B4	MSPA	
14	RESBR2	Dt0Sub	0 V		
16	/Pe0Fg	0 V	/Pe1Fg	MSPE	
18	/Pe2Fg	0 V	/Pe3Fg	0 V	
20	/I0Fg	0 V	/I1Fg	/I2Fg	_II
22	NRMSB	0 V	/MITL	0 V	
24	NRLSB	0 V	/I2B4	DEFON	
26	0 V			0 V	
28	FMS	FMD	PS	SIMI	
30		BS	PM (24V alarm)		
32	L+ (24 V)	L+ (24 V)	M	M	

5) (pins 2 to 28)

6) (pins 30 to 32)

Jumper necessary

Jumper possible

Protruding pin

_I for I/O bus I

_II for I/O bus II

Primarily responsible for : I0, I1 and I2, i.e. for the alarms 1 to 48

2) Filter jumpers not recommended.
5) Wrap pins or maxi-termi-point pins.
6) Bus board

Fig. 4.18 X2 backplane connector: jumpers for a non-redundant group interrupt module

These jumper settings are to be performed in addition to the ones shown in Figs. 4.10 to 4.14.

4.5 Module Replacement

The EAVU disconnects completely from all three I/O bus interfaces once it has been reset (by removing the module fuse or switching off the **L+** supply of the extension unit in the SES). The same happens when the 5-V bus supply fails. The front panel ribbon cable connectors of I/O bus I or II may be removed without disturbing bus traffic with the other EAVUs after the EAVU has been reset or switched off.

An EAVU module may be inserted into an EAVU slot of an extension unit and the I/O bus cables can be connected without disturbing the system after the EAVU front panel fuse has been removed or the **L+** supply switched off. The EAVU becomes active and can be addressed approximately 200 ms after the module fuse has been installed and/or the L+ supply voltage switched on. No further system software intervention is required to give the EAVU control over the connected modules if the DefOn jumper has not been inserted.

Caution

The module fuse may not be installed before the module has been inserted, and must be removed when the module is removed without the module power supply being switched off.

Control over the connected I/O modules is removed from the EAVU concerned and the common fault LED lights up if the system software detects a faulty EAVU in the single-channel part. A dark "ON" LED (green) and a blinking common fault LED thus indicate a defective EAVU module.

Caution

The EAVU modules are mostly equipped with HCMOS circuits. Please observe the "Guidelines for Handling Electrostatically Sensitive Devices and Modules".

5 Technical Data

Operating voltage	L+	+24 V range:	19 to 33.5 V, 100 mA load (+PM and PS load)
Signal voltage	PS	+24 V output:	derived from L+ *)
Alarm voltage	PM	+24 V output:	derived from L+ *)
Operating voltage	5-V-Bus	+5 V range:	4.5 to 5.5 V, 300 mA load
Blinking voltage	BS	+24 V range:	20 to 33 V, 0.01 mA load
Reference potential	M1	0 V, (for 24 V)	
Reference potential	0 V	0 V, (for 5 V)	

Module fuse	F1	1.6 A, quick-acting
PS fuse	F2	1.6 A, quick-acting
PM fuse	F3	1.6 A, quick-acting

Storage temperature	-40°C to 70°C
Operating temperature (cabinet)	0°C to 40°C

*) The EAVU consumes up to 100 mA from the backplane PM if this voltage is fed redundantly and the module and PM fuses have blown. The EAVU consumes up to 10 mA from PS if this voltage is fed redundantly and the PS fuse has blown.

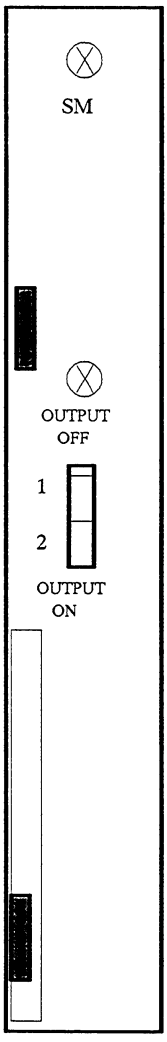
SIEMENS

TELEPERM M

I/O Bus Interface Module

6DS1 312-8BB

Technical Description C79000-T8076-C403-02



Contents

1 Application

The I/O bus interface module (EABA) 6DS1 312-8BB converts the high-speed data processing level area of the AS 235/AS 235 H central unit into the area of the slower noise-immune peripheral I/O bus.

Bus conversion has several effects: it keeps the data traffic between CPU and memory at a high rate, maintains a suitable connector pin assignment for the I/O bus, and isolates I/O module access with wait states. The module processes signals that are specific to the I/O bus and performs signal conditioning for interrupt signals. The module also processes alarm, cabinet lamp and time synchronization signals. Jumper settings permit the module to be matched to applications in the AS 235/AS 235K/AS 235H/MS 236 systems.

Application:

The module is intended to be used in the AS 235 H system and replaces the 6DS1 312-8AB module previously used for the AS 235/AS 235 K/MS 236 systems.

The module may not be mixed with the 6DS1 312-8AB version.

It may not be used in an AS 220 S, H, E, EHF, K / OS 250 S, E / AS 230, 230 K / AS 231system either.

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2 Design

Printed circuit board	Double-size Eurocard
Width	1 SPS
Connections	
Backplane connector 1:	48-way male connector ES 902 with 8-bit central unit connection
Backplane connector 2:	48-way male connector ES 902 with I/O bus interface
Features	Conversion from 8-bit central bus to I/O bus, Triggering cabinet fault lamp, Watchdog function, Cabinet alarm processing, Signal conditioning, Interrupt routing, Access time conditioning

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3 Method of Operation

3.1 Conversion from 8-Bit Central Unit Bus to I/O Bus

The module is connected to the 8-bit central unit bus of the automation system. The data, address and control signals from this bus are routed via decoupling networks and drivers to the I/O bus.

Wait cycles that are controlled by an internal 1-MHz clock pulse are inserted in order to adapt the bus signals to the slower execution cycles on the I/O bus.
The module bus drivers are able to feed three extension racks with TELEPERM M I/O modules (up to 42 I/O modules) in an AS 235 system or four extension racks with EAVU modules in an AS 235 H system.

Two I/O buses have been implemented for I/O module control in an AS 235 system. They feed the I/O interfaces of the extension units in basic and extension cabinet via an I/O bus interface module each (EABA1 and EABA2). The I/O interfaces in the basic unit of an AS 235/235 K system are also connected to these two I/O buses.

Each module receives its own PESP signal (PESPA or PESPB) which enables the individual address ranges.

The PESPA or PESPB signals represent the peripheral areas of the modules No. 0...61 and 100...160, respectively.

The read and write signals are only routed to the I/O address range which is defined by the address.

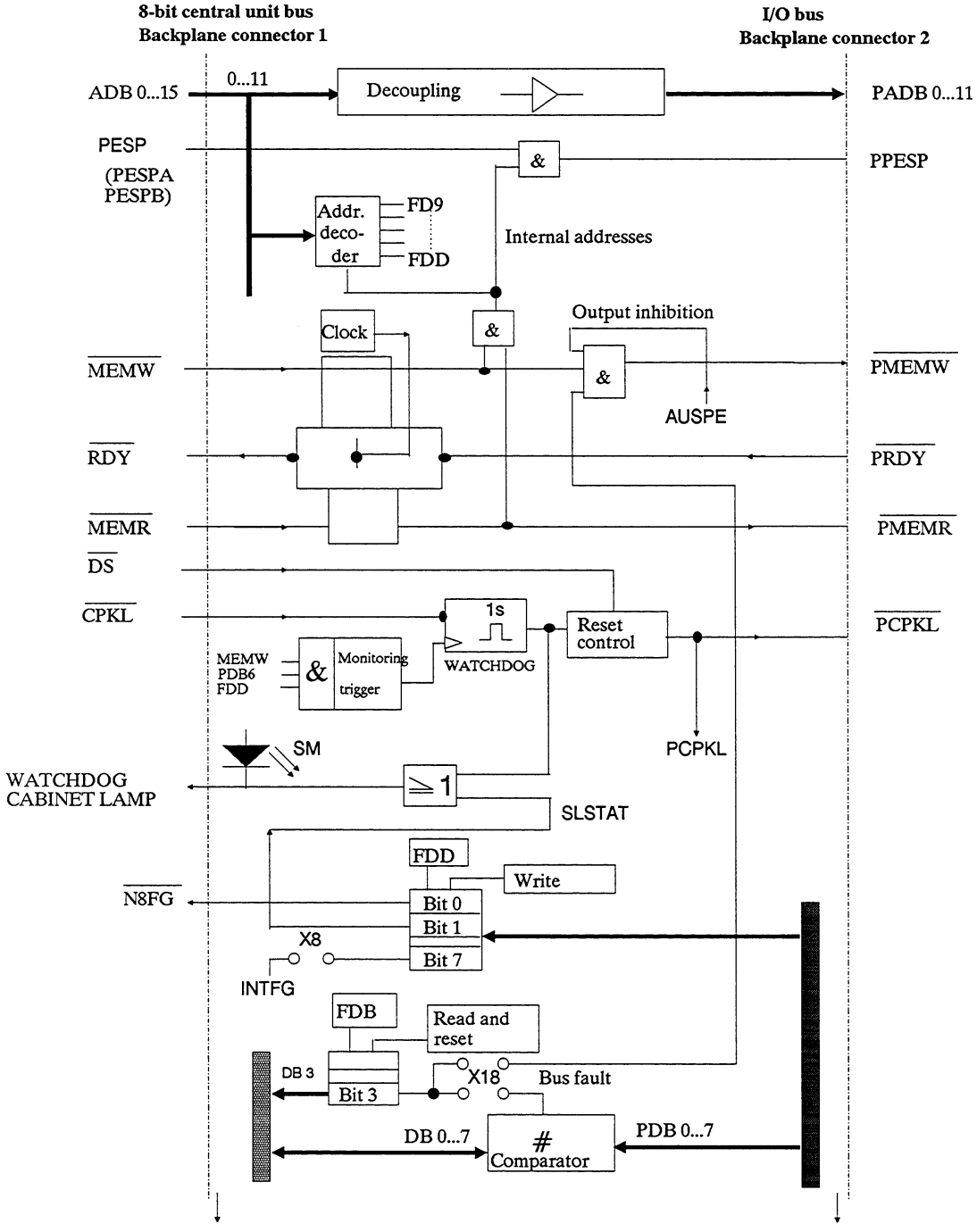

Fig. 3.1 Block diagram

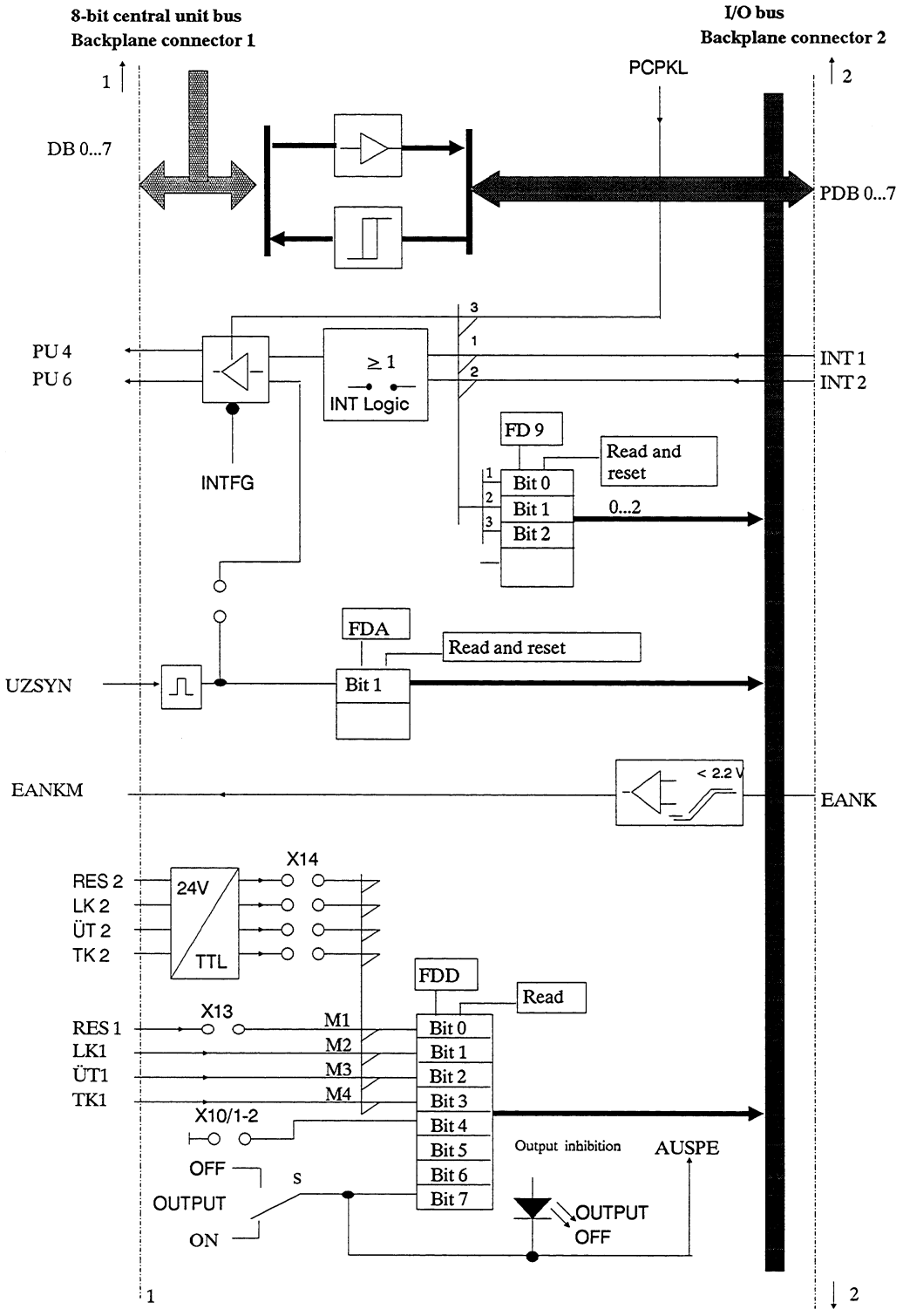

Fig. 3.2 Block diagram (continued)

3.2 Addressing Module-internal Functions

Module-internal addresses are decoded via a PROM element, and, according to the individual slot, are adjusted automatically to the I/O address range.

All subsequent addresses consist of a 12-bit I/O address (hexadecimal) and the PESP code P.

PESPA: P = 8 (hexa) PESPB: P = 4 (hexa)

3.3 Triggering Alarm and Output Signals and Watchdog

The binary outputs are triggered by a write command under the address $PFDD_H$ while the corresponding data bit is set to "1" or "0".

Output port functions under address $PFDD_H$: (see Chapter 6.2 Address Assignments):

DB0 N8 enabled (N8FG)
Output for disabling the local bus interface module (N8).
The software uses the N8FG signal for enabling/disabling direct memory access (DMA).
DB0 ⇒ "0" = N8FG = "H" (N8 enabled)
DB0 ⇒ "1" = N8FG = "L" (N8 disabled)

DB1 Cabinet lamp 1, static (SLSTAT)
The SLSTAT output in an AS 235 system triggers the cabinet lamp directly via the alarm logic module (ML). This function is used for indicating I&C alarms that have been detected by the central processing unit (e.g. defective signal interface module, cabinet overtemperature, etc.)

DB1 ⇒ "0" = SLSTAT = "H" (Cabinet lamp off)
DB1 ⇒ "1" = SLSTAT = "L" (Cabinet lamp on)

The cabinet lamp in an AS 235 system may also be triggered by the watchdog signal.

⇒ WATCHDOG = "H" (cabinet lamp OFF)

⇒ WATCHDOG = "L" (cabinet lamp ON; the SM LED (system alarm) on the front panel blinks at the same time).

DB2 Not used.

DB3 Not used.

DB4 Not used.

DB5 Not used.

DB6 Triggers watchdog block execution (see Fig. 3). A time counter (watchdog) on the I/O bus interface module monitors the central processing unit. The block execution watchdog is triggered by data bit 6 = "1". The counter output influences the watchdog output and the PCPKL signal. The counter is not re-triggered if the CPU fails, and sets the watchdog output to "L" once it has elapsed. The SM LED starts blinking and the PCPKL output is set to "H" (CPU not operational). This disables data traffic and resets the interfaces on the I/O modules. In certain cases the I/O module functions are also influenced.
The preset value of the block execution time counter is T = 2 seconds.
The monitoring counters on both I/O bus interface modules are triggered by a write command with DB6="1" under the address $PFDD_H$. This means that writing DB6 under PESPB influences EABA 2 and its signals PCPKL and LED-SM.

DB7 Enabling interrupts (INTFG)
Disabling of the PU4 and PU6 interrupt signal has been provided as an option to be used by software variants.

DB7 = "0" PU4/PU6 disabled
DB7 = "1" PU4/PU6 enabled

This inhibition is only effective if the jumper X8 has been inserted. Default jumper setting: interrupt enabled.

3.4 Cabinet Alarm Processing

The cabinet alarm inputs from the basic cabinet are read after a READ command has been issued under address PESPA/FDD_H.
The extension cabinet alarms are read under address PESPB/FDD_H.

Data bit assignments:

DB0 Reserve input M1 = RES1
The reserve input is read into DB0 if the X13 jumper has been inserted. "0" is permanently read if the jumper is open.

DB1 Fan contact. M2 ("0" = fan ready) LK

DB2 Overtemperature M3 ("0" = temperature OK) ÜT

DB3 Door contact M4 ("0" = door closed) TK

DB4 X10/1-2 jumper for software purposes. The X10/1-2 jumper only influences DB4; inserted = "0".

DB5 Not used ⇒ "1"

DB6 Not used ⇒ "0"

DB7 OUTPUT switch for "output disabled" (AUSPE).
The output disable switch (OUTPUT OFF) on the front panel disables the write command to the I/O modules. Since the I/O bus interface module generates a READY signal (acknowledgement) for the write commands at the same time, the selected I/O bus does not issue I&C alarm 305 when the switch has been set to OUTPUT OFF. The OUTPUT OFF LED on the front panel blinks and DB7 = "1" if the output has been disabled.

Warning

The output disable switch on the front panel has mainly been provided for commissioning purposes if process outputs are to be disabled with "STA" in general after the ONLINE enable.
If the switch is used during operation, the following must be taken into account:
States set before, e.g. motor ON, cannot be undone after the switch has been actuated. This means that all binary and analog presettings are frozen which might result in non-permissible operating states.

3.5 EANK and Bus Fault Interpretation

- EANK (multiple addressing)

The potential on the EANK line is monitored by an operational amplifier when an I/O module is addressed

* **One** module has been addressed = EANK approx. 2.5 V
  (2.5 V is the expected value on the EABA during I/O access)
* **Two** or more modules = EANK < 1.7 V
  Monitoring for < 2.2 V = sets the EANKM signal.
  This means that more than one I/O module has been addressed under the same address.
* **No** module reacts = EANK = 5 V
  The module has not been installed, or an address jumper has been set incorrectly, or the address code is defective. An EANK alarm is not issued. This state is detected as a time-out by the CPU watchdog function.

- BUSF (I/O bus fault)

The data lines on the central bus and the I/O bus can be compared by an 8-bit comparator. This comparison is normally performed by a write access using test patterns under address $PFDD_H$. The I/O bus fault is stored if a write access to an I/O module detects a discrepancy between the data on the central bus and the I/O data bus.
The central processor reads the fault port under address $PFDB_H$; the read access resets the fault memory. Setting the fault memory is only possible if the jumper X18/1-2 has been inserted. The fault port is directly connected to the 8-bit central unit bus.
$PFDB_H$ fault port assignment:

DB0 - DB2	-	Static "1"
DB3	-	BUSF stored ("0" = bus fault)
DB4 - DB7	-	Static "1"

One function has been added for special applications which might come up with certain software variants within the context of bus fault detection. Using this function the user can inhibit subsequent write accesses to the periphery after a bus fault has occurred. (The first faulty access cannot be prevented.) This function has the same effect as the front panel switch OUTPUT OFF and is switched on with the jumper combination X18/1-2 and X18/3-4. The function can be switched off by reading the bus fault flag or central reset.

Warning

Due to the technological importance of this additional function the warning contained in Chapter 3.4 must be strictly adhered to.

3.6 Interrupt Inputs

Only INT 1 of I/O bus 1 (EABA1) out of the four interrupt lines that are defined on the I/O bus (INT1...INT4) is used in an AS 23x system (INT2 prepared by jumpers). INT1 is allocated to the interrupt-generating binary input SF61. This module sets INT1 to 0 V until the module is read. After a time-out, INT1 can be temporarily disabled on the I/O bus interface module (jumper X4/1-2 instead of jumper X4/3-4) in order to prevent a central unit blockage due to a permanent INT1 signal (e.g. because of a watchdog time-out PCPKL = 1). .

Setting the X4/3-4 jumper (instead of X4/1-2) causes the INT1 to react in a manner that is compatible to the 6DS1 312-8AB version (without watchdog inhibition).
Standard jumper: AS 235 = X4/1-2,
AS 235 H = X4/1-2.

- Watchdog scanning

The current state of the individual watchdog signals can be scanned via the PESP/FD9$_H$ port (depends on software variant). Jumper X7 must have been inserted for this purpose. A watchdog time-out corresponds to "0". Jumper not inserted = static "1".

PFD9$_H$ interrupt port assignment:

DB0	-	INT1 directly	(0 = interrupt)
(DB1	-	INT2 stored	(0 = interrupt))
DB2	-	Watchdog scan	(enabled by jumper X7)
DB3	-	Static "0"	
DB4-DB7	-	Static "1"	

3.7 Time Synchronization

The X10/X11 jumper specifies whether the rising or the falling edge of the RES1 signal triggers a minute synchronization interrupt.

The time interrupt is stored; the memory state can be read via DB1 and port PESPA/FDA$_H$ and is reset when it is read. The CPU is offered the interrupt memory as PU6-N minute synchronization impulse via jumper X10/7-8 of EABA1. The PU6 memory can be read via port PESPA/FDA$_H$ which enables the system to recognize whether a time interrupt has occurred (this port is only relevant on EABA1). Reading resets the interrupt memory.

PESPA/FDA$_H$ UZ port assignment:

DB0	-	Static "0"
DB1	-	Time synchronization stored ("0" = active)
DB2, DB3	-	Static "0"
DB4-DB7	-	Static "1"

4 Technical Data

Design	Printed circuit board, 233.4 x 160 mm, 1 SPS
Connections	
Backplane connector 1:	48-way male connector ES 902 (central unit connection)
Backplane connector 2:	48-way male connector ES 902 (I/O bus interface)
Supply voltage	+ 5 V ± 0.25 V
Current consumption	< 0.9 A
U_e input level for digital inputs (I/O bus)	"0" < 1.5 V "1" > 3.5 V
U_e input level for TK2, LK2, ÜT2, RES2	"0" < 2.5 V "1" > 15 V, < V 33
Operating temperature	0 to 55 ° operation without fan

I/O bus interface range

I/O bus interface	No. of allocated modules (BGNR)
1	0 - 61
2	100 - 160

Distinction is made by the slot in the AS 23x and the qualifier signals PESPA and PESPB.

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5 Installation and Commissioning

5.1 Installation

The **Guidelines for Handling Electrostatically Sensitive Devices and Components** must be observed when installing the interface module.

The I/O bus interface module can be installed in a slot of the basic unit. It is fastened by the locking bars of the subrack.

The I/O bus interface module occupies two slots in an AS 235/AS 235 K/MS 236 system and two slots per central processing unit in an AS 235 H system.

The first module in an AS 235/MS 236 system is used for I/O bus 1 of the basic cabinet, including five I/O slots in the basic subrack. The first module in an AS 235 K system is used for five I/O slots in the basic subrack and for four ES 100 K racks. The first module in an AS 235 H system is used for connecting the extension subrack in the basic cabinet.

The second module for I/O bus 2 drives the 6th I/O slot in the basic subrack of an AS 235/AS 235 K/MS 236 system and, in an AS 235/MS 236 and AS 235 H system, the extension units in the extension cabinet. Four additional ES 100 K racks may be connected to the 6th slot of an AS 235 K system.

There are no slot-related address selections; all configurable jumpers are used for function selections.

Note: The I/O bus interface modules may not be interchanged once the jumpers have been set.

5.2 Commissioning

Jumper settings in an AS 235 /235 K or MS 236 system: X4-X20

	1st interface module EABA1		2nd interface module EABA2		Factory default setting
	Standard	Option	Standard	Option	
X4/1-2	X				X
X4/3-4					
X4/5-6					
X7/1-2					
X8/1-2					
X9/1-2	X		X		X
X10/1-2					X
X10/3-4		X			
X10/5-6	X		X		X
X10/7-8		X			X
X13/1-2	X		X		X
X14/1-2					
X14/3-4					
X14/5-6					
X14/7-8					
X18/1-2					
X18/3-4					
X19/1-2	X				X
X20/1-2	X		X		X

X=jumper inserted

Jumper settings in an AS 235 H system: X4-X20

	1st interface module EABA1		2nd interface module EABA2		Factory default setting
	Standard	Option	Standard	Option	
X4/1-2	X				X
X4/3-4					
X4/5-6					
X7/1-2					
X8/1-2					
X9/1-2	X		X		X
X10/1-2					X
X10/3-4		X			
X10/5-6	X		X		X
X10/7-8		X			X
X13/1-2	X		X		X
X14/1-2					
X14/3-4					
X14/5-6					
X14/7-8					
X18/1-2					
X18/3-4					
X19/1-2					X
X20/1-2	X		X		X

X = jumper inserted

Meaning of the X4-X20 jumpers

	Inserted	Not inserted
X4/1-2	INT1 interrupt with WATCHDOG inhibition	No INT1 interrupt (2nd module)
X4/3-4	INT1 interrupt without WATCHDOG inhibition (compatible with -8AB version)	No direct INT1 (standard)
X4/5-6	INT2 (stored) for interrupt	No INT2 (standard)
X7	WATCHDOG scan possible	No WATCHDOG scan
X8	Interrupt inhibition can also be selected by software	No interrupt inhibition by software
X9	Test jumper for WATCHDOG counter	No WATCHDOG
X10/1-2	System software switch 1 active	System software switch 1 passive
X10/3-4	Negative edge of external minute impulse effective	One of the two jumpers must be inserted
X10/5-6	Positive edge of external minute impulse effective	
X10/7-8	Minute impulse sets PU6 interrupt to EABA1	No interrupt by minute impulse
X13	RES input can be read by the software	RES signal without I&C alarm, not effective (alternative of X10/7-8)
X14/1-2	Reserved for TK2 converter (not standard)	Standard : open = no conversion of TK2, RES2, LK2, ÜT2 on this module
X14/3-4	Reserved for RES2 converter (not standard)	
X14/5-6	Reserved for LK2 converter (not standard)	
X14/7-8	Reserved for ÜT2 converter (not standard)	
X18/1-2	Bus fault reading possible	Bus fault reading not possible
X18/3-4	Write/output inhibit upon bus fault ON	No write inhibit upon bus fault
X19	INT1 filter active	INT1 filter passive
X20	INT2 filter active	INT2 filter passive

Interrupt routing for 6DS1 312-8BB

Jumper X4/3-4: Alternative of INT 1 standard jumper without WATCHDOG influence (version compatible with 6DS1312-8AB)

Jumper X4/1-2: Standard jumper for process interrupts to EABA1. INT1 is suppressed after a watchdog time-out. No effect on EABA2.

Jumper X4/5-6: Reserved for possible software variants with stored INT 2. Not suitable for software variants A, F (235/236).

Jumper X10/7-8: Interrupt for minute impulses. Only on EABA1. No effect on EABA2.

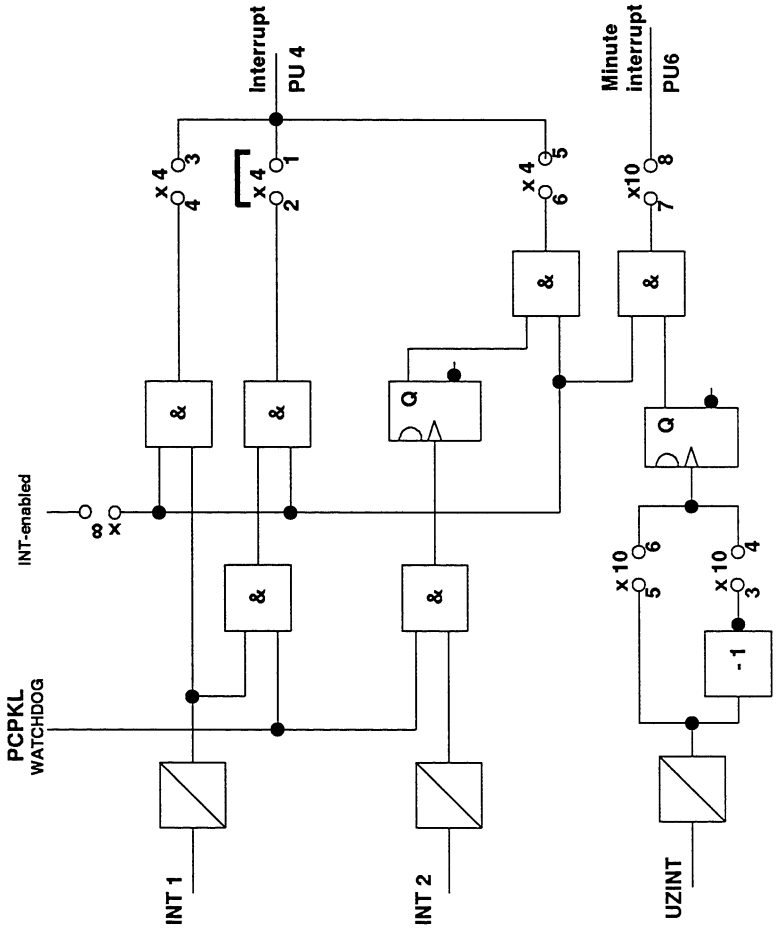


Fig. 5.1 Interrupt routing

Time synchronization

PU6 interrupt after (external RES1)	Jumper inserted [3]	Open
negative edge	X10/5-6	X10/3-4
positive edge	X10/3-4	X10/5-6

PU6 to CPU [1]	With minute synchronization	Without minute synchronization
1st I/O bus interface module [2]	X10/7-8 inserted	X10/7-8 open
2nd I/O bus interface module	X10/7-8 open	X10/7-8 inserted

1) The PU6 interrupt has no effect on the second I/O bus interface module EABA2.

2) The X13 jumper has no meaning for RES1 in "with minute synchronization" mode and has therefore **not** been inserted.

3) The X10/3-4 and X10/5-6 jumpers may not be inserted at the same time.

Monitoring functions (watchdog)

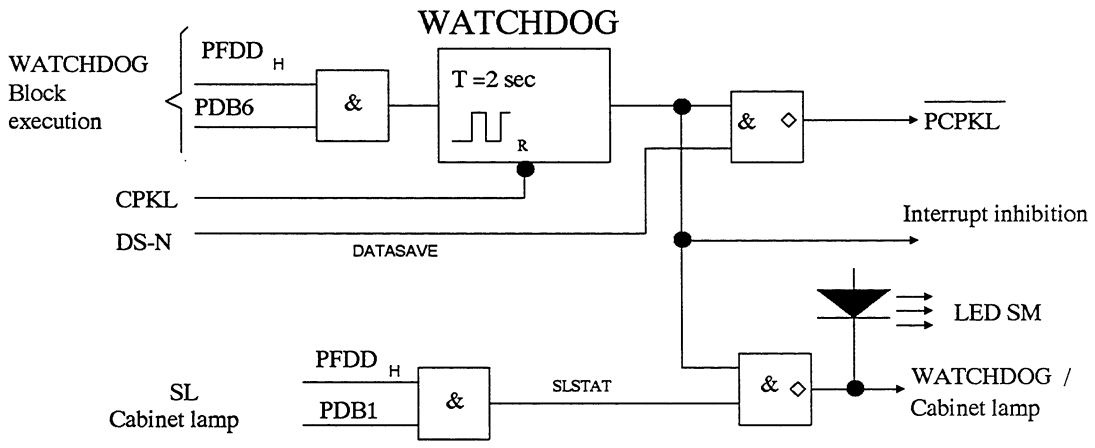


Fig. 5.2 Monitoring functions

Location of the jumper sockets

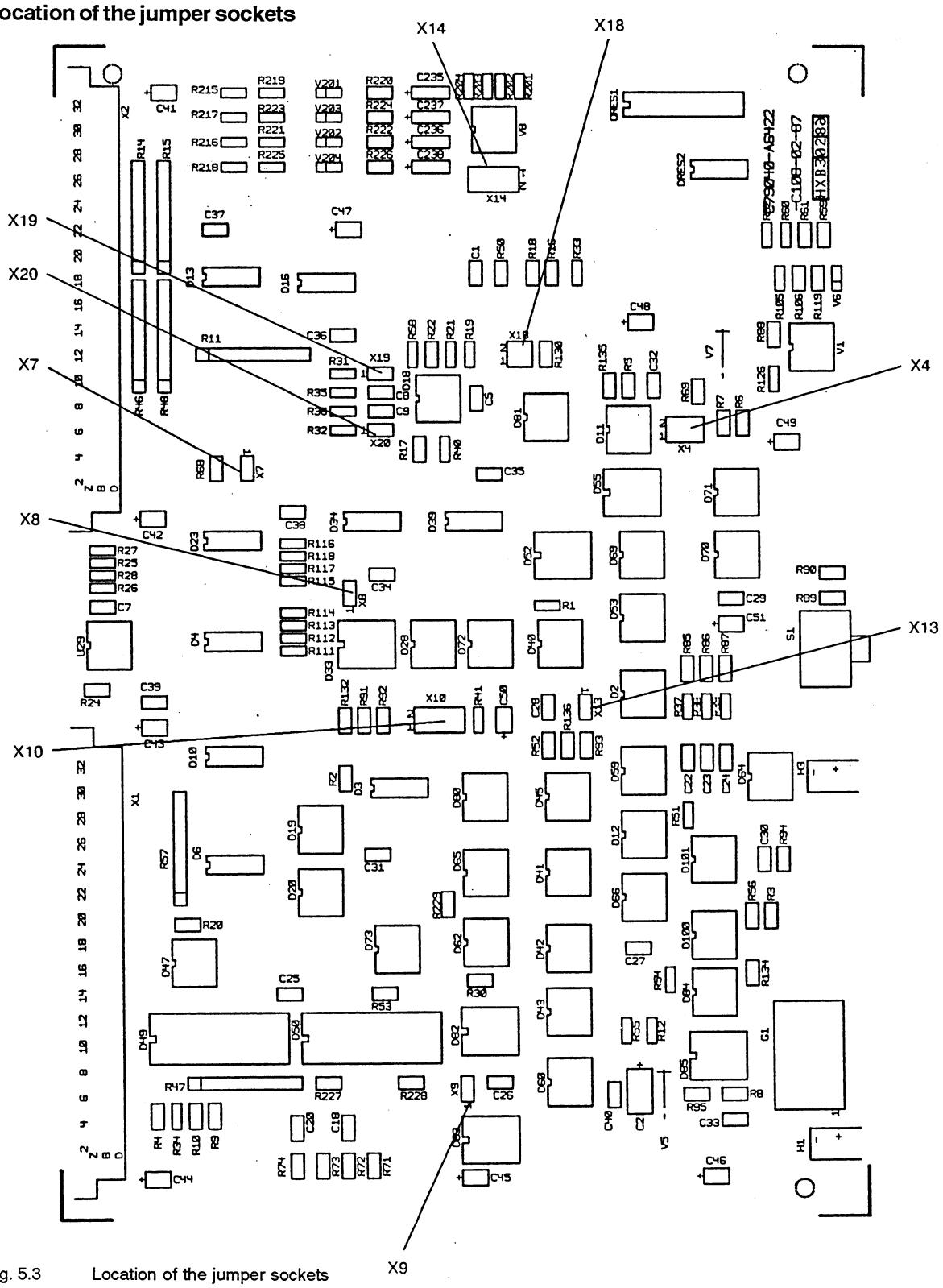
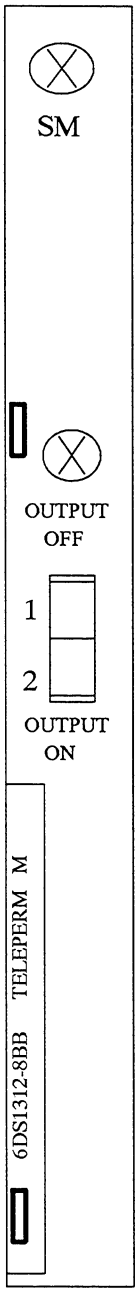


Fig. 5.3 Location of the jumper sockets

5.3 Operation and Monitoring



Blinks when a system alarm is waiting and after WATCHDOG time-out.

Blinks when output inhibition has been activated.

This switch enables all write commands to the I/O section to be disabled. The disabled state is indicated by the LED above this switch.

In order to prevent time-out, a RDY (acknowledgement) signal is generated on the I/O bus interface module when output inhibition is selected (-> no I&C alarm S305 when data is written).

Warning

When output inhibition has been activated(OUTPUT switch in OFF position) the states of binary and analog outputs are kept, i.e. frozen, on most I/O modules. This might result in non-permissible states on the process side.

Fig. 5.4 Front panel controls

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6 Maintenance

6.1 Functions

The interface module is connected to the 8-bit central unit bus of the automation system.
The data, address and control signals from this bus are routed via decoupling networks and drivers to the I/O bus.
Wait cycles that are controlled by an internal 1-MHz clock pulse are inserted in order to convert the bus signals to the slower execution cycles on the I/O bus.

The central processing unit is monitored by a time counter (WATCHDOG). In an AS23x system, the WATCHDOG is triggered in ZYK2 (125 ms).

The watchdog issues a signal (runtime T = 2 seconds) if the CPU fails and the watchdog times out. This signal activates the cabinet alarm lamp (by the WATCHDOG signal) and sets the PCPKL peripheral reset signal to an active state.
Refer to the individual I/O module descriptions (jumper ARS) in order to find out whether this signal only resets the I/O module interfaces or includes additional functions.

Timing

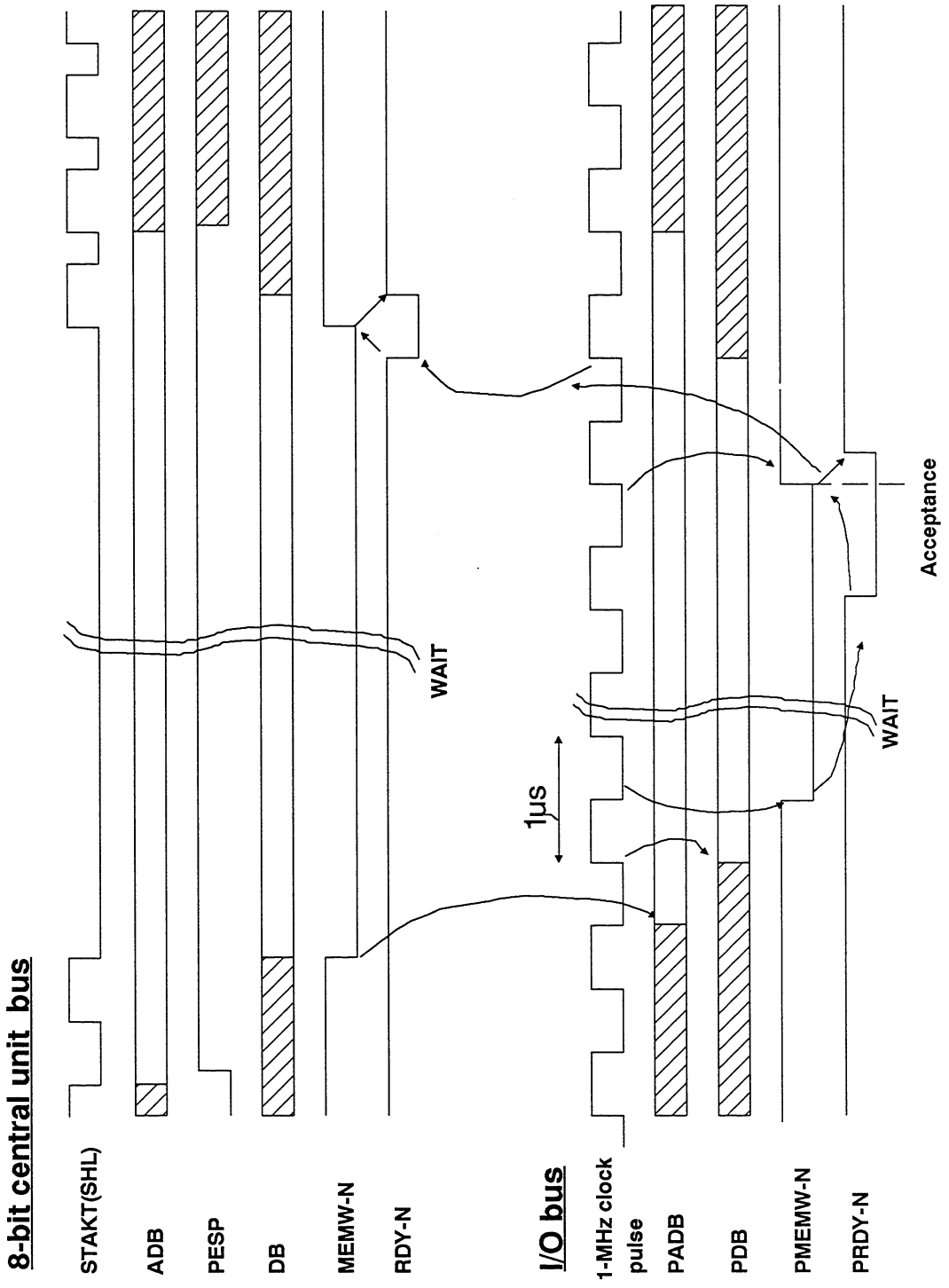


Fig.6.1 Write cycle

Timing

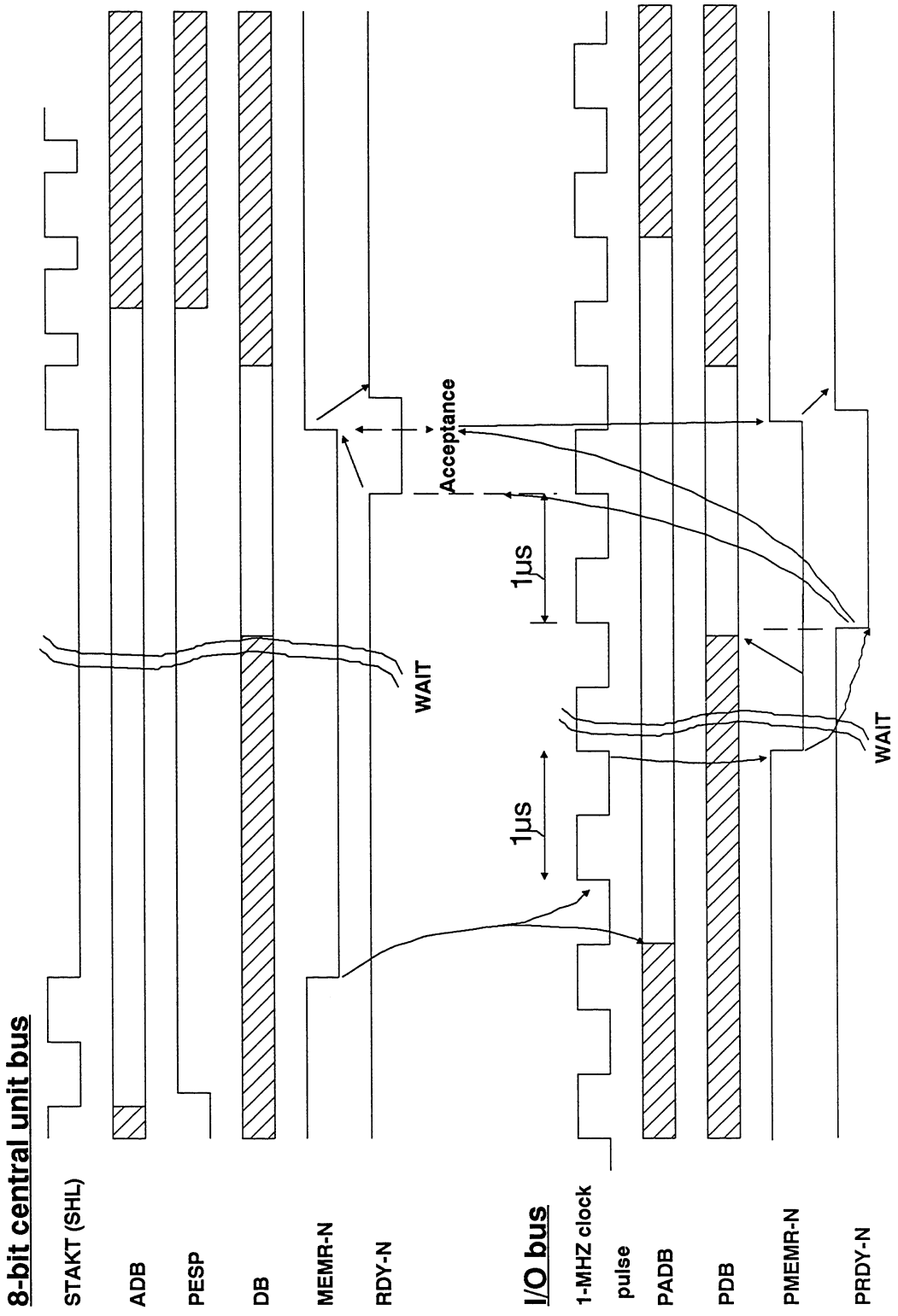


Fig. 6.2 Read cycle

6.2 Address Assignments

The module addresses in hexadecimal notation must be supplemented by PESPA or PESPB.

Address (hexa)	Bit	I/O bus interface No.	Direction	Meaning
FDO to FD8		1,2		Not used
PESPA FD9	0 1 2 3 4 5 6 7	1	6DS1 312 → ZT	INT1 directly (SF 61) process alarm (INT2 stored) } Reset WATCHDOG1 by reading 0 1 1 1 1
PESPB FD9	0 1 2 3 4 5 6 7	2	6DS1 312 → ZT not standard	(INT2 stored) } Reset WATCHDOG 2 by reading 0 1 1 1 1
PESPA FDA	0 1 2 3 4 5 6 7		6DS1 312 → ZT	0 (INT minute impulse } Reset stored) } by reading 0 0 1 1 1 1
PESPB FDA		2		not used
FDB	0 1 2 3 4 5 6 7	1,2	6DS1 312 → ZT	1 1 1 BUSF-N stored Bus fault flag, Reset 1 by reading 1 1 1

Address (hexa)	Bit	I/O bus interface No.	Direction	Meaning
PESPA FDB	0 1 2 3 4 5 6 7	1	→ ZT write to 6DS1 312	Test bit pattern output (cannot be read back) for bus fault monitoring on I/O bus 1
PESPB FDB	0 1 2 3 4 5 6 7	2	→ ZT write to 6DS1 312	Test bit pattern output (cannot be read back) for bus fault monitoring on I/O bus 2
FDC		1,2		Not used
PESPA FDD	0 1 6 7	1	ZT→ write 6DS1312	N8FG SLSTAT1, static cabinet lamp WATCHDOG 1 trigger (INT enabling signal)
PESPB FDD	1 6	2	ZT→ write 6DS1312	SLSTAT2, static cabinet lamp WATCHDOG 2 trigger
PESPA FDD	0 1 2 3 4 5 6 7	1	6DS1 312 read → ZT	RES1 reserve contact LK1 fan contact ÜT1 overtemperature contact TK1 door contact (1st system jumper X10/1-2) 1 0 Output inhibition, switch 1
PESPB FDD	0 1 2 3 4 5 6 7	2	6DS1 312 read → ZT	RES2 reserve contact LK2 fan contact ÜT2 overtemperature contact TK2 door contact (2nd system jumper X10/1-2) 1 0 Output inhibition, switch 2

6.3 Connector Pin Assignments

Backplane connector 1

Pin	d		b		z	
2	M1 REServe contact	E	0 V		+5 V	
4	M2 fan contact	E	PESP(A,B)	E	UZSYN	E
6	M3 overtemperature	E	ADB0	E	CPKL	E
8	M4 door contact	E	ADB1	E	MEMR	E
10	WATCH DOG /SL	A	ADB2	E	MEMW	E
12			ADB3	E	RDY	A
14	EANKM	A	ADB4	E	DB0	B
16			ADB5	E	DB1	B
18			ADB6	E	DB2	B
20			ADB7	E	DB3	B
22	PU4	A	ADB8	E	DB4	B
24			ADB9	E	DB5	B
26	PU6	A	ADB10	E	DB6	B
28			ADB11	E	DB7	B
30						
32	N8FG	A	0 V			

E = signal input A = signal output B = bus signal

Backplane connector 2

Pin	d		b		z	
2	-		0 V		+5 V	
4	PMEMW	A	PMEMR	A	+5 V	
6	-		PRDY	E	-	
8	PCPKL	A	-		PPESP(A,B)	A
10	-		(INT2) 1)	(E)	INT1	E
12	EANK	E	(INT4) 2)	-	(INT3) 2)	-
14	-		PDB1	B	PDB0	B
16	PDB4	B	PDB3	B	PDB2	B
18	PDB7	B	PDB6	B	PDB5	B
20	-		PADB1	A	PADB0	A
22	PADB4	A	PADB3	A	PADB2	A
24	PADB7	A	PADB6	A	PADB5	A
26	PADB10	A	PADB9	A	PADB8	A
28	(ÜT2)	(E)	-		PADB11	A
30	(LKM2)	(E)	(RES2)	(E)	-	
32	(TK2)	(E)	OV		DS	E

1) INT2 interrupt line is reserved and currently not used.

2) INT3 and INT4 interrupt lines are reserved for other purposes.

6.4 Signal Names

Signal on central unit bus	Signal on I/O bus	Meaning
ADB 0...11	PADB 0...11	Address bits 0...11
DB 0...7	PDB 0...7	Data bits 0...7
CPKL	-	CPU operational; has the same function as the ZRS "central reset" signal
-	PCPKL	Signal "CPU operational" to the peripherals corresponds to CPKL OR WATCHDOG with reset function on the I/O modules.
MEMR	PMEMR	Read signal
MEMW	PMEMW	Write signal
PESP	PPESP	Peripheral memory area
PESPA	-	PESP signal of the 1st module
PESPB		PESP signal of the 2nd module
RDY	-	Acknowledgement to CPU
	PRDY	Acknowledgement from I/O modules

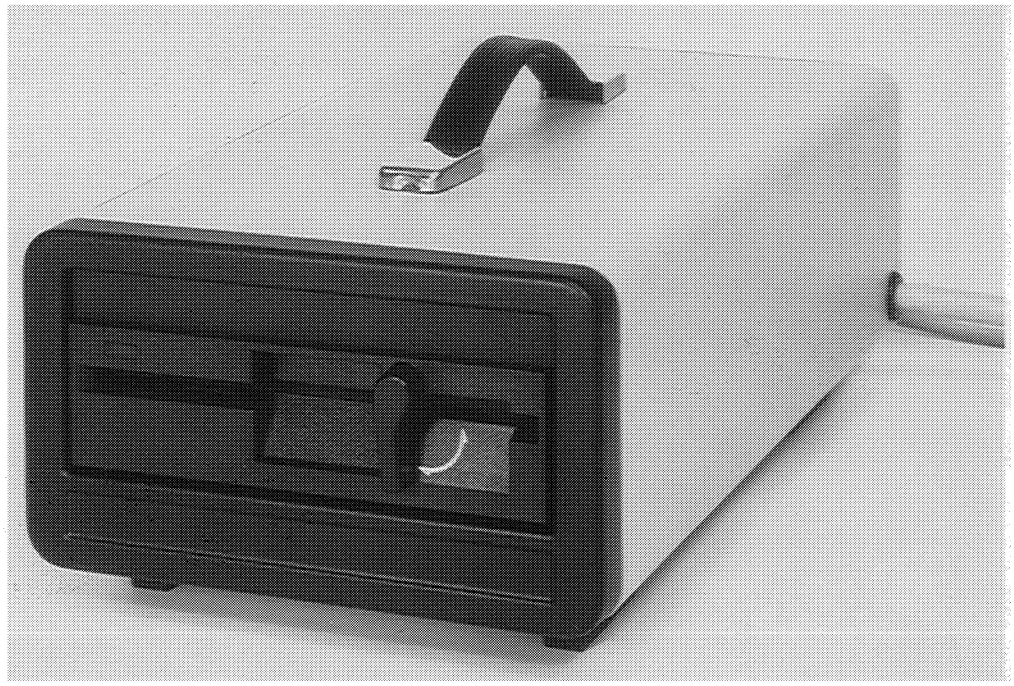
SIEMENS

TELEPERM M

Mini Floppy Disk Unit

6DS3 900-8AC/8AD

Instructions C79000-B8076-C137-05



Contents

1 Application

The mini floppy disk unit is used for the following purposes

- Loading at initial start-up
  Loading the system software in the AS 230/231 (version E), AS 235

- Archiving the contents of the memory as a prerequisite to loading operations
  Archiving of a system
  Copying (e.g. copying the configuration data from the configuring workstation of the engineering department onto the system at the place of installation)

- Archiving and loading of the RAM contents of a system

- Archiving of the memory contents after changes in the system configuration.

Model 6DS3900-8AC is designed for use in the AS 220 (S/K/H/E/EHF), AS 230, AS 230 K, AS 231 and OS 250 (S/E). It is a fully compatible replacement for the mini floppy disk unit 6DS3900-8AB used until now.

It is advisable to use model 6DS3900-8AD in the AS 230, AS 230 K/AS 231 systems from software version D onwards. This reduces the number of disks required to a quarter.

Using single-sided (SS), single-density (sd) floppy disks, the mini floppy disk unit 6DS3900-8AD can also be used with the AS 220/230/231 systems with software version B or C and with the OS 250 system. In these cases however, note that the **existing archived** contents of the memory must be loaded into the system using the existing drive or the mini floppy disk unit 6DS3900-8AC and subsequently archived using the mini floppy disk unit 6DS3900-8AD, due to the change in format.

It is vital that the mini floppy disk unit 6DS3900-8AD, revision level 4, is used in the systems AS 230, AS 230 K, AS 231 (version E) and AS 235 .

2 Design

The mini floppy disk unit consists of a 5 1/4" disk drive fitted into a compact table-top casing together with a power supply module for 24 V DC. The unit is provided with 3-m long signal and power cables.

The drive is fitted to the front plate of the casing by means of two guide rails on the sides. A cross member closes the rear of the drive. The drive module is locked in position by two snap-action fasteners at the rear which engage with a partition wall in the housing.

The DC/DC flyback converter is fitted in the rear part of the housing with a partition wall between it and the drive and provides the + 5-V, + 12-V output voltages required for the drive. The converter is connected to the drive by means of a four-core cable with a flat connector through the partition wall. A separate screened cable with connector is provided for power supply to the converter. The cable is clamped to the casing and its screen contacted.

Similarly, the signal cable with the ES 902 front connector is also clamped to the casing and its screen contacted. The flat connector for the disk drive is fitted on a plate. A bracket is fitted for guiding and fixing the connector to the partition wall in the casing.

The rear of the casing is provided with a cover which makes contact with the casing by suitable flat springs.

3 Method of Operation

3.1 Mini Floppy Disk Unit in the System

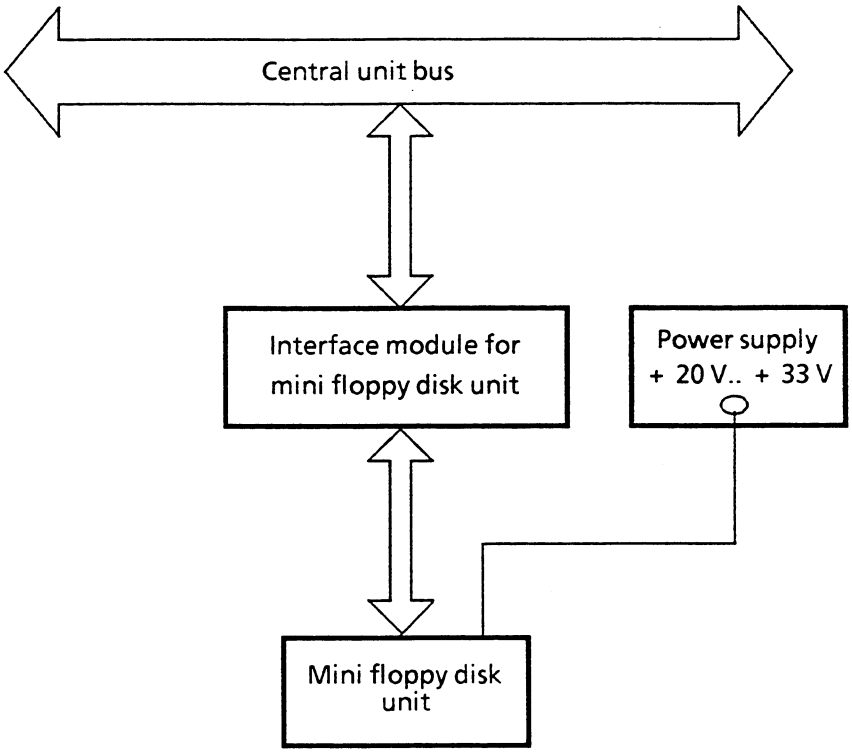
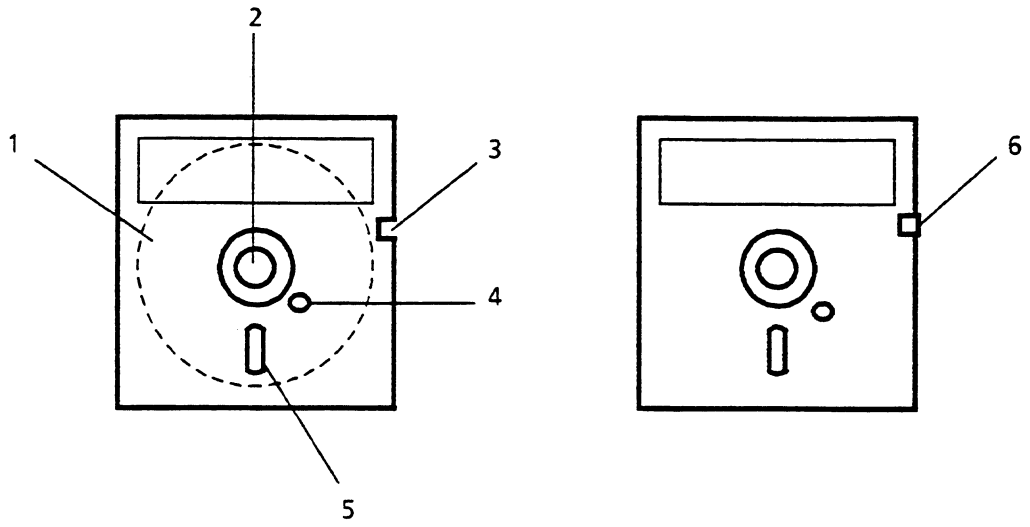


Fig. 1 Mini floppy disk unit in the system

The disk drive interface of the mini floppy disk unit is connected to the central unit bus interface of the AS 220, AS 230, AS 231, AS 235, OS 250 and the compact versions AS 220 K, AS 230 K systems via the interface module 6DS1 326-8BB (6DS1 326-8AA or 6AB5102-0AA70 for older systems). Data between the interface module and the memory is exchanged sector by sector using DMA. This ensures quick data access and low loading on the central processor. Data is exchanged between the interface module and the drive using the frequency multiplex method, at a maximum rate of 125 kbit/s.
With version E (does only apply for 6DS3900-8AD), the transfer rate is 300 kbit/s in high-density mode.

3.2 Data Medium (Mini Floppy Disk Unit)



1 Flexible disk
2 Conical shaft
3 Write protect slot
4 Index hole
5 Opening for read/write head
6 Write protect cover

Fig. 2 Mini floppy disk

The recording medium is a floppy disk of 5 1/4" (approx. 130 mm) diameter enclosed in a jacket measuring 133.4 mm x 133.4 mm (normal density / double sided / 96 tpi / 80 tracks / soft-sectored).

High density disks are needed when using high density mode (double-sided / high density / 96 tpi).

It is possible to both read and write on the disk when the write protect slot is open. The disk can be protected against write operations by covering this slot with an adhesive label.

Like any other magnetic medium, floppy disks are sensitive to external physical influences and should therefore be handled carefully. Corresponding instructions are provided on the cover of the disk. For reasons of safety, we recommend that the contents of the disk be refreshed every two years.

3.3 Recording and Data Format

The information is recorded on concentric tracks: 35 (with mini floppy disk unit 6DS3 900-8AC) or 80 (with mini floppy disk unit 6DS3 900-8AD), each having 16 sectors (15 in HD mode) and 128 bytes (512 in HD mode) in the so-called soft-sectored format. Each sector consists of an address and data field; the corresponding CRC values ensure the correctness of the recorded information.

3.4 Floppy Disk Drive

In order to reduce wear and tear on the drive, the drive motor starts before every access operation and switches off when the operation is complete.

The drive is not ready for operation until the disk has been properly inserted, i.e. the drive lever is properly closed. This is indicated by the red LED on the front lighting up.

IMPORTANT

The drive lever may not be opened during operation.

4 Technical Data

4.1 Mini Floppy Disk Unit

- Power supply

Supply voltage	20 V to 33 V	(including ripple)
Permissible ripple	3.6 V_{ss}	
Power consumption		
Standby	0.28 A	
In operation	0.52 A	
On startup of motor (400 ms)	0.74 A	

- Ambient conditions

In operation	
Temperature	+ 10 °C to + 40 °C
Relative humidity (no condensation)	20 % to 80 %
During transport and storage	
Temperature	-20 °C to + 65 °C

- Sensitivity to vibrations, oscillations

In operation	< 0.5 g ; < 55 Hz < 0.25g ; 55 Hz to 500 Hz
Transport and storage	< 2 g ; < 100 Hz

- Dimensions and weight

Dimensions (h x w x d)	120 mm x 180 mm x 320 mm
Weight	approx. 3 kg
Cable length	3 m

4.2 Floppy Disk Drive

- Data transfer rate

6DS3 900-8AD	125 kbit/s/300 kbit/s
6DS3 900-8AC	125 kbit/s

- Spindle speed: 300 1/min
  360 1/min with HD format

- Access

Average latency	< 100 ms
Drive motor acceleration time, max.	400 ms
Head positioning time	< 50ms
Track to track	
...-8AC	< 6 ms
...-8AD	< 3 ms
Head settling time	< 15 ms

- MTBF according to manufacturer 10,000 h
- MTTR 30 min

4.3 Mini Floppy Disk

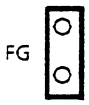
	MDE 6DS3 900-8AC	Compatible mode	High density mode
Recording method	FM	FM	MFM
Number of tracks	35	80	80
Number of sides	1	2	2
Capacity			
- per disk	16 sectors/track	16 sectors/track	15 sectors/track
- per track	71.680 byte	327.680 byte	1.228.800 byte
- per sector	2.048 byte	2.048 byte	7.680 byte
	128 byte	128 byte	512 byte

5 Commissioning

5.1 Jumper Settings

- Jumper settings 6DS3 900-8AC

The jumpers on the E board of the disk drive are set in the works as follows:



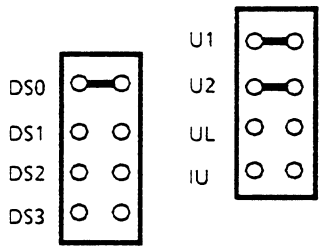


Fig. 3 Jumper settings on the BV drive (6DS3 900-8AC)

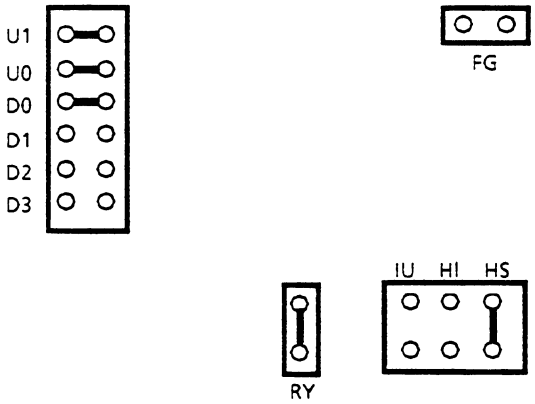


Fig. 4 Jumper settings on the BR drive (6DS3 900-8AC)

- Jumper settings on drive type 6DS3 900-8AD

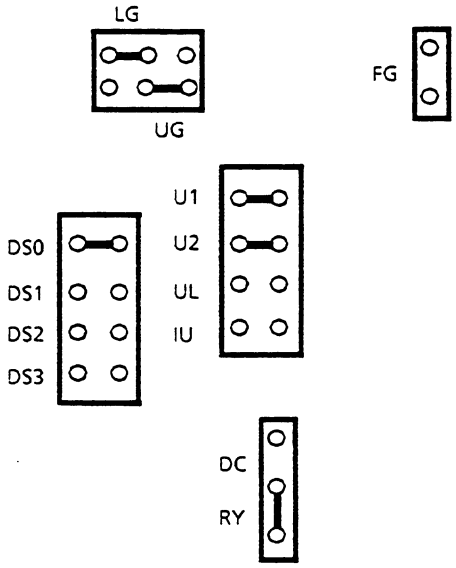


Fig. 5 Jumper settings on GFV drive FD-55-15 (6DS3 900-8AD)

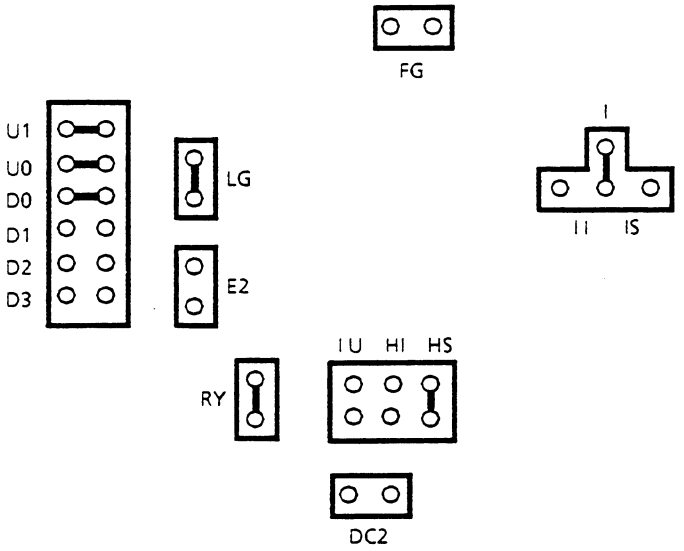


Fig. 6 Jumper settings on GFR drive (6DS3 900-8AD)

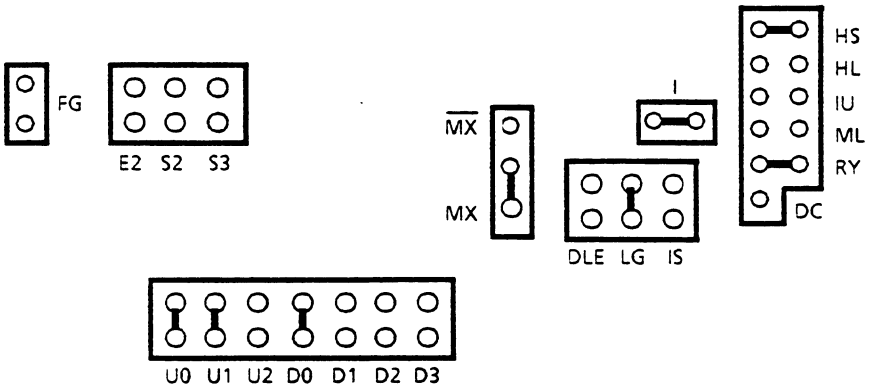
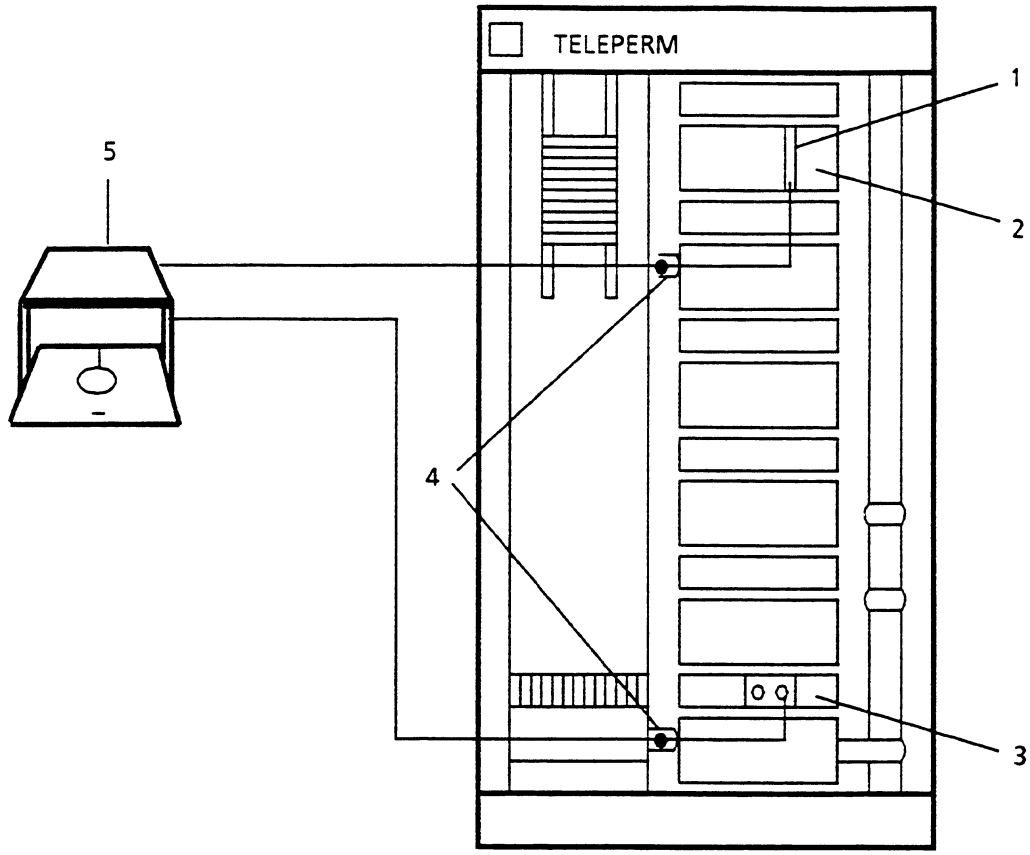


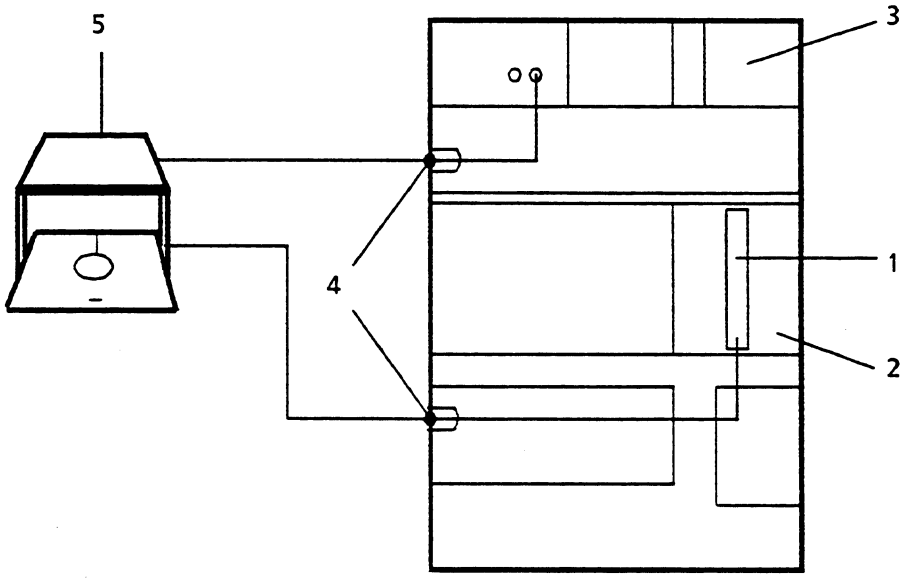
Fig. 7 Jumper settings on GFR drive FD-55-192 (6DS3 900-8AD)

5.2 Connection



1 Mini floppy disk interface module
2 Basic unit
3 Power supply subrack
4 Screen contact to frame
5 Mini floppy disk unit

Fig. 8 Connection to a standard cabinet

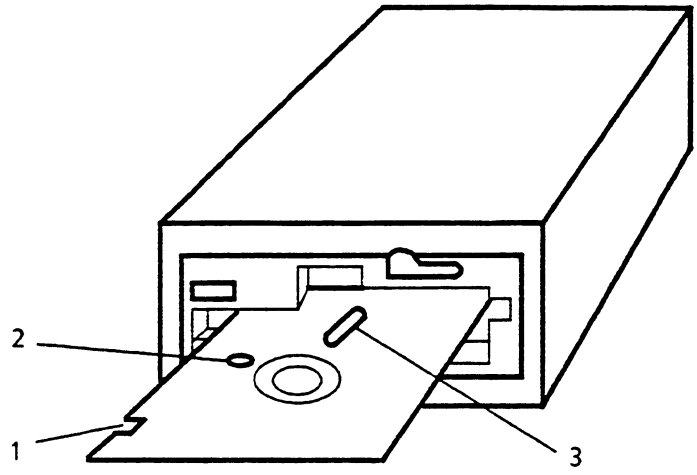


1 Mini floppy disk interface module
2 Basic unit
3 Power supply subrack
4 Screen contact to frame
5 Mini floppy disk unit

Fig. 9 Connection to a compact cabinet

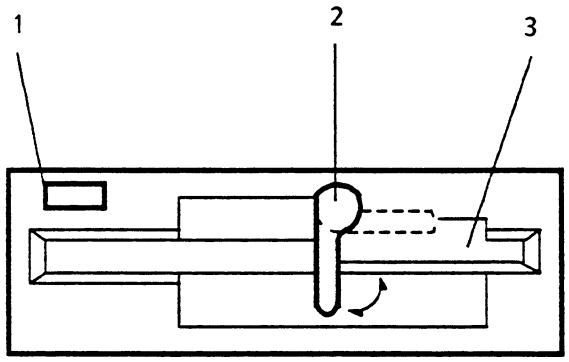
5.3 Operation

Insert the disk so that the write protect slot (1) of the disk jacket is to the left and the opening (3) for the read/write head is pointing towards the drive.



1 Write protect slot
2 Index hole
3 Opening for read/write head

Fig. 10 Inserting the floppy disk



1 Red LED "in operation"
2 Drive lever
3 Slot for inserting floppy disk

Fig. 11 Locking the drive lever

CAUTION

The lever must not be opened when formatting, reading or archiving.

6 Maintenance

The drive and the disks must be kept in a clean surrounding; the temperature and humidity values given must be observed (see Chapter 4.1). The read/write head is the most sensitive part of the drive and should not be subject to humidity, dust or smoke.

The disk drive heads must be cleaned if the unit has been at a standstill for some time, is frequently used or is operating in dirty surroundings.

This should be done using a cleaning kit for disk drives (consisting of cleaning fluid and a cleaning disk) obtainable from specialized dealers.

7 Parts List

Pos.	Description	Order no.	Maker's designation	Spares group *)	Number per product	Contained in, or applicable from revision level
1	Mini floppy disk drive (40 tracks)	C79451-Z1329-U012	TEAC FD-55-BR	R1		For version -8AC
2	Mini floppy disk drive (80 tracks)	C79451-Z1329-U122	TEAC FD-55-GFR-541	R1		For version -8AD up to rev. level 5
3	Mini floppy disk drive (80 tracks)	C79451-Z1329-U130	TEAC FD-55-GFR-192	R1		For version -8AD from rev. level 6 onwards
4	PCB for power supply module	C79232-A3000-B10		R1		

*) R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

Place of delivery: ANL 434 ED Erlangen

Parts List
Mini floppy disk unit
6DS3900-8AC u. AD

C79000-E8076-C137

Sheet: 1

1

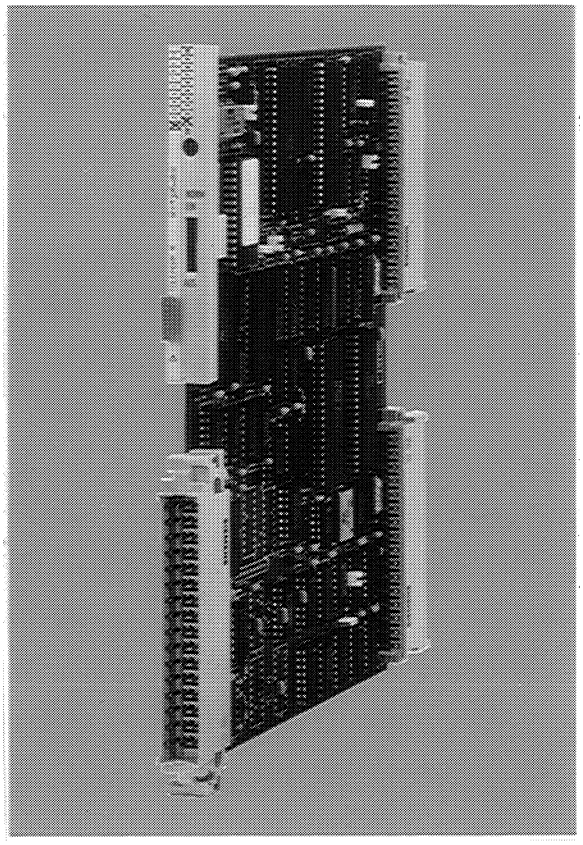
SIEMENS

TELEPERM M

Interface Module for Mini Floppy Disk Unit

6DS1326-8BB

Instructions C79000-B8076-C287-04



Contents

1 Application

The interface module for mini floppy disk unit (MDA) *) 6DS1326-8BB is used to connect the peripheral memory unit (mini floppy disk unit 6DS3900-8A.) to TELEPERM M systems. It is a fully compatible replacement for the former interface modules 6AB5102-0A*70 and 6DS1326-8AA.

Installation in the TELEPERM M system

The interface module 6DS1326-8BB is installed in the following TELEPERM M systems, each equipped with permissible mini floppy disk units.

Mini floppy disk unit (MDE)

System	Version	6DS3 900-8AB[1)]	6DS3 900-8AC	6DS3 900-8AD
AS 220 S		X	X	
AS 220 K		X	X	
AS 220 H		X	X	
AS 220 E		X	X	
AS 220 EK		X	X	
AS 220 EHF		X	X	
AS 230	B/C	X	X	
AS 230 K	B/C	X	X	
AS 231		X	X	
AS 230	D	X	X	X
AS 230 K	D	X	X	X
AS 230	≥E			X
AS 230 K	≥E			X
AS 231	≥E			X
AS 235				X
AS 235 K				X
AS 235 H				X
MS 236				X
MS 236 K				X
OS 250 E	Cabinet	X	X	
OS 250 E [2)]				
OS 250 S [2)]				

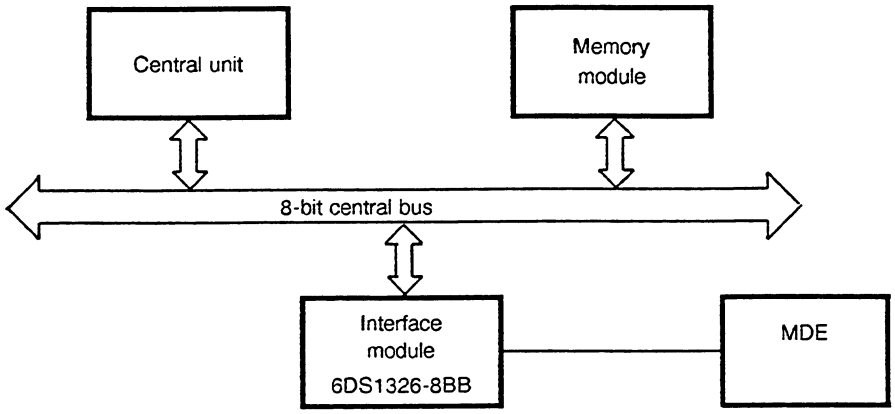
Table 1 Allocation of MDE to systems

*) In former TELEPERM M/ME descriptions, the mini floppy disk interface unit used to be abbreviated MFA.

1) No longer delivered

2) TEAC drive FD 55 BR installed in configuring device

The central unit of an AS/OS system communicates with the mini floppy disk interface module via the central bus (see Fig. 1).



MDE Mini floppy disk unit
Fig. 1 Interfaces of the mini floppy disk interface module

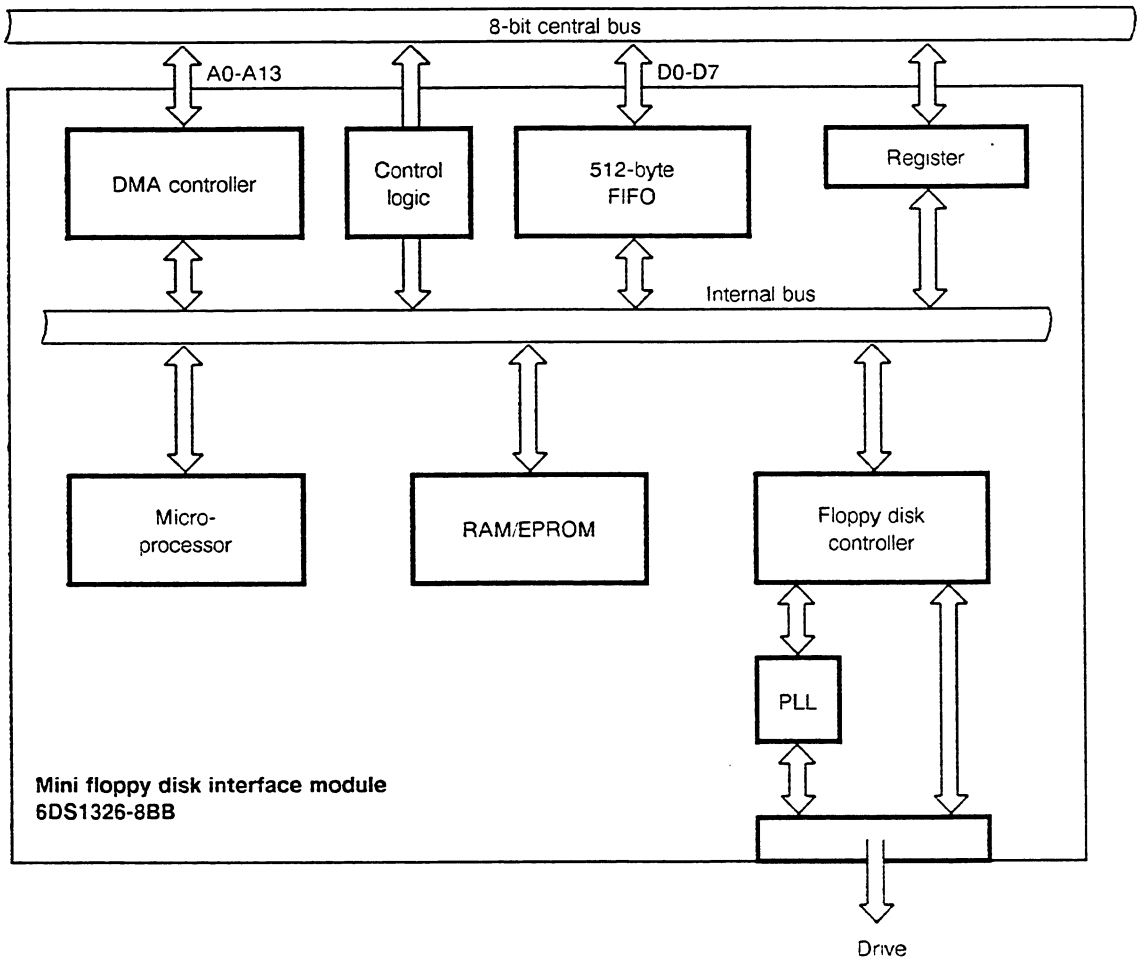


Fig. 2 Block diagram of the mini floppy disk interface module (MDA)

2 Method of Operation

The interface module for mini floppy disk unit has 2 operating modes.

- Compatible mode

In this mode, the module is a fully compatible replacement for the former interface modules 6AB5102-0A*70 and 6DS1326-8AA within the TELEPERM M range.

The recording format is 128 bytes/track, single density, with 16 sectors per track.

- Extended mode

This mode can only be used in the AS 230(K)/231 systems (from version E onwards) and AS 235 /MS 236. The recording format is 512 bytes/sector in high density mode, with 15 sectors per track.

Mode switchover is done via the system software of the automation system.

3 Module Startup Procedure

A module startup procedure is initiated via the central reset signal (ZRS).

Upon startup due to power failure (cold start), the firmware of the module carries out a test routine taking a few seconds.

The module is "BUSY" during this time and the red LED on the module's front lights up. Once the LED goes out, the module is ready for operation.

The test routine is not started upon a warm restart (without a power failure) and the LED flashes for a short period of time (approx. 0.2 s during ZRS).

The module is also "BUSY" during this time. Once the LED goes out, the module is ready for operation.

Should a fault be detected during the test routine, the red LED starts flashing.

The sequences are as follows:

1 x flashing	FIFO defective	FIFO	=	First-in-first-out memory
2 x flashing	RAM defective			
3 x flashing	FDC defective	FDC	=	Floppy disk controller

4 Technical Data

Supply voltage	5 V (4.75 V < Uo < 5.25 V)
Current consumption	approx. 1.5 A
Ambient temperature	0 - 50°C
Length of cable to mini floppy disk unit	max. 3 m
Noise coupling on data cable	max. 1 kV
Order No.:	6DS1326-8BB

5 Installation and Commissioning

5.1 Jumper Settings

The module has 3 plannable jumpers (X9, X13. X27) and 5 test jumpers.

Caution:

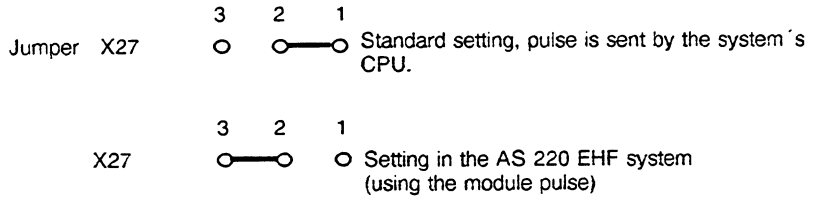
The test jumpers must not be removed or rearranged.

The basic module address is set via jumper X13. This jumper must be inserted in all AS 220 and OS 250 systems, but left open in the AS 230/231, AS 235/AS 235 K/ AS 235 H, MS 236 / MS 236 K.
Jumper X9 is inserted in all AS 220 and OS 250 systems to ensure that the load of the open-collector line lies within a defined range. In the AS 230/231, AS 235 / AS 235 K / AS 235 H, MS 236 / MS 236 K, this jumper is left open.

Caution:

If this jumper is not inserted in the AS 220/OS 250 systems, then malfunctions may occur in the DMA daisy chain mode between the local bus interface module and the interface module for mini floppy disk unit.

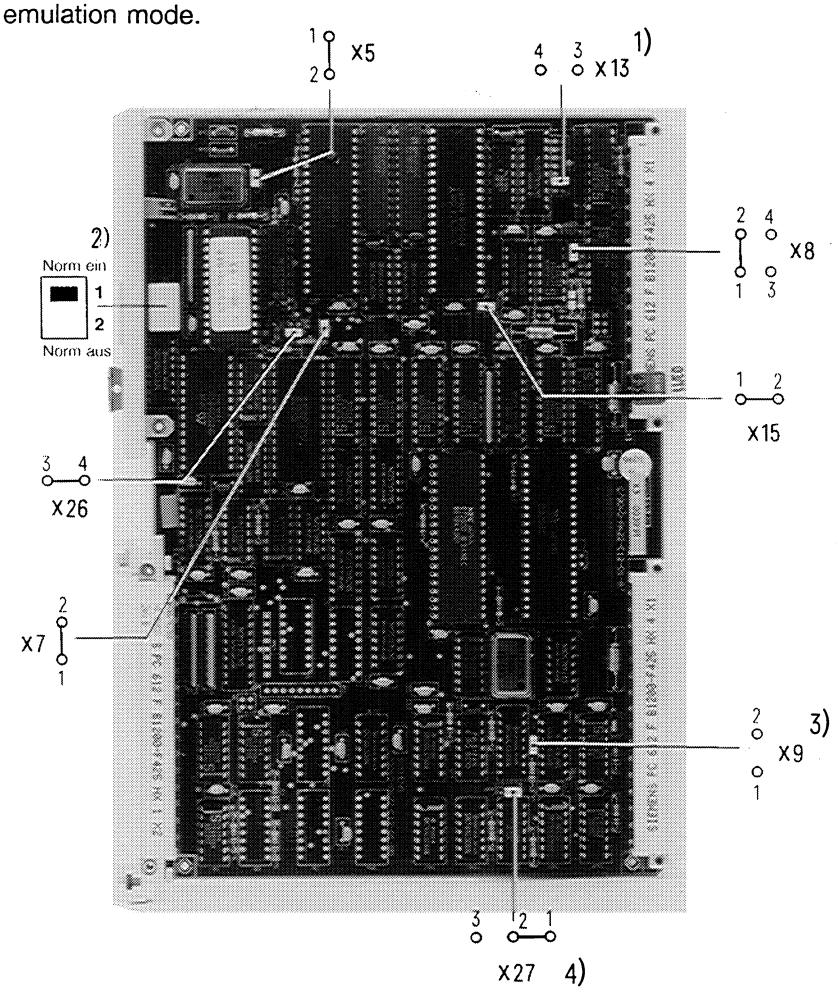
Jumper X27 is used to select the synchronization pulse for controlling communication between the interface module for mini floppy disk unit and the CPU in the central unit.
In the AS 220 E (K), OS 250 E, AS 220 S (K), AS 220 H, OS 250 S, AS 230 (K) and AS 231, AS 235 / AS 235 K / AS 235 H, MS 236 / MS 236 K systems. it is the CPU which sends the synchronization pulse.
In the AS 220 EHF system, a pulse generated by the interface module for mini floppy disk unit is used instead of an external pulse signal. This module therefore also functions in AS 220 EHF system configurations without monitor coupler modules 6DS1122-8AA (and without monitor interface modules 6DS1300-8AB).



- NORM switch

This switch is recessed in the front panel of the module and is concealed by a cover when delivered. The standard setting for this switch is "NORM EIN". It has no significance in any of the AS 220 and OS 250 systems and should, in these cases, always be set to "NORM EIN".In the AS 230/231, floppy disks preceding versions to C.06 and D.03 have certain floppy-disk-internal information which must be conditioned in an emulation mode to ensure that the archived data can be read.

This mode is activated by setting the switch to "NORM AUS" and can be visually checked by means of a flashing LED located above the switch. Data can be read but not written in emulation mode.



1) Jumper open AS 230/AS 231, AS 235/AS 235 K/AS 235 H/MS 236/MS 236 K
Jumper inserted AS 220/OS 250

2) Standard setting

3) Jumper open AS 230/AS 231/MS 236/MS 236 K
Jumper inserted AS 220/OS 250

4) Jumper 1-2 : standard setting
Jumper 2-3 : setting in the AS 220 EHF system

The jumper must be inserted at X27 in one of these two settings.

Test jumpers X5, X7, X8, X15, X26 must be inserted.

Fig. 3 Interface module for mini floppy disk unit 6DS1 326-8BB, jumper settings

5.2 Connector Pin Assignments

- Connector pin assignments: 8-bit central bus - Mini floppy disk interface unit (MDA)

	d	b	z
2		0 V	+5 V
4		PESP	Φ2 TTL
6	ADB 12	ADB 0	$\overline{\text{CPKL}}$
8	ADB 13	ADB 1	$\overline{\text{MEMR}}$
10	ADB14	ADB 2	$\overline{\text{MEMW}}$
12	ADB15	ADB 3	$\overline{\text{RDY}}$
14		ADB 4	DB 0
16		ADB 5	DB 1
18		ADB 6	DB 2
20	$\overline{\text{IRD}}$	ADB 7	DB 3
22	IRE	ADB 8	DB 4
24	IRF	ADB 9	DB 5
26		ADB 10	DB 6
28		ADB 11	DB 7
30			
32		0 V	

Table 2 Backplane connector 1

	d	b	z
2			
4			
6			
8			
10			
12			
14			
16			
18			
20	$\overline{\text{HLDA}}$		
22			
24			
26			
28			
30			
32	$\overline{\text{HOLD}}$	0 V	

Table 3 Backplane connector 2

- Connector pin assignments: MDA - MDE

	d	b	z
2			0 V
4			$\overline{\text{DSO}}$
6			
8	$\overline{\text{DIR}}$	0V	
10	0 V	$\overline{\text{HDLD}}$	
12	WRGAT	0 V	
14	0 V	0 V	
16	$\overline{\text{WRDAT}}$	$\overline{\text{STEP}}$	
18	0 V		0 V
20	$\overline{\text{SIDE}}$		$\overline{\text{MOT-ON}}$
22	0 V		0 V
24	$\overline{\text{READY}}$ O	(ENABLE)	$\overline{\text{READ}}$
26	0 V	0 V	0 V
28		$\overline{\text{TRKOO}}$	$\overline{\text{DENS}}$
30		0 V	0 V
32		$\overline{\text{WPRT}}$	$\overline{\text{INDEX}}$

Table 4 Front connector

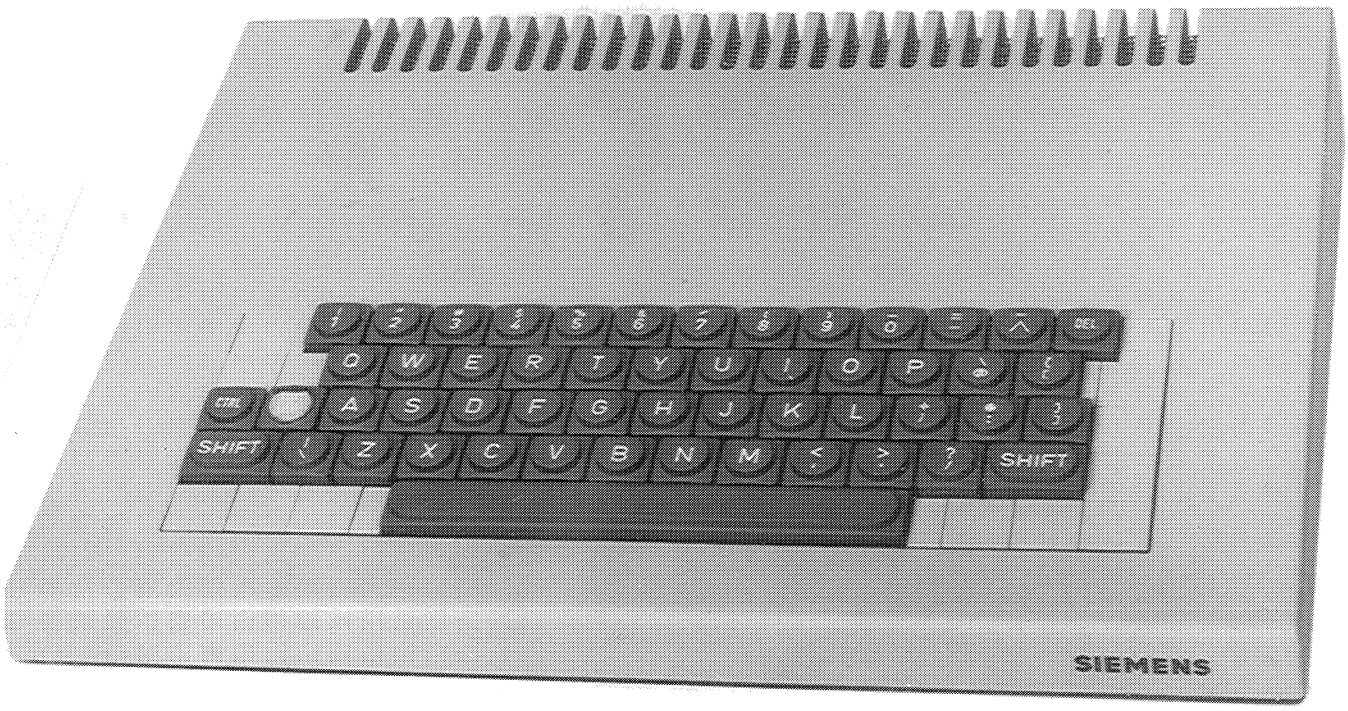
SIEMENS

TELEPERM M

Alphanumeric Keyboard

6DS3 303-8AA

Instructions C79000-B8076-C036-04



CONTENTS

1 Application

The alphanumeric keyboard is used in the TELEPERM M Process Control System. It is connected through the process operation keyboard (PBT) or directly to an AS/OS system. The connection to the higher-order system is made through a serial interface (line current 20 mA-TTY). The line current is supplied from the keyboard.

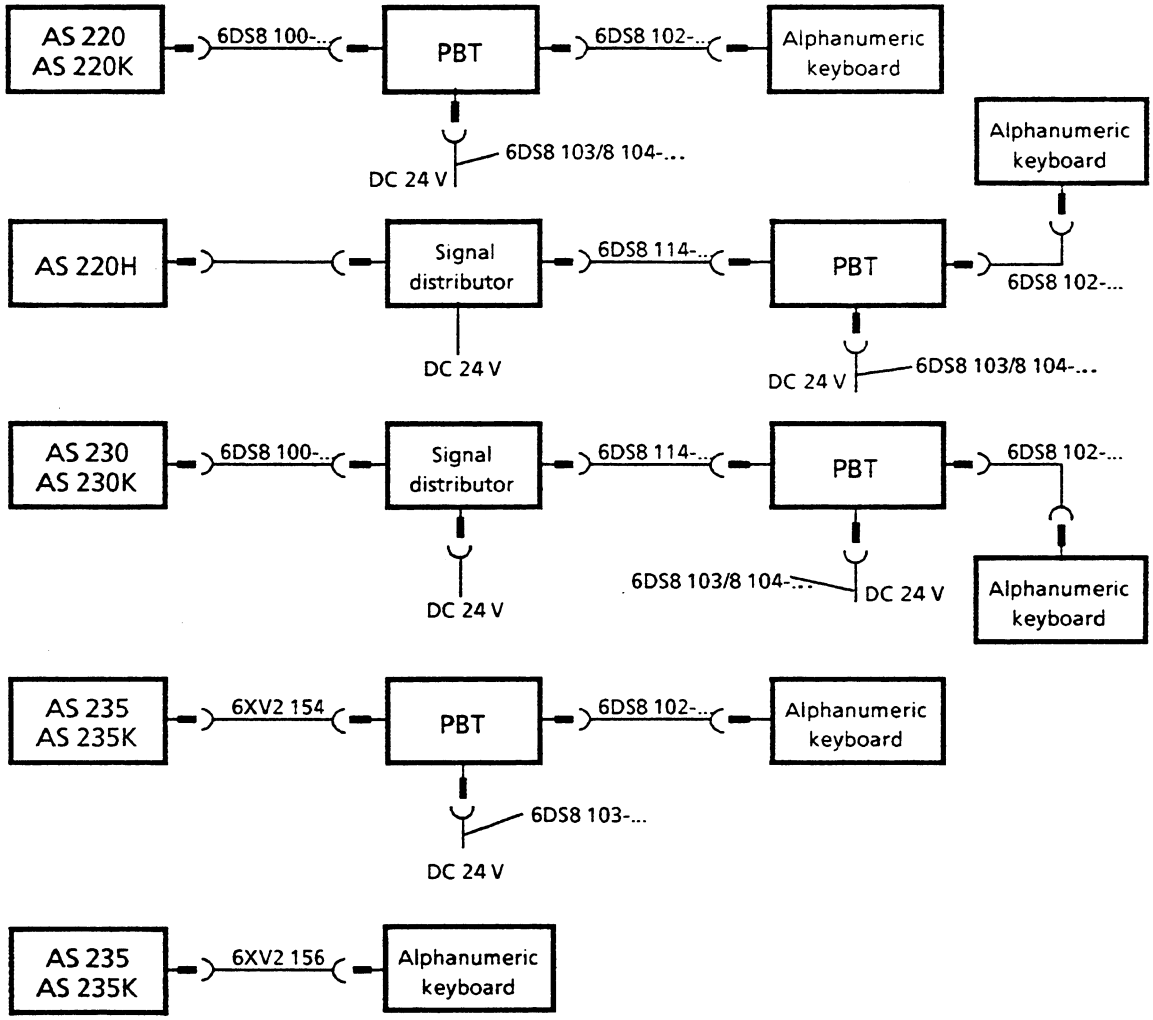


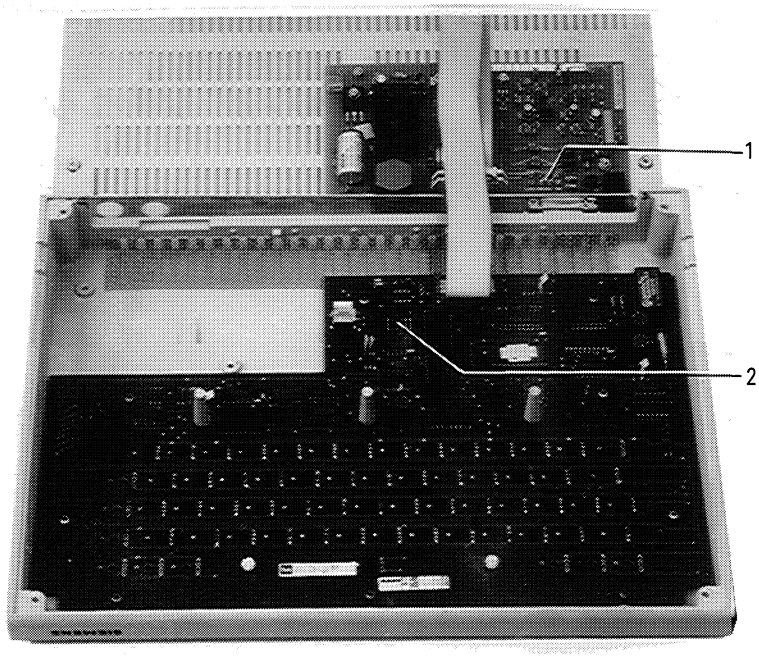
Fig. 1 Keyboard connection

2 Design

The alphanumeric keyboard is housed in a desk-shaped table-top casing. It consists of the

- keypad with keyboard control and serial interface and the
- power supply p.c. board.

A 24 V supply voltage must be provided. All other necessary voltages are produced from this voltage. The supply is fed in via the signal cable.



Bottom part

1 Line current
Interface settings
X5 to X12

2 Jumper setting
Transmission mode ST 3

Upper part

Fig. 2 Keyboard opened

3 Technical Data

Printed circuit board in table-top casing with base plate and common connector for power and data lines.

Dimensions	57 mm x 370 mm x 280 mm (h x w x d)
Weight	approx 2.6 kg
Power supply	DC 24 V; 200 mA (tolerances as per SN 26555
Interface	TTY interface; 20 mA single line current, active
Transmission speed	110, 300, 1200, 2400, 4800 und 9600 bits/s Standard: 1200 bits/s
Connection	Connector with 15 leads
Permissible ambient temperature	+ 5 to + 40 °C
Relative humidity	Max. 95 % at 25 °C

4 Installation and Commissioning

All components supplied must be checked for possible damage before installation.

WARNING

When operating electrical equipment, certain parts of this equipment have a dangerously high voltage level.

Non-compliance with the warnings may therefore result in severe personal injury or substantial damage to property.

Only suitably qualified personnel should be allowed to work on this equipment or in its vicinity.

These persons must be fully conversant with all warnings and maintenance measures as set out in these instructions.

It is assumed that this product be transported, stored and installed as intended, and maintained and operated with care to ensure that the product functions correctly and safely.

QUALIFIED PERSONNEL

as referred to in these instructions as well as the warnings on the product itself are persons who are familiar with the installation, commissioning and operation of the product and are suitably qualified for their job, such as:

a) Personnel who have been trained to work with the equipment and who are authorized to energize, deenergize, ground and tag circuits, equipment and systems in accordance with the established safety practices.

b) Personnel who have been trained in accordance with the established safety practices to use and service appropriate safety equipment .

c) Personnel who have been trained in first aid.

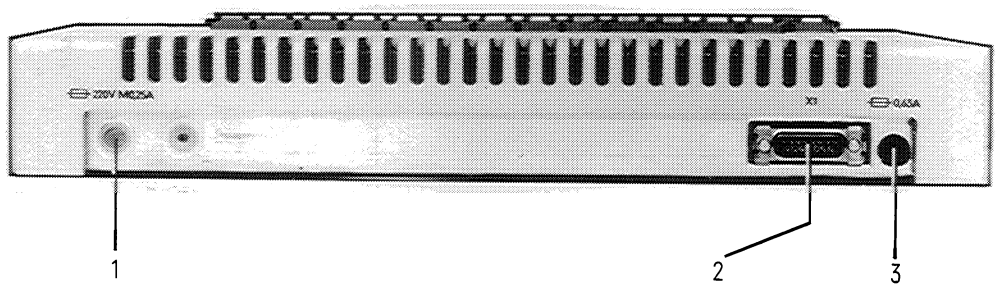
d) Personnel who are suitably trained to work with process control equipment and systems installed in power plants.

Note

The guidelines for handling electrostatically sensitive devices (EGB) must be observed when handling electronic modules. All electrostatically sensitive devices are clearly marked by a label on the transport container and a sticker on the module itself.

4.1 Connection

The alphanumeric keyboard is connected through the cable connector 6DS8102-8.. to the process operation keyboard (plug X1 at the rear, see Fig 3). The 24 V supply voltage is also fed in through the cable connector.



1 Connection not used
2 Connection of cable connector
3 Fuse

Fig. 3 Rear view of the alphanumeric keyboard

4.2 Fuse

The 24 V supply is protected by a T0.63 A fuse. The fuse is located at the rear beside plug X1 (see Fig. 3).
The inscription 220 V/0.25 A has no significance (connections are not occupied).
After application of the supply voltage, the keyboard is ready for operation. There is no ON/OFF switch.

4.3 Jumper Settings

- Supply unit

By means of jumpers, the serial interface can be connected for the active or passive mode (jumpers X5 - X12 on the power supply p.c. board).

- Interface inactive (line current from higher-order device)

- Jumper X6 - X10 inserted
  X7 - X11 inserted

- Interface active (keyboard supplies 20 mA line current)

0 Volt switched:

Jumper X6 - X9 inserted
X7 - X10 inserted
X11 - X12 inserted
} Standard setting

12 Volt switched:

Jumper X6 - X11 inserted
X7 - X12 inserted
X9 - X10 inserted

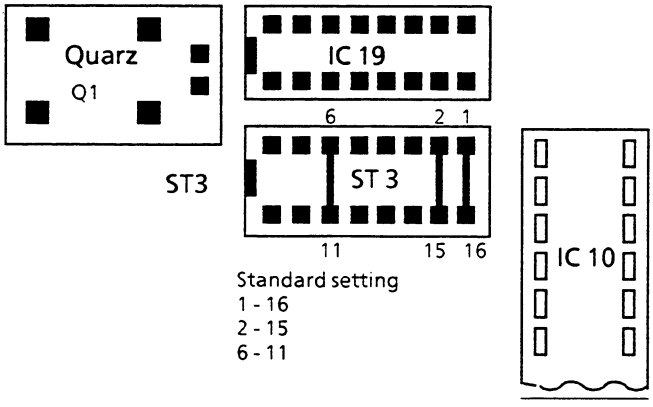
- Key panel

The transmission speed, the number of stop bits and the formation of the parity bit can be set on the jumper pin-board ST3 on the key panel.

Jumper 1 - 16 must be inserted (TTY line current supply)
6 - 11 not inserted: No parity bit
inserted: With parity bit
7 - 10 not inserted: Even parity bit
inserted: Odd parity bit
8 - 9 not inserted: 2 stop bits
inserted: 1 stop bit

Transmission speed	Jumpers			
	2-15	3-14	4-13	5-12
110 Bits/s	x	x	-	x
300 Bits/s	x	-	x	-
1200 Bits/s	x	-	-	-
2400 Bits/s	-	x	-	x
4800 Bits/s	-	-	x	x
9600 Bits/s	-	-	-	x

Location of jumper pin-board ST 3



5 Maintenance

5.1 Mechanical Design

The keypad is fixed to the upper part of the case, the power supply board to the lower part of the case. The two modules are connected through a flat strip cable (see Fig. 2).

5.2 Mode of Operation

A 7-bit code is produced by the keypad. With the transfer signal STB, these 7 bits are transferred into the transmitter (IC10-IM6402), start bits, parity bits and stop bits are added and sent out serially at the set transmission speed. The level conversion for data line is carried out by means of an optocoupler (IC20).

5.3 Coding

Encoding of the keys is carried out through a matrix with line and column lines. Assignment to the particular key code takes place in an EPROM. At its outputs, the EPROM delivers the ISO 7-bit code.

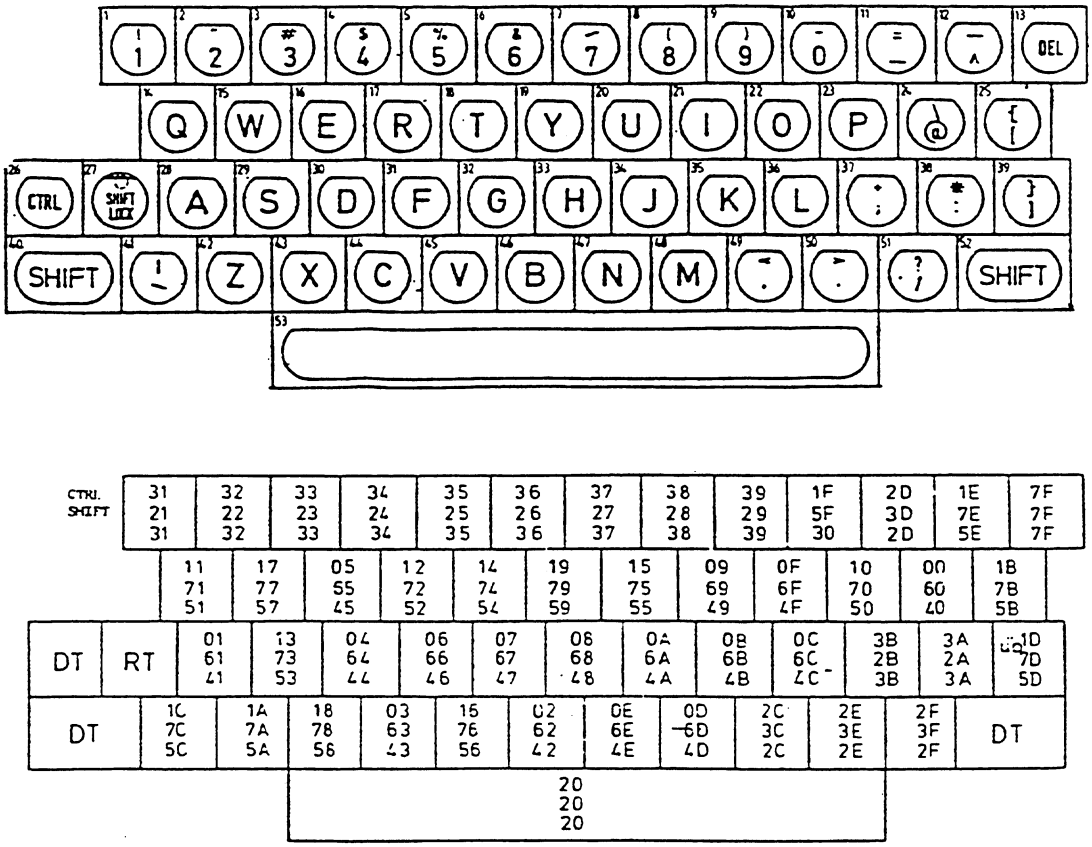


Fig. 4 Key arrangement and coding

5.4 Testing and Corrective Maintenance

- Replacement of keys

The keys have active Hall generators as switching elements. When a key is pressed, the two outputs (the center connections) switch to 0 Volts. In case of a defect, the key can be withdrawn and replaced, after unsoldering the four connections. In order to provide a firm base for the key (to avoid pressure on conductor paths), it must be firmly seated on the board during soldering in.

- Voltages

When the + 5 V voltage on the power unit has reached its nominal value, a red LED lights up.

5.5 Connector/Cable Connector Allocation

Pin No.	Designation
1	S1 –
2	S2 +
3	–
4	–
5	–
6	0 V
7	Signal ground
8	+ 24 V
9	–
10	–
11	–
12	–
13	0 V
14	Signal ground
15	+ 24 V

Transmission data

- **Cable connector**

Allocation

Signal name	15-way male connector	Core colour	15-way socket connector	Signal name
-E21	Pin no. 1	blue 1	Pin no. 1	S1
+ E22	2	red 1	2	S2 +
-S21	3	grey 1	3	E1-
+ S22	4	yellow 1	4	E2 +
0V	6	green 1	6	0V
24V	8	brown 1	8	24V
PE	7	white 1	7	PE
PE	14	black 1	14	PE
-DF1	9	blue 2	9	DF1-
+ DF2	10	red 2	10	DF2 +
	11	grey 2	11	
	12	yellow 2	12	
0V	13	green 2	13	0V
24V	15	brown 2	15	24V

5.6 Spare Parts/Repairs

The spare parts list is enclosed in the Appendix.
Ordering address for spare parts

ANL 434 ED (Siemens Erlangen).

Defective parts are to be sent to

GWK QVR (Siemens Karlsruhe)

for repair.

Pos.	Description	Order No.	Maker's Designation	Spare parts group *)	Quantity per product	Contained in or applicable from revision level	
1	Case, upper part	C79372-A3002-B205		N	1		
2	Keypad, alphanumeric	C79372-A3002-B210		RO	1		
3	Power supply unit	C79372-A3002-B225		RO	1		
4	Key (without inscription)	C74451-Z69-U201	Rafi No 3.13001.002	N	52		

*) R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

1) Depends on system design
2) When using only 1 combined pushbutton in the cover panel.

Place of delivery: ANL 434 - ED Erlangen

TELEPERM M Parts List

Alphanumeric Keyboard
6DS3 303-8AA

C79000-E8076-C036-04
11.89

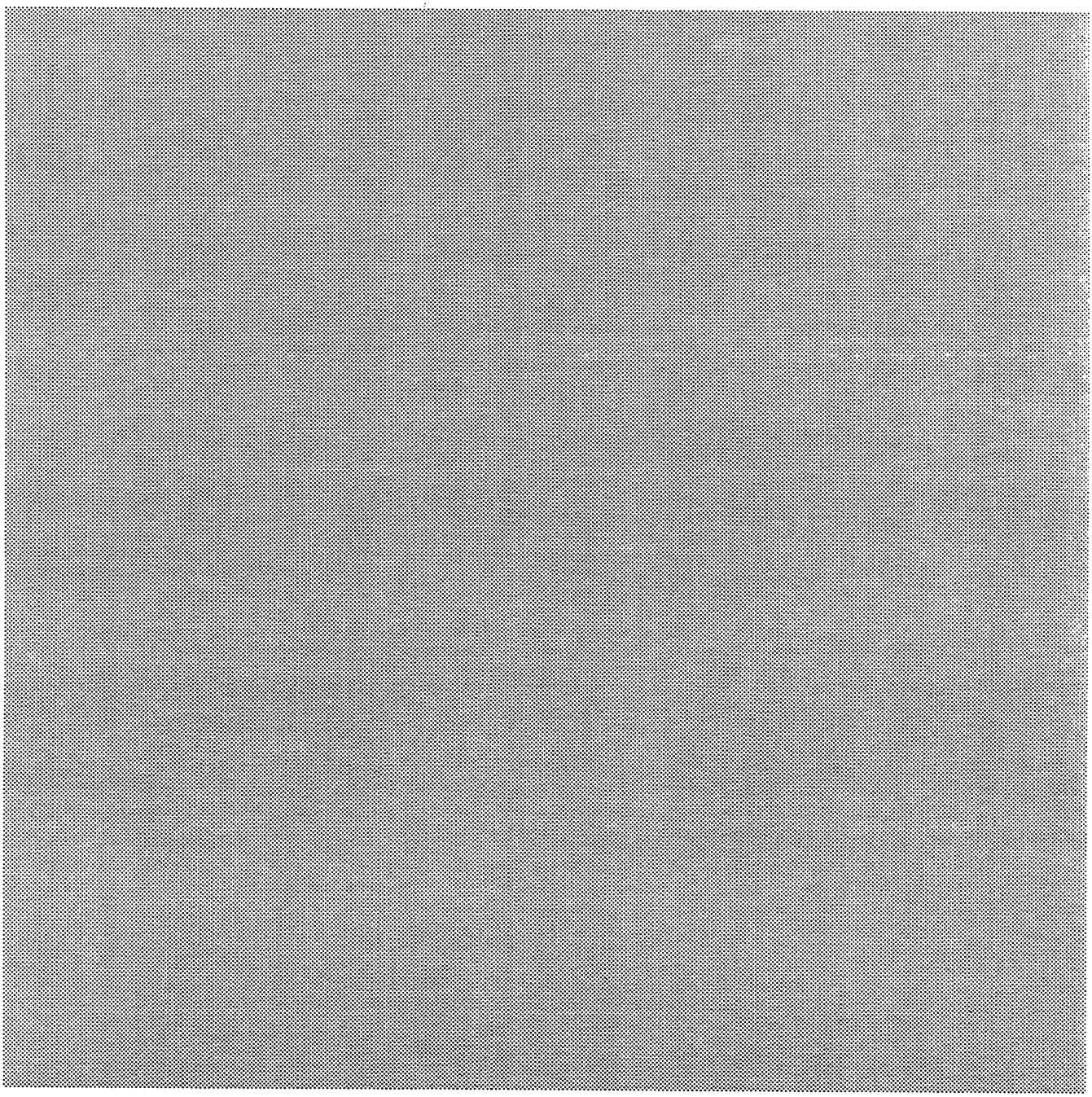
Sheet: 1
Sh.

SIEMENS

TELEPERM M

Process Operation Keyboard
6DS3 305 – 8BA

Instructions C79000-B8076-C410-01



Contents

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1 Description

1.1 Application

The process operation keyboard (PBT) is used with the AS 235, AS 235 H and AS 235 K automation systems to:

- Modify operation modes (e.g. automatic, manual)
- Enter and modify operating values (e.g. setpoint, manipulated variable)
- Select an overview display, area display, group display or loop display
- Acknowledge e.g. a message on the process monitor or an alarm (horn)

The process operation keyboard is used for local operation and process control. Fig. 1.1 shows a process operation keyboard incorporated in the system.

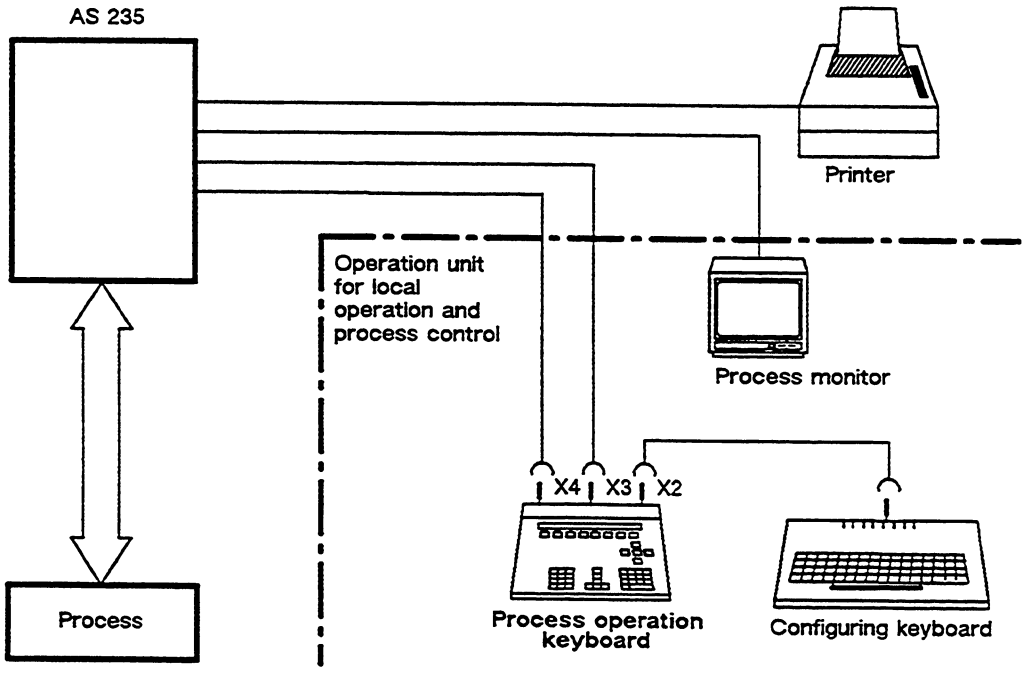


Fig. 1.1 Process operation keyboard in the system

1.2 Design

The process operation keyboard is accommodated in a console housing and consists of a dust-proof and splash-proof touch pad keyboard and an LCD unit.

There are three connectors at the rear:

- Plug X2 for configuring keyboard
- Plug X3 for higher-level system (e.g. AS 235)
- Plug X4 for power supply cable

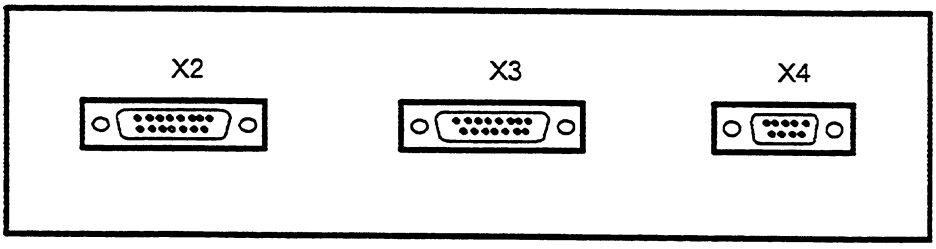


Fig. 1.2 Rear view of process operation keyboard with connectors

It is possible to upgrade the process operation keyboard to the degree of protection IP 54 (see Fig. 1.3) using a kit in order to protect the rear connectors against environmental influences (dust, splashing and gases).

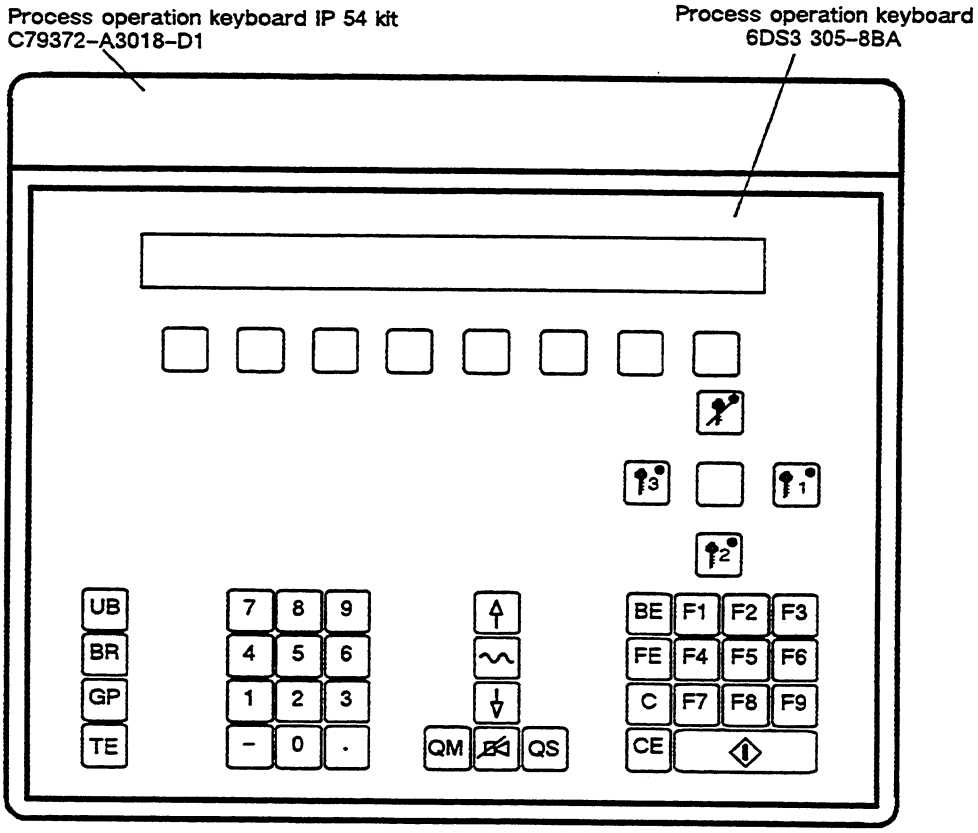


Fig. 1.3 Process operation keyboard (IP 54 design)

2 Installation and Commissioning

2.1 Installation

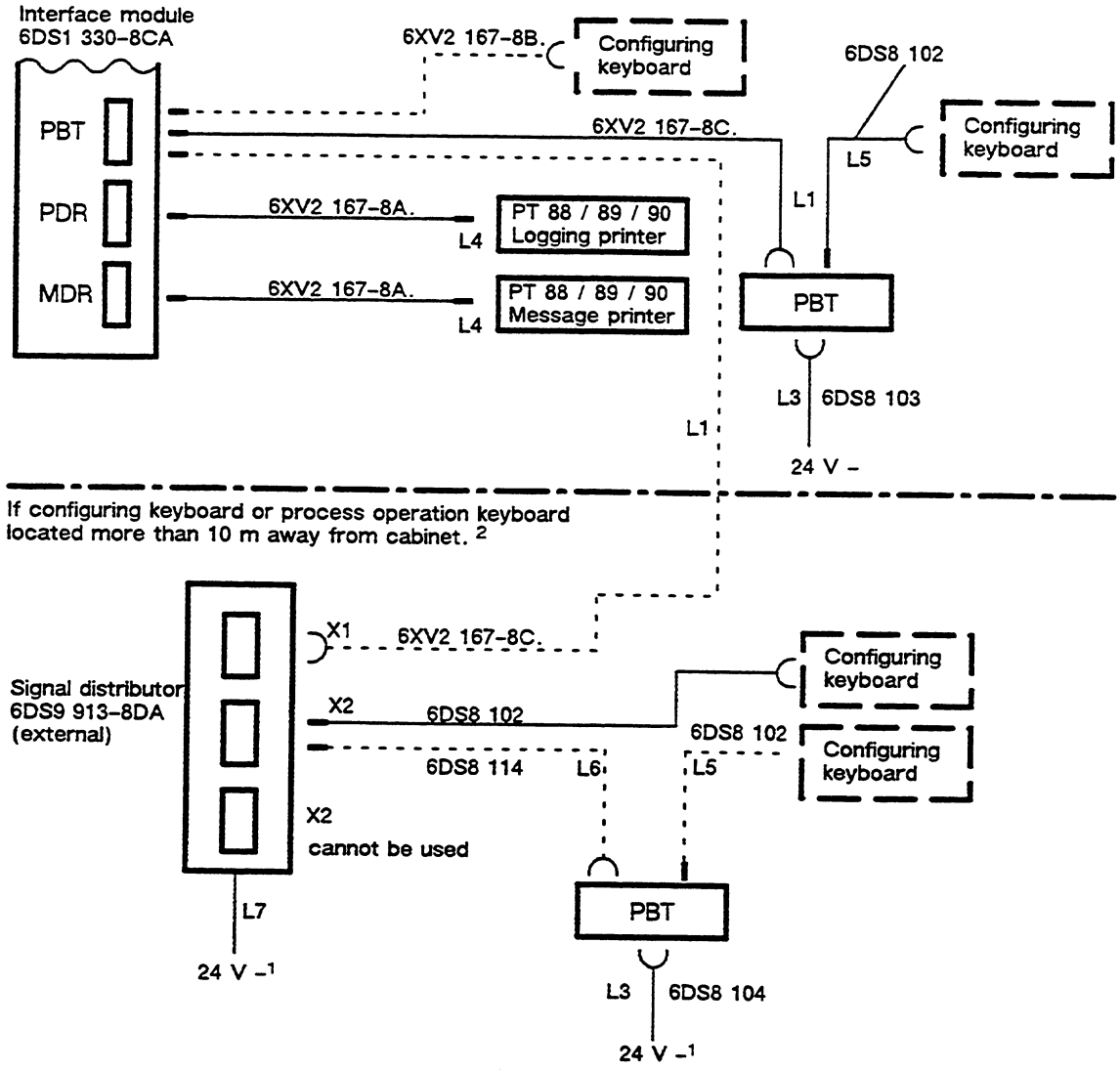
Connect the process operation keyboard as in Fig. 1.1.

Assemble the process operation keyboard IP 54 kit (Order No. C79372–A3018–D1) according to the instructions included with it.

Cable connectors for process operation keyboard (see also Fig. 2.1):

Cable connector	
6DS8 103–8.. [1]	For connection to the socket in the power supply subrack (AS 235 H) or the power supply module (AS 235/AS 235 K)
6DS8 104–8.. [1]	For connection to existing DC 24 V supply
6XV2 167–8C..[1]	For connection of process operation keyboard to signal distribution unit 6DS9 913–8DA or directly to the interface module for operation channel 6DS1 330–8CA of the AS 235 automation system
6DS8 114–8.. [1]	For connection of a process operation keyboard to a signal distribution unit
6DS8 102–8..[1]	For connection of a configuring keyboard (X2 of process operation keyboard)

[1] see length codes in catalog



Cable connector	Length in m	Conditions
6XV2 167-8CB...-8CU	L1 ≤ 150 L1 ≤ 10	L3 to 24 V- external [1] L3 to 24 V- cabinet (power supply subrack)
6XV2 167-8BB...-8BU	L2 ≤ 10 L1 + L2 ≤ 150	L3 to 24 V- external [1]
6DS8 103-8.. 6DS8 104-8..	L3 ≤ 10 L3 ≤ 10	To 24-V connection in AS/MS To existing 24 V external
6XV2 167-8AB...-8AU	L4 ≤ 100	PT 88, 89, 90
6DS8 102-8..	L5 ≤ 30	
6DS8 114	L6 ≤ 150	[2]
	L7 = 2	Fixed connection to signal distributor

[1] External 24-V supply (22 to 30 V).
[2] An external 24-V supply must be installed for the keyboards if they are operated more than 10 m away from the cabinet; the supply must be incorporated into the earthing concept of the system.

Fig. 2.1 Keyboard cable lengths

2.2 Commissioning

The process operation keyboard is ready for operation following connection of a DC 24 V supply to connection X4. A display is located between the keys of key group 5 (see Fig. 3.1). The process operation keyboard is ready for use if it lights up green; a fault is present in the keyboard if it lights up red. An error message (see Section 3.3) is usually displayed.

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3 Operation

3.1 Summary

3.1.1 Display Organization

The process operation keyboard is used for process control. A hierarchically-arranged display organization with different levels is available on the process monitor for operation and monitoring of the process.

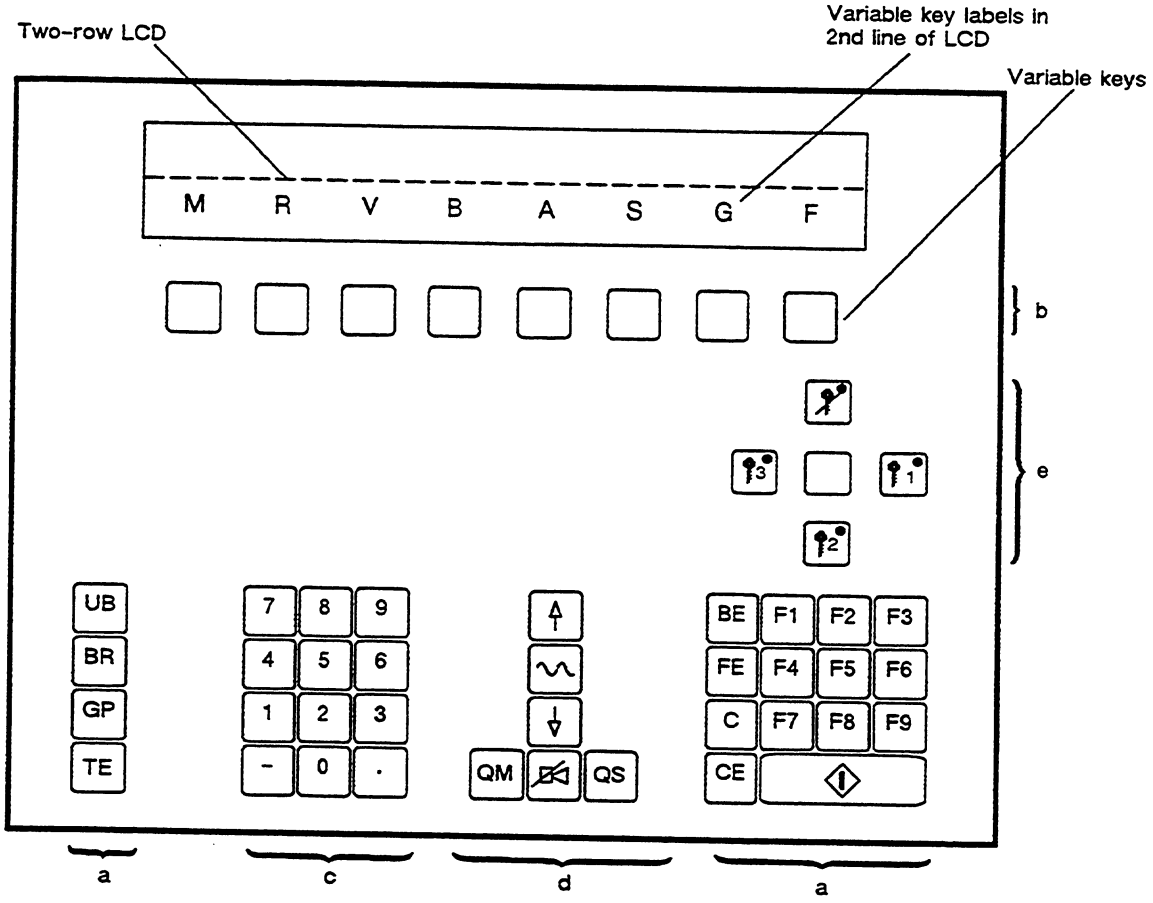
Level	Display	Max. number
4	Overview display	1
3	Area display	1 area
2	Group display	56 groups per area
1	Loop display	56 loop per group

Table 3.1 Display levels

All process information is output in dynamic mode in the displays in order to be able to monitor the process. It is possible to intervene with the process, e.g. in order to modify an operation value. To simplify operation, some of the input sequences are defined as function keys.

3.1.2 Operation, Signalling and Display Elements

The keyboard is divided into five key groups (see Fig. 3.1). Each input must be terminated by the ⏎ key (appears on screen as ";"). Exceptions are the keys which already contain the command.



a) Key group 1 (fixed function keys and execute key ⏎)
b) Key group 2 (variable function keys)
c) Key group 3 (numeric keypad)
d) Key group 4 (adjustment and acknowledgement keys)
e) Key group 5 (authorization keys with LEDs)

Fig. 3.1 Key groups of process operation keyboard

3.2 Operation

3.2.1 Start-up Response and Password Dialog

A selftest (EPROM and RAM tests) is carried out by the process operation keyboard each time it is switched on. If the selftest is executed without errors, the keyboard automatically switches to the last set authorization level.

The authorization level of the keyboard can be changed using the authorization keys.

Authorization	Meaning	Password (delivered state)
0	Keyboard OFF, no operation possible	0000
1	Process operation keyboard ON	1111
2	Configuring keyboard ON	2222
3	Configuring and process operation keyboards ON	3333

Table 3.2 Authorization keys

When pressing e.g. the authorization key 1, the following message appears in the display:

```
Password
```

Authorization level 1 is set if the password "1111" is entered and terminated by the execute key ⏎. The LED integrated in the authorization key then lights up.

Access to another authorization level, e.g. 3, is only possible with the associated password. An entered password must be terminated by the execute key. The process operation keyboard is then at the new authorization level if the input is correct. A message is output in the event of an error, and the old setting is retained.

The password can be changed if it is not terminated by the execute key but by "." or by "-". A request appears in the display to enter the new password (max. 4 digits). The new input must be terminated by the execute key. The input can also be carried out without entering digits. A password is then no longer necessary in order to enter the required authorization level.

3.2.2 Fixed Function Keys (Key Group 1)

Meaning of individual keys:

- [UB] Selection of overview display (if present).
  The function of the [◈] key is already included.

- [BR] Selection of the/an area display.
  Command is not terminated (;) since the number of the required display must subsequently be entered. The keyboard automatically enters a "," prior to the input of a digit in order to retain the syntax rules.

- [GP] Selection of a group display.
  (Response corresponding to BR).

- [TE] Key extension of key group 2,
  (see Section 3.2.3).
  The function of the [◈] key is already included.

- [BE] Operation of a loop.
  After a loop has been selected and this key has been pressed, the labels of key group 2 change according to the selected loop (see Section 3.2.3).
  The function of the [◈] key is already included.

- [FE] Function extensions.
  Overwrites the values defined in the display for key group 2. It is thus possible to select and execute additional commands (see Section 3.2.3).

- [C] Clear input line.
  The complete input line appearing on the screen of the operation unit is cleared when this key is pressed.

- [CE] Clear last character.
  This key clears the last character displayed in the input line of the process monitor. If several characters were sent in succession after pressing a function key, all of them are cleared.

- [◈] Execution of operator input.
  Termination of a command sequence on the screen of the operation unit by means of the execute character ";".
  Certain function keys already contain this execute character in their command sequence.

- [F1] to [F9] Function keys to trigger functions specific to the operation.
These keys trigger single or cyclic processing of blocks and block sequences.
The function keys as well as the blocks or block sequences are defined in the function block FUTA.
"FT,1;" to "FT,9;" are sent as the key codes. The execute character is thus already included.
An extension using key group 2 is possible if the function keys are insufficient (see Section 3.2.3).

3.2.3 Variable Keys (Key Group 2)

The variable keys have the meaning of the corresponding key label displayed in the LCD above them. The keys are labelled according to the higher-level system when one of the BR or GP keys is pressed. For example, the following labels appear with the AS 235 system:

Key	1	2	3	4	5	6	7	8
Label	M	R	V	B	A	S	G	F
Label following pressing of TE	T	C	EM	EV	RE	DZ	EG	FN
Label following renewed pressing of TE	GK	FM	RN	BILD	PKM	PKF	TANZ	TUEB
Label following renewed pressing of TE	SR	RK	EU	EK	RSKB	MSB	TVB	

Table 3.3 Basic labels of variable keys with the AS 235

The basic status is reestablished when the TE key is pressed again unless further system-specific blocks are present.
The key labels are transferred from the AS to the keyboard. A key is blocked if it is not labelled.
These keys can be used to select the individual loop displays if the respective loop display No. is added using the keys of key group 3. The BE key must first be pressed if an operation is to be carried out on the selected loop. The label of key group 2 then changes according to the label in the loop display of the selected loop (M, R, etc.).

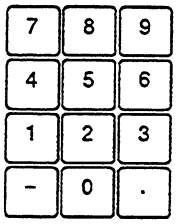
The variable keys can be influenced using the FE key. The labels sent from the AS or MS are overwritten. Input texts for which own function keys do not exist are displayed instead. Assignment of variable keys by pressing FE:

Key	1	2	3	4	5	6	7	8
Label	QF;	QF,*;	BI;	FT,		WDH	ENDE	LICHT

Table 3.4 Labelling of variable keys with function extensions

- QF; The command sequence is sent to the AS and means the output of all I & C messages.
- QF,*; The command sequence is sent to the AS and means the output of all I & C messages without release.
- BI; The command sequence is sent to the AS and triggers a hardcopy of the screen contents.
- FT, The command sequence is sent to the AS. A number sequence must then be entered using key group 3 and terminated by the execute key ⏎ . Thus function keys greater than 9 defined using FUTA and not present on the process operation keyboard can also be executed.
- WDH Pressing this key repeats the last input line. The execute character ";" is suppressed, however, to enable a correction using CE.
- LICHT The illumination of the display is switched on. The illumination is switched off automatically after a certain time if no further keys are pressed or if the key has been pressed again.
- ENDE The original state is reestablished by pressing this key or the FE key.

3.2.4 Numeric Keypad (Key Group 3)



This key group consists of digits 0 to 9 and the special characters "." (decimal point) and "–" (minus sign).
The keys are only used together with other keys and only send the displayed character.
Exception:
a "," is inserted following BR or GP prior to the subsequent digits.

A decimal point and minus sign are only meaningful in two cases:

- During the input of analog values in operation mode (BE pressed)
- To modify the password (see Section 3.2.1).

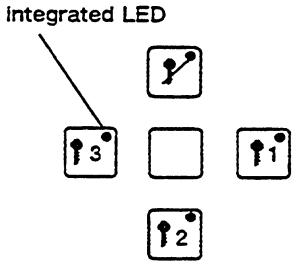
3.2.5 Positioning and Acknowledgement Keys (Key Group 4)

Meaning of keys:

- QM — Acknowledgement of a message in the 1st line on the screen (I & C alarm or message of the MEL or PKF block).
  The function of the ⏎ key is already included.
- QS — Start of next control step (only with function block S in operating mode "Step control").
  The function of the ⏎ key is already included.
- Acknowledgement of an alarm (horn).
  The function of the ⏎ key is already included.
- Increase
- High-speed
- Decrease

Analog values, e.g. setpoint or manipulated value, can be adjusted in steps using these keys. The adjustment is approx. 1 % of the range per processing cycle or 10 % of the range if the high-speed key is pressed at the same time.

3.2.6 Authorization Keys (Key Group 5)



Authorization keys 0 – 3 (see Section 3.2.1)

- Keyboard OFF
- Only process operation with process operation keyboard and configuring keyboard
- Configuring keyboard ON
- Configuring and process operation keyboard ON
- Message and operation display (see Section 3.3)

3.2.7 Reset

The process operation keyboard is reset by simultaneously pressing the following keys (software reset):

+ TE + CE

3.3 Messages

The message and operation display present inside the authorization keys always lights up green. Maloperations or faulty interfaces are indicated in plain text; the process operation keyboard nevertheless continues in normal mode.

Fundamental errors which influence the operation state of the process operation keyboard lead – if still possible – to red flashing of the display.

The LEDs on the authorization keys indicate the set authorization level.

3.3.1 Message Texts in Normal Operation

The following messages can be displayed on the LCD during normal operation of the keyboard depending on the input, the keyboard status and the connections:

`EPROM - Test` `(EPROM test)`

Is carried out when the process operation keyboard is started up. The display disappears if the test is carried out correctly. The message and operation display flashes red in the event of a fault and – if still possible – an error number appears. The red LED flashes.

`RAM - Test` `(RAM test)`

The test is carried out after the EPROM test when the keyboard is started up. The display disappears if the test is carried out correctly. Otherwise the operation display flashes red and an error number is output. The red LED flashes.

`Schnittstelle 1 unklar!` `(Interface 1 not ready)`

The cable connection between the process operation keyboard and the AS is not OK (not inserted, incorrect cable, line interruption).

`AS 235- System unklar!` `(AS 235 system not ready)`

Connection to system has been made, but the system does not register or not correctly.

`PBT - Anlauf!` `(Process operation keyboard start-up)`

Only serves as information for start-up or restart of keyboard. Usually only flashes very briefly.

`Passwort:` `(Password)`

Request to enter the password for the selected authorization level.

`Passwort nicht geändert (Password not changed)`

The message is output if an attempt is made to change the password but the new password is not correct. The old password is then retained.

`Passwort falsch!` `(Password incorrect)`

The entered password is illegal for the desired authorization. The old authorization level remains set.

`Passwort: ▮▮▮▮ Neues Passwort:` `(Password: ▮▮▮▮ New password:)`

The input of the current password of an authrorization level was not terminated by the execute key ⏎ but by "." or "-". The keyboard requests the input of a new password.

`Alpha-Tastatur unklar` `(Alphanumeric keyboard not ready)`

The message appears if the alphanumeric keyboard (configuring keyboard) is permissible (authorization level 2 or 3) but is not connected or no longer connected.

3.3.2 Faults During Normal Operation

There are numerous positions within the program which are never branched to during correct execution. A hardware or software error must have occurred if these are reached.

It may be the case that a correct error display is not possible when such a fault occurs. It is also difficult to carry out an analysis.

The process operation keyboard attempts in these cases to output an error number on the LCD. These error numbers always appear in the first line. Further text is present in some cases. The display inside the authorization keys subsequently flashes red. The processor branches into a wait loop so that no further operations are possible.

The keyboard can only leave this state by switching off and on again, a software reset has no effect.

Note the error number in such a case, restart if necessary, or obtain further information in test mode (see Section 3.4). Send the process operation keyboard for repair together with this information (see Section 4).

3.4 Maintenance

3.4.1 Test Mode

A test cable, Order No. C79372-A3018-D2, is required to enter test mode.

The test cable must be connected to the process operation keyboard with the power disconnected (remove plug X4). The two serial interfaces (plugs X2 and X3) of the keyboard must be connected using the test cable. The power supply to the keyboard can then be reconnected (insert plug X4).

The following test steps are carried out in test mode by operations in the defined sequence:

- LED test
- Initialization and deletion of LCD
- EPROM test
- LCD test
- RAM test
- Key test
- Interface test
- Test of authorization memory
- Reset of passwords

Errors (e.g. pixel errors, key functions) must be checked visually on the LCD during the test. In addition, the display of an error number automatically leads to a test abort.

3.4.2 Test Sequence

The process operation keyboard immediately switches on the LED of authorization key "0" following resetting. The processor cannot start-up at all if this does not take place, i.e. if no LED lights up at all or if other LEDs light up as well, or if all LEDs light up continuously. Further troubleshooting is then not possible in test mode.

The keyboard starts the test when any key is pressed. The reason for this is the speed with which the following LED test is executed.

- LED test

Any characters are possible and permissible on the LCD.

All LEDs are switched off.

The message and operation display lights up red and green briefly in succession.

The LEDs on the authorization keys 0,1,2 and 3 light up briefly in succession.

All LEDs are switched off again.

- Initialization and deletion of LCD

The following text appears in the display if any key is pressed:

"LCD - initialisiert" (LCD initialized)

The authorization keys 0 and 1 light up.

- EPROM test

The EPROM test is activated by pressing any key.

"EPROM-Test" (EPROM test)

appears on the LCD.

The message and operation display lights up green and remains green during further execution of the test. Authorization key 2 lights up. The keyboard then indicates its readiness for the LCD test by the message:

"LCD-Anzeigetest....Drücke eine Taste" (LCD test...press a key)

- LCD test

The authrorization keys 0 and 2 light up if a key is pressed.

The following message is first displayed in line 1:

"LCD-Anzeigetest.... Drücke eine Taste" (LCD test...press a key)

Line 2 is enclosed by black blocks and can be visually checked. The test waits until any key is pressed.

The procedure is then repeated with replaced lines. A key must be pressed to continue if correct.

The above two steps are repeated with spaces initially in line 2 and then in line 1 after pressing a key.

At the end, the following is written in line 1:

"THE QUICK BROWN FOX JUMPS OVER THE LAZY"

and in line 2:

"DOG. 1234567890 <> = , . : ? ! % @"

- RAM test

The RAM test is activated by pressing any key.
The LEDs of authorization keys 1 and 2 light up and the following message appears in the display as long as the test is running:

"RAM-Test" (RAM test)

The key test starts immediately when this test has been executed correctly.

- Key test

Inputs must be made to carry out this test. The following steps are executed:

The authorization keys 0, 1 and 2 light up.

"Tasten - Test" (Key test)

is written in line 1; line 2 is empty.
If a key is now pressed, the respective key is indicated by an associated text in line 2 on the LCD.

You can decide whether to test all keys or only individual keys, and whether only once or several times.
The key is terminated by the execute key ⏎, which is also displayed when pressed.
The interface test is then activated.

- Test of serial interfaces

Authorization key 3 lights up during this test.

"Schnittstellen - Test" (Interface test)

is written in line 1.

"Schnittstellen-Test läuft ***(*)" (Interface test running ***(*))

is displayed in line 2.

- Test of authorization memory

The authorization keys 0 and 3 light up during this test.
The next test step

"Passwort rücksetzen" (Reset password)

is selected when this test has been terminated.

- Resetting the passwords

It is possible to reset all passwords to the state when delivered.

Note:
If this is not required, you must switch off at this point!

Resetting is carried out as follows:

The authorization keys 1 and 3 light up.

The following is displayed:

```
"Passwörter rücksetzen: "Taste drücken"   (Reset passwords: press key)

"andernfalls abschalten"                  (otherwise switch off)
```

If any key is pressed

```
"Testmodus beendet"                       (Test mode terminated)
```

is output, and the process operation key can be switched off.

The test cable must be removed if test mode is no longer required.

3.4.3 Measures With a Faulty Keyboard

A faulty process operation keyboard must be returned to the spare parts service together with specification of the error number (see Sections 3.3.2 and 3.4.1):

ANL A434 ED
Spare Parts Services
Erlangen
Germany

4 Spare Parts

Item	Description	Order No.	Maker's designation	Spares group [1]	Number per product	Contained in, or applicable from Revision level
1	Process operation keyboard (PBT)	6DS3 305-8BA		R0		Can replace version -8AA if the printer is not connected via the PBT. Cannot be used with signalling systems
2	IP 54 kit	C79372-A3018-D1		N	1 [2]	
3	Cable inlet	C79103-A9001-D6		N	3 [2]	For IP 54 kit
4	Gasket	C79372-A3018-C7		N	1 [2]	For IP 54 kit
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20						

[1] R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

[2] Order in GWK from PL AZ

Available from: ANL A434 - ED
Erlangen

Spare Parts List
Date: 20.01.92

Empty page

5 Appendix

5.1 Technical Data

Interface	
– Configuring keyboard (plug X2)	20–mA current loop interface, floating, passive, transmission rate 1200 bit/s
– Automation system (plug X3)	20–mA current loop interface, floating, active, transmission rate 1200 bit/s
– Power supply (plug X4)	DC 24 V (18 to 33 V), 200 mA
Alphanumeric display unit	LCD 2 lines 40 characters / line With illumination
Variable function keys for operation	8
Permissible ambient temperature	
Operation	0 to 40 °C
Storage and transport	– 40 to + 70 °C
Permissible relative humidity	max. 95 % at 25 °C
Degree of protection to DIN 40050	IP 20 (IP 54 with kit)
Dimensions (h x w x d)	80 mm x 370 mm x 324 mm
Weight	Approx. 3 kg
Radio interference suppression	Limit class B according to VDE 0871 provision 1046/1984 or 843/1986
Safety requirements	VDE 0805 ≙ IEC 950 ≙ EN 60950

5.2 Pin Assignments

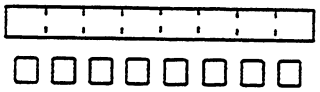
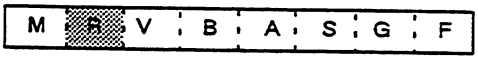
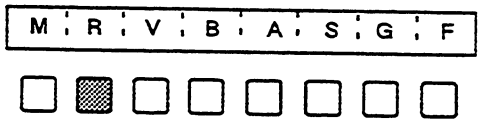
Pin	Plug X2 to configuring keyboard	Plug X3 to system	Plug X4 power supply
1	E21 – } Receive	S11 – } Transmit	0 Volt
2	E22 + } Configuring keyboard	S12 + } AS/MS	0 Volt
3		E11 – } Receive	
4		E12 + } AS/MS	System earth
5	Test	Test	System earth
6	0 Volt		
7	System earth	System earth	DC + 24 V
8	DC + 24 V		DC + 24 V
9			
10			Omitted, since 9-pin plug
11	S21 – } Transmit		
12	S22 + } Only for test purposes		
13	0 Volt	0 Volt	
14	System earth	System earth	
15	DC + 24 V		

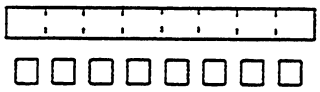
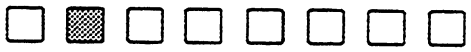
Table 5 .1 Plugs X2, X3 and X4

5.3 Keyboard Assignments (Summary)

Key selection	Explanation	Example
UB	Selection of an overview display (if present)	
BR ◈	Selection of an area display	Selection of area display "BR1" (more than one area display possible with MS) BR 1 ◈
GP [No.] ◈	Selection of a group display	Selection of group display "GP15" GP 1 5
GP ◈	Switch off operating mode **"BE"**	
TE	Key extension for keys with variable labels	**Selection of block type:** previous labels: M R V B A S G F TE Subsequent labels: T C EM EV RE DZ EG FN **Selection of operating elements:** previous labels: W= Y= WE=1 WI=1 YA=1 YH=1 TE Subsequent labels: AC=1 HD=1 E1=1 AU=1 QR=1
BE	Switch on operating mode **"BE"**	
FE	Function extension for keys with variable labels	**Function selection:** previous labels: M R V B A S G F FE Subsequent labels: QF QF,* BI FT WDH ENDE LICHT

Key selection	Explanation	Example
[C]	Clearing of input line	
[CE]	Clearing of last key character in the input line	
[↵]	Execution of an entered command	
[F1] [F2] [F3] [F4] [F5] [F6] [F7] [F8] [F9]	Function keys for triggering specific functions	
[↑] Increase [↓] Decrease	For adjustment of operating values in steps of 1%	Increase controller setpoint by 1%: [W=] [↑] Display in input line on screen: "W=>;" Then increase by further 1%: [↑] Display in input line on screen: ">;"
[↑] (simultaneously) [~] High-speed increase [↓] (simultaneously) [~] High-speed decrease	For adjustment of operating values in steps of 10%	Decrease controller manipulated variable by 10 %: [Y=] [↓] (simultaneously) [~] Display in input line on screen: "Y=<<;" Then decrease by further 10 %: [↓] + (simultaneously) [~] Display in input line on screen: "<<;"

Key selection	Explanation	Example
[QM]	Acknowledgement of a message in the message line on the process monitor	
[QS]	"Acknowledge step" switch to next sequence (only if S block is used and in operating mode "Step control") Request for operator input appears above input line: "QS" (red on black)	
[⌀]	Acknowledgement of an alarm	
[7] [8] [9] [4] [5] [6] [1] [2] [3] [-] [0] [.]	Numeric keypad plus [-] corresponding to "minus sign" [.] corresponding to "decimal point"	–42.5: [-] [4] [2] [.] [5]
	Select loop display of a particular block type	Step 1: Search for controller block "R": Press [TE] key repeatedly until R block appears on keyboard (if not already present):  Step 2: Select controller block "R" by pressing the associated key:  Step 3: Enter controller number e.g. "11" using numeric keypad: [1] [1] Subsequently terminate operator input: [⏎]

Key selection	Explanation	Example
	Operation of a specific loop display (operation mode "BE" switched on)	Step 1: Switch on operation mode "BE" by pressing the [BE] key; the following appears on the keyboard: W= | Y= | E=1 | I=1 | A=1 | H=1 | | Step 2: To modify the manipulated variable Y, press the associated key: W= | Y= | E=1 | I=1 | A=1 | H=1 | |  Step 3: Enter the desired value using the numeric keypad (requirement: controller block to "Manual"): [3] [6] Step 4: Subsequently terminate operator input: 

5.4 Abbreviations

AS Automation system

EPROM Erasable programmable read-only memory

LCD Liquid-crystal display

LED Light-emitting diode

MS Signalling system

PBT Process operation keyboard

RAM Random-access memory

5.5 Subject Index

SIEMENS

TELEPERM M

Process Communication Keyboard

6DS3 305-8AA

Instructions C79000-B8076-C038-05

CONTENTS

1 Application

The process communication keyboard (PTB) is used in the TELEPERM M process control system. The number of keys has been limited in order to make rapid and simple operation possible.

The functions of the keys can be preset by the higher-level system or from the keyboard itself and can be changed depending on the previous history ("dynamic marking"). By this operator prompting a low probability of errors is achieved.

The process communication keyboard is connected to the higher-level system via a serial interface (TTY - 20 mA.) An alphanumeric keyboard and a printer can be connected to the process communication keyboard (also via a TTY interface).

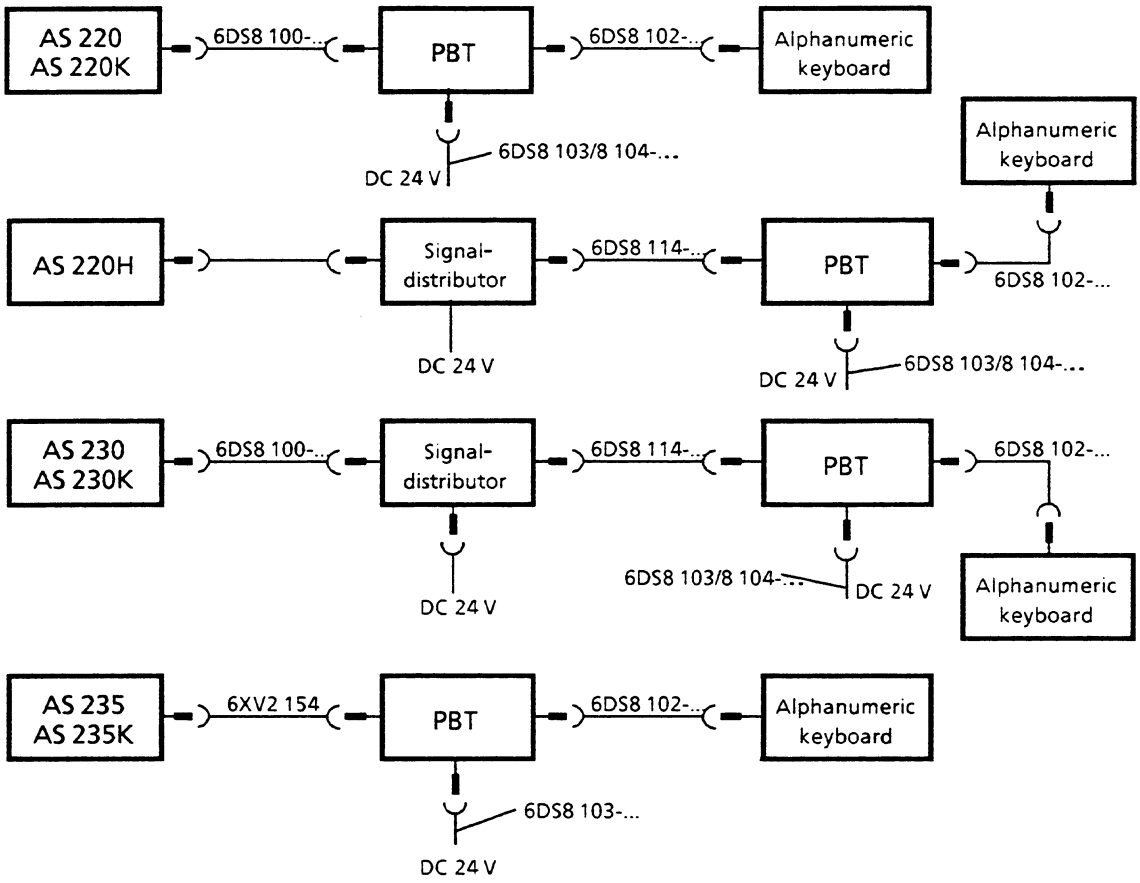


Fig. 1 Connection of the process communication keyboard in the system

2 Design

The process communication keyboard is housed in a desk-shaped table-top casing.

It consists of:

- basic module with microprocessor, microprogram, power supply and serial interfaces
- keypad
- display module with 40 alphanumeric characters for dynamic marking and with one red and one green LED.

A supply voltage of 24 V must be provided. The necessary voltages are produced from this by a switched-mode power supply unit.
The connections to the higher-level system, the printer, the alphanumeric keyboard and the power supply are made via four plugs at the rear of the process communication keyboard.

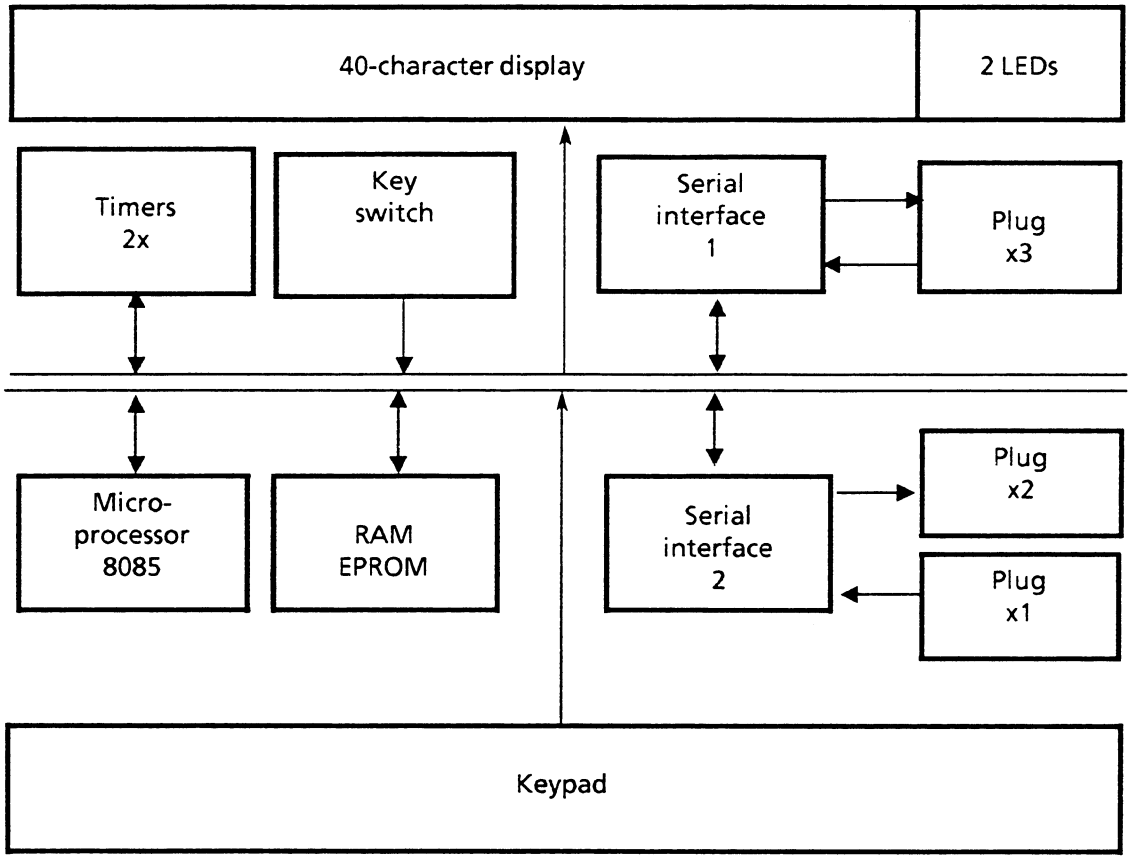


Fig. 2 Block diagram of the process communication keyboard

3 Technical Data

Design	Printed circuit board in table-top casing with base plate, separate plug-and-socket connections for power supply, data line for interface connections for power supply, data line for interface connection and for the alphanumeric keyboard/printer.
Dimensions (H x W x D)	78 mm x 370 mm x 280 mm
Weight	approx. 3.6 kg
Power supply	+ 24 V DC ; 700 mA
Interfaces	2 Teletype-interfaces; 20 mA single current; interface 1 switched to system in active mode ; interface 2 switched to devices in passive mode.
Transmission-rate	Interface 1: 1200 bits/s - standard setting Interface 2: 300 and 1200 bits/s Standard: 1200 bits/s
Display	40-character, alphanumeric
Connection	Power supply: 9-way plug Interface 1: 15-way plug Interface 2: 15-way plug (2x)
Permissible ambient temperature	up to + 40 °C
Permissible relative humidity	max. 95 % at 25 °C

4 Installation and Commissioning

All components supplied must be checked for possible damage before installation.

WARNING

When operating electrical equipment, certain parts of this equipment have a dangerously high voltage level.

Non-compliance with the warnings may therefore result in severe personal injury or substantial damage to property.

Only suitably qualified personnel should be allowed to work on this equipment or in its vicinity.

These persons must be fully conversant with all warnings and maintenance measures as set out in these instructions.

It is assumed that this product be transported, stored and installed as intended, and maintained and operated with care to ensure that the product functions correctly and safely.

QUALIFIED PERSONNEL

as referred to in these instructions as well as the warnings on the product itself are persons who are familiar with the installation, commissioning and operation of the product and are suitably qualified for their job, such as:

a) Personnel who have been trained to work with the equipment and who are authorized to energize, deenergize, ground and tag circuits, equipment and systems in accordance with the established safety practices.

b) Personnel who have been trained in accordance with the established safety practices to use and service appropriate safety equipment

c) Personnel who have been trained in first aid.

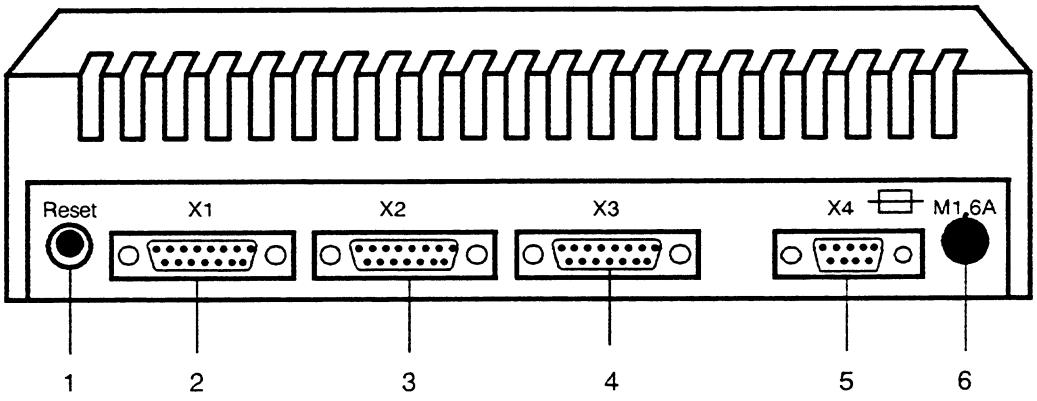
d) Personnel who are suitable trained to work with process control equipment and systems installed in power plants.

NOTE

The guidelines for handling electrostatically sensitive devices (EGB) must be observed when handling electronic modules. All electrostatically sensitive devices are clearly marked by a label on the transport container and a sticker on the module itself.

4.1 Cable Connection

The cable connections are located on the rear panel of the process communication keyboard (see Fig. 3)



1 Reset button
2 Alphanumeric keyboard
3 Printer
4 Higher-level system
5 Power supply
6 Fuse

Fig. 3 Rear panel of the process communication keyboard with cable connections.

4.2 Supply Voltage/Fuse/Reset

The 24-V supply must be fed in via plug X4. The fuse (M 1.6 A) for the supply voltage and the reset button are located on the rear panel (see Fig. 3)

4.3 Switching on and off

There is no on/off switch.
After the voltage is applied via plug X4, the process communication keyboard is ready for operation. The green LED on the right of the display panel indicates that the keyboard is ready for operation. If the red LED lights up, there is a fault in the system or in the peripherals.

4.4 Jumper Settings

The pin assignment for plugs X1, X2 and X3 can be changed by the setting of jumpers. The serial interfaces can be connected either actively or passively (via X15 to X18, see circuit diagram).

- The transmission rate to the higher-level system is fixed at 1200 bits/s and cannot be changed.

Jumper		
A-B	Supply voltage 24V to plug X3/8,15	
X-Y	Transmission rate from the alphanumeric keyboard 300 bits/s	
X-Z	Transmission rate from the alphanumeric keyboard 1200 bits/s Standard setting: Jumper inserted	
X5	Only necessary for testing of PCB in the factory (Up to rev. level 9 not inserted)	
X6	From rev. level 10 onwards, 1-14, 3-12, 5-10, 7-8 are inserted	
X7	Only for test purposes (used by manufacturer)	
X80	Only for test purposes	
X81	"	
X100-X101	"	
X102-X103	"	
X104	24 V-supply voltage (test point)	Connection for
X105	0V for X104	
X106	24 V-supply voltage (test point)	suppressor choke
X107	0V for X106	
X15	Standard setting	3-4, 1-5, 2-6 via R95 (270 ohms) inserted
X16	"	1-3, 2-4, 5-6 via R96 (270 ohms) "
X17	"	1-4, 2-5 "
X18	"	1-4, 2-5 "

4.5 Voltage Adjustments

The various voltages can be adjusted by means of potentiometers.

R104	5-V supply voltage
R57	Switching threshold for reset signal. To be set to 4.75 V. To adjust, set the 5-V supply voltage to 4.75 V with R104, then RS pulse must occur. Then turn supply voltage up to 5 V with R104.
R135	50-V anode voltage for display tube
R138	9 V AC for heater
R117	Switching threshold for thyristor V120 (protective circuit is activated, if 5-V voltage rises above 6.5 V).

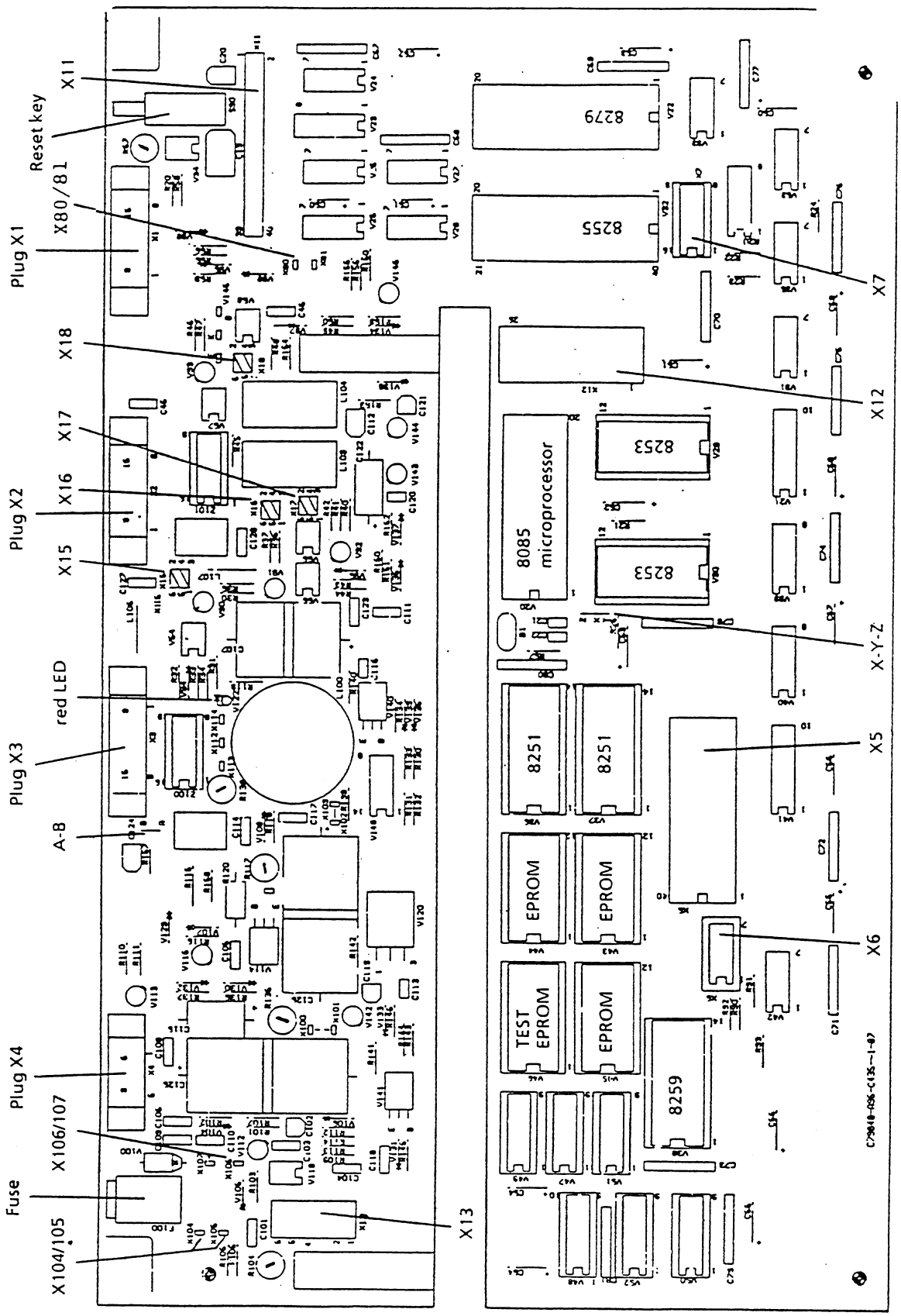


Fig 4 Location of the jumpers, plugs and components

4.6 Keyswitch Positions

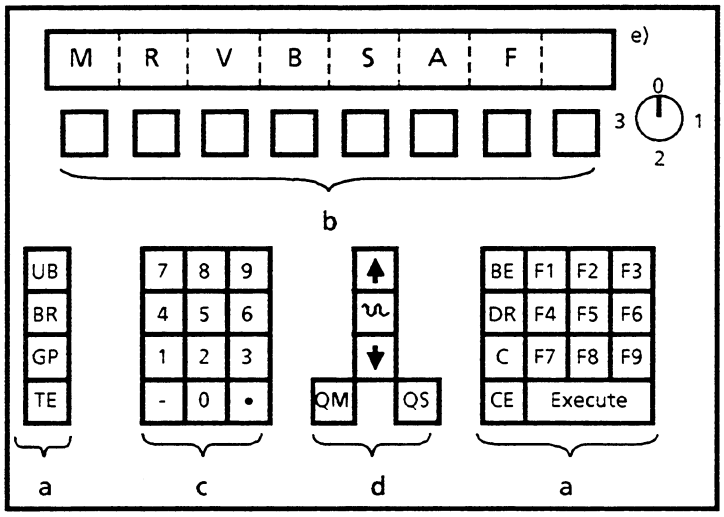
The keyswitch has four positions:

- Position 0: Process communication keyboard is blocked for all operations
- " 1, 3: Process communication keyboard can be operated (in the initial state)
- " 2: Process communication keyboard is blocked alphanumeric keyboard and printer are enabled in the initial states

Irrespective of the switch position, the AS/OS system can output texts on the printer or on the display of the process communication keyboard or can enable the alphanumeric keyboard.

4.7 Key Functions

The process communication keyboard comprises 43 keys, which are divided into four key groups (Fig. 5)
Every input must be concluded with the "EXECUTE" key (;), exept for keys which already include the "Execute" (;) function.



a) Key group 1
b) Key group 2
c) Key group 3
d) Key group 4

e) LED display for the dynamic marking of key group 2

Fig. 5 Process communication keyboard, key groups

- Key group 1

UB Selection of the overview display
(only with OS 250 and OS 251/1 systems)
"Execute" key function (;) is already included.

BR Selection of the area display.

GP Selection of a group display
In addition, the number of the group display must be input through key group 3.

TE Key extension of key group 2
by a further eight markings, "Execute" key function is already included

BE Operation of a loop
The marking of key group 2 is changed according to the loop selected.
"Execute" key function (;) is already included.

DR Print the marking of key group 2
Only operative with AS 230/231/235.

C Clear
Clear the input line appearing on the monitor of the operator control station.

CE Clear Entry
Clear the last character of the input line on the monitor.

EXECUTE Execution of an operator input

Termination of an input with: ";"

F1 to F9 User keys
Keys normally blocked; are enable if required by the AS/OS system. Key code is "FT, 1; ".... "FT, 9;".
The "Execute" key function (;) is already included.

- Key group 2

This group consists of eight keys with variable marking by means of the 40-character display module above key group 2 (Fig. 5, e).

The key marking must be transmitted from the AS/OS system.
When an enable key is operated, it sends the characters with which it is marked, up to the blank, to the interface module. Unmarked keys are blocked.

If all eight keys are enabled they can be bracketed with numeric keys (key group 3) or with the setting keys (↑, ↓, ~), i.e. they can be input before and after a variable key. In the start-up phase and after each change of marking, the keys are blocked and must be enabled by the AS/OS system according to the marking.

- Key group 3

7	8	9
4	5	6
1	2	3
-	0	•

This key group consists of 12 keys. They can be enabled or blocked by the AS/OS system only as a complete block.
They send only the characters shown and are used in conjunction with other keys.
After "BR" or "GP", BR, (character) or GP, (character) is transmitted.

- Key group 4

-	↑ INCREASE	Step-by-step adjustment of values by approx. 1 % of the range per processing cycle.
-	↓ DECREASE	
-	~ High speed	For operation only in conjunction with the **INCREASE** or **DECREASE** keys. Adjustment by approx. 10 % per cycle
-	QM	Acknowledgement of a message
-	QS	Acknowledgement of addresses.

The "Execute" key function (;) is already included in the key code for this key group.

- Combination of key group 1 + key group 3
(New functions applicable for PBTs from revision level 14 onwards)

Key	Function	Operative in system
DR + 2	QF	AS 220, AS 230, AS 235, OS 250
DR + 3	F;	AS 220, AS 230, AS 235, OS 250
DR + 4	Z;	AS 230, AS 235
DR + 5	BI;	AS 220, AS 230, AS 235, OS 250
DR + 6	R;	AS 220, OS 250
DR + 1	—	no function

DR + n means: Press DR and the respective numeric key simultaneously.

4.8 Self-test/Start-up Phase/Error Messages

After switching on or operation of the reset button, the firmware runs through a self-test and parameterization routine. During the self-test routine, the following checks are carried out:

- RAM-Test
  RAM defects are located by writing and check-reading of various character combinations.
- EPROM horizontal check sum test
  The horizontal check sum of each EPROM (exept for the last three bytes) is determined and compared with the value stored in two bytes ('7FD'H; '7FE'H) in the EPROM.
- EPROM position test
  It is ascertained whether the EPROMs 2 and 3 are plugged into the correct locations.

As long as no errors occur, the message "PTB-SELF-TEST" apppears on the display during the test time (approx. 15 s):

The following errors are signalled on the display:

"FEHLER IM RAM V...!"
("ERROR IN RAM V...!")

"FEHLER IM EPROM V...!"
("ERROR IN EPROM V...!")

"EPROM KENNUNG V... FALSCH"
("WRONG EPROM IDENTIFIER V...!")

	Component	Address
RAM	V47/48 V49/50 or. V51/52	'2000'H - '23FF'H '3000'H - '33FF'H '3400'H - '37FF'H
EPROM	V43 V44 V45	'0000'H - '07FF'H '4000'H - '47FF'H '5000'H - '57FF'H

Prerequisite for the complete self-test is that EPROM No. 1 (V43; containing the test and start-up program) is in the correct location, that the test program (firmware) is free of errors and that a display is possible.

After a successful (error-free) run of the self-test routine, the process communication keyboard goes into the parameterization routine. This gives information to the process communication keyboard on the system connected (AS/OS) and information to the system on the status of the process communication keyboard (PTB).

The process communication keyboard sends a message to the system with the "Start-up" identification code. On the display the message

"PBT-ANLAUF" ("PBT START-UP")

appears until the system has acknowledged, but not longer than 3 seconds.

If there is no acknowledgement by the system, the display shows

"AS/OS-SYSTEM UNKLAR" ("AS/OS SYSTEM NOT READY")

The start-up message is repeated every 3 seconds.

If the connection to the system was made correctly and the current loop then fails, the display shows:

"SCHNITTSTELLE 1 UNKLAR" ("INTERFACE 1 NOT READY")

In position 2 of the keyswitch, the current loop is checked by the alphanumeric keyboard (interface must be enabled by the system). If the connection is interrupted, the following message appears:

"ALPHA TASTATUR UNKLAR" ("ALPHANUMERIC KEYBOARD NOT READY")

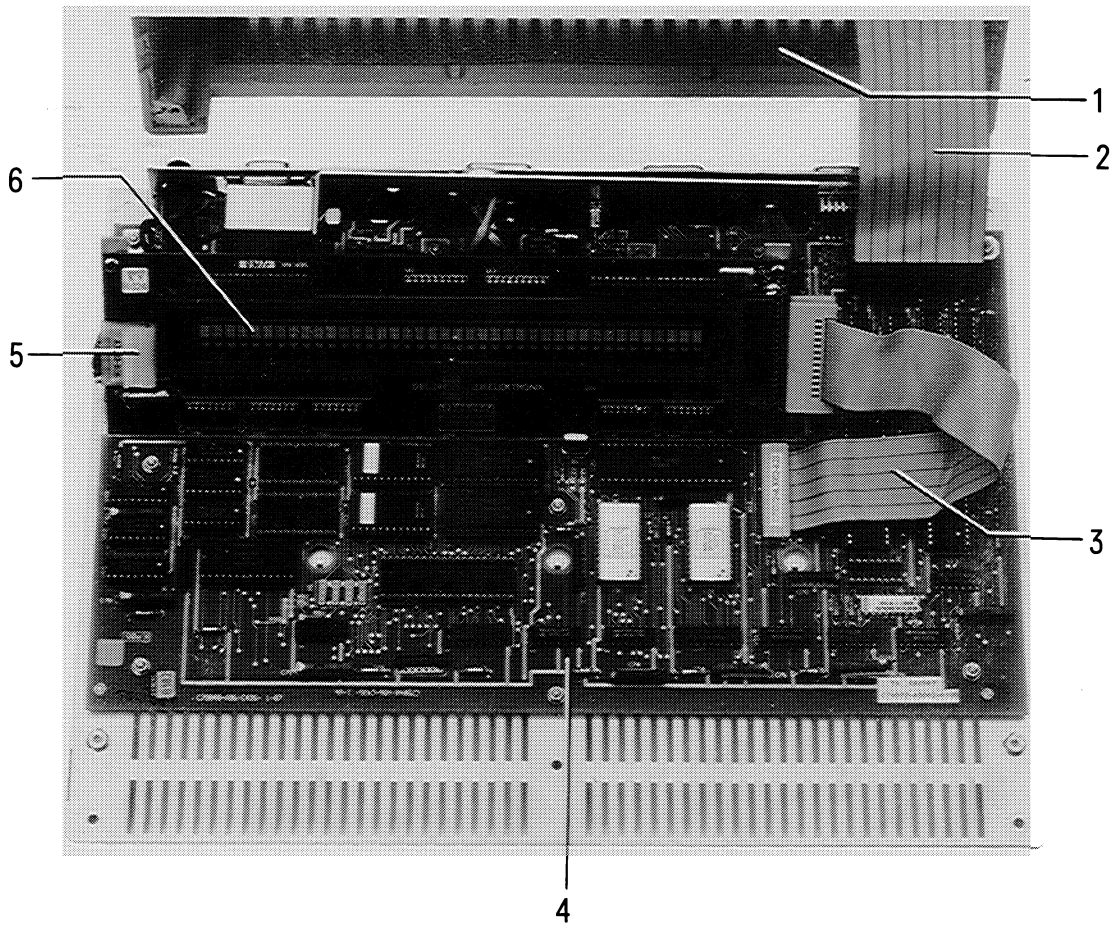
A check is made every three seconds to determine whether a printer is connected (current loop). The current status is stored. If the current status changes from "DRUCKER KLAR" ("Printer ready") to "DRUCKER UNKLAR" ("Printer not ready") (current loop interrupted, plug removed), the following message appears:

"DRUCKER UNKLAR" ("PRINTER NOT READY")

5 Maintenance

5.1 Mechanical Design

After removing 4 screws from the base plate, the process communication keyboard can be opened. The keypad is fixed to the upper part of the case, the basic module to the base plate. The two are connected via a ribbon cable with plugs. For test purposes, the keypad can be placed beside the lower part.
The display module is screwed to the basic module. It receives its supply voltage via one connector cable and is supplied with data via a second.



1 Rear of keypad
2 Ribbon cable between keypad and basic module
3 Data cable for display module
4 Basic module
5 Power cable for display module
6 Display module

Fig. 6 Process communication keyboard opened

5.2 Mode of Operation

- Microprocessor and microprogram memory

The process communication keyboard is a microprogrammed control unit designed with a 8085 microprocessor. The control sequences are stored in a microprogram of approximately 6 Kbytes length (EPROM).
3-Kbyte RAMs are available as working and data memory.

- Keyswitch

The keyswitch has four positions (see Fig. 2.7). The relevant switch position can be interrogated by the microprogram.

- Timers

The timers generate
- the basic clock pulse,
- the transmission clock pulses for the data rates of the serial interfaces,
- the clock pulses for cyclic monitoring of the interfaces (RST5.5),
- the repetition frequency for the INCREASE/DECREASE keys (RST6.5),
- the prompt functions in the program.

- Display module

The display module receives the character information in ASCII code via the data bus. The characters are stored on the display module and are read out cyclically for display. Character repetition is carried out by a separate microprogram on the display module.
A maintenance test program for the display module can be started via the input T0 (see 3.4, Testing and corrective maintenance).

- Keypad

The keypad is connected to the microprocessor via the integrated encoder module 8297. Encoding of the keys is carried out by means of a matrix with column and row lines.
The encoder module selects the row lines cyclically and scans the column lines to determine whether a key has been activated.

- Serial interfaces

The process communication keyboard has two serial interfaces.
In all cases, the current loop of 20 mA is supplied by the lower-level unit, i.e. by the process communication keyboard towards the AS/OS system and by the printer and the alphanumeric keyboard to the process communication keyboard.

- Power supply

The process communication keyboard must be supplied with 24 V DC.
From this voltage, the voltages + 5 V, 9 V, + 15 V and + 50 V are generated via a switched-mode power supply unit. The 24-V supply is protected by an M 1.6 A fuse. In the case of a voltage failure, an errror message is sent to the system

5.3 Plug/Cable Connector Allocations

Plugs X1, X2, X3, X4:

Pin	Plug X1 and X2 to the alphanumeric keyboard and printer	Plug X3 Serial. interface to AS/OS	Plug X4 Supply voltage
1	E21 - } Reception	S11 - } Transmission	0 V
2	E22 + } alphan.keyboard.	S12 + } AS/OS	0 V
3	S21 - } Transmission	E11 - } Reception	-
4	S22 + } printer	E12 + } AS/OS	Signal ground
5	-	-	Signal ground
6	0 V	0 V	-
7	Signal ground	Signal ground	+ 24 V
8	+ 24 V	+ 24 V (via A-B)	+ 24 V
9	DF1 – Printer fault	-	-
10	DF2 + Printer fault	-	Not applicable. 9-way plug
11	-	-	
12	-	-	
13	0 V	0 V	
14	Signal ground	Signal ground	
15	+ 24 V	+ 24 V (via A-B)	

Cable connector allocation

Cable connector 6DS8 100-...

Allocation

Signal	48-way female connector	Core color	15-way socket connector
S11	b8	blue	1
S12	b6	red	2
E11	b12	grey	3
E12	b10	yellow	4
PE	-	-	7
PE	-	-	14
-	b14	-	-
-	b24	-	-

Cable connector 6DS8 102-..

Allocation

Signal name	15-way male connector		Core color		15-way socket connector		Signal name
-E21	Pin-No.	1	blue	1	Pin-No.	1	S1-
+ E22		2	red	1		2	S2 +
-S21		3	grey	1		3	E1-
+ S22		4	yellow	1		4	E2 +
0 V		6	green	1		6	0 V
24 V		8	brown	1		8	24 V
PE		7	white	1		7	PE
PE		14	black	1		14	PE
-DF1		9	blue	2		9	DF1-
+ DF2		10	red	2		10	DF2 +
		11	grey	2		11	
		12	yellow	2		12	
0 V		13	green	2		13	0 V
24 V		15	brown	2		15	24 V

Cable connectors: 6DS8 103-... / 6DS8 104-...

Allocation

Signal name	9-way socket connector		Core color
0 V	Pin-No.	1	blue
0 V		2	blue
Signal ground		4	green/yellow
Signal ground		5	green/yellow
+ 24 V		7	brown
+ 24 V		8	brown

Cable connector: 6XV2154-8A...

Allocation

Control station interface 235			PBT		
Signal name	15-way male connector	Core pair	Core color	15-way	Signal-name
- TXD1	3	1	bl	3	- E11
+ TXD1	4		rt	4	+ E12
- RXD1	1	2	gr	1	- S11
+ RXD1	2		ge	2	+ S12
-	Pin 7,13 at housing	1) Screen		Isolated with sleeve	
OV (ground)	6,13	-	-	-	-
24V (L +)	8,15	-	-	-	-

1) Screen contacted on housing

5.4 Testing and Corrective Maintenance

- Display module test

The display module has an integrated self-test program. To start the program, the pin T0 must be connected to 0 V .
For this purpose, the data line is to be disconnected from the display module. T0 is the bottom pin on the back of the PCB (pin is marked). The self-test program writes the complete character set on the display tube and shifts the characters.
In the case of a defect, the complete display module is to be replaced.

- Keys/voltages

Key replacement
The keys have active Hall generators (SAS 261) as switching elements.
In the case of a fault, a key can be withdrawn and replaced after unsoldering the four connections. In order to provide a firm base for the key (to avoid pressure on conductor paths), it must be firmly placed on the board during soldering in.

Voltages
When the 5-V voltage is present, a red LED (V122) lights up on the process communication keyboard control unit.
If one of the other voltages is absent, the indication :

"PBT SPANNUNG UNKLAR" ("VOLTAGE NOT READY")

appears on the display module (if still possible)

Printer/keyboard not ready
In the case of error messages from the alphanumeric keyboard or from the printer, check the serial interface from the devices (20 mA current loop)

5.5 Spare Parts/Repairs

The parts list is enclosed in the appendix.
Order spare parts from:

ANL 434 - ED (Siemens Erlangen)

Defective parts are to be sent for repair to:

GWK QVR (Siemens Karlsruhe)

Pos.	Designation	Order No.	Marker's designation	Spare group *)	Number per product	Contained in or applicable from Rev. level	
1	Process communication keyboard control unit (basic module)	C79372-A3002-B100		R1	1		
2	Display module	W79025-B0240-N040		N	1		
3	Keypad of process communication keyboard	C74451-Z69-U246		R0	1	Replaces C79372-A3002-B103	
4	Keyswitch	C79050-X3202		N	1		
5	Key	C74451-Z69-U213	Rafi no. 3.13001.012	N	43		
6	Green LED	W79025-L2513-H120		N	1		
7	Red LED	W79025-L1323-H120		N	1		
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							
24							

*) R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

Place of delivery: ANL 434 - ED Erlangen

TELEPERM M Parts List

Process Communication Keyboard
6DS3 305-8AA

C79000-E8076-C038-05
11.89

Sheet: 1 Sh

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TELEPERM M

AS 235 H Automation System

6DS2 131, 6DS2 132

Spare Parts List C79000-E8076-C293-05

	1	2	3			4
Item	Designation	Order no.	Maker's Designation	Rep. Ident.	Number	Notes
	Power supply and Central modules					
1	Buffered module DC 24 V	C79451-A3125-B227		R1	1	
2	Power regulation module DC 24 V / DC 5 V	C79451-Z1359-U9	Fa. Wiener Typ SW01	R1	2	
3	Alarm logic module	6DS1 901-8AA		R1	1)	
4	Flashing pulse generator	6DS1 922-8AA		R1	1	
5	Interface module for I/O bus	6DS1 312-8BB		R1	1)	
6	Operation channel interface module	6DS1 330-8CA		R1	1)	
7	Interface module for mini floppy disk unit	6DS1 326-8BB		R1	2	
8	N8-H interface module	6DS1 220-8AA		R0	2	7) replaced by item 9 N-AS (H)
9	N-AS interface module	6DS1 223-8AA		R1	2	Replaces item 8 6DS1200-8AC
10	Central processor module	6DS1 141-8AA		R1	2	
11	Comparator and coupler module	6DS1 142-8AA		R1	1	
12	Synchronization module	6DS1 143-8AA		R1	2	
13	I/O comparator and switchover module	6DS1 144-8AA		R1	1)	
14	Memory module with back-up battery, 1 Mbyte user RAM	6DS1 837-8AA		R0 3)	2	7) **no spare part;** replaced by item 22
15	Memory module with back-up battery, 2 Mbyte user RAM	6DS1 837-8BA		R0 3)	2	7)) **no spare part;** replaced by item 22
16	Memory module with back-up battery, 3 Mbyte user RAM	6DS1 837-8CA		R0 3)	2	7) **no spare part;** replaced by item 22
17	Memory module with back-up battery, 1 Mbyte user RAM	6DS1 837-8DA		R0 3)	2	7)) **no spare part;** replaced by item 22
18	Memory module with back-up battery, 2 Mbyte user RAM	6DS1 837-8EA		R0 3)	2	7)) **no spare part;** replaced by item 22
19	Memory module with back-up battery, 3 Mbyte user RAM	6DS1 837-8FA		R0 3)	2	7)) **no spare part;** replaced by item 22

Place of delivery:
ATD TD3 LSE LC Erlangen

1) Depending on system design
2) Parts list of devices in instruction of devices
3) Prefer item 18
4) Interface for PT90
5) Place of delivery A&D SE PL P
6) According to IATA no source of danger
7) Type canceled

*) R1/7: Repairable, exchange part
R0: Repairable, no exchange part
N : Not repairable

Date	15.08.97
Editor	Kelber
Group	515
Dep.:	A&D SE PL BG

TELEPERM M Spare parts list

AS 235 H Automation System

State	Notification	Date	Name
05	Mon./DR neu	23.02.99	Ke.
04	neu angelegt	18.08.97	Ke.

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C79000 - E8076 - C293 - 05

FILE: ERS-235H.DOC

	1	2	3	4		
Item	Designation	Order no.	Maker's Designation	Rep. Ident.	Number	Notes
20	Memory module with back-up battery, 4 Mbyte user RAM	6DS1 844-8CA		R0 [3]	2	[7] **no spare part;** replaced by item 22
21	Memory module with back-up battery, 4 Mbyte user RAM	6DS1 844-8DA		R0 [3]	2	[7] **no spare part;** replaced by item 22
22	Memory module with back-up battery, error correction, 4 Mbyte user RAM	6DS1 844-8FA		R1	2	replaces item 14 - 21
23	Back-up battery 3,4 V / 3,6 V	W79084-U1001-B2	Typ AA/S [6] $Li\text{-}SOCl_2$	N	2	for item 14 - 22
24	Battery compartment for 6DS1844-8xx	C79458-L443-B6		N	2	for item 20 - 22
25	Video relay complete	C79165-A3012-B434		N	[1]	
	Input and output devices					
27	Process operation keyboard	6DS3 305-8AA		R0	[1]	[2] [7] **no spare part;** replaced by item 28
28	Process operation keyboard PBT 65	6DS3 305-8BA		R0	[1]	[2] replaces item 27 Var. 6DS3305-8AA
29	Configuring keyboard	6DS3 303-8AA		R0	[1]	[2]
30	Mini floppy disk unit (80 tracks)	6DS3 900-8AE		R0	[1]	[2] replaces item 31
31	Mini floppy disk unit (80 tracks)	6DS3 900-8AD		R0	[1]	[2] [7] **no spare part;** replaced by item 30
32	51 cm process monitor, AC 230 V	6DS3 401-8BK		R0	[1]	[2] [7] **no spare part;** replaced by item 35
33	51 cm process monitor, AC 230 V D serie, with automatic contrast function	6AV8 011-1JE22-0DA0		R0	[1]	[2] [7] **no spare part;** replaced by item 35
34	51 cm process monitor, AC 230 V D serie, without automatic contrast function	6AV8 021-1JE22-0CA0		R0	[1]	[2] [7] **no spare part;** replaced by item 35
35	36 cm process monitor, AC 230 V	C79145-A3032-A22		R0	[1]	[2] [7] **no spare part;** replaced by item 35
36	Monitor SCM 2140-I 51 cm, AC 230 V	6GF6 100-1BV		R0	[1]	[2] in exchange for item 31 - 34
37	Wire printer PT 88	6DS4 202-8AA		R0	[1]	[7] **no spare part;** replaced by item 46 or 48
38	Ink jet printer PT 88	6AC7 201-4DE		R0	[1]	[7] **no spare part;** replaced by item 46 or 48

Place of delivery:
ATD TD3 LSE LC Erlangen

[1] Depending on system design
[2] Parts list of devices in instruction of devices
[3] Prefer item 18
[4] Interface for PT90
[5] Place of delivery A&D SE PL P
[6] According to IATA no source of danger
[7] Type canceled

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R0: Repairable, no exchange part
N : Not repairable

Date	15.08.97
Editor	Kelber
Group	515
Dep.:	A&D SE PL BG

TELEPERM M Spare parts list

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State	Notification	Date	Name
05	Mon./DR neu	23.02.99	Ke.
04	neu angelegt	18.08.97	Ke.

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C79000 - E8076 - C293 - 05

FILE: ERS-235H.DOC

	1	2	3	4		
Item	Designation	Order no.	Maker's Designation	Rep. Ident.	Number	Notes
39	Wire printer PT 89	6DS4 203-8AA		R0	1)	7) **no spare part;** replaced by item 46 or 48
40	Ink jet printer PT 89 S	6AC7 201-4DF		R0	1)	7) **no spare part;** replaced by item 47 or 49
41	Report printer PT90 - 11	S22287-A90-T1		R0	1)	7) **no spare part;** replaced by item 47 or 49
42	Interface adapter V.24 / TTY	S22287-B101-A1		R0	1)	4) part of item 41
43	Wire printer SICOMP DR210-N, paper width 254mm	6AP1 800-0AA00		R0	1)	7) **no spare part;** replaced by item 46 or 48
44	Wire printer SICOMP DR211-N, paper width 406mm	6AP1 800-0BA00		R0	1)	7) **no spare part;** replaced by item 46 or 48
45	TTY-SS with emulation ECMA (part of DR210 / 211)	6AP1 800-0AC80		N	1)	7) part of item 43 a. 44
46	Printer DR215-N, 9 needles, paper width 254mm	6AP1 800-0BB00		R7	1)	In exchange for item 37, 38, 43
47	Printer DR216-N, 9 needles, paper width 420mm	6AP1 800-0BD00		R7	1)	In exchange for item 39, 40, 41, 44
48	Printer DR235-N, 24 needles, paper width 254mm	6AP1 800-0BF00		R7	1)	In exchange for item 37, 38, 43
49	Printer DR236-N, 24 needles, paper width 420mm	6AP1 800-0BH00		R7	1)	In exchange for item 39, 40, 41, 44
50	TTY-SS with emulation ECMA (part of DR215 / 216)	6AP1 800-0AG10		N	1)	For item 46, 47,
51	TTY-SS with emulation ECMA (part of DR235 / 236)	6AP1 800-0AG30		N	1)	For item 48, 49,
52	AS / OS printer converter	6DS3 932-8AA		N	1)	7)
53	I/O remote bus coupling module	6DS1 322-8AA		R1	1)	State ≥ 6
54	Terminator for I/O remote bus coupling module	6ES5 760-1AA11		N	1)	5)
	Subrack					
56	Subrack Basic unit	6DS9 027-8AB		R0	1)	5)
57	Subrack extension unit WW	6DS9 002-8BB		R0	1)	5)
58	Subrack extension unit MTP	6DS9 002-8BA		R0	1)	5)

Place of delivery:
ATD TD3 LSE LC Erlangen

1) Depending on system design
2) Parts list of devices in instruction of devices
3) Prefer item 18
4) Interface for PT90
5) Place of delivery A&D SE PL P
6) According to IATA no source of danger
7) Type canceled

*) R1/7: Repairable, exchange part
R0: Repairable, no exchange part
N : Not repairable

Date	15.08.97
Editor	Kelber
Group	515
Dep.:	A&D SE PL BG

TELEPERM M Spare parts list

AS 235 H Automation System

State	Notification	Date	Name
05	Mon./DR neu	23.02.99	Ke.
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	1	2	3	4			
	Item	Designation	Order no.	Maker's Designation	Rep. Ident.	Number	Notes
	59	Power supply DC 24/5 V for extension unit (EU)	6DS1 006-8AA		R0	1per EU	
A	60	Overvoltage protection 5 V	C79451-A3117-B88		N	1	For item 59
	61	Power supply subrack	6DS4 432-8AA		R0	1)	5)
	62	Feeder unit DC 24 V (SES)	6DS4 428-8AA		R0	1)	5)
—	63	Fan module	6DS9 943-8AA		R0	1)	5)
	64	Connector block for 20m local bus	6DS9 207-8AA		N	1	
	65	Interference filter	C79458-L445-B3		N	1)	
B	66	Diode module	C74103-A1900-A351		N	1)	5)
	67	Coupling diode model for SRL	C79451-A3125-B187		N	1	
	68	Diode for overvoltage protection	W79020-W311-R23		N	24	
	69	Fuse switch 16 A	W79051-B3012-A160	ETA	N	15	
	70	Fuse switch 4 A	W79051-B3031-A400	ETA	N	9	5)
C	71	Monitor cable-clamping rail	C79363-A3006-B10		N	1)	5)
		Systemsoftware					
	73	AS 235 H System software, version F	6DS5 323-8AF00-3XX3		N	1)	5) 7)
—	74	AS 235 H System software, version G	6DS5 323-8AG00-1XX3		N	1)	5) for 6DS1844-8xx only
	75	Floppy disks (pack of ten) 5 ¼" double sided	6AY2 904-0AC00		N	1)	
D							

Place of delivery:
ATD TD3 LSE LC Erlangen

1) Depending on system design
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TELEPERM M Spare parts list

AS 235 H Automation System

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

Siemens Aktiengesellschaft

Order No. C79000–E8076–C293
Printed in the Federal Republic of Germany

SIEMENS

TELEPERM M
System Cabinets

Parts List Order No. C79000-E8076-C006-10

Item	Designation	Order no.	Maker's designation	Spares group *)	Number per product	Contained in or applicable from revision level	
	Standard cabinet						
1	Small limit pushbutton	W79050-M9501-U101		N	1)		
2	Signal lamp, red	C74230-Z1041-G1	2)	N	1		
3	Pushbutton	W79050-E1501-A911	2)	N	1		
4	Door contact with mounting parts	6DS9 905-8CA		N	1)		
5	Indicator lamp	3SB1001-0QC20	2)	N	1)		
6	Switching element (test pushbutton)	3SB1300-1B	2)	N	1		
7	Lamp 30 V/2 W (cabinet or cabinet row lamp)	C1230-Z73-A9		N	1)		
8	Lamp 30 V / 2 W	W79064-A8001-C24		N	1)		
9	Lamp 24 V / 2 W	3SB1 902-8AF		N	1)	Alternative to item 8	
10	Thermostat	W79086-D1-A65		N	1)		
11	Interference suppression unit (screen bar / cabinet frame)	C79165-A3012-B19		N	1)		
12	Mains filter 2 x 10 A	W79041-E4103-K1		N	1)		
13	Overvoltage arrester	C79451-A3125-B4		N	1)		
14	Ground bar	6DS9 906-8QA		N	1		
15	Cable clamps	C79363-A3006-B10		N	1)		
16	Cabinet connection element (Maxi-Termi-Point system)	6DS9 907-8AA		N	1)		
17	Cabinet connection element (wire-wrap system)	6DS9 907-8BA		N	1)		
18	Screw attachment SAE 32S	6XP1 828		N			
19	Cabinet connection element 32/3 with jumpers SL, 1-16 and 17-32 jumpered separately	6XP1 821		N			
20	Cabinet connection element 32/3 with jumpers SL, 1-16 jumpered	6XP1 819		N			
21	Cabinet connection element 32/3 with jumpers SL, 17-32 jumpered	6XP1 820		N			
22	Cabinet connection element 32/1 with jumpers SL, 1-16 and 17-32 jumpered separately	6XP1 815		N			
23	Cabinet connection element 32/1 with jumpers SL, 1-16 jumpered	6XP1 813		N			
24	Cabinet connection element 32/1 with jumpers SL, 17-32 jumpered	6XP1 814		N			

*) R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

1) Depending on system design
2) When using only 1 combined pushbutton in the cover panel

Place of delivery: ANL - A434 ED Erlangen

TELEPERM M Parts List

System cabinets

C79000-E8076-C006-10
08.90

Sheet: 1 +
3 Sh.

Item	Designation	Order no.	Maker's designation	Spares group *)	Number per product	Contained in or applicable from revision level	
25	Interference suppression filter	C79451-A3125-B121		N	1)		
26	Capacitor, complete	C79195-A3205-B72		N	1		
27	Capacitor MP 0,6 µF / 440 V	W79016-N6604-M440		N	1		
	Heat exchanger cabinet (up to release 3/up to 1.87)						
30	Heat exchanger, complete	(8ME7222-8NX04)				Not available, replace by item 31	
31	Conversion set with door, heat exchanger and monitor	C79165-A3012-D32		N			
32	Fan monitor R2E 175	GWE: 197 970		N	1		
33	Capacitor 2 µF / 400 V	GWE: 197 996		N	1		
34	PTC resistor P430-E11	Q63100-P430-E11		N	1		
35	Monitoring circuit	6FW1006-1		N	1		
	Heat exchanger cabinet (from release 4 onwards / from 1.87 onwards)						
40	Heat exchanger, complete	8ME7864-0		N			
41	Isolating element	8ME7885-6A		N	1		
42	Ventilator	8ME7888-4A		N	2		
43	Fan monitor	6FW1007-0		R1	1		
44	PTC resistor	W79028-K7000-V14		N	2		
45	Mains filter	6DS4408-8AA		N	1		

*) R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

1) Depending on system design

Place of delivery ANL - A434 ED Erlangen

TELEPERM M Parts List

System cabinets

C79000-E8076-C006-010
08.90

Item	Designation	Order no.	Maker's designation	Spares group *)	Number per product	Contained in or applicable from revision level	
	Power distribution subracks Parts for 6DS4 407 and 6DS4 417						
96	Interference suppression filter	C79458-L445-B3		N	1)		
97	Z-Diode	C79451-A3125-B3		N	1)		
98	Diode module	C74103-A1900-A351		N	1)		
99	Fuse module	C79451-A3125-B120		N	1	6DS4417-8AA	
100	Basic device	C79451-A1614-B2		R1	1	6DS4417-8AA	
101	Connection distributor	6DS9 207-8AA		N	1		
102	Automatic circuit breaker 16 A	W79051-B3012-A160		N	8	6DS4407-8CA	
103	Fuse T 4 A / 260 V	W79054-L1011-T400		N	2		
104	Fuse T 6,3 A / 260 V	W79054-L1011-T630		N	1		
105	Fuse M 1 A / 260 V	W79054-L1011-M100		N	4		
106	Fuse M 6.3 A / 250 V	W79054-N1011-M630		N	1		
107	Fuse M 1.6 A / 250 V	W79054-N1011-M160		N	6		
108	Fuse M 4 A / 250 V	W79054-N1011-M400		N	3		
109	Connection socket for keyboard	W79071-U2603-L3		N	3		
110	Diode housing	W79451-A3125-B187		N	1		

*) R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

1) Depending on system design

Place of delivery: ANL - A434 ED
Erlangen

TELEPERM M Parts List

System Cabinets

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

Siemens Aktiengesellschaft

Order No. C79000–E8076–C006
Printed in the Federal Republic of Germany

SIEMENS

TELEPERM M
ES 100 K Extension System

Parts List C79000-E8076-C124-02

Notes

Item	Designation	Order No.	Maker's designation	Spares group *)	Number per product	Contained in or appli-cable from Rev. level	
1	Power supply module 220 V AC/24 V DC	C79451-A3260-A20		R1	1	in ES 100 K/ 220 V AC	
2	Power supply module 24 V DC/24 V DC	C79451-A3260-A25		R1	1	in ES 100 K/ 24 V AC	
3	Fuse T4 (slow)	W79054-L1011-T400		N	2	in items 1 and 2	
4	Fuse T6.3 (slow)	W79054-L1011-T630		N	1	in items 1 and 2	
5	Fuse M4 (5 * 20)	W79054-N1011-M400		N	1	in items 1 and 2	
6	Voltage regulator 24 V DC/5 V DC/5 A	C79451-A3260-A15		R1	1	only required if an N-V24 interface is used	
7	Signalling logic module	6DS1901-8AA		R1	1	optional	
8	I/O remote bus coupling module	6DS1322-8AA		R1	1		
9	Terminator for I/O remote bus coupling module	6ES5760-1AA11		R1	1	in the last device of an ES 100 K/ 220 V AC caskade	
10	Mains filter 220 V AC	C79451-A3260-B112		N	1	in ES 100 K/ 220 V AC	
11	Mains filter 24 V DC	C79451-A3260-B117		N	1	in ES 100 K/ 24 V DC	
12	N-V24 interface	6DS1202-8AB		R1	1,2		
13	Power supply for inductive converter	6DS1211-8AA		R1	1		
14	Inductive coupler for inductive converter	6DS1213-8AA		R1	1		
15	Bus interface for inductive converter	6DS1212-8AB		R1	1		
16	Remote bus connector board	6DS9203-8DA		N	1		
	For spare parts for I/O modules see parts list C79000-E8076-C007.						

*) R0 = Repairable, no exchange part
R1 = Repairable
N = Not repairable

Place of delivery: E MA-ED Erlangen

TELEPERM M

ES 100 K

C79000-E8076-C124-02

Sheet 1

1 sh.

SIEMENS

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Order No.: C79000-E8076-C124
Order from: Gerätewerk Karlsruhe

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