

SIEMENS

Technical Description

Order Number: 6AR1930-4AA04-3AA0

February 2001

PMC-CTR357

Order Number: 6AR1324-0BA00-0AA0

PMC VGA Module

SICOMP Industrial Microcomputer

(4)J31069-D2047-U001-A1-7618

Product History of the Technical Description

Revision ¹⁾	Record of changes	Date
A0	First edition	10/97
A1	Supplement of address area of graphics controller, update	02/01

1) Corresponds to the 4th block of digits of the drawing number in the footer

Explanation of Notation

- * An asterisk behind the signal name indicates a low-active signal (e.g., IOR*).
 - / A slash between two signal names separates two level-dependent functions of one signal.
Example: C/D* means Command for high level and Data for low level.
 - Connections indicated with a dash in a connector assignment table are reserved (i.e., bus or I/O interface).
- Signal** Special signals not included in these specifications are indicated in bold print in the signal assignment tables and then explained (e.g., **NMI**).

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ES4/Kt/WW8.0/VS5.0/A4

Safety Notes for SICOMP Boards

ESD protection measures



Caution

When handling boards and other components carrying this symbol, always adhere to ESD protection guidelines (**E**lectrostatic **S**ensitive **D**evelopments).

- Never touch the boards unless required work makes this absolutely necessary.
- When working with the boards, use a conductive and grounded work surface.
- Wear a grounding bracelet.
- Never touch the pins, connections or printed circuits of the boards.
- Never permit the boards or components to be touched by chargeable objects (e.g., synthetic materials).
- Keep the boards or components at least 10 cm away from CRT units and television sets.
- Leave the boards in their special packaging until they are needed. When registering boards, etc. do not remove the boards from their packaging or touch them.
- Boards may only be installed or removed when the voltage is off.

Related SICOMP SMP16 Literature

For more information on installing and handling SICOMP boards, see "SICOMP IMC system manual".

Table of Contents

1	Initial Startup	7
2	Features	8
2.1	Graphics Controller	8
2.2	Technical Data	9
2.3	Mechanical Layout	9
2.4	Environmental Requirements	9
2.5	Scope of Delivery	10
2.6	Recommended Accessories	10
2.7	Recommended Reading	10
3	Interfaces	11
3.1	Signal Assignment of the PMC Plug Connector	11
3.2	Signals of the PS/2 VGA Interface	13
4	Configuration of the Board	14
4.1	Video BIOS	14
4.2	Drivers	15
4.3	Address Area of the Graphics Controller	15
5	Appendix	17
5.1	Abbreviations	17

1 Initial Startup

Only one step is required for the initial startup of the board.

1. Install the PMC module on the SMP16-CPU050/CPU055 CPU board, and screw it to the board.
The notes in the product release letter of the CPU must be adhered to.

2 Features

VGA PMC module for the SMP16-CPU050/CPU055 board

- High-performance 65548 controller from Chips & Technologies
- Compatible with IBM VGA
- 32-kbyte VGA BIOS from Chips & Technologies
- 1-Mbyte monitor screen memory
- Maximum resolution of 1024 x 768
- 15-pin, high-density, sub D plug connector on the front
- 32-bit PCI bus
- Module supply voltage of 5 V
- 5 V/3.3 V PCI level supported
- Single-size PMC module: 149 mm x 74 mm
- 10 mm space between motherboard and PMC module PCB

Note:

The board has no hardware support for distinguishing between black-and-white and color VGA monitors.

2.1 Graphics Controller

The features of the 65548 graphics controller from Chips & Technologies are listed below.

- 32-bit PCI bus with burst mode support
- 32-bit screen memory interface
- Hardware Windows Accelerator features
- 5 V/ 3.3 V PCI interface
- Maximum resolution of 1024 x 768
- True Color representation with up to 640 x 480 pixels
- 256 colors (up to 1024 x 768 in non-interlaced mode)
- Power Management support
- DPMS for CRT power-down (VESA interface standard support)
- DDC for CRT Plug-and-Play (VESA interface standard support)

The maximum possible vertical frequency and the number of colors for various resolutions are summarized in the following table.

Resolution	Colors	Vertical Frequency (Hz)
640 x 480	16 M	60
640 x 480	64 k	75
800 x 600	64 k	60
800 x 600	256	75
1024 x 768	256	75

The vertical frequency is achieved in non-interlaced mode.

2.2 Technical Data

Power Supply	Typical	Maximum
Voltage supply (via PMC plug connector)	+5 V	±5%
Voltage V (I/O) on the PCI bus ¹⁾	+5 V or +3.3	
Current consumption	0.6 A	
Interfaces		
PMC interface (X8 and X9)	64-pin CMC plug connector in acc. w. IEEE P1386	
VGA interface (X7)	15-pin, high-density, subminiature, 3-row female connector in acc. w. DIN 41652 (up to 3-m connection cable permitted)	

1) Set to 5 V for SMP16-CPU050/CPU055

2.3 Mechanical Layout

Dimensions and Weight	Typical
Dimensions	149 mm x 74 mm
Distance to the motherboard	10 mm
Weight	100 g

See the IEEE P1386 standard (Physical and Environmental Layers for S Bus Mezzanine Cards: CMC) for additional information (e.g., layout, size of the front plate, and location of the plug connectors).

2.4 Environmental Requirements

Factor	Operation	Transportation and Storage
Temperature	0° C to 55° C	-40° C to 70° C
Relative humidity	10% to 90%	10% to 90%
Permissible air pressure	450 hPa to 1100 hPa	
Permissible temperature fluctuation	10° C / 30 min. (no condensation) or 0.5° C / min.	
Oscillations in acc. w. IEC 68-2-6, test FC, 20 cycles on 3 axes, approx. 11 min. per cycle	10 Hz to 61 Hz: 0.2 mm amplitude 61 Hz to 500 Hz: 2 g	5 Hz to 8 Hz: 7.5 mm amplitude 8 Hz to 500 Hz: 1 g
Shock	IEC 68-2-27, test E/A 3 times per axis 2 directions per axis Total of 18 impacts 30 g/11 msec	IEC 68-2-29 1000 impacts each at 6 levels 25 g / 6 msec

2.5 Scope of Delivery

Board (order no: 6AR1324-0BA00-0AA0)

- PMC VGA module PMC-CTR357

Documentation (order no: 6AR1930-4AA04-1AA0)

- Technical description PMC-CTR357, in two languages
- Floppy disk with drivers

2.6 Recommended Accessories

To obtain optimal picture quality, the monitor cable should include the following features.

- Single shielding of the analog signals (RED, GREEN, and BLUE)
- Ferrite ring as interference suppression filter over the cable

2.7 Recommended Reading

- Data Sheet F65548 High Performance Flat Panel/ CRT GUI Accelerator, from Chips & Technologies
- PC-Intern, by M. Tischer, publisher: Data Becker, 1992
- PC-Hardwarebuch, by H-P. Messmer, publisher: Addison-Wesley, 1992
- VGA-Kompendium, by M. Michael, publisher: Markt & Technik, 1988
- Physical and Environmental Layers for S Bus Mezzanine Cards: CMC, IEEE P1386
- Physical and Environmental Layers for S Bus Mezzanine Cards: PMC, IEEE P1386.1

3 Interfaces

3.1 Signal Assignment of the PMC Plug Connector

The tables below show the bus signals used by the board. The signal names are based on IEEE P1386.1 (NC = Not Connected).

Table 3.1 Bus signals on plug connector Pn1

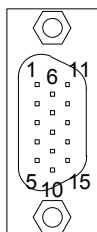
Connection	Signal		Connection
1	NC	NC	2
3	Ground	NC	4
5	NC	NC	6
7	BUSMODE1*	+5V	8
9	NC	NC	10
11	Ground	NC	12
13	CLK	Ground	14
15	Ground	NC	16
17	NC	+5V	18
19	V (I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]*	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V (I/O)	AD[17]	32
33	FRAME*	Ground	34
35	Ground	IRDY*	36
37	DEVSEL*	+5V	38
39	Ground	NC	40
41	NC	NC	42
43	PAR	Ground	44
45	V (I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]*	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	NC	64

Table 3.2 Bus signals on plug connector Pn2

Connection	Signal		Connection
1	NC	NC	2
3	NC	NC	4
5	NC	Ground	6
7	Ground	NC	8
9	NC	NC	10
11	NC	NC	12
13	RST*	NC	14
15	NC	NC	16
17	NC	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	NC	24
25	IDSEL	AD[23]	26
27	NC	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]*	32
33	Ground	NC	34
35	TRDY*	NC	36
37	Ground	STOP*	38
39	PERR*	Ground	40
41	NC	SERR*	42
43	C/BE[1]*	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	NC	50
51	AD[07]	NC	52
53	NC	NC	54
55	NC	Ground	56
57	NC	NC	58
59	Ground	NC	60
61	NC	NC	62
63	Ground	NC	64

3.2 Signals of the PS/2 VGA Interface

Sub D socket
(high-density)



Connection	Signal	Connection	Signal	Connection	Signal
1	RED	6	GND	11	NC
2	GREEN	7	GND	12	DDCDAT
3	BLUE	8	GND	13	HSYNC
4	NC	9	VCC ¹⁾	14	VSYNC
5	GND	10	NC	15	DDCCLK

1) VCC = 5 V $\pm 10\%$; max. current consumption of 100 mA, must be ensured externally

The shield connection of the plug connector is conductively connected with the front plate. NC = Not Connected.

DDCDAT, DDCCLK Data and clock line for DDC in acc. w. VESA Interface Standards Support



Caution

- The feeder line for the VCC voltage (connection 9) must be protected externally! The maximum current consumption is 100 mA.
- When 15-pin, 1:1, VGA connection cables are used, there is a danger of the hardware short circuiting connection 9. This would destroy the PMC-CTR357 module!

4 Configuration of the Board

4.1 Video BIOS

The PMC module has a VGA BIOS which only supports displays on the monitor. During startup, the graphics controller is set to the following standard settings.

- Resolution of 640 x 480
- 16 colors
- Vertical frequency of 60 Hz

The VGA BIOS supports all standard video modes and the extended video modes listed below.

Mode	VESA Mode	Resolution	Type	Colors	Vertical Frequency CRT
20h		640 x 480	Lin. PackPixel	16	60, 72, 75 Hz
22h		800 x 600	Lin. PackPixel	16	56, 60, 72, 75 Hz
24h		1024 x 768	Lin. PackPixel	16	43 ¹⁾ , 60, 70, 75 Hz
30h	101h	640 x 480	Lin. PackPixel	256	60, 72, 75 Hz
32h	103h	800 x 600	Lin. PackPixel	256	56, 60, 72, 75 Hz
34h	105h	1024 x 768	Lin. PackPixel	256	43 ¹⁾ , 60, 70, 75 Hz
40h	110h	640 x 480	Lin. PackPixel	32 k	60, 72, 75 Hz
41h	111h	640 x 480	Lin. PackPixel	64 k	60, 72, 75 Hz
42h	113h	800 x 600	Lin. PackPixel	32 k	56, 60 Hz
50h	112h	640 x 480	Lin. PackPixel	16 M	60 Hz
60h		132 x 25	Text (8 x 16)	16	70 Hz
61h		132 x 50	Text (8 x 8)	16	70 Hz
72h / 75h	104h	1024 x 768	Planar	16	43 ¹⁾ , 60, 70, 75 Hz
79h	101h	640 x 480	PackPixel	256	60, 72, 75 Hz
7Ch	103h	800 x 600	PackPixel	256	56, 60, 72, 75 Hz
7Eh	105h	1024 x 768	PackPixel	256	43 ¹⁾ , 60, 70, 75 Hz

¹⁾ Interlaced

Available settings are restricted by the technical specifications of the monitor or display being used. The PanelCLK for displays depends on the display being used.

4.2 Drivers

A driver floppy disk containing drivers for the following operating systems is included with this documentation.

- Windows 3.11
- Windows 95
- Windows NT 4.0

The driver floppy disk contains a separate subdirectory for each operating system. For Windows 3.11, the WINSETUP.EXE installation program on the floppy disk must be called. For Windows 95 and Windows NT, installation is performed with operating system support. For details, see the applicable description. The driver for Windows NT is available as a self-unpacking file.

The settings for resolution and vertical frequency are performed by the system controller of the operating system. For this purpose, Windows 3.11 offers the ChipsCPL utility program in the system control window.

For programming at the DOS level, subdirectory VESA contains a driver for VESA 1.0.

Note:

The latest drivers for the Windows 3.11, Windows 95, Windows NT and OS/2 operating systems are available on the Internet from Chips & Technologies for the F65548 graphics controller. Internet address:

http://support.intel.com/support/graphics/mobile/lst_548.htm (state November 2000).

If the above address is no longer valid, start at the homepage and use search word "65548".

4.3 Address Area of the Graphics Controller

The hardware and software of the graphics hardware is fully compatible with the VGA standard (video graphics array). VGA analog monitors (PS/2 standard-compatible) or multisync monitors can be connected.

The monitor screen memory of the graphics adapter is 1 Mbyte in size and is located in the address area from A0000h to BFFFFh. The monitor screen memory is addressed via the PCI bus.

Addressing in a 64-kbyte window and mapping are handled by the graphics controller. The included drivers address the 1-Mbyte monitor screen memory linearly in the PCI memory area.

The VGA BIOS is located on a 512k x 8 flash EPROM. If supported by your CPU, Shadow mode should be selected in the CPU BIOS to increase performance. BIOS is located in the address area from C0000h to C7FFFh.

The graphics controller uses the I/O address areas listed below.

Table 4.1 I/O address areas for the graphics controller

Port Address	Read Register	Write Register
3B4h	CRTC index	CRTC index
3B5h	CRTC data	CRTC data
3B8h	Monochrome mode register (MODE)	Monochrome mode register (MODE)
3BAh	Status register (STAT)	Feature control register (FCR)
3C0h	Attribute controller index / data	Attribute controller index / data
3C1h	Attribute controller index / data	Attribute controller index / data
3C2h	Feature read register (FCR)	Miscellaneous output register (MSR)
3C3h	-	Video subsystem enable (VSE)
3C4h	Sequencer index	Sequencer index
3C5h	Sequencer data	Sequencer data
3C6h	Color palette mask	Color palette mask
3C7h	Color palette state	Color palette read mode index
3C8h	Color palette write mode index	Color palette write mode index
3C9h	Color palette data	Color palette data
3CAh	Feature read register (FEAT)	-
3CCh	Miscellaneous output register (MSR)	-
3CEh	Graphics controller index	Graphics controller index
3CFh	Graphics controller data	Graphics controller data
83D0h - 83D3h	BitBlt offset	BitBlt offset
87D0h - 87D3h	BitBlt pattern ROP	BitBlt pattern ROP
8BD0h - 8BD3h	BitBlt BG color	BitBlt BG color
8FD0h - 8FD3h	BitBlt FG color	BitBlt FG color
93D0h - 93D3h	BitBlt control	BitBlt control
97D0h - 97D3h	BitBlt source	BitBlt source
9BD0h - 9BD3h	BitBlt destination	BitBlt destination
9FD0h - 9FD3h	BitBlt command	BitBlt command
A3D0h - A3D3h	Cursor control	Cursor control
A7D0h - A7D3h	Cursor color 0-1	Cursor color 0-1
ABD0h - ABD3h	Cursor color 2-3	Cursor color 2-3
AFD0h - AFD3h	Cursor position	Cursor position
B3D0h - B3D3h	Cursor base address	Cursor base address
03D4h	CRTC index	CRTC index
03D5h	CRTC data	CRTC data
03D6h	CHIPS™ extensions index	CHIPS™ extensions index
03D7h	CHIPS™ extensions data	CHIPS™ extensions data
03D8h	CGA mode register (MODE)	CGA mode register (MODE)
03D9h	CGA color register (COLOR)	CGA color register (COLOR)
03DAh	Status register (STAT)	Feature control register (FCR)
03DBh	-	Clear light pen FF (ignored)
03DCh	-	Set light pen FF (ignored)

5 Appendix

5.1 Abbreviations

BIOS	B asic I nput O utput S ystem
CMC	C ommon M ezzanine C ard
CRT	C athode R ay T ube
DDC	D igital D isplay C ontrol
DPMS	D igital P ower M anagement S ignals
PCI	P eripheral C omponent I nterconnect
PMC	P CI M ezzanine C ard
VESA	V ideo E nhanced S tandard A dapter
VGA	V ideo G raphic A rray

