SIEMENS

SIMATIC S5

IP 281

Equipment Manual

Release 01
Order No: 6ES5998–0KP21

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Guidelines for Handling Electrostatic Sensitive Devices (ESD)

1 What Does ESD Mean?

Almost all SIMATIC–TELEPERM modules contain many integrated blocks or elements which use MOS technology. The technology used makes these electronic components very sensitive to overvoltages and thus to electrostatic discharge.

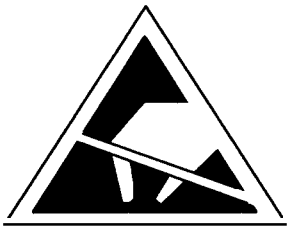
The German abbreviation for such modules is

"EGB": Elektrostatisch Gefährdeten Bauelemente
Baugruppen

Next to this abbreviation you will often find the common international abbreviation

"ESD": Electrostatic Sensitive Device

When found on cabinets, module subracks or packaging, the symbol shown below indicates that electrostatic sensitive components have been used in this device and the module is thus sensitive to touch.



ESDS can be destroyed by voltages and energies far below those perceived by humans. Such voltages can even occur when a component or a module is touched by a person who is not statically discharged. Components which have been subjected to such overvoltages can usually not be immediately identified as defective since a malfunction may not occur until the module has been in operation for a longer period of time.

To be perceived by humans, the following minimum voltages are required:

- **To be felt – 3500 volts**
- **To be heard – 4500 volts**
- **To be seen – 5000 volts**

But a fraction of this voltage can already damage or destroy electronic components.

Components which have been damaged, overloaded or weakened by static discharge can malfunction temporarily when average technical specifications are deviated from. A few examples are listed below."

- **Temperature changes**
- **Impact**
- **Jarring**
- **Changes in stress**

Only through rigorous use of protective measures and careful adherence to the handling guidelines can malfunctions and downtime of ESD modules be effectively prevented.

2 When Does a Static Charge Occur?

You can never be absolutely certain that you yourself or the materials and tools you are using are not electrostatically charged.

Small charges of up to 100 V are common but these can increase to 35,000 V in a very short time!

Examples:	**– Walking on carpeting**	up to	**35000 V**
	– Walking on plastic flooring	up to	**12000 V**
	– Sitting on upholstered chair	up to	**18000 V**
	– Unsoldering device made of plastic	up to	**8000 V**
	– Plastic coffee cups	up to	**5000 V**
	– Plastic covers	up to	**5000 V**
	– Books and pads with synthetic binding	up to	**8000 V**

3 Important Protective Measures Against Static Charging

- **Since most plastics have a strong tendency to charge, it is imperative that they be kept away from sensitive components.**
- **Be sure to provide good grounding of people, your workplace and the packaging when working with electrostatic sensitive components.**

4 Handling ESD Modules

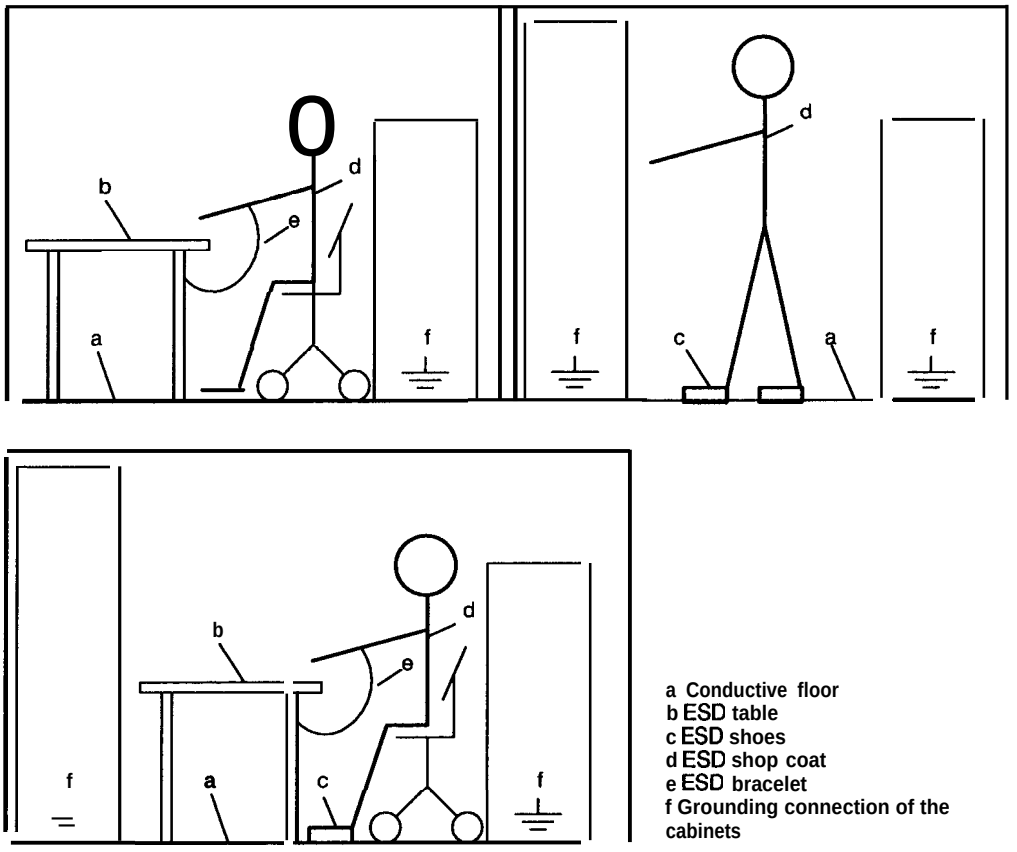
- **As a matter of principle, electronic modules should not be touched unless the work to be performed on them makes this absolutely necessary.**
- **Components should not be touched unless**

  – you are continuously grounded with an ESD bracelet

  or

  – you are wearing ESD shoes or ESD shoe protective grounding strips on an ESD floor.
- **Before touching an electronic module, your own body must be discharged. The easiest way to do this is to touch a conductive, grounded object (e.g., blank metal parts of switching cabinets, water pipes, etc.) immediately prior to touching the component.**
- **Modules should not come in contact with chargeable and highly insulating materials (e.g., plastic foil, insulating tabletops, synthetic fiber clothing).**
- **Modules should only be placed on conductive surfaces (e.g., table with ESD covering, conductive ESD foam, ESD packaging bag, ESD shipping container).**
- **Do not allow modules in the vicinity of CRTs, monitors or television sets (minimum distance to the screen > 10 cm).**

Required ESD protective measures are shown in the figure below.



a Conductive floor
b ESD table
c ESD shoes
d ESD shop coat
e ESD bracelet
f Grounding connection of the cabinets

5 Measuring and Modifying ESD Modules

- Measurements may not be performed on the modules unless
  - the measuring device is grounded (e.g., with protective conductor) or
  - the measuring head is briefly discharged (e.g., touching blank metal part of the controller housing) prior to measuring when using a floating measuring device.
- For soldering use only a grounded soldering device.

6 Shipping ESD Modules

As a matter of principle, modules and components must always be stored or shipped in conductive packaging (e.g., metallized plastic boxes, metal cans).

When packaging is not conductive, the modules must be wrapped in conductive material prior to packaging. For example, conductive foam rubber, ESD bags, household aluminum foil or paper can be used (never use plastic bags or foil).

Be sure that the conductive packaging of modules with built–in batteries does not touch or short circuit the battery connections (if necessary, cover the connections with insulating tape or material beforehand).

Notes on Safety for the User

1 General Information

This manual contains information required for operation of the described products in accordance with their intended applications. The manual is written for qualified personnel who have received special training or have adequate knowledge of measuring, and closed and open loop control technology (subsequently called automation technology).

Safe installation and commissioning, and safe operation and maintenance of the described products are dependent on a knowledge of the safety notes and warnings contained in this manual and correct observation of same. Only qualified personnel as described in item 2 have the specialized technical knowledge required to fully understand the safety notes and warnings as stated in this manual, to interpret this information correctly in concrete situations, and to put this information to use in actual practice.

This manual is a permanent part of the scope of delivery even if a separate order is required for logistics reasons. For clarity's sake, this manual does not contain all details concerning all models of the described product, and cannot cover every conceivable setup, and type of operation or maintenance. Contact your local
Siemens office if you desire additional information or if special problems arise which are not covered in sufficient detail by this manual.

In addition, be aware that the contents of this product documentation do not constitute a part of a previous or existing agreement, promise or a legal relationship, and are not intended to alter same. All obligations on the part of Siemens are based on the respective purchase order which also contains the complete and solely valid warranty provisions. The information in this manual neitherwidens nor restricts these contractual warranty regulations.

2 Qualified Personnel

Unqualified work on the device/system or noncompliance with warning notes contained in this manual and warnings posted on the device/system cabinet can cause severe personal injury or property damage. For this reason, only sufficiently qualified personnel may perform work on this device/system.

The following personnel are considered qualified for the purposes of the safety-related notes in this manual or on the product itself:

. Either programming personnel familiar with the safety concepts of automation technology

- Oroperating personnel who have been instructed in the handling of devices used in automation technology, and who are aware of the portions of this manual covering operating

- Or maintenance and service personnel who have been trained to make repairs on devices used in automation technology, and are authorized to commission, ground and label electrical circuits and devices/systems in accordance with safety standards.

3 Notes Concerning Danger

The following warnings are provided for your personal safety and for the prevention of damage to the described product or connected devices.

Notes on safety and warnings to avoid endangering the life and health of users or maintanence personnel and to prevent property damage are indicated as shown below. The terms used in this manual and the notes on the products themselves have the following meaning:

Danger

Indicates that loss of life, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that loss of life, severe personal injury or substantial property damage can result if proper precau– tions are not taken.

Caution

Indicates that minor personal injury or property damage can result if proper precautions are not taken.

Note

Important information concerning the product, handling of the product or that part of the manual which requires particular attention.

Attention

Corresponds to the above definition for “note” or “caution” when used in this manual for information concerning safety.

4 Operation in Accordance with Intended Use

- The device/system and/or the system components may only be used for the applications contained in the catalog and technical specifications, and only in combination with devices or components of other manufacturers which have been recommended and/or approved by Siemens.

- The described product has been developed, manufactured, tested and documented in compliance with applicable safety standards: Under normal circumstances, the product will not damage human health or property if the described handling regulations and safety notes concerning programming, installation, operation in accordance with intended use, and maintenance are adhered to.

Warning

- When the housing or the protection against accidental contact is removed, or when the system cabinet is opened, certain parts of these devices/systems which can contain dangerous voltages become accessible.
- Work on this device/system may only be performed by appropriately qualified personnel.
- This personnel must be thoroughly familiar with all sources of danger and maintenance measures as specified in this manual.
- Correct and safe operation of the product requires proper shipment, storage, setup and installation, and careful operating and maintenance.

5 Notes on Programming and Installing the Product

Since the product is normally used as a part of a larger svstem or plant, these notes are intended as a guide to safe integration of the product into its environment. "

The following facts require particular attention.

Note

Even when devices of automation technology are designed to provide maximum conceptual safety (e.g., multi–channel setup), it is still absolutely essential to adhere precisely to the instructions in this manual since safety measures built into the device/system to prevent dangerous errors can be rendered useless by improper handling; incorrect handling can also create additional danger sources.

Notes on installation and maintenance of the product – based on the application – are listed below.

Warning

- **The safety and accident prevention regulations applicable to the specific application must be adhered to.**
- **Built–in devices for housings or cabinets may only be used and operated when completely installed in the housing or cabinet; desktop or portable models may only be used and operated when the housing is closed.**
- **A power disconnector switch or a fuse must be provided in the building installation for facilities with a fixed connection (stationary devices/systems) without all–pole power disconnector switches and /or fuses. The facility must be connected to a protective conductor.**
- **The grounded protective contact electrical outlet for devices/systems with permanently connected, non–removable connection lines and without all–pole power disconnector switches must be installed near the device and be easily accessible.**
- **Before commissioning devices operated with power network voltage, check to determine whether the set nominal voltage range matches the local power voltage.**
- **When a 24–V supply is used, a reliable electrical separation of extra low voltages must be provided. Use only powerpacks manufactured in accordance with IEC 364–4–41 or HD 384.04.41 (VDE 0100, part 410).**
- **Fluctuations or variations of the power voltage from the nominal value may not exceed the tolerance ranges stated in the technical specifications. Otherwise the occurrence of malfunctions and dangerous states on the electrical module systems cannot be excluded.**
- **Measures must be provided by which an interrupted program can be properly restarted aftera drop in voltage or a power loss. This must not cause dangerous operating situations even for short times. If necessary, "emergency OFF" must be forced.**
- **"Emergency OFF" systems in accordance with EN 60204 IEC 204 (VDE 01 13) must remain effective in all operating modes of the automation system. Releasing the "emergency OFF" system must not cause uncontrolled or undefined restarts.**

Caution

- **Installation of connection and signal lines must be such that inductive and capacitive interferences do not affect the automation functions.**
- **Installation of automation systems and their operating components must be such that they are sufficiently protected against accidental activation.**
- **Appropriate safety measures must be provided on the 1/0 coupling of the hardware and software to prevent a line or wire break from causing undefined states in the automation system.**

6 Active and Passive Errors of an Automation System

- Depending on the task to be performed by an electronic automation system, both active and passive errors can bedangerous errors. In a drive control system, for example, the active error is usually dangerous since it can cause the drive to be switched on. In contrast, a passive error in a message function can prevent a dangerous operating state from being reported.
- The distinction between possible errors and their classification as dangerous or not dangerous based on their task is important to all safety measures concerning the-delivered product.

Warning

Everywhere where errors in the automation system can cause substantial property damage or even personal injury (i.e., can be dangerous errors), additional external measures must be taken or systems created which will ensure or force safe operation when an error occurs (e.g., with an independent limit value switch, mechanical locks, etc.).

7 Maintenance and Repair Procedures

When measurements or tests must be performed on an active device, the specifications and instructions contained in accident prevention regulation VBG 4.0, and §8 "Permissible Deviations during Work on Active Parts" in particular, must be complied with. Suitable electrical tools must be used.

Warning

- Repairs on an automation system may only be performed by **Siemens** Service personnel or by repair shops authorized by **Siemens**. When replacing parts or components, use only parts contained in the spare parts list or listed under the section on spare parts in this manual. Unauthorized opening and faulty repairs can result in death or severe personal injury, and substantial property damage.
- Before opening the device always pull the power plug or open the disconnection switch.
- When replacing fuses, use only the types specified in the technical specifications or the maintenance instructions of this publication.
- Do not throw batteries in an open fire and do not perform soldering on the body of the battery. Danger of explosion (maximum temperature of 100° C). Do not open or recharge lithium batteries or batteries containing mercury. When replacing, use only the same types.
- Always dispose of batteries or accumulators at a special waste collection point.
- Use of monitors:
  Faulty work (particularly changes in the high–voltage or installation of another type of picture tube) can result in increased emission of X–rays. A device which has been thus modified no longer meets certification criteria and may not be operated.

ENVIRONMENTAL
PROTECTION
IN ACTION

Information Concerning
Packaging Material/Notes on Disposal

Dear Customer !

Our high–quality products cannot reach you safely without effective protective packaging. The size of the packaging is kept to an absolute minimum.

All our packaging materials are harmless to the environment and can be disposed over without danger.

Wood is not chemically treated.

Cardboard is made primarily of waste paper which can then be torn up and given to a waste paper collection.

Sheeting is made of polyethylene (PE), tapes of polypropylene (PP) and CFC–free padding of foamed polystyrene (PS).

These materials are pure hydrocarbons and can be recycled. Please dispose of these valuable secondary raw materials at a recycling center.

Recycling saves raw materials and cuts down on the amount of refuse.

Ask your city administration for the address of the recycling center nearest you to dispose of packing materials and discarded devices.

Thank you for your help !

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Warning

Risks involved in the use of so–called SIMATIC–compatible modules of non–Siemens manufacture

"The manufacturer of a product (SIMATIC in this case) is under the general obligation to give warning of possible risks attached to his product. This obligation has been extended in recent court rulings to include parts supplied by other vendors. Accordingly, the manufacturer is obliged to observe and recognize such hazards as may arise when a product is combined with products of other manufacture.

For this reason, we feel obliged to warn our customers who use SIMATIC products not to install so-called SIMATIC–compatible modules of other manufacture in the form of replacement or add-on modules in SIMATIC systems.

Our products undergo a strict quality assurance procedure. We have no knowledge as to whether outside manufacturers of so–called SIMATIC– compatible modules have any quality assurance at all or one that is nearly equivalent to ours. These so–called SIMATIC– compatible modules are not marketed in agreement with Siemens; we have never recommended the use of so–called SIMATIC–compatible modules of other manufacture. The advertising of these other manufacturers for so–called SIMATIC–compatible modules wrongly creates the impression that the subject advertised in periodicals, catalogues or at exhibitions had been agreed to by us. Where so–called SIMATIC–compatible modules of non–Siemens manufacture are combined with our SIMATIC automation systems, we have a case of our product being used contrary to recommendations. Because of the variety of applications of our SIMATIC automation systems and the large number of these products marketed worldwide, we cannot give a concrete description specifically analyzing the hazards created by these so–called SIMATIC–compatible modules. It is beyond the manufacturer's capabilities to have all these so–called SIMATIC– compatible modules checked for their effect on our SIMATIC products. If the use of so–called SIMATIC– compatible modules leads to defects in a SIMATIC automation system, no warranty for such systems will be given by Siemens.

In the event of product liability damages due to the use of so–called SIMATIC–compatible modules, Siemens is not liable since we have taken timely action in warning users of the potential hazards involved in so–called SIMATIC–compatible modules. "

Table of Contents

Introduction

Setup of the Manual

This equipment manual is intended as an aid to installing and operating the IP 281 module.

Before starting to work with the module, take thetimeto lookthrough this equipment manual. You can start by looking up passages which are of particular interest to you. The goal is to obtain an overview of the information provided.

The individual sections are self–contained and provide blocks of information on the following subjects,

- Installation
- Commissioning
- Handling

Sections 2,3 and 6 contain information on special tasks which you will have to perform when preparing the module for operation.

Abbreviations

Abbreviations which are not part of everyday usage are written out in full the first time they appear. In addition, a list of all abbreviations is provided in the “Definition of Terms” at the end of the manual.

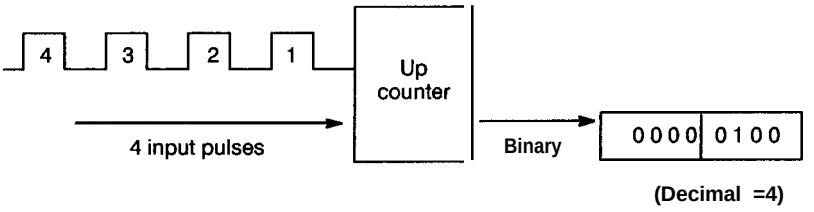
Cross References

Cross references to parts of other sections are not made unless the repetition of facts would require too much space and it can be assumed that the description at another location is sufficient. Only the applicable subsection number is given for cross references to parts of other sections. Example: (→ section 2.1)

Principle of Operation of a Counter Module

Counting is primarily the acquisition and summation of events. In the world of electronics, this is the summation of pulses. Two directions of counting are available.

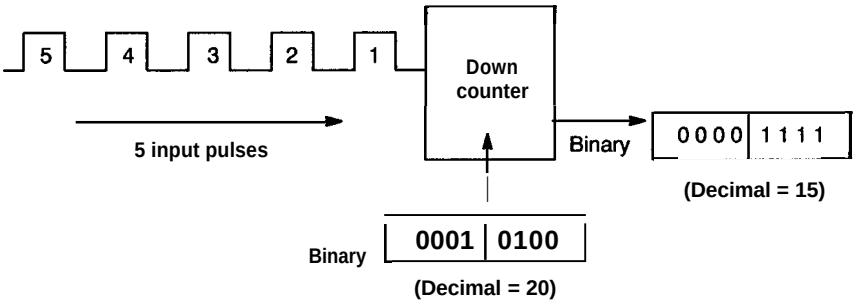
Counting up



When counting up, the pulses are added (to a start value in some cases). This can be used, for example, for simple acquisition of a piece count.

Counting down

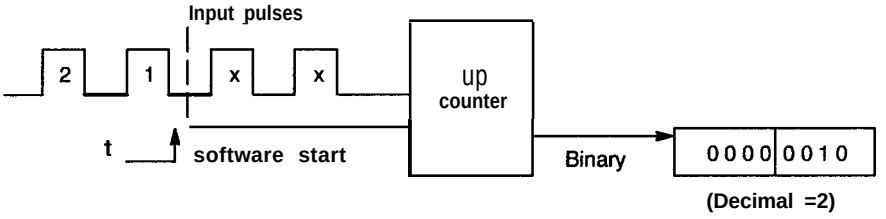
Starting with a start value which you have stored in a register (memory location) of the IP 281, the counter is decremented by the number of input pulses.



This can be used, for example, to count out an exact number of pieces and then package them. The counter is provided with an output signal here which can be used, for example, to close a valve when counter status zero is reached,

Counting with software start (or software stop)

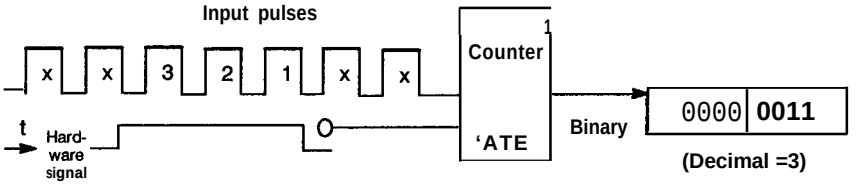
It is often necessary to link the pulses (depending on other input variables) starting at a defined point in time, and then use this group information to start or stop the counter.



This can be used, for example, if you know that the characteristics (differences in shape, color, material or other differences) of the first products will be different from the serial product.

Counting with hardware gate control

If a hardware signal is to start a high–speed counting procedure directly from the system (i.e., from the process), this signal is best applied directly to the gate of the counter. This permits the counter to be started without loading the S5 cycle.



A defined stop of the counting procedure can also be performed with the gate.

Application Areas of the IP 281

The IP 281 counter module permits the acquisition and conditioning of counting pulses up to a counting frequency of 250 kHz.

Why is such a conditioning module required when STEP5 programmable counters are already available for all programmable controllers?

These software counters have limits. To count 50 Hz pulses, for example, the programmable controller must process the counter program portion at time intervals of less than 10 msec. (Twice the "processing frequency" is required since the software counter must also acquire the falling edge of the counting signal in order to be able to recognize the rising edge.)

– Multiple calling of the counter program portion (with direct access to the periphery)

– Counting input as interrupt input

When a software counter is used as an interrupt program, the sampling time limit of the signal is shortened to the run time of the longest individual block. This applies particularly to the use of input module 432. The delay time of the input filter of this module can be shortened to 0.3 msec. Theoretically, this makes it possible to acquire frequencies up to approximately 1.5 kHz. However, the operating system cannot recognize the pulses since the interval between two signal edges is too small (i.e., all counting pulses are not acquired).

Considering the above arguments, software counters and the IP 281 conditioning counter module can be used for the following application areas.

Low frequencies are counted with software counters. Higher frequencies (up to 250 kHz) are counted with special counter modules such as the IP 281.

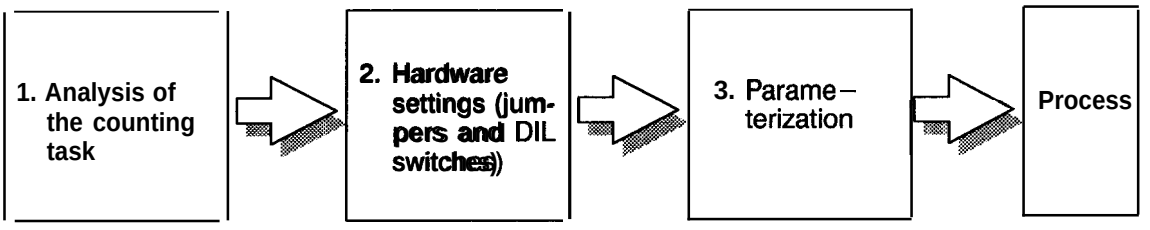
There is no clearcut boundary between the two methods (between 50 Hz and several 100 Hz).

The IP 281 offers additional advantages which speak for the use of this module.

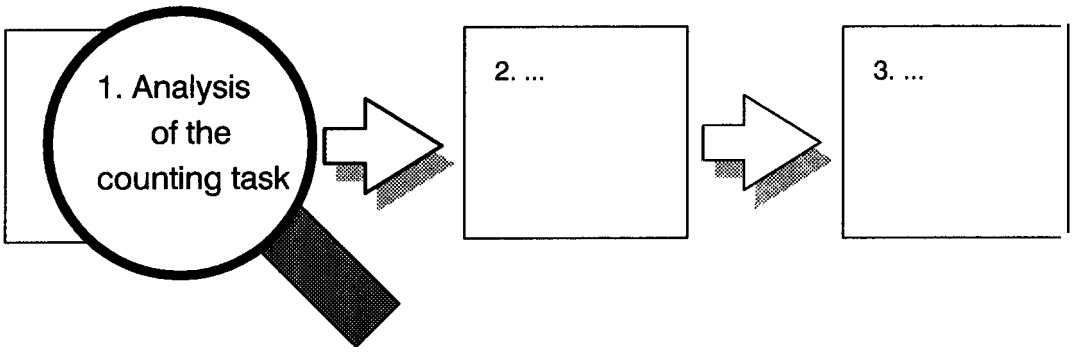
- Depending on the degree of expansion, the module is equipped with one or two counters. The counters can be used together or separately.
- The external addressing of counting gate inputs offers additional ways to start and stop the counters.
- Start values can be specified for the counters by the S5 program. The point in time at which these values are loaded in the counters can be specified by the S5 program or directly by the external signals.
- Each counter can report events (e.g., overflow or end of counting). This message can be both an interrupt to the programmable controller, and an external hardware output.

The counter module is used as the connecting element between high–speed events in the process, and the program in the programmable controller.

Use of the IP 281 counter module requires that the following steps be performed.



Analysis of the Counting Task



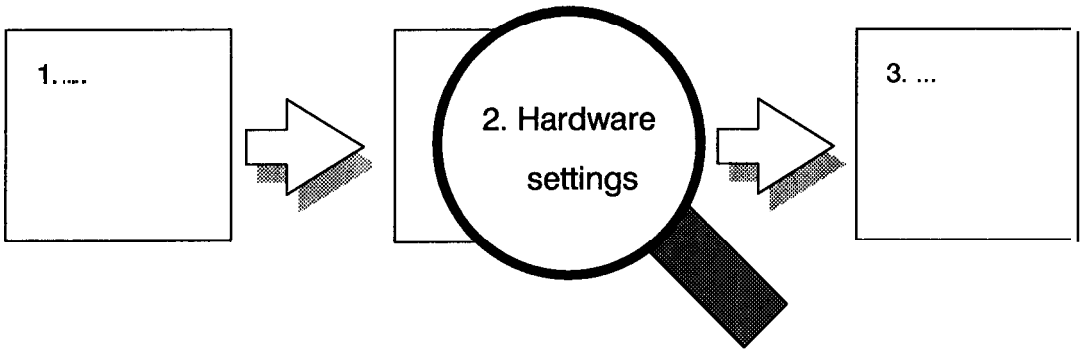
There are many ways to adapt the IP 281 to the counting task. The following questions must be answered by the analysis of the counting task.

- **Which encoder is to be used?**
- **What counting range is required?**
- **What counting frequency is required?**
- **Is this a one–time counting procedure or is the counting procedure repeated continuously?**
- **Is the counting procedure to be controlled by a hardware or software gate?**
- **Are reactions outside the module to be triggered when certain values are reached?**
- **Is the combination of two counters useful?**
- **Is the counting procedure to begin at a certain value?**
- **Is the counting procedure to stop at a certain value?**

After all these questions have been answered, the module can then be set for your particular application as shown below.

- **Hardware settings**
  and
- **Parameterization**

Hardware Settings



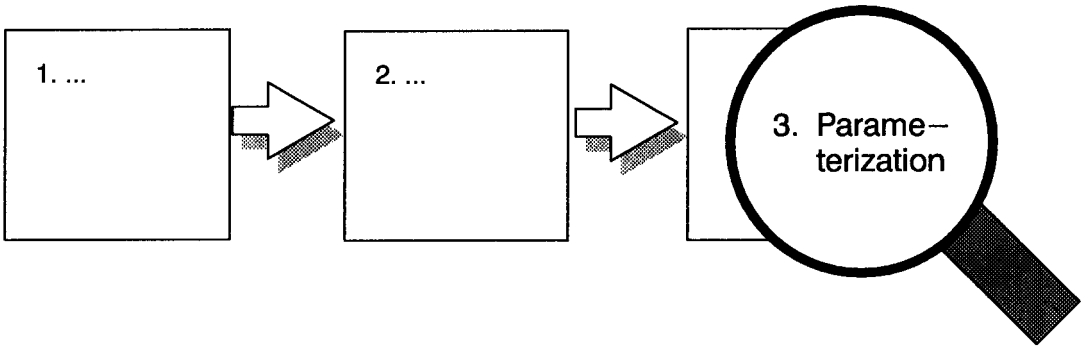
The IP 281 counter module is equipped with one or two counters. Each counter can be set separately.

The hardware settings described in section 2 are used to adapt the counter module to specific counting applications.

Plug connectors on the front of the module are used to connect the encoder inputs, the digital inputs and the digital outputs. It is easiest to use prefabricated cables.

The conditions described in section 8.7 concerning the time relationships of the input signals (e.g., pulse widths and pulse sequences) must be adhered to.

Parameterization



The IP 281 counter module is set via various registers for the counting task. The registers are written via the programmable controller S5 commands.

1 General Function Description

1 General Function Description

1.1 Short Description

The IP 281 is a counter module for use in SIMATIC S5 controllers. It is modular in design. The IP281 consists of a basic module with a counter for direct connection of incremental encoders, and an optional plug–in submodule containing a second counter with the same specifications. Use of the second counter increases the range of applications.

The IP 281 is a hardware module with a complex gate array in which all counting functions and the bus interface are integrated. It is operated in the 1/0 area of the SIMATIC S5. Access times are very short since the S5 uses simple transfer commands to access all registers of the IP 281 directly. For example, a 16–bit counter value can be read by the CPU 9446 in less than 5.6 µsec. This makes the IP 281 also suitable for rapid, closed–loop control applications among other things.

The IP 281 is equipped with the following features.

- **One–time, two-time and four–time evaluation of the encoder signals**
- **Operation in 16 or 32–bit mode**
- **Choice of positive or positive and negative counting range**
- **Loading the counters with defined, initial values**
- **Comparison per counter with an interrupt value (comparator)**
- **Transfer of values from counter 1 to counter 2 as interrupt or load value**
- **Gate control**
- **Gate start, gate stop and setting via digital inputs**
- **Direct triggering of control procedures outside the module via digital outputs**
- **Possible connection of incremental, 24 V encoders or 5 V (RS 422) encoders with two pulse trains displaced by 90”**
- **Possible connection of directional encoders**
- **Encoder supply via the module (24 V standard, 5.2 V optional)**

1.2 Application Area

The IP 281 module is designed for use in SIMATIC S5 systems, and can be used in the following programmable controllers.

- PLC S5–115U (CPUs 941 A/B to 944A/B)
- PLC S5–135U (CPUs 922, 928A and 928B)
- PLC S5–155U (CPUs 922, 928A, 928B, 946 and 947)
- PLC S5–115H (CPU 942H)
- PLC S5–155H (CPU 946R/947R)

Ordering notes

The IP 281 counter module is available under the following order numbers.

IP 281 counter module with 24 V encoder supply:	**6ES5 281–4UA11**
IP 281 counter module with 24 V and 5.2 V encoder supply:	**6ES5 281–4UP11**
IP 281 plug–in submodule for counter 2:	**6ES5 281–4UB11**

1.3 Hardware Description

1.3.1 Mechanical Setup

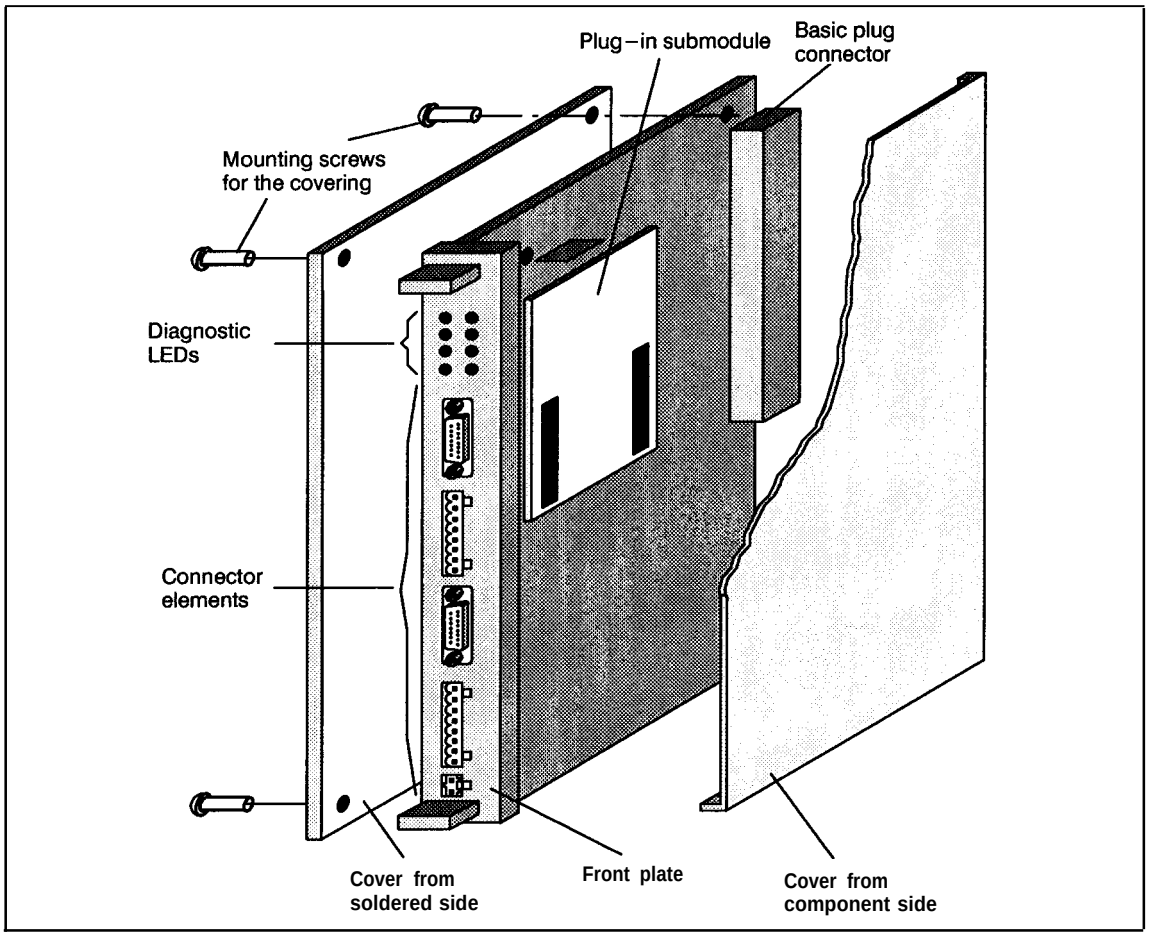


Figure 1.1: Setup of the IP 281

The IP 281 consists of a basic module and a plug–in submodule available as an optional expansion.

Basic Module

- **Double Europe format: 233 mm x 160 mm**
- **Mounting width: 1 1/3 SEP**
- **Front plate: plastic with diagnostic LEDs and connector elements**
- **Plastic covering on both sides**

Counter 1 is included on the basic module.

Plug–in Submodule

- **Dimensions: 90 mm x 90 mm**

Counter 2 is included on the plug– in submodule.

Mounting the plug–in submodule

Make the required hardware settings on the plug– in submodule prior to installation (-t section 2.3).

The plastic covering must be removed (four screws) before the plug–in submodule can be installed.

The plug–in submodule is equipped with four plastic distance pins. When inserting the submodule, all pins must snap into place in the receptacle holes.

The plug–in submodule can be removed manually from the basic module.

> **Caution**
>
> **To avoid damaging the module, do not use tools to remove the plug–in submodule.**

After installation, replace plastic coverings and screw down.

1.3.2 Diagnostic LEDs

Eight (8) LEDs are installed on the front plate.

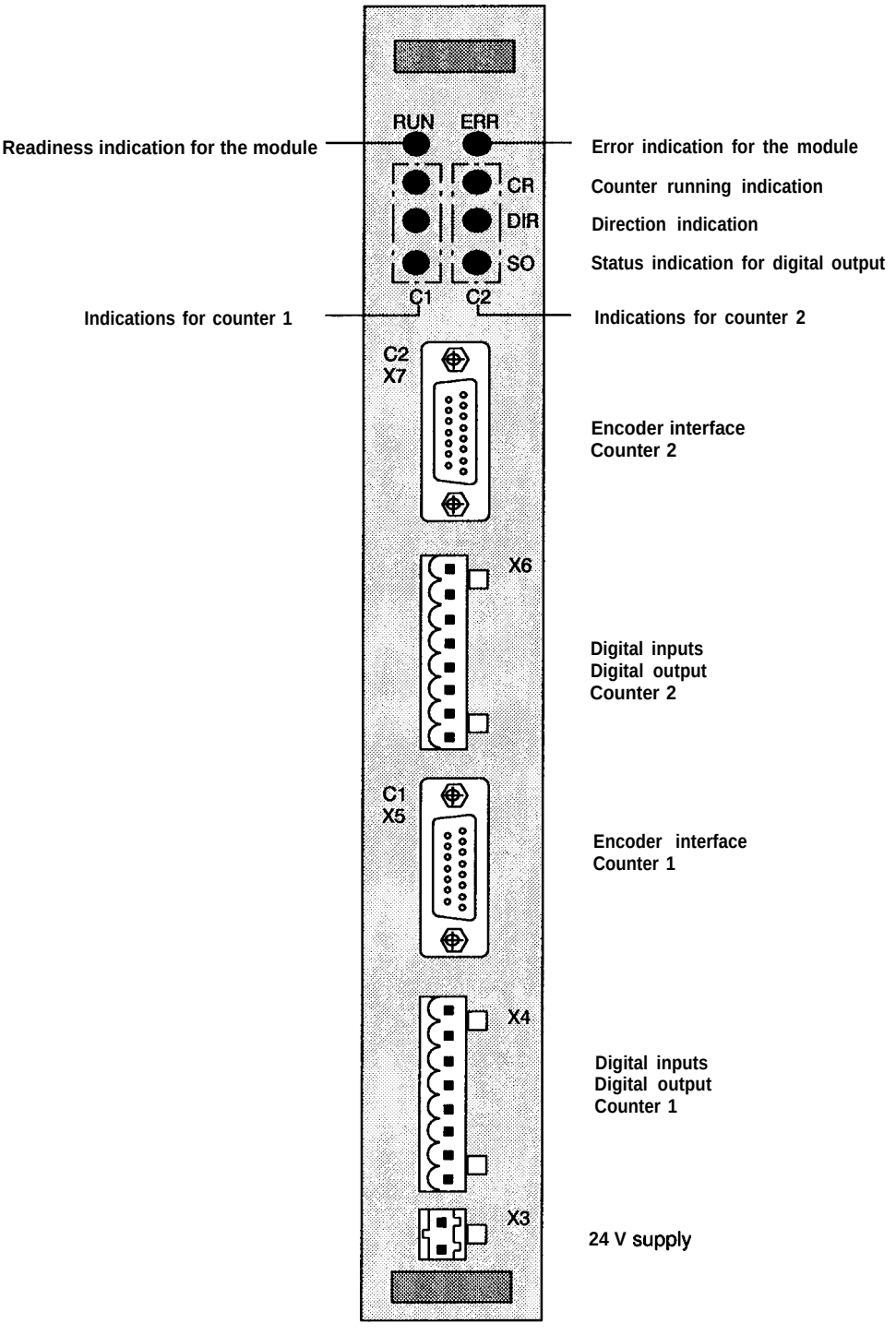


Figure 1.2: Front plate with indication and connector elements

Description of the Diagnostic LEDs

RUN LED (Running)
ERR LED (Error)

These two LEDs indicate that the module is ready for operation or that malfunctions have occurred.

Indication RUN	Indication ERR	Meaning
0	O	Voltage supply error (of S5)
0	☼	RESET is active.
☼	O	Module is operating correctly.
☼	☼	Parameterization error or wire break

CR LED (Counter running)

This LED indicates the status of the applicable counter.

Indication	Status of the Counter
☼	CRS = 1 or CRS changing very quickly; counter is counting at high speed.
0	CRS = O (RESET status)
Flashing	CRS changing; counter is counting at low speed.

DIR LED (Direction)

This LED indicates the direction of counting. When the encoder is stationary, the direction which was last indicated is retained.

Indication	Direction of Counter
☼	(LED for counter 2 goes on even when the plug-in submodule is not inserted.)
0	Down

SO LED (Status output)

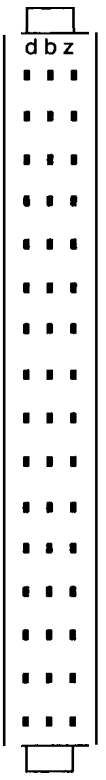
This LED indicates the status of the digital output.

Indication	Status of the Digital Output
☼	Active (24 V on the digital output) (LED for counter 2 goes on even when the plug-in submodule is not inserted.)
0	Inactive (O V on the digital output)

1.3.3 Plug Connector Allocation

S5 interface, basic plug connector X I

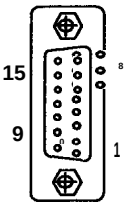
The basic plug connector (48–way, multi–pointterminal strip, DIN 41612, model F) is located on the back of the module. Its allocation is shown below.



	d	b	z
	Signal	Signal	Signal
2		MI	5 V
4		PESP	
6		ADB 0	RESET
8		ADB 1	$\overline{\text{MEMR}}$
10		ADB 2	$\overline{\text{MEMW}}$
12		ADB 3	$\overline{\text{RDY}}$
14	$\overline{\text{IRA}}$	ADB 4	DB 0
16	$\overline{\text{IRB}}$	ADB 5	DB 1
18	$\overline{\text{IRC}}$	ADB 6	DB 2
20	$\overline{\text{IRD}}$	ADB 7	DB 3
22		ADB 8	DB 4
24		ADB 9	DB 5
26		ADB 10	DB 6
28		ADB 11	DB 7
30		BASP	
32		MI	

Encoder inputs, plug connectors X5 and X7

Type of plug connector: 15–way, sub D socket with screw lock The pin allocations of plug connectors X5 (for counter 1) and X7 (for counter 2) are identical.



5 V Encoder Signals in Accordance with RS 422

Pin	Designation	Meaning
6	5.2 V	5.2 V encoder supply (option)
7[1]	GND	Reference potential of the module (S5 bus)
10	N	Zero marking pulse (N)
11	$\overline{N}$	Zero marking pulse ($\overline{N}$)
12	E	Counting signal (track $\overline{B}$)
13	B	Counting signal (track B)
14	$\overline{A}$	Counting signal (track $\overline{A}$)
15	A	Counting signal (track A)

24 V Encoder Signals

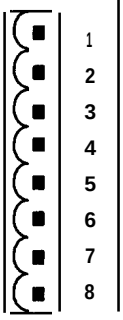
Pin	Designation	Meaning
1	A*	Counting signal (24 V, track A*)
4	B*	Counting signal (24 V, track B*)
5	24 V	24 V encoder supply
7'	GND	Reference potential (24 V)
8	N*	Zero marking pulse (24 V)
9	RE	Load resistance for A*, B* and N*

1 Change the jumper so that the reference potential on pin 7 corresponds to the-connected encoder (→ sections 1.4.1 and 2.3).

Pins 2 and 3 are not used.

Digital inputs and outputs, plug connectors X4 and X6

Type of plug connector: 8–way, pin plug connector with screw connection for the individual leads.
The pin allocations of plug connectors X4 (for counter 1) and X6 (for counter 2) are identical.



	Designation	Meaning
1	STA	Gate start input
2	0 V_{extDI}	Reference potential for digital input
3	STO	Gate stop input
4	0 V_{extDI}	Reference potential for digital input
5	SET	Set input
6	0 V_{extDI}	Reference potential for digital input
7	DQ	Digital output
8	0 V_{extDQ}	Reference potential for digital output

24 V supply, plug connector X3

Type of plug connector: 2–way, pin plug connector with screw connection for the individual leads

	Designation	Meaning
1	24 V_{ext}	24 V supply voltage
2	0 V_{ext24}	External reference potential

1.3.4 Functional Setup of the Module

The IP 281 module provides the hardware for counting with one or two counters. It operates without a separate processor and represents only a slight load for the SIMATIC S5. The necessary logic and the two, 16/32-bit counters are implemented in a gate array (ASIC).

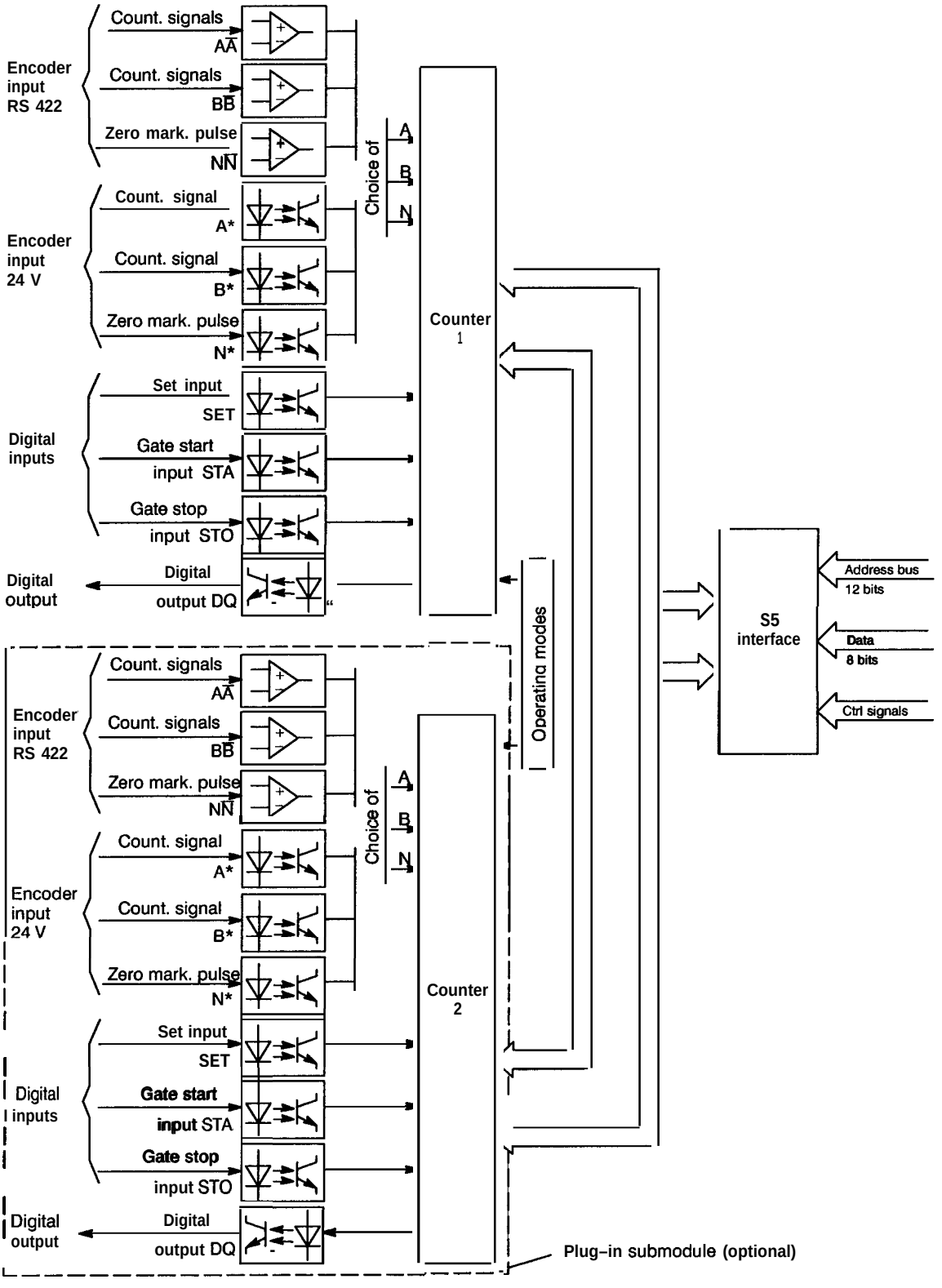


Figure 1.3: Function elements of the IP 281

The following flowchart shows the principle of operation of a counter. It indicates the most important hardware components and how the registers affect the counter, See section 6.8 for a detailed diagram.

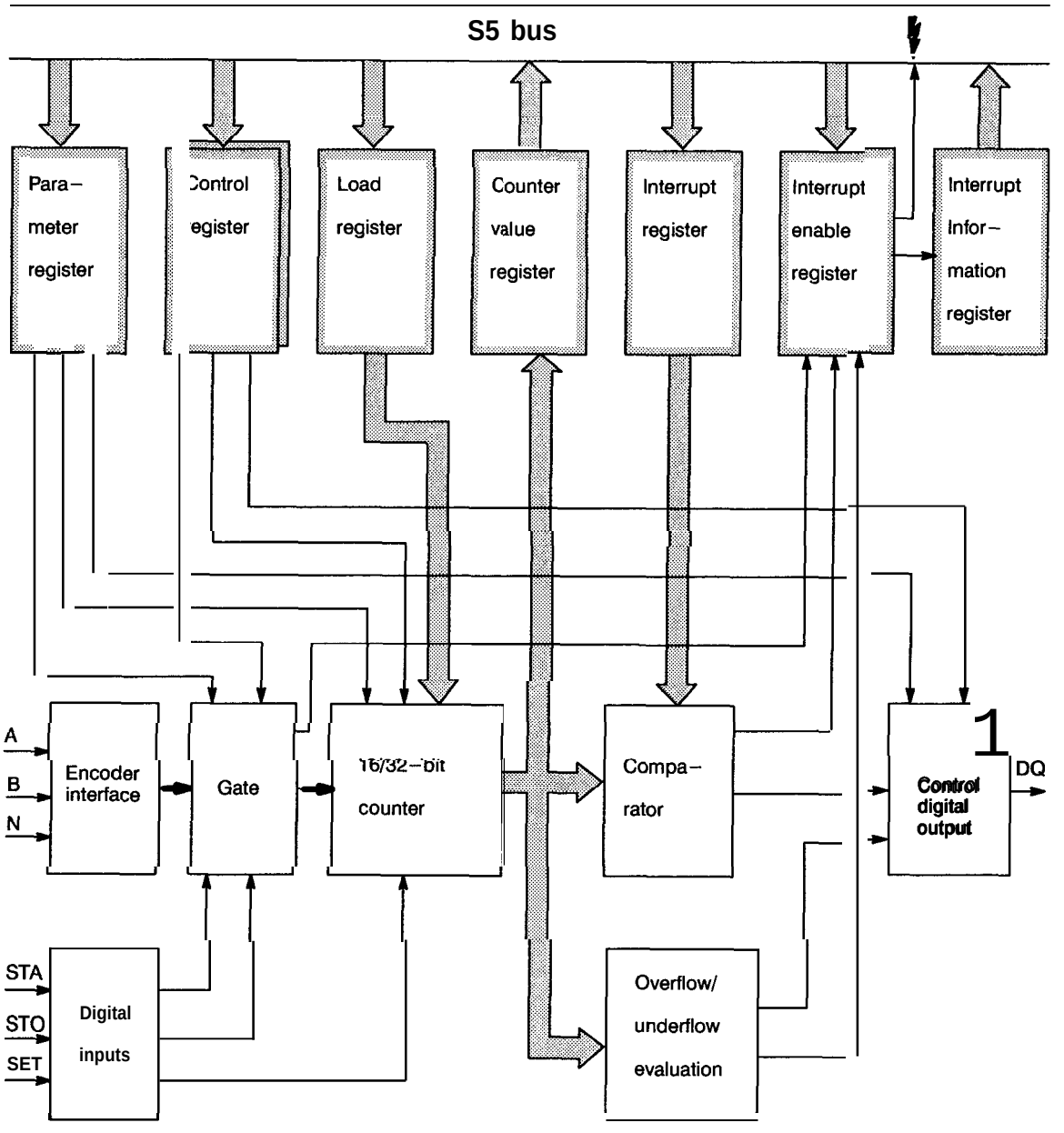


*Figure 1.4: Principle of operation of a counter in the **IP** 281*

1.4 Process Interfaces

Each counter is equipped with the following inputs and outputs as the interface to the process.

Encoder interface

The encoder interface can be set to 24 V connection or to 5 V connection (RS 422). This is perfromed with plug–in jumpers (→ section 2.3 for the hardware settings).

The following signals are evaluated.

- **A$\overline{A}$ or A* Counting pulse train, track A**
  A* for 24 V signals
- **B$\overline{B}$ or B* Counting pulse train, track B**
  B* for 24 V signals
- **N$\overline{N}$ or N* Zero marking pulse N,**
  N* for 24 V signals

Digital inputs

Three digital inputs separated by optocouplers are available.

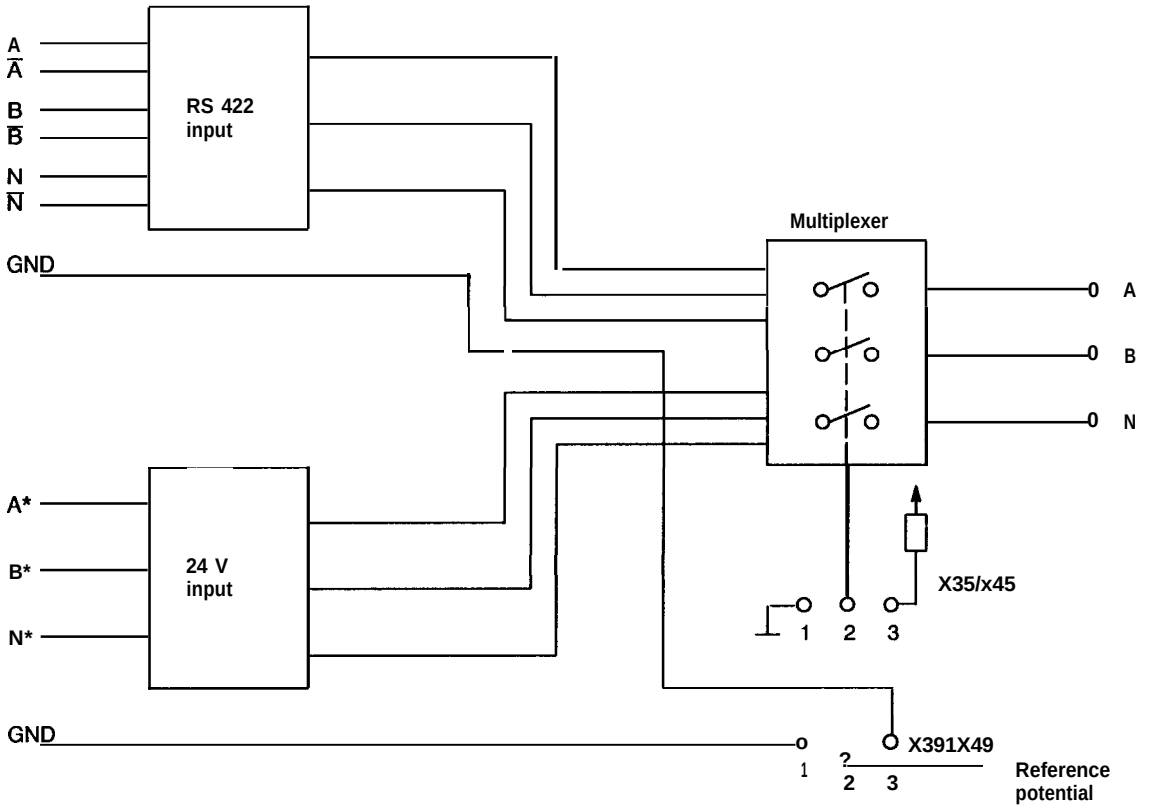
- **STA Gate start input**
  This input is also used during level control to stop the counter (→ section 6.6.3).
- **STO Gate stop input**
  This input must be low for level control (→ section 6.6.3).
- **SET Set input (preliminary contact) (e.g., proximity switch)**

Digital output

- **DQ 24 V digital output**

1.4.1 Encoder Interface

The encoder interface can be operated with either24V level or 5 V level (RS 422). Plug–in jumpers X35 (counter 1) and X 45 (counter 2) are used to make the switch–over.



Counter 1	Counter 2	Allocation	Selected Interface
x35	x45	1–2	For 24 V encoder
x35	x45	2–3	For 5 V encoder in accordance with RS 422

The 5 V area and the 24 V area are free–floating. To insure that this separation is retained, the corresponding reference potential must be circuited on pin 7 of the encoder interface depending on the encoder selected (-t section 2.3, selecting the reference potential).

Counter 1	Counter 2	Allocation	Reference Potential
x39	x49	1–2	For 24 V encoder
x39	x49	2–3	For 5 V encoder (RS 422)

Caution

Incorrectly inserted jumpers (e.g., S5 reference potential for 24 V encoders) can lead to interference caused by grounding loops. In addition, potential isolation between the 24 V encoder inputs and the S5 backplane is lost.

Status on delivery: Jumper 1–2 inserted → reference potential for 24 V encoder

1.4.1.1 24 V Encoder Interface

The 24 V encoder interface includes the inputs for the three counting signals A*, B* and N*, a connection for load resistances and the encoder supply.

Signal inputs

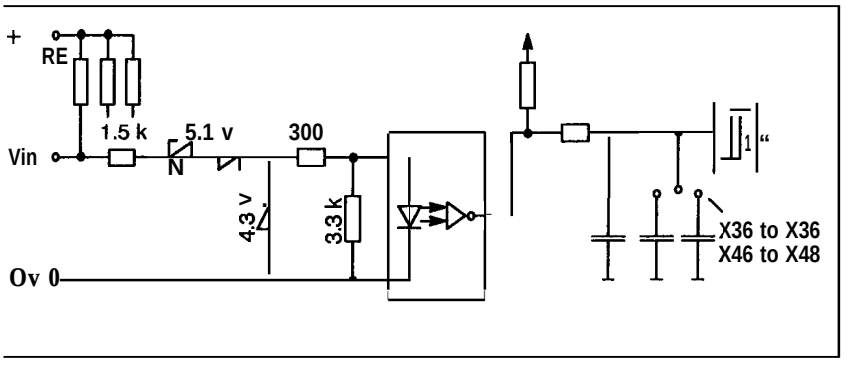
The inputs are potentially isolated from the S5 bus and the digital inputs via optocouplers. The three encoder inputs are non–floating relative to each other. Encoders with two pulse trains (A* and B*) displaced by 90° can be connected.

Each input is equipped with an RC filter for the suppression of interferences.

Plug–in jumpers (--t section 2.3) can be used to set this filter to three limit frequencies (≤ 250 kHz, s 50 kHz, s 1 kHz).

When the module is operated on the 24V encoder interface, the reference potential GND must be set for 24 V (→ section 2.3) and the wire break recognition must be switched off.

Input circuitry



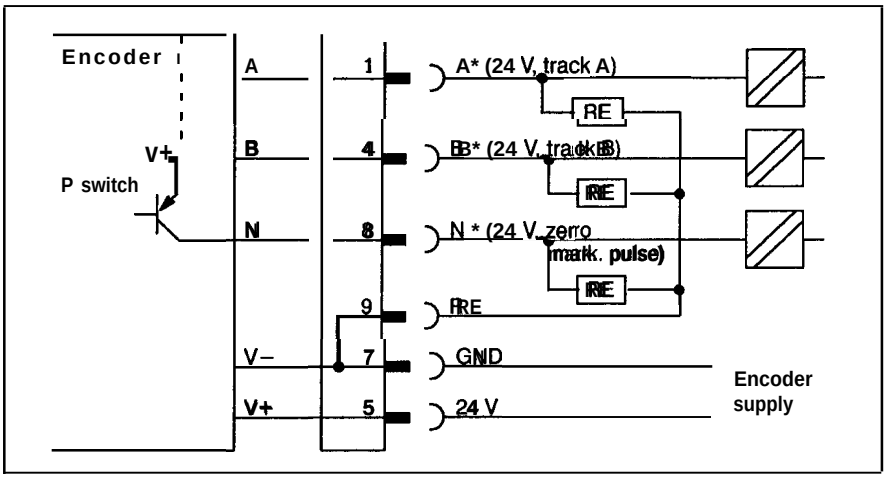
Load resistances

Use the common connection (pin 9) to apply them to GND or 24 V depending on the type of encoder.

Caution

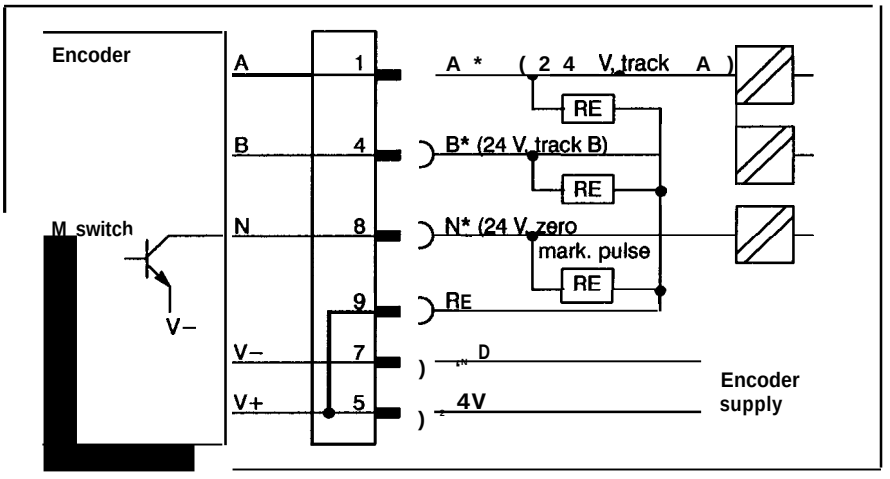
Pin RE on the plug connector must always be connected otherwise inputs A*, B* and N* will be coupled together (i.e., triggering of one input can cause another input to be triggered).

Encoder with P switching outputs



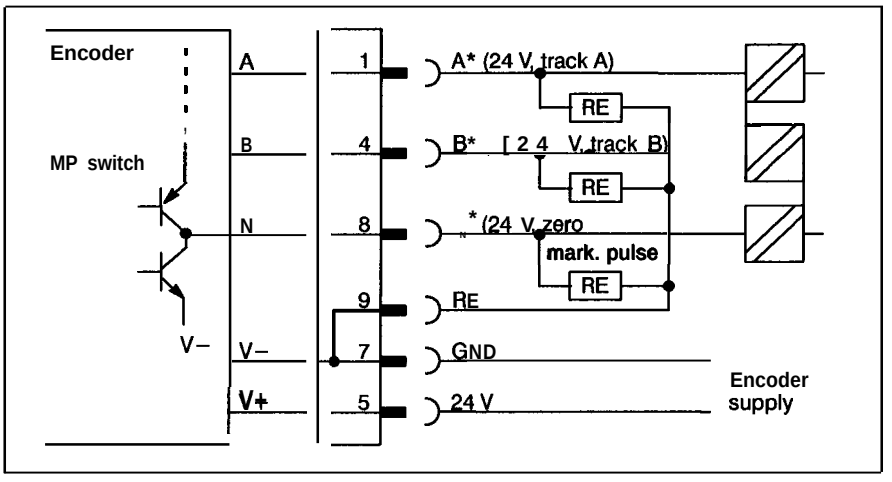
Pin 7 and pin 9 must be jumpered.

Encoder with M switching outputs (open collector)



Pin 5 and pin 9 must be jumpered.

Encoder with MP switching outputs (push-pull outputs)



Pin 7 and pin 9 must be jumpered.

Counting with one counting input

When only one counting input is used, this must be applied to input A*.

The direction of counting is set on counting input B*. There are two ways to do this.

– Connect a directional encoder to counting input B* (low level → up, high level -t down).

– Change the direction of counting by inverting bit 11 in parameter register 1/2 (inversion of counting input B*). The following applies to counting input B* when it is not connected or low: Bit 11 = O -t up, bit 11 = 1 → down.

  Counting mode direction evaluation EVDI (-t section 6.2.2) must be set for counting with one counting input.

Encoder supply

The encorder supply (24 V) is provided with potential isolation from the digital inputs and the S5 bus. Potential isolation from the digital output is not provided. The encoder supply is available on connection plug connector X5/X7. It is short circuit proof (--t section 1.4.4).

1.4.1.2 5 V Encoder Interface in Accordance with RS 422

The 5 V encoder interface contains the inputs for the three, differential counting signals A/$\overline{A}$, B/E and N/$\overline{N}$. A 5.2 V encoder supply is available on the module as an option.

Signal inputs

The signal inputs are provided with potential connected to the S5 bus. The inputs are potentially isolated from the following.

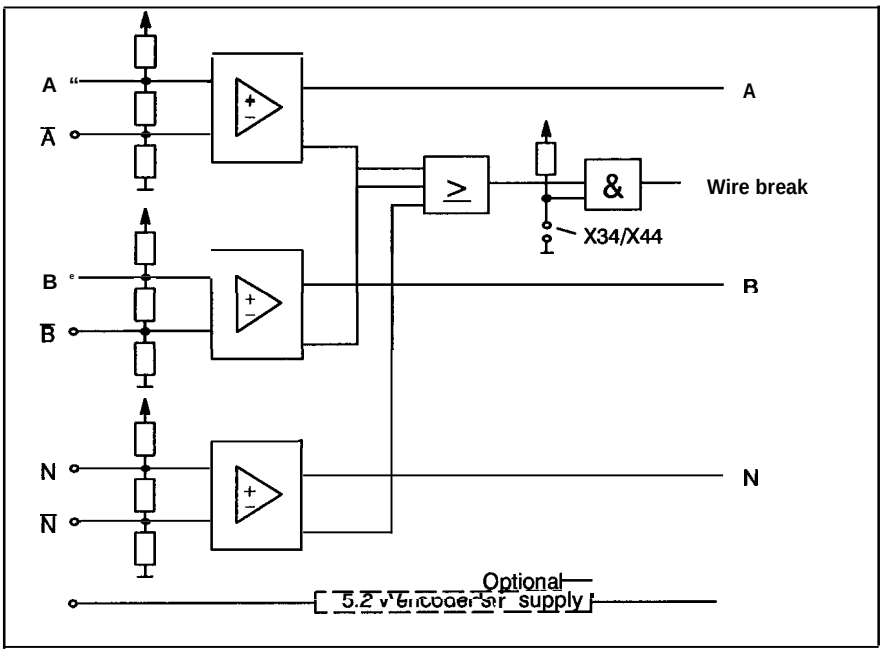
– Digital inputs
– Digital output
– 24 V supply

Encoders with two, differential signals displaced by 90° (track A/$\overline{A}$, track B/$\overline{B}$ and zero marking pulse N/$\overline{N}$ in accordance with RS 422) can be connected,

When the module is operated via the RS 422 interface, the reference potential must be set for the S5 bus (→ sections 1.4.1 and 2.3).

Wire break recognition

The inputs are equipped with wire break recognition. This can be switched on and off with plug– in jumpers X34/X44.



The wire break recognition detects the following errors.

- **Wire break on the signal input**
- **Wire break on the inverted signal input**
- **Short circuit between signal input and inverted signal input**
- **Short circuit between signal input and O V[1]**
- **Short circuit between signal input and 5 V[1]**

1 Is not detected unless the voltage difference between user signal and short circuit < 1.1V.

When the wire break recognition is active and an error occurs, the error is entered in status register 3 and the ERROR LED goes on. There is one wire break recognition for each counter.

The message is retained for the duration of the error.

When the wire break recognition is active and counting inputs are open, this causes a wire break message.

☞ The wire break recognition must be switched off for unconnected plug connector/unused input X5/X7.

The wire break recognition can cause errors when very long connection lines are used. Switch off the wire break recognition if this happens.

5.2 V encoder supply

An optional model of the basic module is also available with a short circuit proof, 5.2 V encoder supply on plug connector X5/X7(+ section 1.4.4).

This 5.2 V encoder supply cannot be retrofitted later.

1.4.2 Digital Inputs (DI)

Each counter is equipped with three digital inputs.

- STA = Input, gate start
- STO = Input, gate stop
- SET = External set input (preliminary contact) (e.g., proximity switch)

The inputs for counter 1 are located on plug connector X4; the inputs for counter 2 are located on plug connector X6 (→ section 1.3.3).

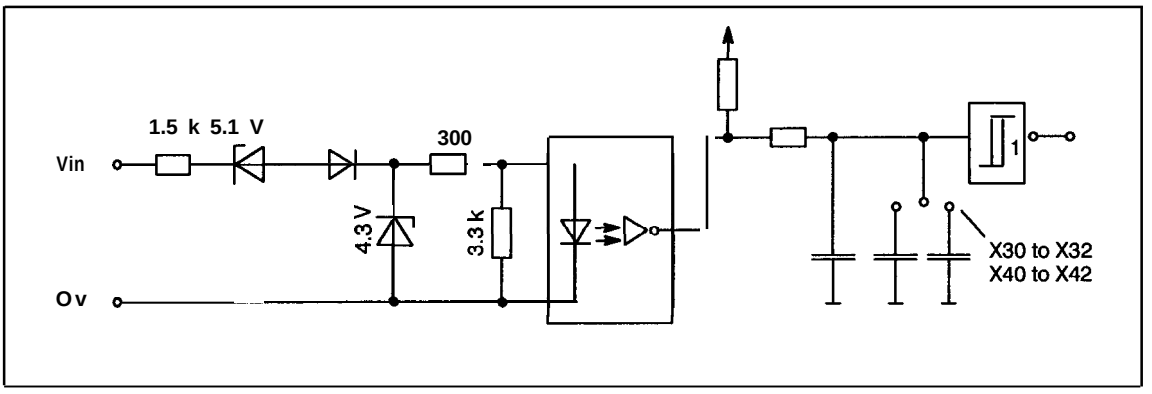
The digital inputs are potentially isolated from the following.

– S5 bus
– Digital output
– Encoder interface

The digital inputs are 2–way. They are operated with a nominal voltage of 24 V. The function of digital inputs STA and STO is described in sections 6.6.2 and 6.6.3; the function of digital input SET is described in section 6.5.1.2.

Each digital input is equipped with an RC filter (for the suppression of interferences) following the optocoupler. Plug–in jumpers (→ section 2.3) can be used to set this filter to three limit frequencies (≤ 250 kHz, ≤ 25 kHz, ≤ 100 Hz).

Input Circuiting of the Digital Inputs

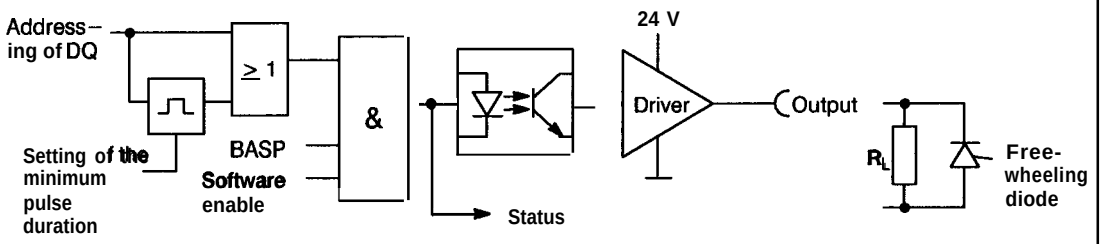


1.4.3 Digital Output (DQ)

Each counter is equipped with one, two-way, digital output with a nominal voltage of 24 V. The digital output for counter 1 is available on plug connector X4; the digital output for counter 2 is available on plug connector X6 (→ section 1.3.3).

The digital output can be used to directly trigger processes external to the module. The functions of the digital outputs are described in section 6.7. Direct connection of a relay is possible (maximum load current of 600 mA).

The connected relay must be equipped with a free-wheeling diode.



When activated, the output remains active for the minimum pulse duration. This minimum pulse duration can be set to three different times (10msec/100 msec/500 msec) for each output individually (→ section 2.3). If the triggering event lasts longer than the minimum pulse set, the output remains active until the event has disappeared again.

The digital output is potentially isolated via optocouplers from the following.

- **S5 bus**
- **Digital inputs**
- **5.2 V encoder supply**

The digital output is supplied by the 24 V direct voltage fed by X3. A P switch is used as the output driver. The digital output is short circuit proof and protected against overload.

The digital outputs are disabled after startup of the IP 281. They are enabled by control register3.

The BASP signal is active during an interference, and during startup and stop of the PLC. The BASP signal is used for the S5 as an "EMERGENCY OFF" for the digital outputs. Since certain applications require that the outputs not be switched off when an error occurs, the IP 281 offers the capability of switching off the BASP function for both digital outputs together (→ section 2.3). Remember that, in such situations, the digital outputs are nolonger protected by the safety system of the SIMATIC S5.

Warning

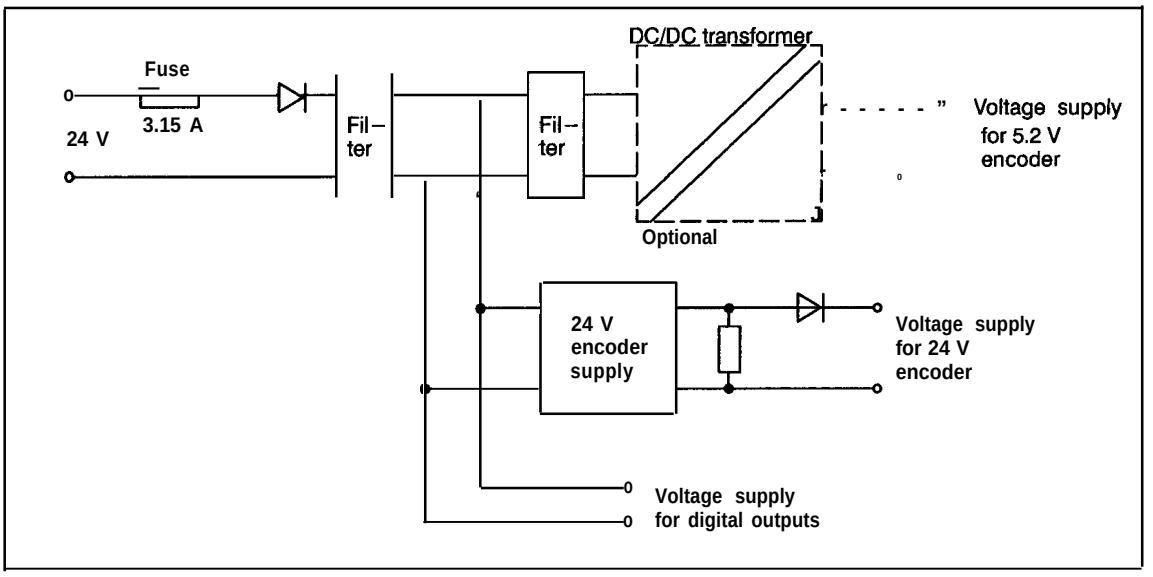
When the BASP function is switched off, other suitable measures must be provided to ensure that persons and systems are not endangered when the outputs are not switched on.

1.4.4 Voltage Supply for Incremental Encoders

The module is available in the two configurations.

– With voltage supply for 24 V encoder
– With voltage supplies for 24 V encoder and 5.2 V encoder

☞ **The voltage supply for the 5.2 V encoder cannot be retrofitted.**



Both encoder supplies are short circuit proof and protected against overload. A diode is used to protect against feedback for the 24 V encoder supply.

The supplies for the encoder and the digital outputs are generated from the externally fed 24 V supply. A diode is used to protect the module against polarity reversal of the 24 V supply. A fuse is located on the input of the 24 V supply. The fuse is not triggered unless errors are present on the module. The fuse is not triggered when an output or the encoder supply short circuits since short circuit proof drivers are used for these outputs.

The 5.2 V supply is potentially isolated from the external, 24 V supply.

The voltage supplies for the encoders are available on the encoder interfaces X5/X7 (→ section 1 .3.3).

1.5 Communication with the SIMATIC S5

The IP 281 is an intelligent 1/0 module. It can be addressed in the following areas.

- Analog 1/0 area (P area), addresses F080H to FOFFH ≙ 128 to 255
- Expanded 1/0 area (Q area), addresses F1OOH to F1FFH ≙ 0 to 255

The module occupies 8 bytes of input/output address area. The addresses for input and output are identical and can be selected as desired in the above stated address areas. The basic address is set with DIL switch S1 (→ section 2.2). The basic address is always a multiple of eight.

Decoding of the addresses depends on the PLC. PLCS5–115U evaluates addresses up to 8 bits; PLCs S5–135U and S5–155U evaluate 12–bit addresses. The type of decoding must beset with the DIL switch (→ section 2.2) based on the PLC in which the IP 281 is used.

The module is accessed with simple transfer commands (LPB, LPW, LQB, LQW, TPY, TPW, TQB, TQW) given by the S5 CPU.

The IP 281 can be used in the individual PLCs with the CPUs listed below.

PLCS5–115U
- CPUs 941A to 944A
- CPUs 941 B to 944B

PLCS5–11 5H
- CPU 942H

PLC S5–135U
- CPU 922
- CPU 928A
- CPU 928B

PLC S5–155U (in S5–150U mode without “interrupt”/S5-155U mode, full operation)
- CPU 922
- CPU 928A/CPU 928B
- CPU 946/947

PLC S5–155H (without “interrupt”)
- CPU 946R/947R

PLCS5–115U is not equipped with an expanded I/O area.

Due to internal synchronization, the IP 281 increases the command run times by approximately 0.4 µsec per byte accessed.

The IP 281 can trigger interrupt processing on the S5 CPU (→ section 4).

2 Hardware Settings

2 Hardware Settings

2.1 Location of the Setting Elements

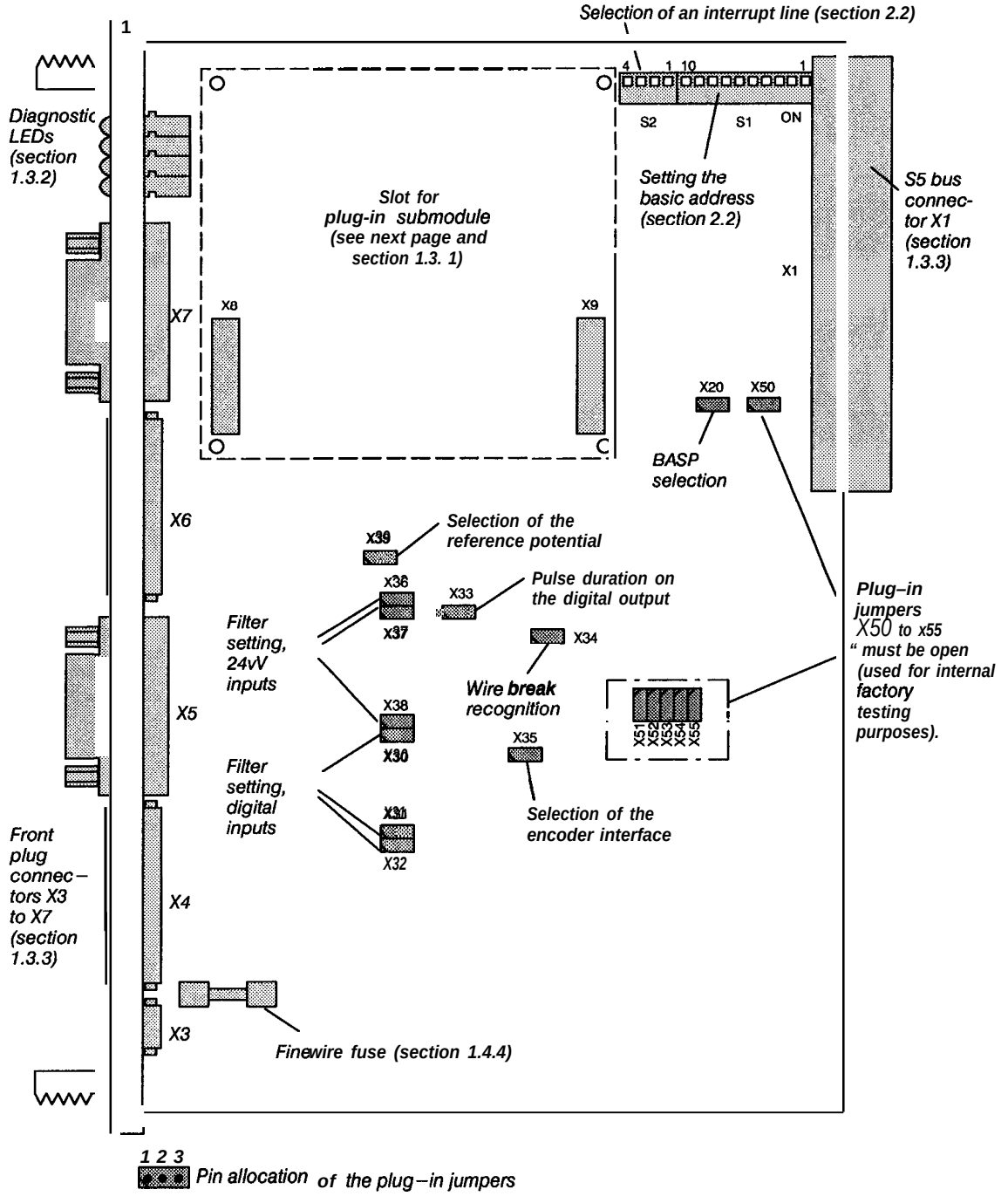


Figure 2.1: Setting elements on the basic module

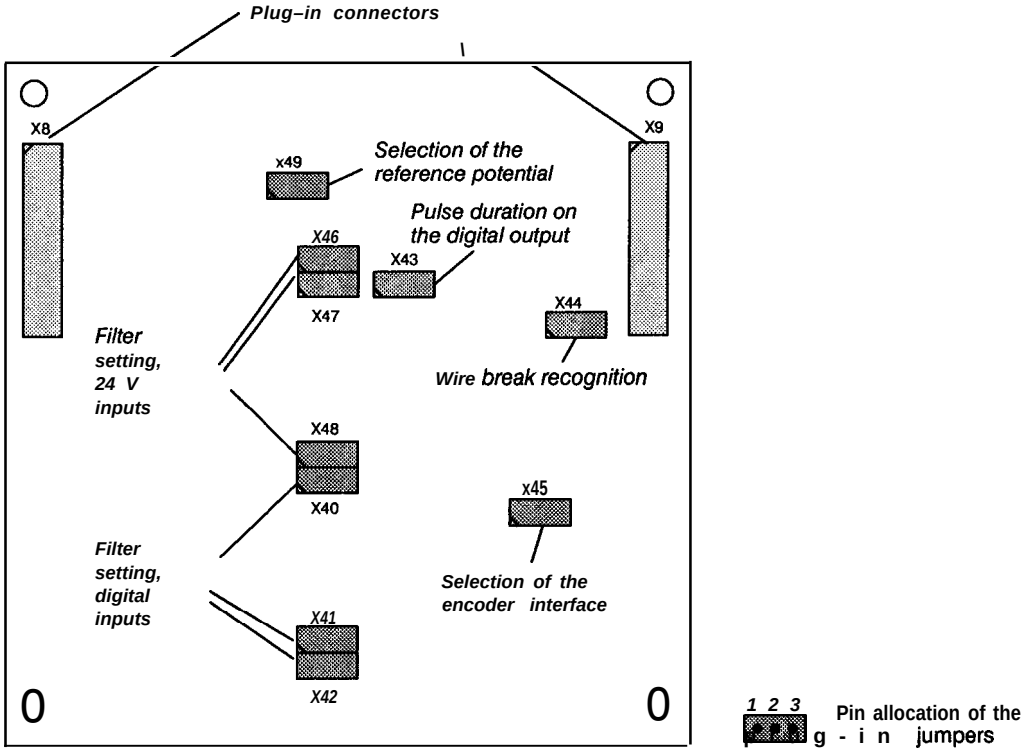


Figure 2.2: Setting elements on the plug-in submodule

Before the plug–in jumpers can be set, the cover must be removed by unscrewing four screws (→ figure 1.1). If settings on the plug–in submodule are to be adjusted, it must first be removed from the basic module by hand.

Caution

To avoid damaging the module, do not use tools to remove the plug–in submodule.

After setting the plug–in jumpers, install the plug–in submodule again (→ section 1.3.1). Replace the cover and screw down.

2.2 Setting the DIL Switches

Address decoding and basic address

DIL switch S1 is used to set the basic address and select the address decoding.

The register address for read and write accesses of the individual registers is generated from the set basic address and the offset (-t section 3).

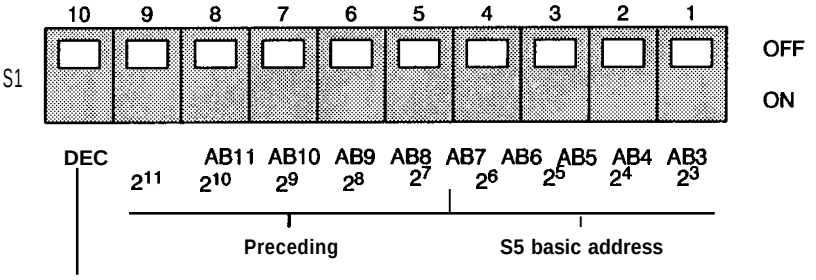
The module occupies the address area from basic address +0 to basic address +7 in both the input and output area.

Switches S1.1 to S1.9 are used to set address bits AB3 to AB11.

The address is always a multiple of 8 since address bits AB0 to AB2 are fixed.

Switch S1 .10 is used to switch between simple address decoding (8 bits) and expanded address coding (12 bits).

Status on delivery: all switches "OFF"



Selection of address decoding
OFF= Simple address decoding
ON = Expanded address decoding

Setting the basic address for PLC S5–115U and PLC S5–115H

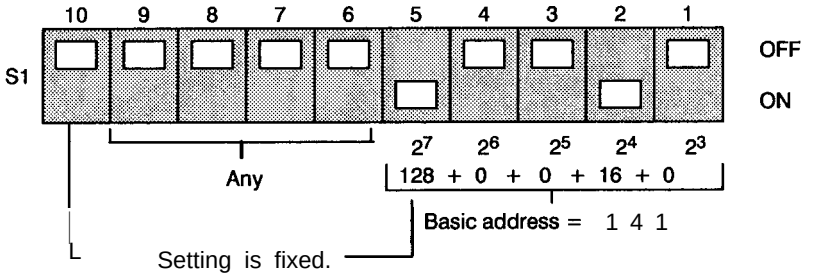
PLCSS5–11 5U andS5–115H evaluate only address bits AB0 to AB7. Set DIL switch S1 as shown below.

Switch	Meaning	Setting
S1 .1 to S1.5	AB3 to AB7	Basic address
S1 .6 to S1 .9	Disregard	Any
S1.10	12/8-bit decoding	OFF

Since the IP 281 is always addressed in the analog 1/0 area when used with PLCS5–115U and PLCS5–115H, possible basic addresses are 80H (128) to F8H (248).

Example:

Basic address of the module: 090H ≙ address 144 ≙ PY144 toPY151



Setting the basic address for PLCS5-135U, PLC S5-155U PLC S5-155H

PLCS S5-135U, S5-155U and S5-155H evaluate address bitsAB11 to ABO. Set DIL switch S1 as shown below.

Switch	Meaning	Setting
S1 .1 to S1.5	AB3 to AB7	Basic address
S1 .6	Selection of area	Areas OFF = P area ON = Q area
SI.7 to S1.9	AB9toAB11	OFF
S1.10	12/8-bit decoding	ON

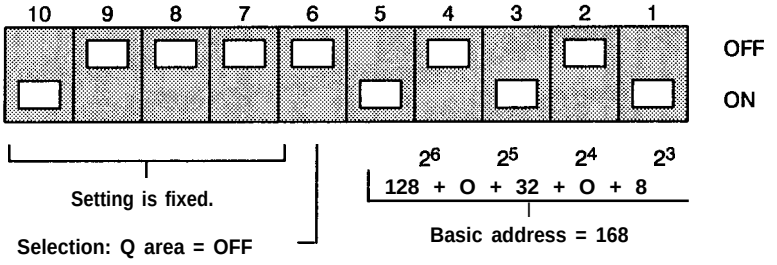
The module can be operated in both the analog 1/0 area (P area) and the expanded 1/0 area (Q area) when used withPLCSS5-135U, S5- 155U and S5-155H. Available basic addresses are listed below.

P area: 80H (128) to F8H (248), addresses F080 to FOF8
Q area: OH (0) to F8H (248), addresses F1OO to F1F8

The Q area can only be used in expansion units.

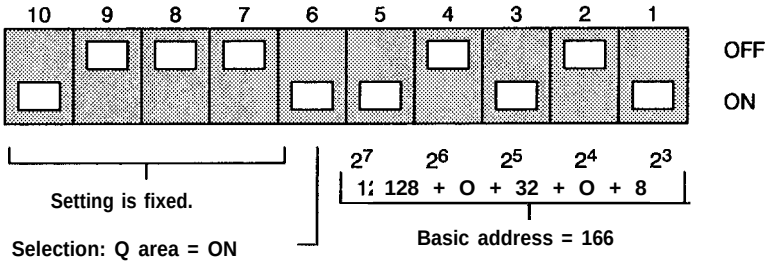
1st example: **P area**

Basic address of the module: **A8H ≙ address 168 ≙ PY168 toPY175**



2nd example: **Q area**

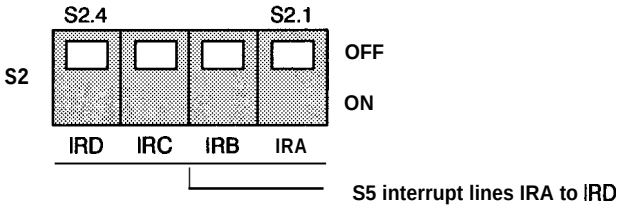
Basic address of the module: **A8H≙ address 168 ≙ OYB168 toOY175**



Selecting the interrupt line

DIL switch S2 is used to select the S5 interrupt line which triggers the interrupt on the PLC (→ section 4).

Only one switch may be set to ON.



OFF: No interrupt
ON: Interrupt via the applicable line

Status on delivery: all switches OFF

2.3 Setting the Plug-In Jumpers

Location of the plug–in jumpers

The design of both counters is identical (i.e., the location of the components on the module and the plug–in submodule are geometrically identical). This makes it easier to set the plug –in jumpers.

The settings are made with plug–in jumpers X20, X30 to X39 (basic module) and X40 to X49 (plug–in submodule).

Plug–in jumper X20 affects both counters.

Counter 1 is set with X30to X39; counter 2 is set with X40 to X49. Plug–in jumpers with the same relative position have the same function.

☞ Plug-in jumpers X50 to X55 are used for internal factory testing purposes. Leave them open.

BASP function for digital outputs

Plug–in jumper X20 can be used to switch the EMERGENCY OFF function (BASP) on or off for both counters together (→ section 1.4.3).

Jumper X20	Effect
O O O 1 2 3	Not permitted
O—O O 1 2 3	The digital outputs are switched off when the BASP signal is active.
0 0———0 1 2 3	The digital outputs are not switched off when the BASP signal is active.

Warning

When the plug–in jumper is inserted on 2–3, the digital output is not switched off even when an error occurs. This can lead to destruction of system components and injury to persons.

Status on Delivery	
Jumper X20	Effect
O—O O 1 2 3	The digital outputs are switched off when the BASP signal is active.

Setting the input filter

The 24 V counting inputs and the digital inputs are equipped with RC filter for the suppression of interferences. These filters can be set individually to various limit frequencies.

Input signals and interferences whose frequencies are above the limit frequency are filtered out.

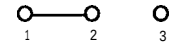
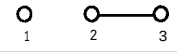
Digital inputs

Plug–in jumpers X30 to X32 and X40 to X42 are used to set the maximum signal frequency for the digital inputs.

Allocation of the Plug-In Jumpere

Function	Counter 1	Counter 2
Gate start input	X30	X40
Gate stop input	X31	X41
Set input	X32	X42

Setting the Limit Frequency

Jumpers X30 to X32 X40 to X42	Maximum signal frequency
0 0 0 1 2 3	250 kHz
 1 2 3	25 kHz
 1 2 3	100 Hz

Status on Delivery

Jumpers X30 to X32 X40 to X42	Maximum signal frequency
 1 2 3*	250 kHz

*** Plug–in jumper premounted on pin 3**

24 V encoder inputs

Plug–in jumpers X36 to X38/X46 to X48 are used to set the maximum counting frequencies for the 24 V encoder inputs.

Allocation of the Plug-In Jumpers		
Function	Counter 1	Counter 2
Track A	X36	X46
Track B	x37	x47
Zero marking pulse	X38	X46

Setting the Limit Frequencies	
Jumpers X36 to X38 X46 to X46	Maximum counting frequency
0 0 0 1 2 3	250 kHz
O—O O 1 2 3	50 kHz
O O—O 1 2 3	1 kHz

Status on Delivery	
Jumpers X36 to X38 X46 to X48	Maximum counting frequency
0 0 O 1 2 3*	250 kHz

*** Plug–in jumper premounted on pin 3**

Minimum pulse duration for digital outputs

Plug– in jumpers X33/X43 are used to set the minimum pulse duration for the digital outputs. This is the minimum time a digital output remains active after activation.

Allocation of the Plug–In Jumpers	
x33	Minimum pulse duration, digital output 1
x43	Minimum pulse duration, digital output 2

Setting the Minimum Pulse Duration	
Jumpers X33/X43	Minimum pulse duration
0 0 0 1 2 3	Approx. 500 msec
O—O O 1 2 3	Approx. 100 msec
O O—O 1 2 3	Approx. 10 msec

Status on Delivery	
Jumpers X33/X43	Minimum pulse duration
0 0 O 1 2 3*	Approx. 500 msec

*** Plug–in jumper premounted on pin 3**

Wire break recognition

Plug–in jumpers X34/X44 are used to switch the wire break recognition on or off for the individual counters (→ section 1.4.1.2).

Allocation of the Plug–In Jumpers	
x34	Wire break recognition for counter 1
x44	Wire break recognition for counter 2

Setting the Wire Break Recognition	
X341X44	Meaning
0 0 0 1 2 3	Not permitted
O—O O 1 2 3	Wire break recognition switched off
O O—O 1 2 3	Wire break recognition switched on

The wire break recognition can only be used during operation of the RS 422 interface.

The wire break recognition must be switched off when the counter is operated with the 24 V encoder interface.

Status on Delivery	
x34/X44	Meaning
O—O O 1 2 3	Wire break recognition switched off

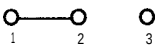
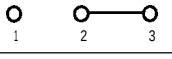
Selecting the encoder interface (RS 422/24 V)

Plug– in jumpers X35/X45 are used to select the encoder interface (24 V encoder or 5 V encoder in accordance with RS 422) for the respective counter.

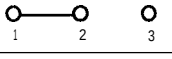
Allocation of the Plug-In Jumpers

x35	Interface selection, counter 1
x45	Interface selection, counter 2

Interface Selection

X351X45	Selection
0 0 0 1 2 3	Not permitted
 1 2 3	For 24 V encoder
 1 2 3	For RS 422 encoder

Status on Delivery

X351X45	Selection
 1 2 3	24 V encoder selected

Caution

If you switch the encoder interface, you must also switch the reference potential for plug connector X5/X7 otherwise the potential isolation is removed (→ following page and section

Selecting the reference potential for the encoder

Plug– in jumpers *X39/X49* **are used to set the reference potential for the encoders.**

The encoder interfaces can be operated as either 24 V interfaces or 5 V (RS422). If the interface is adjusted, the corresponding reference potential must beset to prevent the potential isolation between the 24 V area and the 5 V area from being **removed.**

Allocation of the Plug–In Jumpers	
x39	Reference potential for counter 1 (X5)
x49	Reference potential for counter 2 (X7)

Reference Potential Selection		
X391X49	Meaning	Use
0 0 0 (1 2 3)	Not permitted	
o—o o (1 2 3)	0 V_{ext24} is connected to pin 7 24 V encoder (X51X7).	
o o—o (1 2 3)	MI from S5 bus is con– nected to pin 7 (X5/X7).	RS 422 encoder

Caution

Incorrectly inserted jumpers can lead to interferences caused by grounding loops. In addition, the potential isolation of the 24 V encoder inputs to the S5 is lost.

Status on Delivery		
x39/x49	Meaning	Use
o—o o (1 2 3)	O V_{ext24} is connected to pin 7 (X5/X7).	24 V encoder

3 Software Settings

3 Software Settings

3.1 General

3.1.1 Definition of the Registers

Select register	**Used as an addressing aid for the selection of a register set**
Global registers	**Registers containing information for both counters. Global registers are control register 3, status register 3 and the interrupt information register.**
Control register 3	**The general module functions are set here.**
Status register 3	**Indicates the status of the module**
Interrupt information register	**Information concerning the interrupts triggered is stored here.**
Specific registers	**Registers which are available for each individual counter**
Control registers 1 and 2	**The control of the respective counter is specified here.**
Parameter registers 1 and 2	**Counting mode, operating mode, counting pulse evaluation, gate control, input behavior of the counting inputs, method of operation of the digtal output, and synchronization are parameterized here for the respective counter.**
Interrupt enable registers 1 and 2	**The interrupt sources which will trigger interrupts are set here for the respective counter.**
Load registers 1 and 2	**A start value can be entered here for the respective counter.**
Interrupt registers 1 and 2	**An interrupt value can be entered here for the respective counter.**
Counter value registers	**The respective counter uses these registers as intermediate storage to allow the contents of the counter to be read out.**

3.1.2 Selecting the Registers

Principle of selection

The registers of the IP 281 are divided into sets of registers for read and write accesses. Before a register can be accessed, the corresponding register set must be set with the select register (→ section 3.2).

The desired register can then be read or written via the register address.

Register address

The register address consists of the following components.

- The basic address set (via DIL switch S1 for the IP 281) (-t sect. 2.2) and
– The offset in the respective register set (-t section 3.2)

Register address = basic address + offset

☞ **Anerror message is notgenerated when an address is accessed which is not assigned to a register. The access is acknowledged with $\overline{RDY}$.**

3.1.3 Reading and Writing the Registers

The registers are read or written via the programmable controller using S5 commands. The permissible commands are found in section 3.10.

Writing the registers

The use of word commands is recommended for registers which are longer than one byte (load, interrupt and parameter registers) .
(Exception: CPU 944, only byte commands are permitted.)

The IP 281 does not accept the values until the last byte is written (access to the byte with the highest offset address of the corresponding register). It is mandatory that the sequence from the lowest address to the highest address (or from the highest byte to the lowest byte) be adhered to to prevent the registers from accepting erroneous values.

Reading the registers

The contents of the registers are stored intermediately during read accesses. Intermediate storage is performed when the lowest address/ highest byte of the register to be read is accessed.

☞ The entire register must be read to obtain a valid value.

No other register can be read until the entire register has been read. As soon another readable register is accessed, the new contents are intermediately stored and the old value is lost.

Example:

Read byte 3 of CVR1	→ Value is stored.
Read byte 2 of CVR1	-t Value of CVR1 is still valid.
Read byte 1 of CVR1	→ Value of CVR1 is still valid.
Read byte O of CVR1	→ Read CVR1 is concluded.
Read byte 3 of CVR1	-t Value is stored.
Read byte 2 of CVR1	→ Value of CVR1 is still valid.
Read STATUS1	-t Value of CVR1 is lost. STATUS1 is valid.
Read byte 1 of CVR1	→ Value is invalid.

It is recommended that registers which are longer than one byte (IIR and CVR) be read with word commands,
(Exception: CPU 944: Only byte commands are permitted.)

Access via byte commands

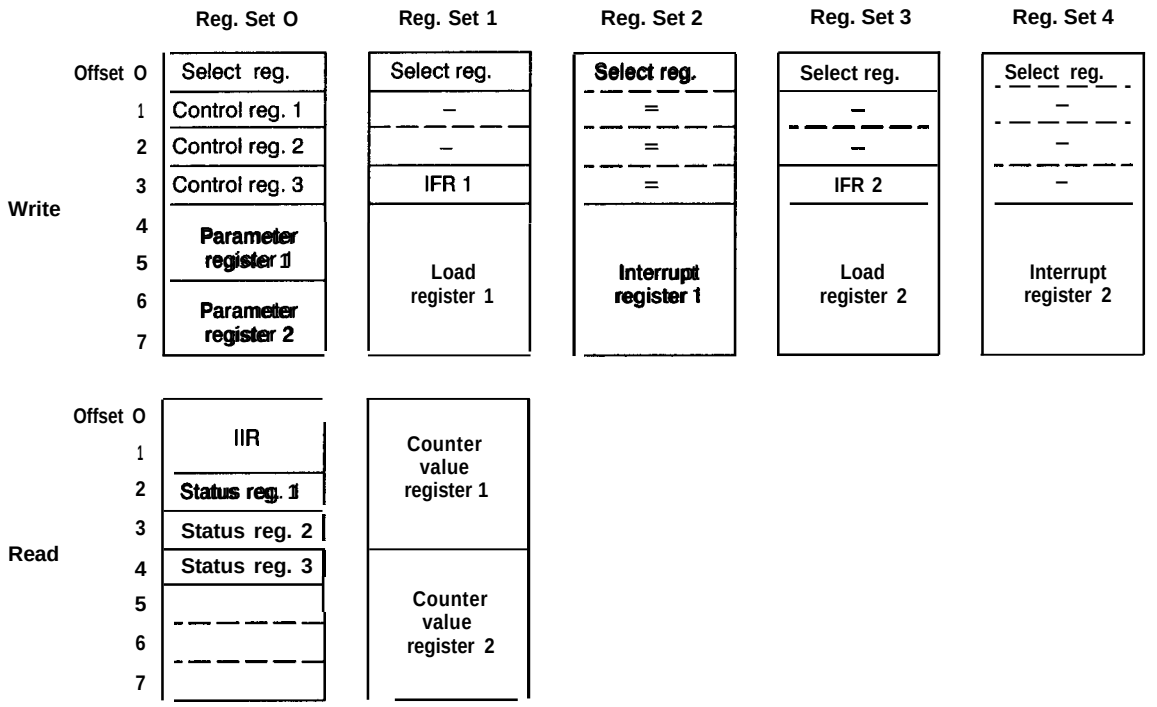
CPU 944 inPLCS5–115U does not permit word commands. When byte command addressing is used, the access sequence shown below must be adhered to.

– Sequence of byte addresses for 2–byte registers:
  1st byte address: n
  2nd byte address: n+1

– Sequence of byte addresses for 4–byte registers:
  1st byte address: n
  2nd byte address: n+1
  3rd byte address: n+2
  4th byte address: n+3

3.2 Select Register

A register set is selected to address the registers for the IP 281. The allocation of the registers to the sets is shown in the following figure.



When a counter is operated in 16–bit mode, only byte O and byte 1 are used when 4–byte registers are used (i.e., the offset addresses for the load, interrupt and counter status registers are incremented by 2).

A register set is selected in the select register. The register set remains selected until a new value is entered in the select register.

Register Set	Contents of the Select Register
0	OH
1	IH
2	2H
3	3H
4	4H

The ERROR LED goes on for all other entries. The select register is **always** addressed with offset address O regardless of the register set selected. The select register can-not be read back.

Caution

When a set is selected in the interrupt program (e.g., to read out the IIR), this call causes the current set selection in the cyclic program to be lost. This makes it necessary to save the selected set for all read and write procedures for which the interrupts are not disabled IA/RA). The selected set address must then be saved in a selected memory location and reloaded at the end of the interrupt program.

3.3 Load Register

Each counter is equipped with a load register. A defined value (load value), which is used to load the counter for certain events, can be stored in this register.

The load register can be written at all times (except with operating mode TCLR). It cannot be read back.

The load value is entered as a 16–bit or 32– bit value in the register (depending on the counting mode set).

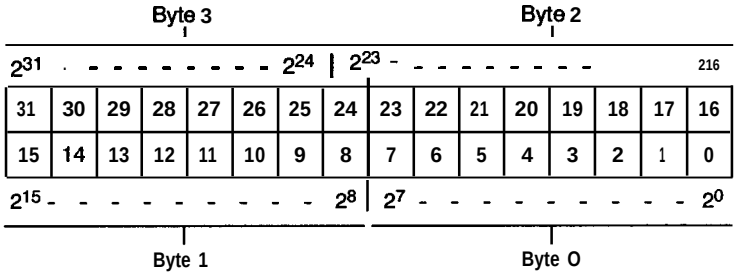
The following methods can be used to enter the values in the load register.

– Writing the load register from the PLC
– Transfer when in TCLR operating mode (→ section 6.4.3)

☞ Load register 2cannot rewritten from the PLC in operating mode TCLR.

Contents of the register after RESET: O

Load register 1/2



For counting modes 1 and 3 (16–bit):

Offset 6	Byte 1
7	Byte 0

For counting modes 2 and 4 (32–bit):

Offset 4	Byte 3
5	Byte 2
6	Byte 1
7	Byte 0

Example: **Writing load register 1 (32 bits)**

Prerequisites:
- **Load value is in DB 20.**
  DW 10 (high word, bits 31 to 16)
  DW 11 (low word, bits 15to O)
- **Counting mode 2 or 4 is selected (i.e., offset= 4).**
- **Basic address of the module: 136**

With word commands:

```
L  KH  1
T  PY  136     }   Set register set 1 for access to the load register
C  DB  20          Call data block 20
L  DW  10      \
T  PW  140')   |
L  DW  11      |   Transfer load value from DB to the IP 281
T  PW  142*)   /
```

With byte commands:

```
L  KH  1
T  PY  136     }   Set register set 1
C  DB  20          Call data block 20
L  DL  10      \
T  PY  140'    |
L  DR  10      |
T  PY  141 *   |   Transfer load value from DB to IP 281
L  DL  11      |
T  PY  142*    |
L  DR  11      |
T  PY  143*    /
```

Example: **Writing load register 1 (16 bits)**

Prerequisites:
- **Load value is in DB 20.**
  DW 11 (bits 15 to O)
- **Counting mode 1 or3 is selected (i.e., offset= 6).**
- **Basic address of the module: 136**

With word commands:

```
L  KH  1
T  PY  136     }   Set register set 1
C  DB  20          Call data block 20
L  DW  11          Transfer load value from DB to IP 281
T  PW  142'    }
```

With byte commands:

```
L  KH  1
T  PY  136     }   Set register set 1
C  DB  20          Call data block 20
L  DL  11
T  PY  142*        Transfer load value from DB to IP 281
L  DR  11
T  PY  143*    }
```

*** Register address = basic address + offset**

3.4 Interrupt Register

Each counter is equipped with an interrupt register. A defined value (interrupt value) can be stored in this register and continually compared to the current counting value (hardware comparator). A digital output can be activated (→ section 6.7) or an interrupt generated (→ section 4.4) when the counting value reaches the interrupt value.

A digital output must be enabled in control register 3 (→ section 3.9) before it can be activated. An interrupt must be enabled in the interrupt enable register (→ sections 3.6 and 4.4) before it can be generated.

The interrupt register can be written at all times. It cannot be read back.

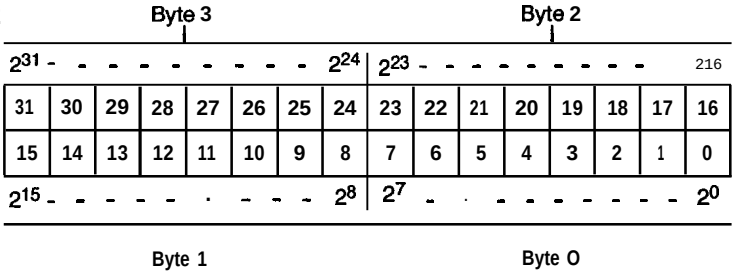
The following methods can be used to enter the interrupt value in the interrupt register.

– Writing the interrupt register via the S5 from the PLC
– Transfer in TCAR operating mode (→ section 6.4.2)

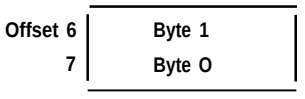
interrupt register 2cannot rewritten from the PLC in operating mode TCAR.

Contents of the interrupt register after RESET: 0

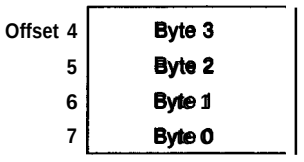
Interrupt register 1/2



For counting modes 1 and 3 (16–bit):



for counting modes 2 and 4 (32–bit):



Example: **Writing interrupt register 1 (32 bits)**

Prerequisites:
- **Interrupt value is in DB 20.**
  DW 10 (high word, bits 31 to 16)
  DW 11 (low word, bits 15 to O)
- **Counting mode 2 or 4 is selected (i.e., offset= 4).**
- **Basic address of the module: 136**

With word commands:

```
L   KH   2     } Set register set 2 for access to the interrupt
T   PY  136    } register
C   DB   20      Call data block 20
L   DW   10    \
T   PW  140*    } Transfer interrupt value from DB to IP 281
L   DW   11     }
T   PW  142'   /
```

With byte commands:

```
L   KH   2
T   PY  136    }  Set register set 2
C   DB   20      Call data block 20
L   DL   10    \
T   PY  140'    |
L   DR   10     |
T   PY  141 *   } Transfer interrupt value from DB to IP 281
L   DL   11     |
T   PY  142*    |
L   DR   11     |
T   PY  143'   /
```

Example: **Writing interrupt register 1 (16 bits)**

Prerequisites:
- **Interrupt value is in DB 20.**
  DW 11 (bits 15 to O)
- **Counting mode 1 or 3 is selected (i.e., offset= 6).**
- **Basic address of the module: 136**

With word commands:

```
L   KH   2     } Set register set 2
T   PY  136    }
C   DB   20      Call data block 20
L   DW   11
T   PW  142*   }  Transfer interrupt value from DB to IP 281
```

With byte commands:

```
L   KH   2
T   PY  136    }  Set register set 2
C   DB   20      Call data block 20
L   DL   11
T   PY  142*    Transfer interrupt value from DB to IP 281
L   DR   11
T   PY  143*   }
```

*** Register address = basic address + offset**

3.5 Counter Value Register (CVR)

The counter value register (CVR) is used to read out the counter status. It contains either 16 bits (modes 1 and 3) or 32 bits (modes 2 and 4) depending on the counting mode set.

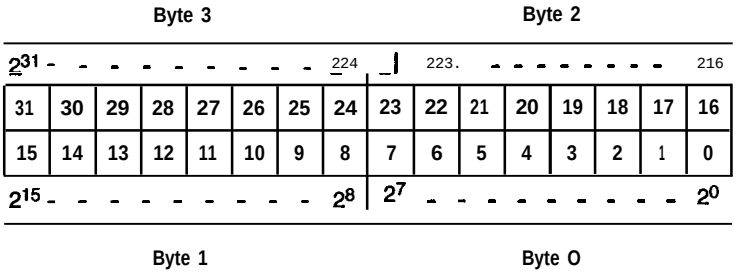
The CVR can be read by the S5 at all times. The counter values can be read asynchronously (each counter individually) or synchronously (counter 1 and counter2 simultaneously (→ section 6.5.3)).

With high–byte addressing (byte 1 for 16 bits; byte 3 for 32 bits), the counting value is interme–diately stored in the CVR until the lowest byte (byte O) is addressed and output (→ section 3.1.3).

Each counter is equipped with a CVR register.

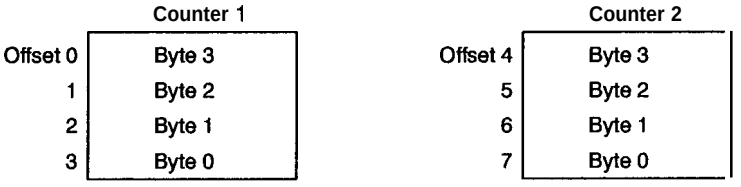
– CVR 1 for counter 1
– CVR 2 for counter 2

Counter value register



For counting modes 1 and 3 (16–bit):

For counting modes 2 and 4 (32–bit):



Example: **Reading CVR 1 (32 bits)**

Prerequisites:
- **Memory for counter is in DB 20.**
  DW 20 (high word, bits 31 to 16)
  DW 21 (low word, bits 15to O)
- **Counting mode 2 or 4 is selected (i.e., offset= O).**
- **Basic address of the module: 136**

With word commands:

```
L  KH  1
T  PY  136     } Set register set 1 for access to the counter value register
C  DB  20      Call data block 20
L  PW  136*    \
T  DW  20      |
L  PW  138*    | Read counter value and store in DW 20/DW 21.
T  DW  21      /
```

With byte commands:

```
L  KH  1
T  PY  136     } Set register set 1
C  DB  20      Call data block 20
L  PY  136*    \
T  DL  20      |
L  PY  137*    |
T  DR  20      |
L  PY  138'    | Read counter value byte by byte and store
T  DL  21      | in DW 20/DW 21
L  PY  139*    |
T  DR  21      )
```

Example: **Reading CVR 1 (16 bits)**

Prerequisites:
- **Memory for counter is in DB 20.**
  DW 21 (bits 15 to O)
- **Counting mode 1 or 3 is selected (i.e., offset= 2).**
- **Basic address of the module: 136**

With word commands:

```
L  KH  1       }
T  PY  136     } Set register set 1
C  DB  20      Call data block 20
L  PW  138*    Read counter value and store in DW 21
T  DW  21      }
```

With byte commands:

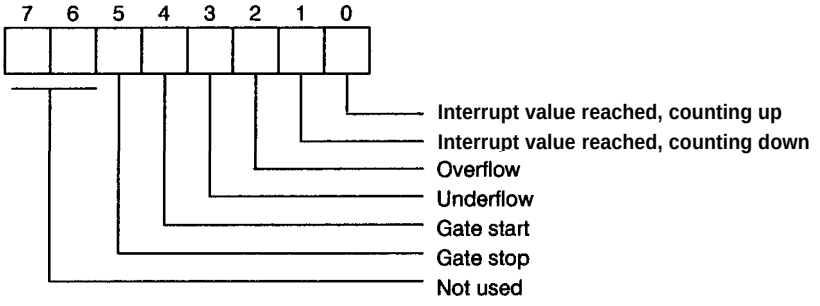
```
L  KH  1       }
T  PY  136     } Set register set 1
C  DB  20      Call data block 20
L  PY  138*
T  DL  21      Read counter value byte by byte and store
L  PY  139'    in DW 21
T  DR  21      }
```

*** Register address = basic address + offset**

3.6 Interrupt Enable Register (IFR)

Each counter is equipped with an interrupt enable register with which the interrupt sources can be enabled or disabled (-t section 4.4).

Allocation of the IFR



The interrupt is disabled when a "O" is entered; the interrupt is enabled when a"1" is entered.

RESET status

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

All interrupts are disabled.

Example: **Setting the IFR for counter 2**

Basic address of the module: 136

```
L   KH   3          Set register set 3 for access of the IFR for
T  PY  136      }   counter 2
L KMOOO11OOO       Enable counter underflow interrupt and gate
T  PY  139      }   start interrupt
```

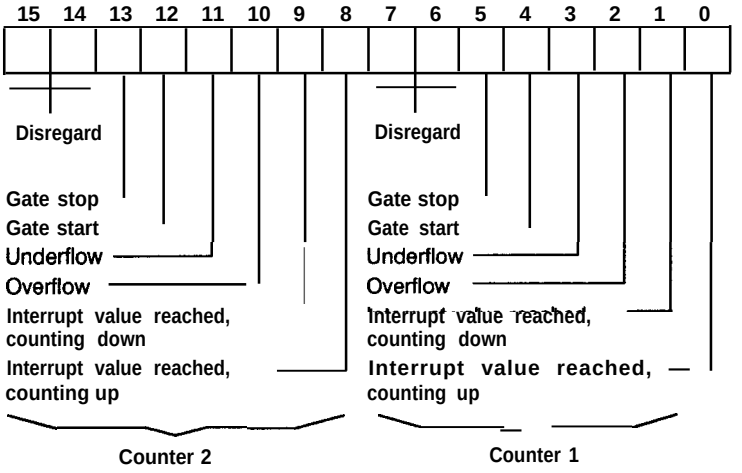
7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0

An interrupt is triggered for "counter underflow" and "gate start"; the other interrupts are suppressed.

3.7 Interrupt Information Register (IIR)

The interrupt information register is a 2–byte register in which the causes of an interrupt are entered. There is one common IIR for both counters.

Allocation of the IIR



The cause of an interrupt is identified by a set bit.

RESET status All bits: 0

Reading the IIR

☞ The IIR must be read during interrupt processing. This read access resets the S5 interrupt and the IIR.

The S5 can determine the cause of an interrupt by reading the IIR.

Offset 0	Byte 1
1	Byte 0

The entire IIR must always be read (2 bytes). Use of the word commands LPW/LOW is recommended for this purpose.

☞ Word commands cannot be used with CPU 944. Byte commands must be used for the access.

During the access to the IIR with byte commands, the interrupt must be disabled with the S5 command 1A and enabled again after the access with the S5 command RA.

New interrupts which occur while the IIR is being read are stored intermediately. These are entered in the IIR after the read access, and another interrupt is triggered.

Example: **Reading the IIR**

Prerequisites:
- **Memory for IIR value is DW 30 of DB 20.**
- **Basic address of the module: 136**

With word commands:

```
L  KH  O        Set register set O for the access to the IIR register
T  PY  136   }
C  DB  20       Call data block 20
L  PW  136*     Store IIR in DW 30
T  DW  30    }
```

With byte commands:

```
L  KH  O        Set register set O
T  PY  136   }
C  DB  20       Call data block 20
IA              Disable interrupts
L  PY  136*
T  DL  30
L  PY  137'     Store IIR in DW 30
T  DR  30    }
RA              Enable interrupts
```

*** Register address = basic address + offset**

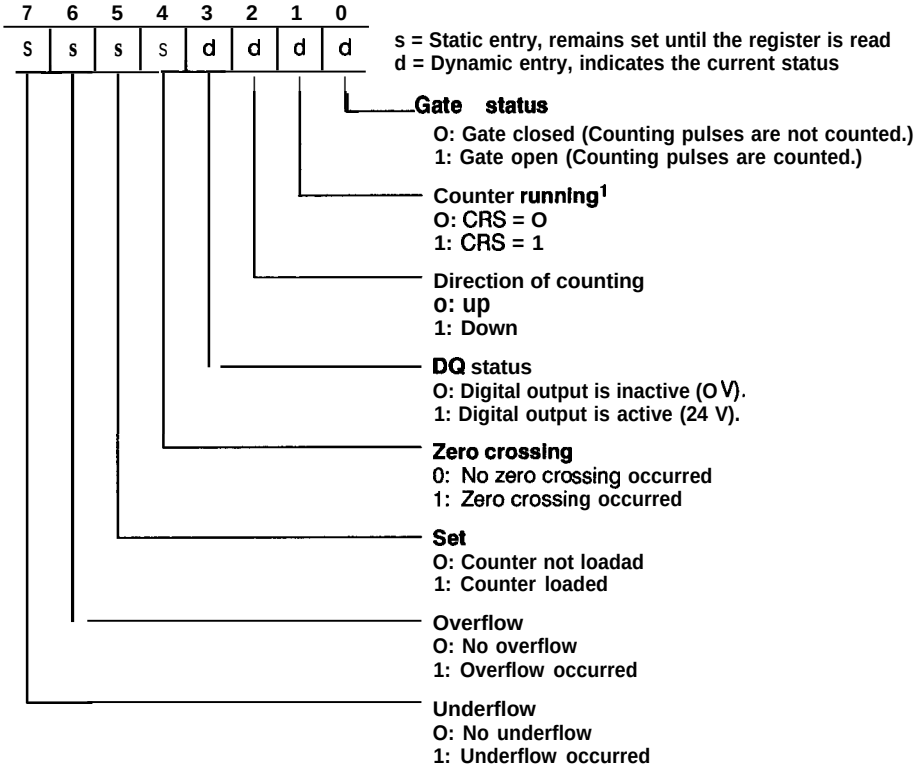
3.8 Status Register

There are three status registers containing information about the current status of the respective counter (status register 1 or 2) or the module (status register 3) (→ section 5.4).

Each status register contains 1 byte and can only be read.

The static entries are reset when the status register is read.

Contents of Status Register 1 /2



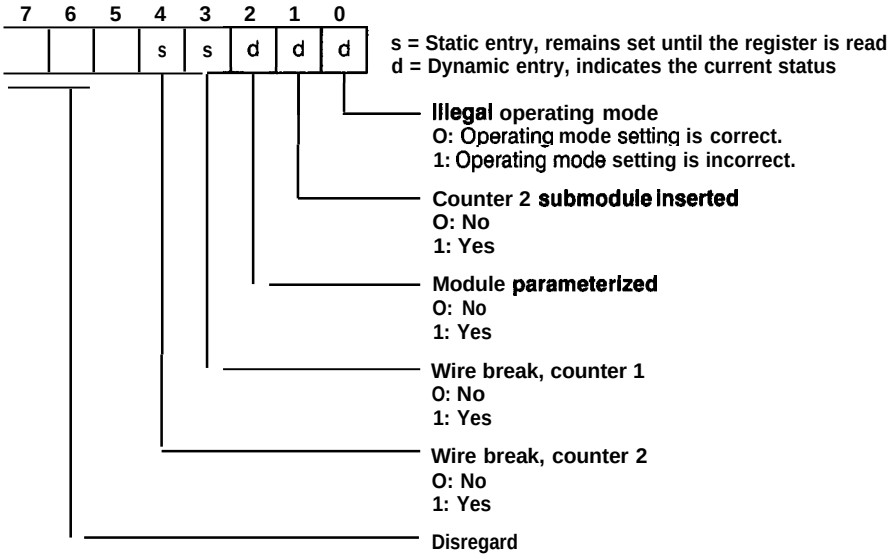
1The CRS bit (last position of the respective counter) is entered in the status register.

RESET Status

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Offset		
	2	Status register 1
	3	Status register 2

Contents of Status Register 3



RESET Status

7	6	5	4	3	2	1	0
			①	①	o	②	o

① Depending on whether a wire break has occurred
1 : Wire break
O:NO wire break

② 1: Counter 2 submodule inserted
O: Counter 2 submodule not inserted

Offset 4 | Status register 3 |

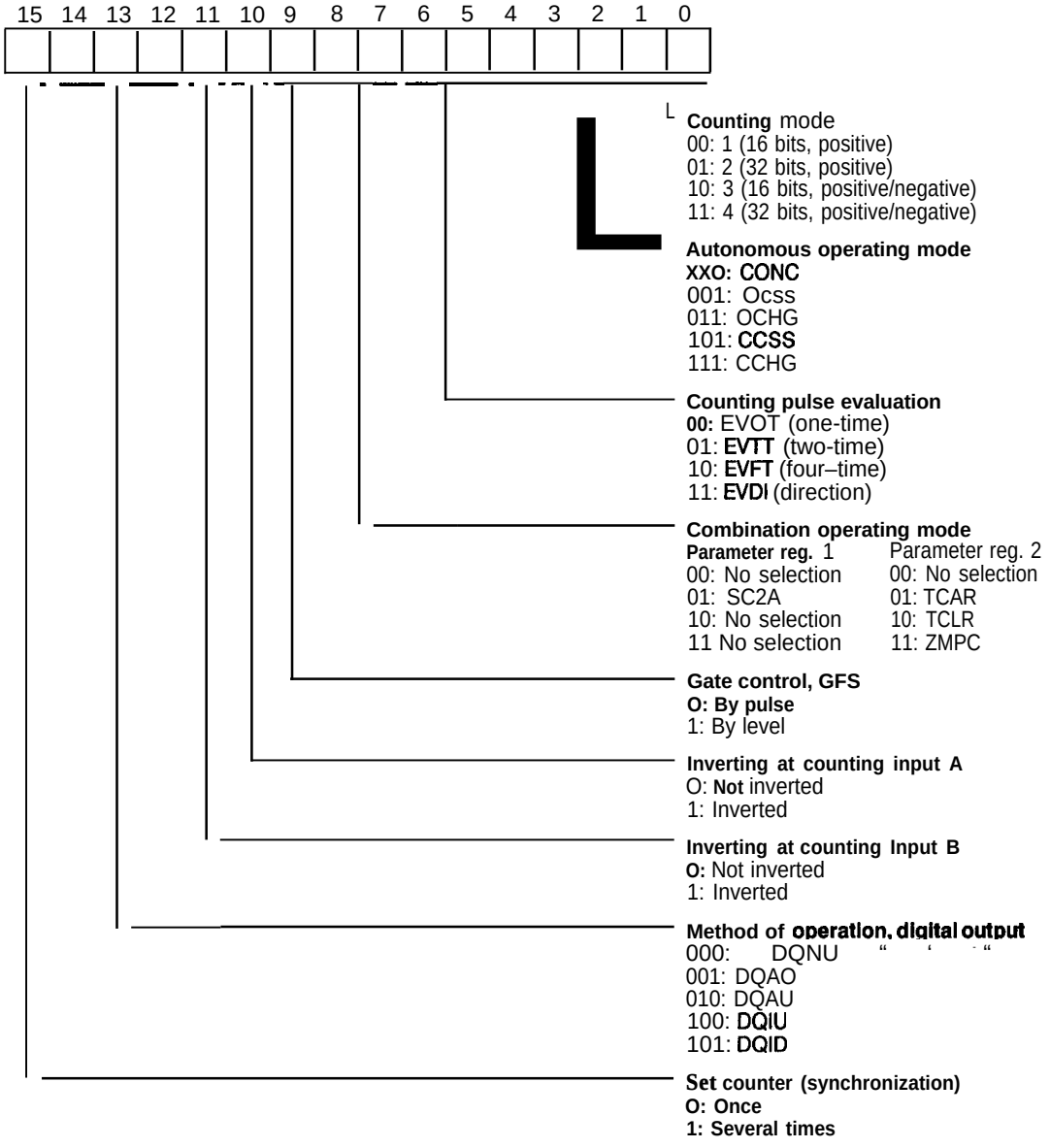
3.9 Parameter Registers and Control Registers

The method of operation of the counters is set in the parameter registers and the control registers. Each counter is equipped with one parameter register (1 or 2) and one control register (1 or 2). Settings affecting both counters are made in global control register 3.

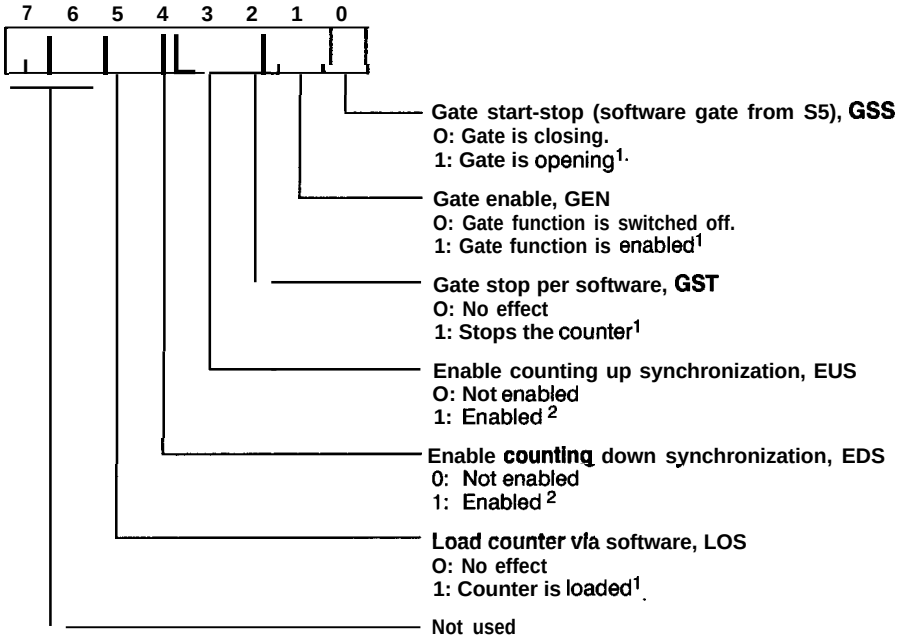
It is recommended thatthe 16-bit parameter registers rewritten with word commands (exception: PLC S5–115U, CPU 944A/B).

Allocation of Parameter Registers 1/2

Except for bits 7 and 8, the allocation of parameter registers 1 and 2 is identical. See section 6 for the operating modes and functions.



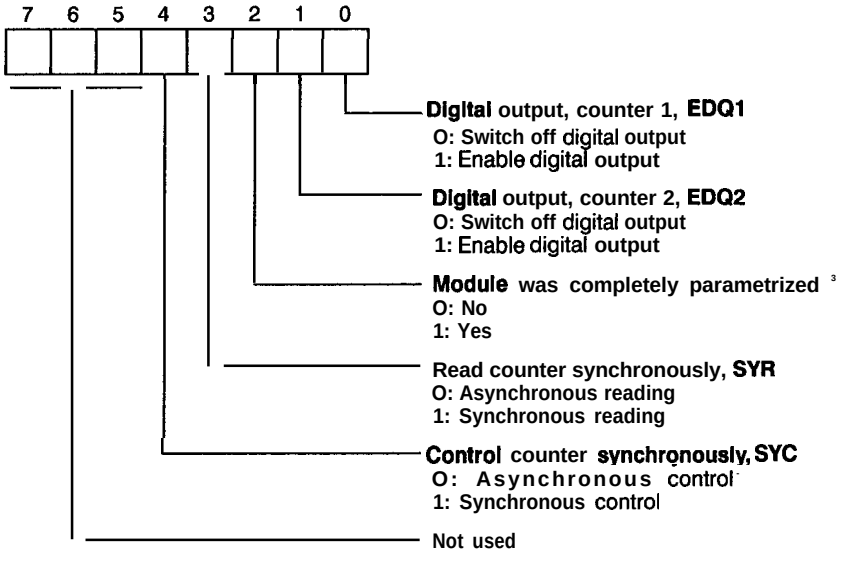
Allocation of Control Registers 1 and 2



1 0 → 1 edge required

2 0 → 1 edge: synchronize once; 1 level: multi-synchronization

Allocation of Control Register 3



3 The parameterization bit with which you document the complete parameterization of the module must be set during startup aftertheparameter register (or both registers) was/weretransferred tothe iP261. To accomplish this, write control register 3 as the last write access. The parameterization bitistransferred by the module to status register 3. For all additional entries in control register 3, the parameterization bit must be checked first (must be 1) in status register 3, and the parameterization bit must then be set.

3.10 Overview of the Register Addresses

Select Register	Offset Address	Read Write	Selected Register	S5 Command	Register Length in Bytes
XX [1]	0	W	Select register	TPY/TOY	1
OH	1	W	Control register 1	TPY/TOY	1
OH	2	W	Control register 2	TPY/TOY	1
OH	3	W	Control register 3	TPY/TOY	1
OH	4 5	W	Parameter register 1 Byte 1 Byte O	TPW/TOW TPY/TOY	2
OH	6 7	W	Parameter register 2 Byte 1 Byte O	TPW/TOW TPY/TOY	2
OH	0 1	R	IIR Byte 1 (counter 2) Byte O (counter 1)	LPW/LOW LPY/LOY	2
OH	2	R	Status register 1	LPW/LOY	1
OH	3	R	Status register 2	LPY/LOY	1
OH	4	R	Status register 3	LPY/LOY	1
IH	3	W	IFR 1	TPY/TOY	1
1H	4 5 6 7	W	Load register 1 Byte 3 Byte 2 Byte 1 Byte O	TPW/TOW TPY/TOY	2 or 4 depending on the mode of the counters
IH	0 1 2 3	R	Counter value register 1 Byte 3 Byte 2 Byte 1 Byte O	LPW/LOW LPY/LOY	2 or 4 depending on the mode of the counters
1H	4 5 6 7	R	Counter value register 2 Byte 3 Byte 2 Byte 1 Byte O	LPW/LOW LPY/LOY	2 or 4 depending on the mode of the counters
2H	4 5 6 7	W	Interrupt register 1 Byte 3 Byte 2 Byte 1 Byte O	TPW/TOW TPY/TOY	2 or 4 depending on the mode of the counters
3H	3	W	IFR 2	TPY/TOY	1
3H	4 5 6 7	W	Load register 2 Byte 3 Byte 2 Byte 1 Byte O	TPW/TOW TPY/TOY	2 or 4 depending on the mode of the counters
4H	4 5 6 7	W	Interrupt register 2 Byte 3 Byte 2 Byte 1 Byte O	TPW/TOW TPY/TOY	2 or 4 depending on the mode of the counters

1 XX = Any

4 Interrupt Processing

4 Interrupt Processing

4.1 What Is Interrupt Processing?

Interrupt processing takes place when a signal external to the processor (CPU, central processing unit of the PLC) interrupts the running program and triggers a separate program (the interrupt program).

Interrupt processing is involved when such an interrupt signal is acquired via interrupt lines and fed to the central processing unit. Process interrupt processing is involved when acquisition is via input byte IB 0.

Only interrupt processing can be triggered on the IP 281. Process interrupt processing is not availabe on this module.

The interrupt program acknowledges the queued interrupt and evaluates it by reading and storing current actual values, for example, or by generating an immediate reaction on a digital output module. After the interrupt program is processed, processing of the interrupted program is continued at the point at which it was interrupted.

Interrupt processing is used to achieve fast reactions to changes in signal status.

4.2 Interrupt Processing

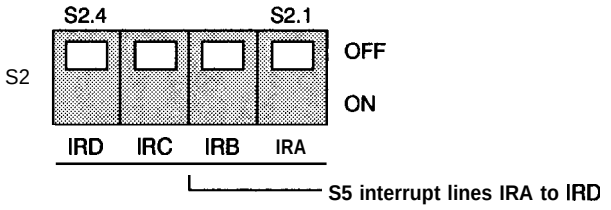
This type of interrupt acquisition uses special interrupt lines on the S5 backplane bus to feed the interrupt signal to the central processing unit.

Slot selection

When selecting the slots, remember that interrupt lines are not available on all slots (→ section 8.5 and equipment manual of the PLC).

Interrupt line selection

One interrupt line on the module must be selected via DIL switch S2 to feed the interrupts from the IP 281 to the central processing unit.



OFF: **No interrupt**
ON: **Interrupt via the applicable line**

The switch for the selected interrupt line must be set to ON: all other switches must beset to OFF. All four switches must beset to OFF when the IP 281 is operated without the triggering of interrupts.

Several IP 281 modules can reconnected to one interrupt line. The module which triggered the interrupt is determined in your interrupt program by reading the interrupt information registers on the modules.

One organization block of the interrupt processing is assigned to each interrupt line. It is called when the corresponding interrupt line is activated. When several interrupts are queued, they are processed in the order of their priority (either set in data blockDXO(forS5–135U and S5– 155U) or starting with the organization block with the lowest number).

Interrupt evaluation

Interrupts are evaluated at different locations on different programmable controllers.

PLC	Interrupt pointa Occur At
S5–115H	Synchronization points
S5–115U	Instruction boundaries
S5–135U	Block boundaries (standard setting) or instruction boundaries (can be set in data block DX O)
S5–155U (155U mode)	Instruction boundaries

Remember the following when setting the interrupt points on the S5– 135U.

The advantage of fast acquisition after each instruction (in practical terms, reaction to an interrupt is immediate) must be weighed against the disadvantage that programming the interrupt–controlled program processing becomes much more complicated to ensure error–free "insertion" of the interrupt program after each STEP5 instruction.

Among other things, this requires that certain instruction sequences for an interrupt be disabled by interrupts (either with software via STEP5 instruction or with special functions).

Setting "interrupt at block boundaries" in data block DX O is always recommended when the reaction time permits.

Particularly for interrupts after every instruction, remember that the signal states or values of temporary data must not be overwritten in the interrupt program. These values must be saved at the beginning of the interrupt–controlled program processing, and reloaded again at the end to ensure that they are again available unchanged to the running program. This particularly applies to the scratchpad flag area from flag byte FY 200 to FY 255.

4.3 Reaction Times During Interrupt Processing

The reaction time to an interrupt consists of the following partial times.

– Acquisition time of the module
– Acquisition time in the programmable controller
– Processing time of the interrupt program

Acquisition time of the module

(An enabled interrupt source)
The time between the triggering event and the triggering of the interrupt line is a maximum of 2 µsec. When the event is triggered by external signals, the delay time required to set the input filter must also be added (→ section 8.7).

Acquisition time in the programmable controller

Interrupt acquisition in the PLC depends on the programmable controller and the central processing unit used. Processing times of the system program can be found in the applicable equipment manuals.

Interrupt at synchronization points

The longest reaction time to an interrupt is usually the processing time between two synchronization points.

Interrupt at instruction boundaries

The longest reaction time to an interrupt is usually the processing time in the operating system or the processing time of special functions or integrated function blocks.

Interrupt at block boundaries

The longest reaction time of an interrupt is usually the processing time of the longest running part of the program without block calls or block end instructions.

☞ **Program loops injunction blocks often increase processing time significantly.**

Interrupt disable

Always remember that no interrupts are processed during a programmed interrupt disable. The processing time of a program section containing an interrupt disable may have to be included when determining the reaction time to an interrupt.

Processing time of the interrupt program

The processing time is primarily determined by your own programming,

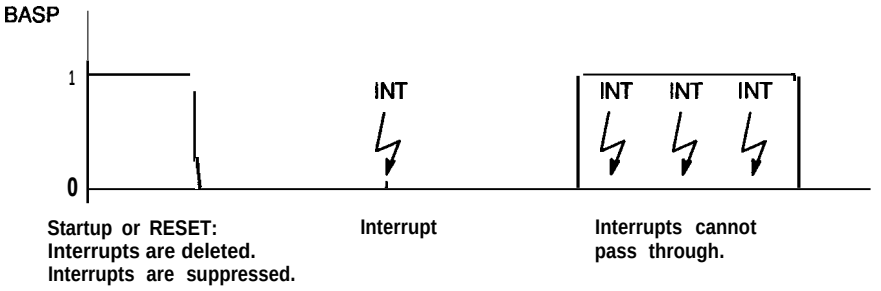
When are interrupts acquired?

Interrupts can be processed when the supply voltage of the module is within the tolerance range, and the RESET signal is inactive ("0").

Incoming interrupts are not processed as long as the BASP signal is active ("I"),

When an interrupt is queued and the BASP signal becomes active, the interrupt is removed by the IP 281 from the S5 bus. The interrupt is output again when the BASP signal becomes inactive again.

This behavior is not affected by plug–in jumper X20 (BASP selection) (→ section 2.3).



Acknowledging the interrupts

When an interrupt is triggered by an interrupt enabled in interrupt enable register IFR (→ section 3.6), the cause is entered in interrupt information register HR.

Interrupts which are not enabled do not trigger an interrupt and are not entered in the HR.

Reading the IIR causes the interrupt to be reset,

Although one byte in the IIR is available to each counter (→ section 3.7), the IIR must always be read in its entirety (2 bytes). For this reason, the use of word commands LPW/LOW is recommended for the access.

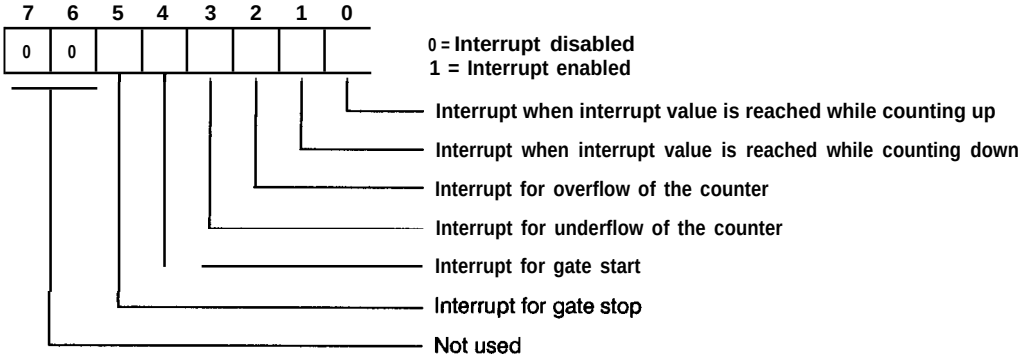
☞ When the CPU 944A/B is used, byte commands must be used for the access. While the IIR is being accessed with byte commands, the interrupt processing must be disabled with the S5 command 1A, and then enabled again with RA after the access.

When several interrupts occur before the IIR is read by the S5 CPU, these are also entered in the IIR.

When interrupts arrive while the IIR is being read, these are stored intermediately. An interrupt is then triggered again after the read procedure is concluded.

4.4 Interrupt Sources

The IP 281 can trigger the interrupt processing on the S5 CPU when various events occur. There are 6 interrupt sources for each counter. These sources can be enabled bythe respective interrupt enable register.



Several interrupt sources can be enabled for one counter. The triggering event (several if necessary) must be determined in the interrupt program by evaluating the interrupt information register (→ section 3.7),

Explanation of the Interrupts

- **Interrupt when the interrupt value is reached while counting up**

  The counter must be counting up. An interrupt is triggered when the counter value reaches the interrupt value. A hysteresis of ± 1 is provided when the interrupt value is reached (→ section 4.6),

- **Interrupt when the interrupt value is reached while counting down**

  The counter must be counting down. An interrupt is triggered when the counter value reaches the interrupt value. A hysteresis of ±1 is provided when the interrupt value is reached (→ section 4.6).

- **Interrupt at counter overflow**

  The interrupt is triggered when a counter overflow occurs. A hysteresis is provided when the overflow occurs (→ section 6.2.1).

- **Interrupt at counter underflow**

  The interrupt is triggered when a counter underflow occurs. A hysteresis is provided when the underflow occurs (→ section 6.2.1).

- **Interrupt at gate start**

  An interrupt is generated when the internal gate (-t section 6.6) is opened.

  When operating mode SC2A is used, the interrupt is also triggered when the interrupt value of counter 1 has not yet been reached (i.e., the interrupt is exclusively dependent on the hardware or software gate).

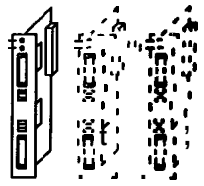
- **Interrupt at gate stop**

  An interrupt is generated when the internal gate (→ section 6.6) is closed.

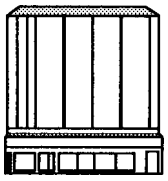
☞ **Nointerruptisgenerated whenthegate isclosedviathe EMERGENCY GATEstop(GST in control register 1/2).**

4.5 Guidelines for Interrupt Processing

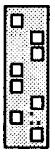
The use of one or more counter modules with interrupt processing requires some preparation. Use the following overview as an aid.



? **Decide how many interrupt-generating modules you want to use,**



? **Check todeterminewhere themodules can be installed (→ section 8.5 and the equipment manual of your PLC).**

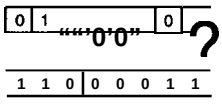


? Select the interrupt linewith DIL switch S2 (→ section 4.2).

```
L    FW 100
T    DW 20
JU   PB 17
A    I   7.5
A    I   6.3
·    Q   5.1
```

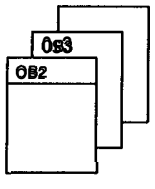
? **The table in section 4.2 shows you where an interrupt will interrupt youruser program:**

- **at block boundaries or at instruction boundaries or at synchronization points.**



? **Allocate theinterruptenable register described infection 4.4**

- **based on your application.**



? **Setup yourinterrupt program in the applicable interrupt OBs.**

4.6 Hysteresis of the Interrupt Value

Each counter is equipped with an interrupt register in which an interrupt can be stored. Acceptance of the interrupt value can be triggered by the S5 (→ section 3.4) or by operating mode TCAR (-t section 6.4.2).

The interrupt value is always compared with the current counter value (hardware comparator).

The following can occur when the counting value reaches the interrupt value.

- **An interrupt is triggered (→ section 4.4).**
- **The digital output is activated (→ section 6.7).**
- **Counter 2 is started (→ section 6.4.5, SC2A).**

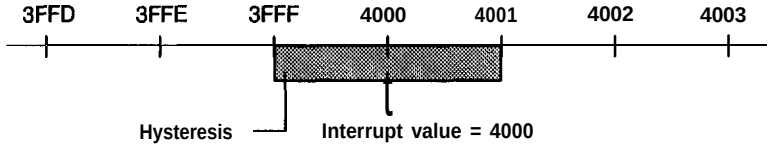
Hysteresis for interrupt processing

When the encoder stops at the interrupt–triggering position, the encoder can oscillate back and forth around this interrupt point. Interrupts would be triggered continuously or the digital output activated.

To prevent this undesired triggering of interrupts, the interrupt values are provided with a hysteresis of ±1.

The counter cannot trigger a new interrupt unless it reaches a value at least 2 greater or 2 less than the interrupt value.

Example:



- **An interrupt is triggered when the value 4000 is reached.**
- **If the counter oscillates between 3FFFand 4001, no further interrupts are triggered even if the counter repeatedly reaches the value 4000.**
- **Anew interrupt is triggered when the counter reaches the value 3FFE (or less) or the value 4002 (or greater) and then assumes the value 4000 again.**

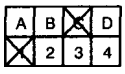
The hysteresis is reset by loading the counter or the interrupt register.

5 Commissioning the Counter Module

5 Commissioning the Counter Module

5.1 Commissioning Guidelines

Hardware settings (items 1 to 5) and software settings (items 6 to 9) must be performed during the commissioning of the counter module.



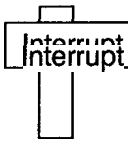
1. **Check the following after unpacking the module.**
   Release status of the module
   (Labelling on the front plate)
   Release status of the plug– in submodule

2. **Use DIL switch S1 to set the basic address for your module.** Section 2.2

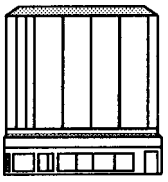
3. **Adjust the module to the application conditions.**
   Interface selection
   - **24 V encoder interface**
     - **–Change interface selection plug –in jumper?**
     - **–Change reference potential plug–in jumper?**
     - **–Change limit frequency plug–in jumper?**
     - **–Circuit pin RE?**
     - **–Change wire break recognition plug–in jumper?**
   - **RS 422 interface**
     - **– Change interface selection plug –in jumper?**
     - **–Change reference potential plug–in jumper?**
     - **–Change wire break recognition plug–in jumper?**

   Limit frequency of the digital inputs
   Minimum pulse duration of the digital outputs

   Section 2.3



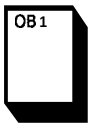
4. **When interrupt processing is used, use DIL switch S2 to select the interrupt line for your module.** Section 2.2



? **5. Switch off the programmable controller and insert the module in the slot provided.**
(Only certain slots are provided for interrupt processing via interrupt lines.)

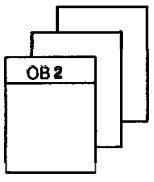
? **6. Setup the registers and write your startup program in 06s 20 to 22 of your programmable controller.** **Section 3.2 to section 3.9**

☞ **Don't forget to include the status registers in your startup program. These registers supply you with information concerning the module or the individual counters.**

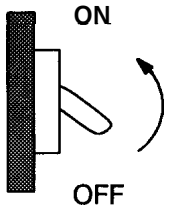


? **7. Now setup your cyclic program in 061.**

☞ **Don't forget to include the status registers in your program. These registers supply you with information concerning the module or the individual counters.**



? **8. If necessary, setup yourinterrupt program in the applicable interrupt organization block.**



? **9. When switching on the programmable controller, proceed in the sequence as recommended below.**

1. Operating mode switch on the central processing unit to STOP
2. Switch on power voltage for the programmable controller. (Perform an "overall reset" for the program memory if switching on for the first time.)
3. Transfer blocks from the programmer to the programmable controller.
4. Start the central processing unit with a "new start".

Caution

It is expressly pointed out that incorrect handling or operating or incorrect connection can damage the IP 281 module. This can also cause extensive damage to your system. We make the assumption that only qualified personnel who are also familiar with the ESD protection regulations will work with the module.

5.2 Startup Behavior of the Counter Module

After switching on the supply voltage and an inactive RESET of the S5, the module is ready for operation and-the green "RUN" LED goes on.

Indication		Meaning
RUN LED	ERR LED	
O	○	Voltage supply missing (from S5)
0	☼	RESET is active.
☼	○	Module is operating correctly.
☼	☼	Parameterization error or wire break

5.3 RESET Behavior

5.3.1 RESET Causes

There are two conditions which can cause a RESET of the IP 281.

– RESET due to the S5 RESET signal

- RESET due to power failure or power too low (hardware RESET)

The module is reset as soon as one of the two causes occurs.

After the reset, the module has the same status as it did after the first startup.

5.3.2 Basic Setting of the IP 281 after RESET

Counting mode	**Counter 1 and counter 2 operate in mode (i.e., they are 6–bit counters and count from O to FFFFH).**
Counter status	**The counters have the value "O".**
Operating mode	**The "continuous counting" (CONC) operating mode is set for both counters.**
Gate	**The gate function is switched off (i.e., the counter counts (regardless of the signals on the STA and STO input).**
Counting pulse evaluation	**One–time evaluation (EVOT) is set for both counters.**
Interrupts	**All interrupts are disabled (IFR = O).**
Registers	**The registers are deleted (= O). The status registers contain the current status.**
Digital outputs	**The DQNU method of operating is set. The digital outputs are inhibited.**

 Order No: 6ES5 998–0KP21

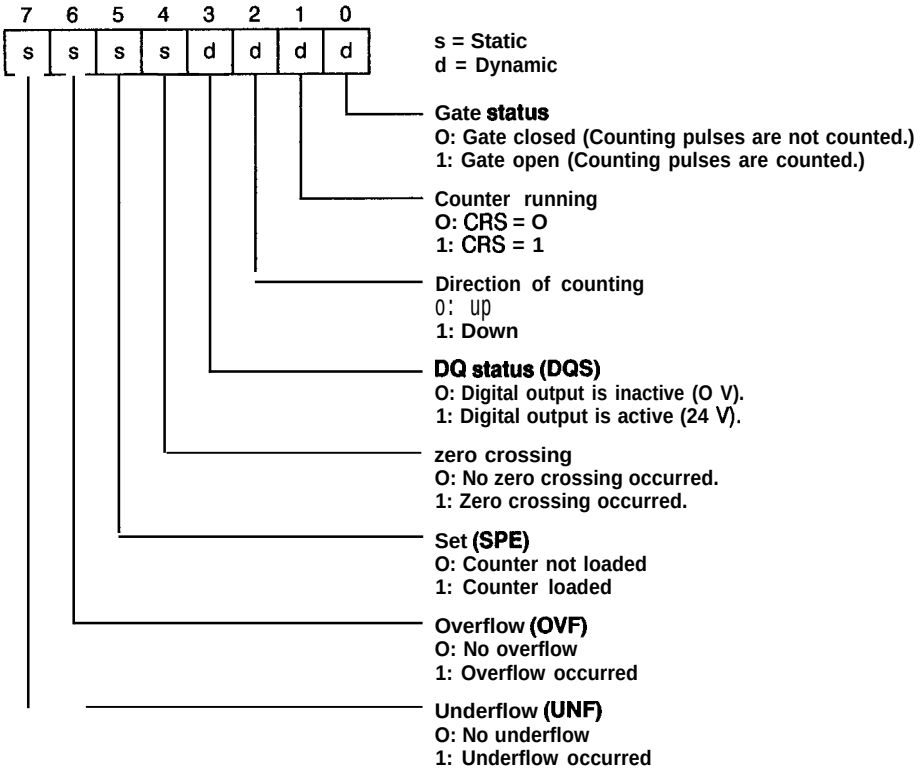
5.4 Evaluation of the Status Registers

Status registers 1 to 3 contain information on the current status of the counters and the module.

There are static entries and dynamic entries.

Static: **The applicable bit is set when the triggering event occurs. Reading the status register causes the static bits to be reset.**
Dynamic: **The current status is indicated.**

Contents of Status Register 1/2

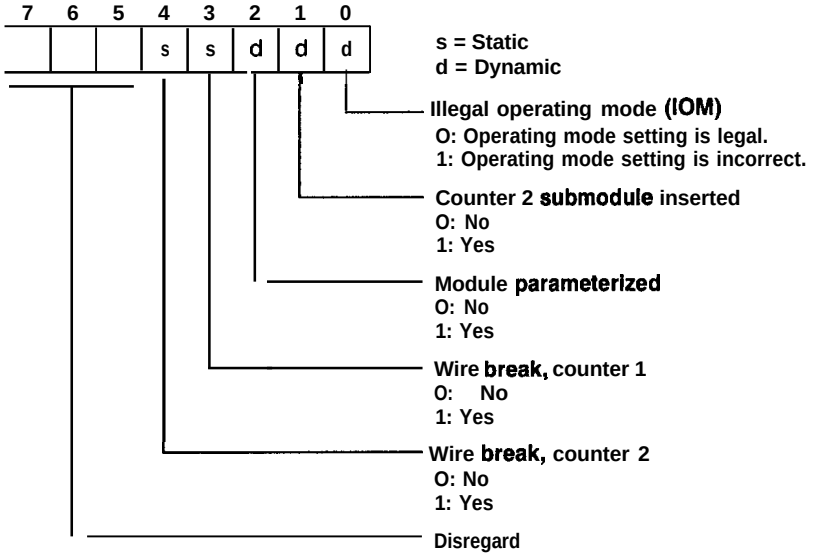


Status after RESET

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Gate status	**Indicates the current status of the internal gate (-t section 6.6)**
Counter running	**The CRS (counter, bit O) of the applicable counter is entered in the status register.**
Counting direction	**This bit indicates the current direction of counting. When stopped, the direction of counting last indicated is retained.**
DQ status	**This bit indicates whether the digital output is active (24 V level on DQ).**
Zero crossing	**This bit is set when the counter reaches the value O during counting. Reading the register causes the bit to be reset.**
Set	**This bit is set each time the counter is loaded. Reading the register causes the bit to be reset.**
Overflow	**This bit is set when the counter exceeds the upper counting range limit (→ section 6,2.1). Reading the register causes the bit to be reset.**
Underflow	**This bit is set when the counter passes below the lower counting range limit (→ section 6.2.1). Reading the register causes the bit to be reset.**

Contents of Status Register 3



Status after RESET

7	6	5	4	3	2	1	0
X	X	X	①	①	0	②	0

① Wire break message is queued: 1
Wire break message is not queued: O

@ Counter 2 submodule is present: 1
Counter 2 submodule is not present: O

Illegal operating mode (IOM)

Monitors the parameterization. The bit is automatically set to O when the parameterization is legal. The parameterization must be checked if the bit is set (→ section 6.4).

Counter 2 sub– module inserted

This bit indicates whether the plug– in submodule is installed.

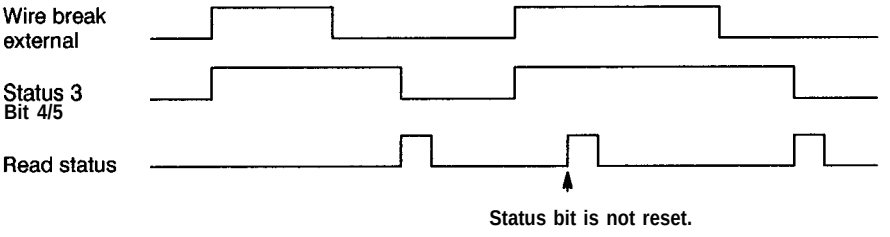
Module parameterized

After the IP 281 has been parameterized, the S5 can use control register3 (set bit 2) to report that the module is parameterized. Assoonasthe bit has been set (during startup) in the control register, it can be read back via the status register for monitoring purposes.

This status bit remains set as long as operation of the module is "normal". It is deleted when a supply voltage failure occurs or the S5 initiates a RESET (i.e., the parameterization is lost).

Wire break, counters 1/2

As soon as a wire break occurs on the RS 422 encoder interface (→ section 1.4.1 .2), the applicable bit is set in status register 3 if the wire break recognition is active. Reading the status register causes the bitto be reset if no more errors are queued.

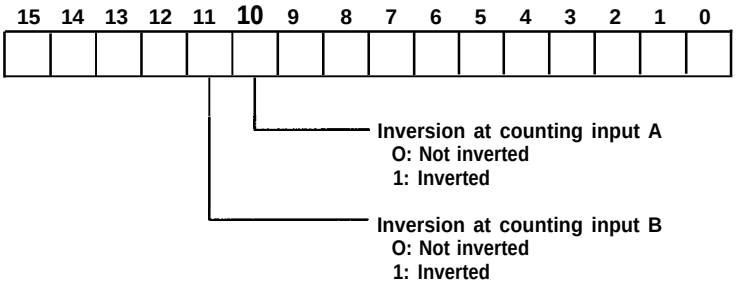


5.5 Changing the Direction of Counting

The direction of counting is determined by two different methods depending on the type of pulse evaluation. When encoders with two pulse trains displaced by 90" (counting pulse evaluation EVOT, EVTT, EVFT) are used, the direction of counting is derived from the signal sequences of A and B (→ section 6,2,2).

By inverting the input signals while retaining the same direction of rotation of the encoder, the direction of counting can be changed without having to change the wiring. The inversion is set in the parameter register of the respective counter.

Parameter Register 1/2



When encoders with one pulse train (counting pulse evaluation EVDI) are used, the direction of counting is specified by the level at counting input B or by bit 11. Inversion is specified at counting input B (→ section 6.2.2).

5.6 Overview of the Operating Modes

Operating Mode		Counting Mode Counter 1	Counting Mode Counter 2	Operating Mode Counter 1			Operating Mode Counter 2			Gate Control Counters 1 and 2			
				CONC	OCSS/CCSS	OCHG/CCHG	CONC	OCSS/CCSS	OCHG/CCHG	Hardware Gate Start	Hardware Gate stop	Software Gate start	Software Gate Stop[1]
			1 2 3 4										
Autonomous operating mode	CONC	1	+ + + +	The autonomous operating modes can be combined aa desired.						+	+	●	●
		2	+ + + +										
		3	+ + + +										
		4	+ + + +										
	OCSS/ CCSS	1	+ + + +							●	●	☞	+
		2	+ + + +										
		3	+ + + +										
		4	+ + + +										
	OCHG/ CCHG	1	+ + + +							+	☞	●	●
		2	+ + + +										
		3	+ + + +										
		4	+ + + +										
combination operating modes	TCAR	1	+ – – –	◆	+	+	–	+	+				
		2	– + – –	◆	+	+	-	+	+				
		3	– – + –	●	+	+	–	+	+				
		4	– – – +	◆	+	+	–	+	+				
	TCLR	1	+ – – –	◆	+	+	–	+	+	+	+	+	+
		2	– + – –	◆	+	+	–	+	+				
		3	– – + –	●	☞	☞		☞	☞				
		4	– – – +	◆	+	+		☞	☞				
	ZMPC	1	◆ ◆ + +	☞	☞	☞		☞	☞	2	2	2	2
		2	◆ ◆ + +	+	+	+	–	+	+	+	+	+	+
		3	◆ ◆ + +	+	+	+	–	+	+				
		4	◆ ◆ + +	+	+	+	–	+	+				
	SC2A	1	+ + + +	+	+	+	–	+	+	+	+	+	+
		2	+ + + +	+	+	+	–	+	+				
		3	+ + + +	+	+	+	–	+	+				
		4	+ + + +	+	+	+	–	+	+				

+ Setting permitted
– Setting not permitted: The ERR LED goes on and the IOM bit 3 is set in status register 3.
. Setting has no effect: The module does not operate in this mode. The ERR LED does not 90 on and the IOM bit is not set in status register 3.
◆ No practical use

1 The software EMERGENCY OFF gate stop is always possible except with counter 2 for ZMPC.
2 When operating mode ZMPC is used, gate control for counter 2 has no effect.

When operating mode ZMPC is used, counter 2 must operate with counting pulse evaluation EVDI, and counter 1 with EVOT, EVTT or EVFT. The counting pulse evaluation can be selected as desired for all other operating modes.

6 Operating Modes and Functions

* Under development

6 Operating Modes and Functions

6.1 Introduction

The IP 281 munter module offers great flexibility in adapting its functions to the requirements of many different counting applications.

Counter settings must be performed specifying the counting mode and the type of counting pulse acquisition (→ section 6.2).

The autonomous operating mode allows the method of operation of each individual counter to be set (→ section 6.3).

The combination operating modes which couple the functions of both counters are particularly useful for certain applications (-t section 6.4).

The counters can be loaded with defined values. Both counters can be controlled synchronously. The counter values can be read out individually or simultaneously (→ section 6.5).

The counters are equipped with a gate control which allows both hardware control by the digital inputs and software control by the S5 (→ section 6.6).

Various methods of operation (i.e., the conditions under which the digital output activates) can be set for the digital output of each counter (→ section 6.7).

6.2 Counter Settings

6.2.1 Counting Mode

The counting mode specifies the counting width and range **for each counter separately.**

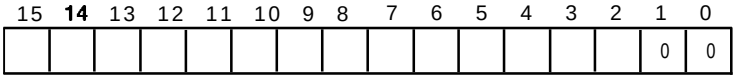
The basic setting for both counters after power–on is counting mode 1.

The counting mode for munter 1 is set in parameter register 1; the counting mode for counter 2 is set in parameter register **2. All counting modes are permitted for the autonomous operating modes and the combination operating modes ZMPC and SC2A. The combination operating modes TCAR and TCLR require that both counters operate in the same counting mode.**

Counting mode 1 **The counter has a counting width of 16 bits and operates in the positive counting range listed below.**

0000 to FFFF (hexadecimal)
0 to **+65,535** (decimal)

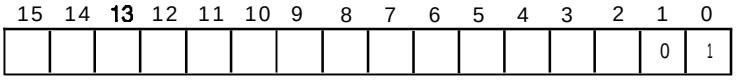
Parameter register 1/2



Counting mode 2 **The counter has a counting width of 32 bits and operates in the positive counting range listed below.**

00000000 to FFFFFFFF [hexadecimal)
0 to4,294 ,967,295 (decimal) “

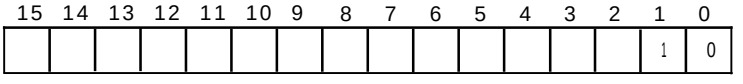
Parameter register 1/2



Counting mode 3 **The counter has a counting width of 16 bits and operates in the positive and negative counting range listed below.**

8000 to 7FFF (hexadecimal)
–32,768 to +32,767 (decimal)

Parameter register 1/2



Counting mode *4* The counter has a counting width of 32 bits and operates in the positive and negative counting range listed below.

80000000	to 7FFF FFFF	(hexadecimal)
–2,1 47,483,648	to +2,147,483,647	(decimal)

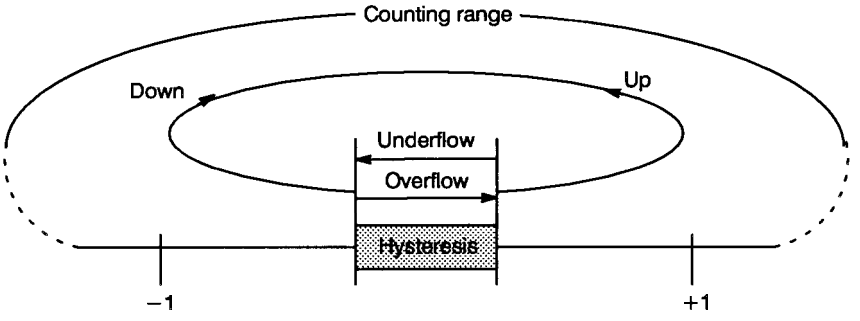
Parameter register 1/2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														1	1

The counters use binary operation in all counting modes and can count up and down in the ranges set.

The counting width also sets the width of the load, interrupt and counter value registers.

Overflow/underflow An overflow occurs when the upper counting range limit is exceeded while counting up. Underflow occurs when the lower counting range limit is exceeded while counting down.



Counting Mode	Upper Counting Range Limit		Lower Counting Range Limit	
1:	FFFE	FFFF	0000	cool
2:	FFFF FFFE	FFFF FFFF	00000000	00000001
3:	7FFE	7FFF	8000	8001
4:	7FFF FFFE	7FFF FFFF	8000 0000	80000001

Hysteresis When an encoder is “stationary”, oscillation of this encoder around the actual value can change the counter status.

When the counter stops on a range limit, this could cause overflow/underflow to be triggered continuously. To avoid this, overflow and underflow are provided with a fixed hysteresis of 1 (i.e., to trigger a new overflow/underflow, the value of the “upper counting range limit+ 1“/’’lower counting range limit –1” must be reached respectively,

When oscillation around the counting range limits occurs, one overflow and one underflow are triggered and the hysteresis then becomes active.

The hysteresis is reset when the counter or the interrupt register is loaded.

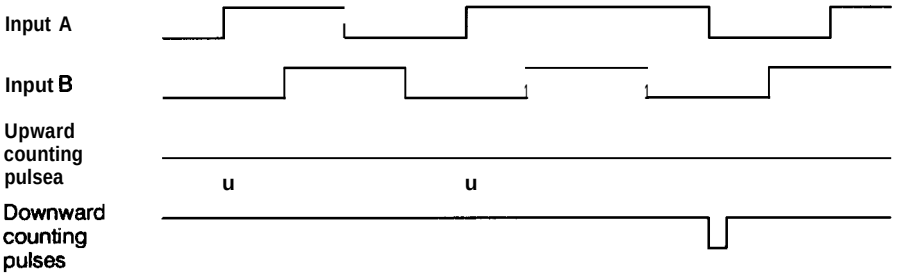
6.2.2 Counting Pulse Evaluation

The counters can operate with one–time, two-time or four–time pulse evaluation, or with direction evaluation.

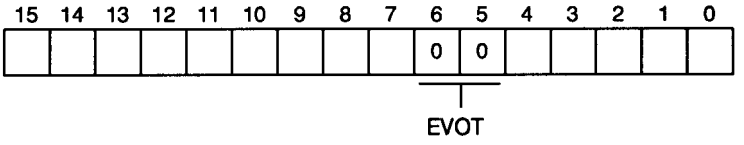
The type of counting pulse evaluation is set for each counter individually in the parameter register.

One-time evaluation (EVOT)

Upward counting pulses are generated with arising edge of A and low level on B. Downward counting pulses are generated with a falling edge of A and low level on B.

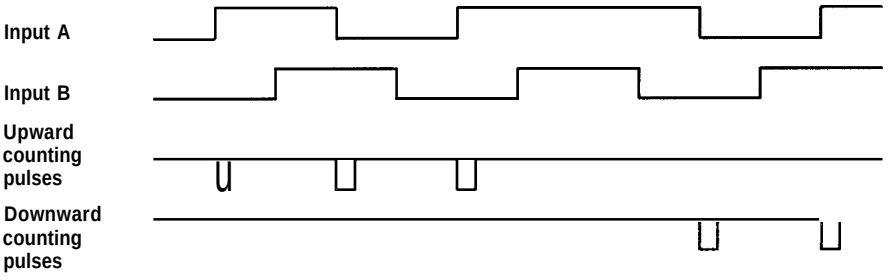


Parameter register 1/2

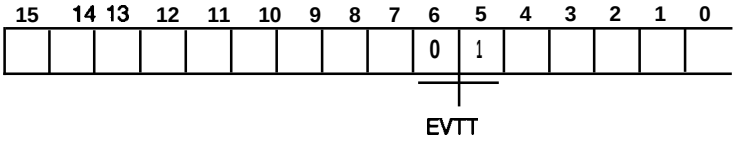


Two-time evaluation (INTT')

A counting pulse is generated for every rising and falling edge of A. The direction of "counting depends on the level at input B.

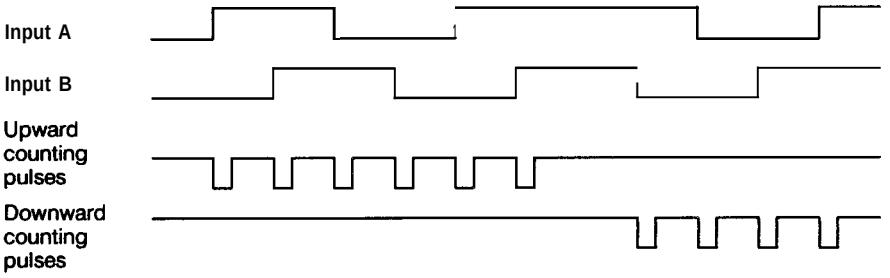


Parameter register 1/2

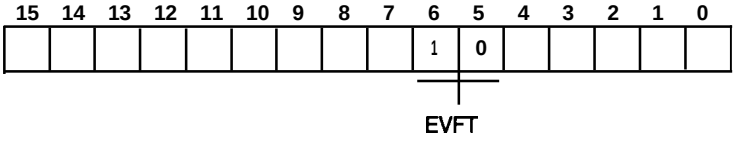


Four-time evaluation (EVFT)

A counting pulse is generated for every rising and falling edge of A and B. The direction of counting depends on the level at inputs A and B.



Parameter register 1/2



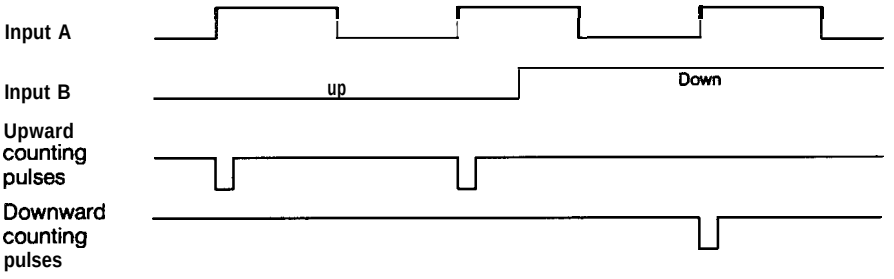
Direction evaluation (EVDI)

When counting with one counting input, the acquisition of counting pulses occurs at counting input A. The positive edge causes a change in the counting value (one–time evaluation). Counting input B is used to evaluate the direction of counting.

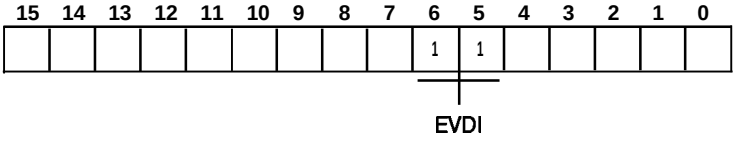
Low level at input B: Counting up
High level at input B: Counting down

Caution

The counting value can become invalid if the encoder is oscillating around its actual value.

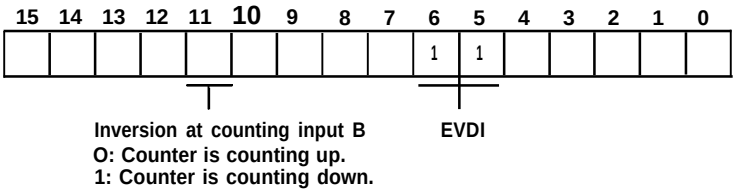


Parameter register 1/2



When the 24 V encoder interface is used, the direction of counting can be specified via the "inversion at counting input B" bit in parameter register 1 /2, without using input B*,

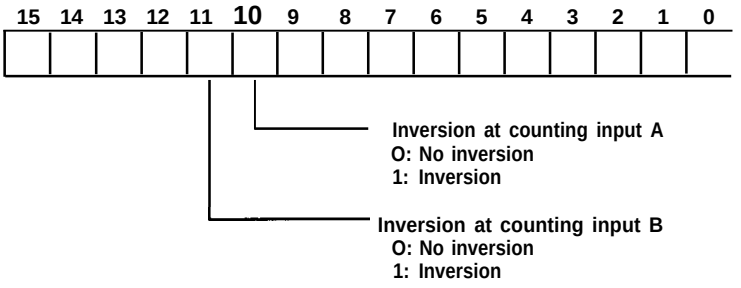
Parameter register 1/2



Inversion of the input signals

Input signals A and B can be inverted. The setting is made in the respective parameter register as shown below.

Parameter register 1/2



When incremental encoders with two pulse trains displaced by 90" are used, the direction of counting can be changed by the **inversion of one counting input, without having to rewire the counting inputs.**

Caution

If the setting (inversion/no inversion) is changed while the counter is running, the level change can cause an extra counting pulse to be generated.

To avoid this error, the counter must be loaded after parameterization (with the value O if necessary).

6.3 Autonomous Operating Modes

6.3.1 Overview

The method of operation of a counter is specified by setting the autonomous operating mode. There are five autonomous operating modes.

Continuous counting, CONC

- **One–time counting with software gate start, OCSS**
- **One–time counting with hardware gate start, OCHG**

Cyclic counting with software gate start, CCSS

- **Cyclic counting with hardware gate start, CCHG**

The autonomous operating modes can be combined as desired when the IP 281 is operated with two counters.

All counter settings (counting mode and counting pulse evaluation) can be selected as desired with the autonomous operating modes.

Available Gate Controls

Operating Mode	Gate Control	
	Hardware Gate	Software Gate
CONC	Yea	No*
OCSS	No	Yes
CCSS	No	Yes
OCHG	Yes	No*
CCHG	Yes	No*

*** The EMERGENCY OFF gate atop is always available (→ section 6.6.5).**

Hardware and software gate control do nottake effect until enabled in control register 1/2 (GEN bit).

The following are permitted with all autonomous operating modes.

– All load capabilities (→ section 6.5.1)
–All read capabilities (→ section 6.5.3)
– All methods of operation of the digital outputs (→ section 6.7)
– All interrupt lines (→ section 4.4)

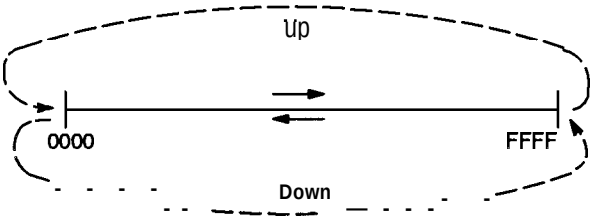
Behavior during overflow and underflow is described in section 6.2.1.

6.3.2 Continuous Counting (CONC)

Method of operation

The counter starts to count at the current counting value and counts continuously. After RESET the current counting value is O.

Example:
Counting mode 1



Gate control

Hardware gate via pulse (→ section 6.6.2)
Hardware gate via level (→ section 6.6.3)

- The gate function is disabled after RESET (i.e., the counter counts).
- Gate control does not take effect until the gate function (GEN bit) is enabled in control register 1/2.

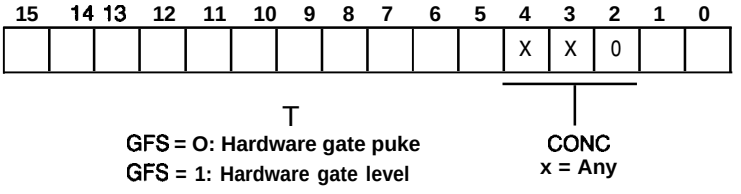
Gate start:
- Pulse at digital input STA
- High level at digital input STA

Gate stop:
- Pulse at digital input STO
- Low level at digital input STA

☞ Thecounter can be loaded with a value by the S5 before the operating mode is set. The counter then begins counting starting with this value (→ section 6.5.1.1).

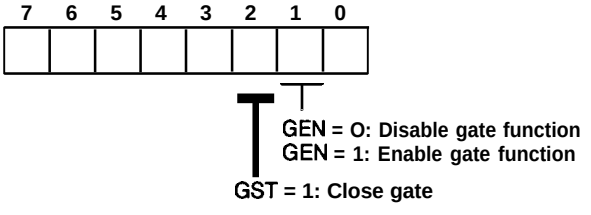
Parameter register 1/2

The operating mode and the type of gate control are set in parameter register 1 /2.



Control register 1/2

The gate function is enabled/disabled with the control register using the GEN bit. An EMERGENCY OFF gate stop is available via the GST bit.



6.3.3 One-Time Counting with Software Start (OCSS)

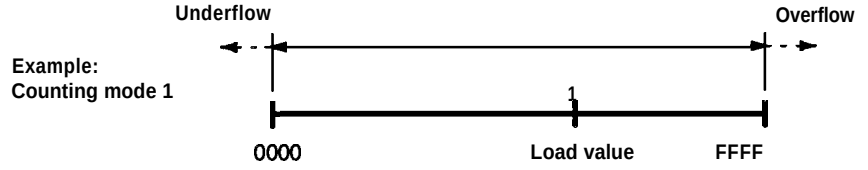
Method of operation

When the software gate opens, the counter is loaded with the value stored in the load register, and begins to count starting with this value.

It is stopped by the following.

- Overflow of the counter
- Underflow of the counter
- The software gate closes.

The counter remains in stop status until the software gate is opened again.



☞ When a range limit is exceeded, the counter stops at this limit (e.g., in counting mode 1, the counter stops at *0000H* when an underflow occurs and at *FFFFH* when an overflow occurs).

Gate control

Software gate control with

GSS bit O in control register 1/2

Start: GSS bit O: 1
stop: GSS bit O: O

☞ Thegate function must be enabled in control register 1/2.

Notes

Evaluation of bit 6 (overflow) and bit 7 (underflow) in status register 1/2 is used to determine whether the counter has exceeded a range limit.

This operating mode cannot be set unless the gate function has been enabled by the GEN bit (bit 1 in control register 1/2). Otherwise the message "illegal operating mode" is output (IOM in status register 3) and the ERROR LED goes on.

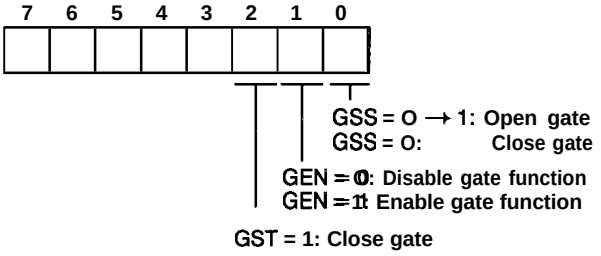
The settings must be performed in the sequence listed below.

1. Enable gate function (GEN in control register 1/2)
2. Set operating mode (parameter register 1/2)

Control register 1/2

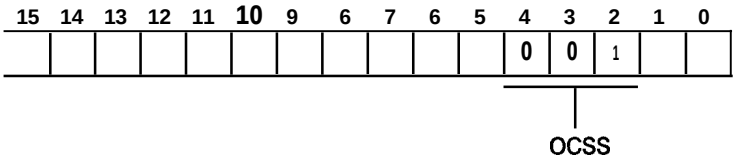
Control register 1/2 is used for the following purposes.

- **Disable/enable the gate function with the GEN bit**
- **Software gate control with the GSS bit**
- **EMERGENCY OFF gate stop with the GST bit**



Parameter register 1/2

The OCSS operating mode is set in parameter register 1/2.



6.3.4 One-Time Counting with Hardware Gate Start (OCHG)

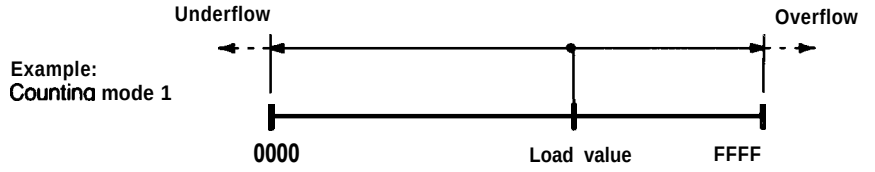
Method of operation

The counter operates as an up/down counter. When the hardware gate opens, the counter is loaded with the value stored in the load register, and begins to count starting with this value.

It is stopped by the following.

- Overflow of the counter
- Underflow of the counter
- Closure of the hardware gate

The counter remains in stop status until the hardware gate is opened again.



☞ When a range limit is exceeded, the counter stops at this limit (e.g., in counting mode 1, the counter stops at *0000H* when an underflow occurs and at *FFFFH* when an overflow occurs).

Gate control

Hardware gate via pulse (→ section 6.6.2)
Hardware gate via level (→ section 6.6.3)'

Start:
- Pulse at digital input STA
- High level at digital input STA

stop:
- Pulse at digital input STO
- Low level at digital input STA

☞ The gate function must be enabled in the control register.

Notes

Evaluation of bit 6 (overflow) and bit 7 (underflow) in status register 1/2 is used to determine whether the counter has exceeded a range limit.

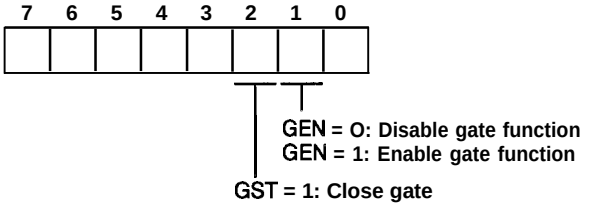
This operating mode cannot be set unless the gate function has been enabled by the GEN bit (bit 1 in control register 1/2). Otherwise the message "illegal operating mode" is output (IOM in status register 3) and the ERROR LED goes on.

The settings must be performed in the sequence listed below.

1, Enable gate function (GEN in control register 1/2)
2. Set operating mode (parameter register 1/2)

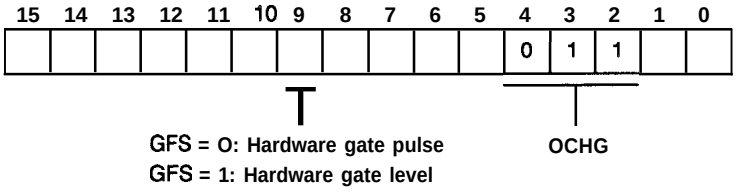
Control register 1/2

The control register is used to enable/disable the gate function with the GEN bit. An EMERGENCY OFF gate stop is available with the GST bit.



Parameter register 1/2

The operating mode and the type of gate control are set in parameter register 1/2.



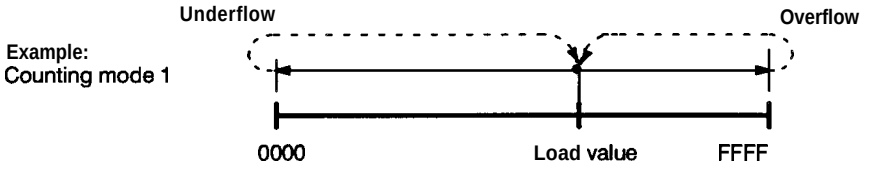
6.3.5 Cyclic Counting with Software Start (CCSS)

Method of operation

When the software gate opens, the counter is loaded with the load value, and begins to count starting with this value.

If a counting range limit is exceeded (overflow or underflow), the counter is loaded again with the load value, and resumes counting starting with this value.

The counter is stopped when the software gate closes.



The counter behaves as shown below when the load value corresponds to a range limit. Example: counting mode 1, 16 bits, positive counting range

Load Value	Direction of Counting	
	Up	Down
0000	(hunter counts "continuously". 0000 to FFFF→0000 to FFFF→	Counter stops at 0rlOOH.
FFFF	Counter stops at FFFFH.	Counter counts 'continuously". FFFF to 0000→FFFF to 0000→

Gate control

Software gate

Start: GSS bit O in control register 1/2: 1
stop: GSS bit O in control register 1/2: O

☞ The gate function must have been enabled in control register 1/2.

Notes

This operating mode cannot be set unless the gate function has been enabled by the GEN bit (bit 1 in control register 1/2). Otherwise the IOM message ("illegal operating mode") is output and the ERROR LED goes on.

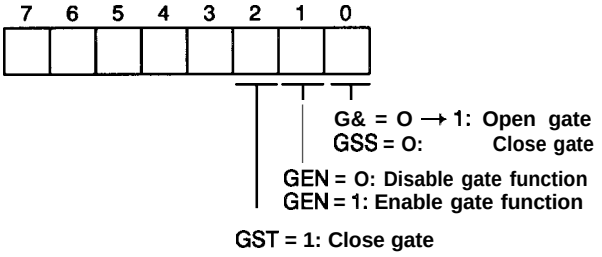
The settings must thus be performed in the sequence listed below.

1. Enable gate function (GEN in control register 1/2)
2. Set operating mode (parameter register 1/2)

Control register 1/2

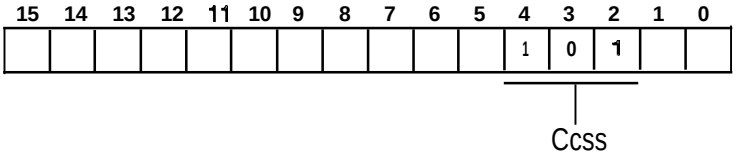
Control register 1/2 is used for the following purposes.

- **Disable/enable the gate function with the GEN bit**
- **Software gate control with the GSS bit**
- **EMERGENCY OFF gate stop with the GST bit**



Parameter register 1/2

The operating mode is set in parameter register 1/2.



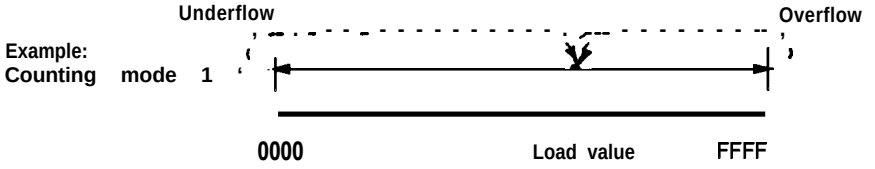
6.3.6 Cyclic Counting with Hardware Gate Start (CCHG)

Method of operation

When the hardware gate opens, the counter is loaded with the load value, and begins to count starting with this value.

If a counting range limit is exceeded (overflow or underflow), the counter is loaded again with the load value, and resumes counting starting with this value.

The counter is stopped when the hardware gate closes.



The counter behaves as shown below when the load value corresponds to a range limit. Example: counting mode 1, 16 bits, positive counting range

Load Value	Direction of Counting	
	up	Down
0000	Counter counts "continuously". 0000 to FFFF→0000 to FFFF→	Counter stops at 0000H.
FFFF	(hunter stops at FFFFH.	Counter counts "continuously". FFFF to 0000→FFFF to 0000→

Gate control

Hardware gate via pulse (→ section 6,6.2)
Hardware gate via level (→ section 6.6.3)

Start: – Pulse at digital input STA
– High level at digital input STA

stop: – Pulse at digital input STO
– Low level at digital input STA

☞ Thegatefunction must be enabled in control register 1/2.

Notes

This operating mode cannot be set unless the gate function has been enabled by the GEN bit (bit 1 in control register 1/2). Otherwise the IOM message is output ("illegal operating mode in status register 3") and the ERROR LED goes on.

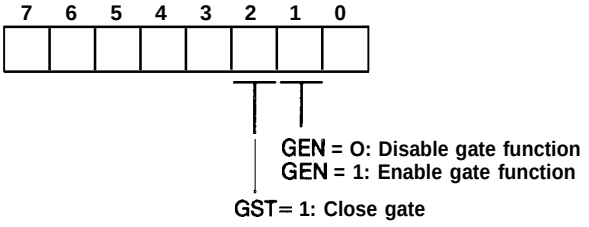
The settings must thus be performed in the sequence listed below.

1. Enable gate function (GEN in control register 1/2)
2. Set operating mode (parameter register 1/2)

Control register 1/2

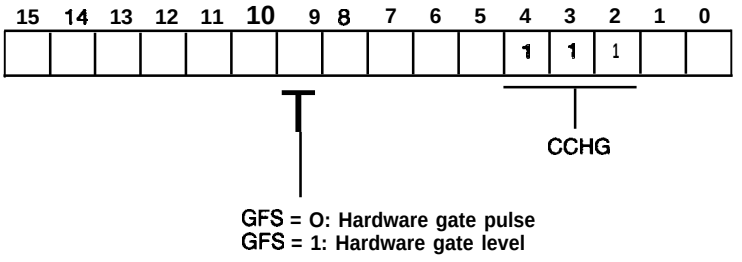
The control register is used for the following purposes.

– Disable/enable the gate function the the GEN bit
– EMERGENCY OFF gate stop with the GST bit



Parameter register 1/2

The operating mode and the type of gate control are set in parameter register 1/2.



6.4 Combination Operating Modes

6.4.1 Overview

Both munters are required for the combination operating modes. The ERROR LED goes on and the IOM bit is set in status register *3* when the plug–in submodule is not installed.

The combination operating modes couple the functions of the counters.

In addition to the combination operating mode, the counting mode, the counting pulse evaluation and the autonomous operating mode must beset for both counters. The permissible settings are shown below.

Combination Operating Mode	Counting Mode		Autonomous Operating Mode		Gate Control	
	Counter 1	Counter 2	Counter 1	Counter 2	Hardware Gate	Software Gate
		1 2 3 4	CONC OCSS/CCSS OCHG/CCHG	CONC OCSS/CCSS OCHG/CCHG		
TCAR	1	+ – – –	◆ + +	– + +	Yes	Yea
	2	+ – –	◆ + +	– + +		
	3	– – + –	◆ + +	– + +		
	4	– – – +	◆ + +	– + +		
TCLR	1	+ – – –	+ + i -	– + +	Yes	Yes
	2	– + – –	◆ + +	– + +		
	3	– – + –	◆ + +	– + +		
	4	– – – +	◆ + +	– + +		
ZMPC	1	● * + +	+ + +	– + +	Yes[1]	Yes[1]
	2	◆ ◆ + +	+ + +	– + +		
	3	◆ ◆ + +	+ + +	– + +		
	4	● * + +	+ + +	– + +		
SC2A	1	+ + + +	+ + +	– + +	Yes	Yes
	2	+ + + +	+ + +	– + +		
	3	+ + + +	+ + +	– + +		
	4	+ + + +	+ + +	– + +		

+ Setting permitted
– Setting not permitted: The ERROR LED goes on and the IOM bit is set in status register 3.
● Setting has no effect: The module does not operate in this setting. The ERROR LED doea not go on and the IOM bit is not set in status register 3.
◆ No practical use

1 In ZMPC operating mode, gate control is only available for counter 1. Gate control for counter 2 has no effect.

When operating mode ZMPC is used, counter 2 must operate with counting pulse evaluation EVDI and counter 1 with EVOT, EVTTor EVFT. The counting pulse evaluation can be selected as desired for all other operating modes.

6.4.2 Transferring the Counting Value to the Interrupt Register (TCAR)

Method of operation

The counting value of counter 1 is entered in the interrupt register of counter 2 when internal gate 1 closes (→ section 6.6).

Gate control

The gate functions available are specified by setting the autonomous operating mode (→ section 6.3) for the individual counters.

☞ An EMERGENCYOFF gatestop (control register 1) does not cause the interrupt value to be transferred.

Load counter

All load capabilities described in section 6.5.1 and allowed by the autonomous operating mode (→ section 6.3) are permitted.

Read counter

All read capabilities are permitted (→ section 6.5.3).

Digital output

All methods of operation are permitted (→ section 6.7).

Interrupt

All interrupt settings are permitted (→ section 4.4).

Special notes

Both counters must operate in the same counting mode. The IOM bit is set in status register 3 and the ERROR LED goes on when two different counting modes are selected.

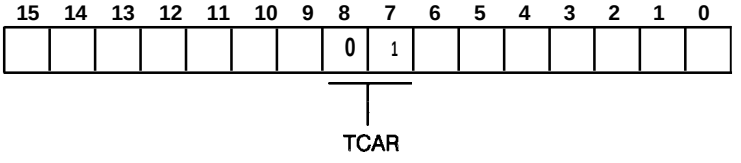
When operating mode TCAR is used, interrupt register 2 (counter 2) cannot be written by the S5.

The interrupt value transferred to counter 2 can be determined by reading counter value register 1 after the internal gate of counter 1 has closed (bit O in status register 1 = O).

Parameter register

Operating mode TCAR is set in parameter register 2.

Parameter register 2



6.4.3 Transferring the Counting Value to the Load Register (TCLR)

Method of operation

The value of counter 1 is entered in the load register of counter 2 when internal gate 1 closes (→ section 6.6).

Gate control

The gate functions available are specified by setting the autonomous operating mode (→ section 6.3) for the individual counters.

☞ An EMERGENCY OFFgate stop (control register 1) does not cause the load value to be transferred.

Load counter

All load capabilities allowed by the autonomous operating mode set are permitted.

Read counter

All read capabilities are permitted (→ section 6.5.3).

Digital output

All methods of operation are permitted (→ section 6.7).

Interrupt

All interrupt settings are permitted (→ section 4.4).

Special notes

Both counters must operate in the same counting mode. The IOM bit is set in status register 3 and the ERROR LED goes on when two different counting modes are selected.

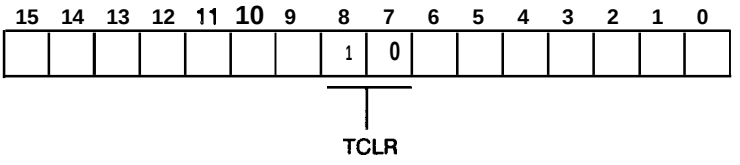
When operating mode TCLR is used, load register 2 of counter 2 cannot be written by the S5.

The load value transferred to counter 2 is determined by reading counter value register 1 after the internal gate of counter 1 has closed (bit O in status register 1 = *O).*

Parameter register

Operating mode TCLR is set in parameter register 2.

Parameter register 2



6.4.4 Connecting the Zero Marking Pulse to Counter 2 (ZMPC)

Method of operation

The zero marking pulse of encoder 1 is the counting signal for counter 2 (zero marking pulse counter). The direction of counting for counter 2 is derived from counting signals A and B of counter 1.

Gate control

Counter 1: – Gate functions specified by the autonomous operating mode set
– All gate functions described in section 6.6

Counter 2: No gate functions available. The zero marking pulses are always transferred to counter 2 (even when the gate of counter 1 is closed).

Load counter

Counter 1: All load capabilities are permitted (→ section 6.5.1).

Counter 2: Only practical via the LOS bit in control register 2

Read counter

All read capabilities are permitted (→ section 6.5.3).

Digital output

All methods of operation are permitted (→ section 6.7).

Interrupt

Counter 1: All interrupt settings are permitted (→ section 4.4).

Counter 2: The gate start and gate stop interrupts cannot be used since counter 2 does not operate with gate functions.

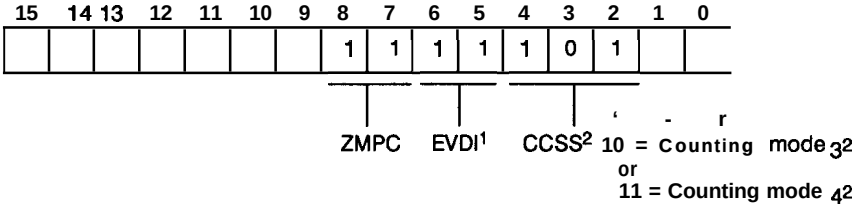
Special notes

The zero marking pulse counter (counter 2) evaluates the rising edge of the zero marking pulse when counting up, and the falling edge when counting down.

Parameter register

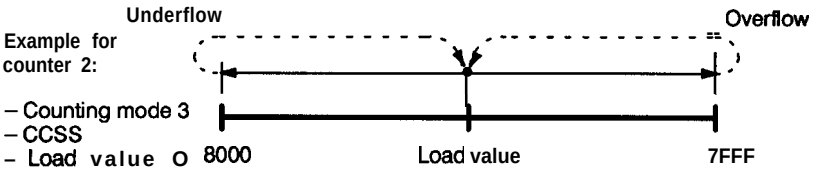
The ZMPC operating mode is set in parameter register 2. The load value should be "O".

Parameter register 2



1 Failure to make these settings will cause the IOM message to occur in status register 3 and the ERROR LED to go on.

2 Recommended setting



6.4.5 Starting Counter2 When the Interrupt Value of Counter 1 Is Reached (SC2A)

Method of operation

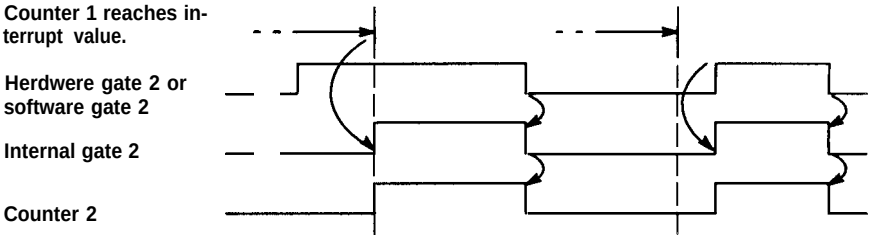
Counter 2 is started when both of the conditions below are met.

- Counter 1 reaches the interrupt value.
- The gate of counter 2 (gate 2) is open.

When counter 1 reaches the interrupt value, the gate function appropriate to the autonomous operating mode set takes effect for counter 2.

Closing of gate 2 (also EMERGENCY OFF gate stop) stops counter 2 and blocks gate function 2. The gate function does not take effect again for counter 2 until interrupt value 1 is reached again.

Example



Gate control

Counter 1:
- Gate functions specified by the autonomous operating mode set
- All gate functions described in section 6.6

Counter 2:
- Same as counter 1 except that the gate function must be enabled by reaching the interrupt value of counter 1

Load counter

Counter 1: All load capabilities described in section 6.5.1 are permitted.

Counter 2: Only practical via LOS bit in control register 2

Read counter

All read capabilities are permitted (→ section 6.5.3).

Digital output

All methods of operation are permitted (→ section 6.7).

Interrupt

All interrupt settings are permitted (→ section 4.4).

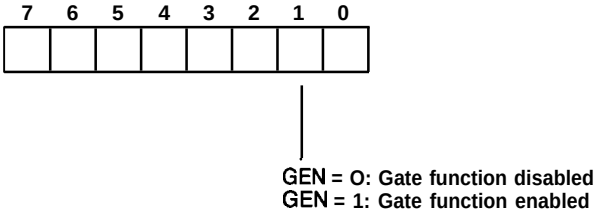
Special notes

The interrupt value of counter 1 is provided with a hysteresis of ±1 (→ section 4.6).

The interrupt at the gate start is also triggered when the interrupt value of counter 1 is not yet reached (i.e., the interrupt is exclusively dependent on the hardware or software gate).

Control register *2*

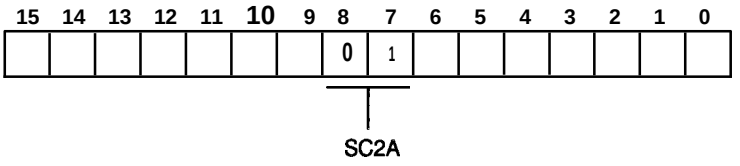
Control register 2



Parameter register

The SC2A operating mode is set in parameter register 1.

Parameter register 1



6.5 Handling the Counters

6.5.1 Loading the Counters

The IP 281 offers several ways to load the counters with a value stored in the load register.

– Loading by the S5
– Loading by zero pulse and SET input (synchronization)
– Loading by operating mode–related loading procedures

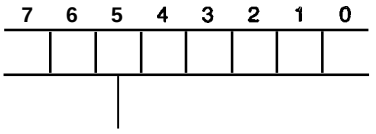
6.5.1.1 Loading by the S5

Method of operation

The counter can be loaded with the load value by the S5 by using the O → 1 edge of the LOS control bit in control register 1/2.

Loading can be performed while the counter is running.

Control register1/2

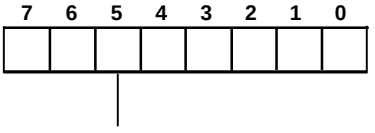


LOS = 0: No effect
LOS = 1: Load counter

Confirmation of loading

The SPE bit is set in the applicable status register 1/2 during when the counter is loaded. The status bit is reset when the status register is read out.

Status register 1/2



SPE = 1: Counter was loaded.
SPE = O: Counter was not loaded.

6.5.1.2 Loading with the Zero Pulse and SET Input (Synchronization)

Method of operation

The respective counter is loaded with the value stored in the load register when the zero pulse occurs. The synchronization can be performed either at the 1st zero pulse or at every zero pulse.

Synchronization can be performed either while counting up or counting down.

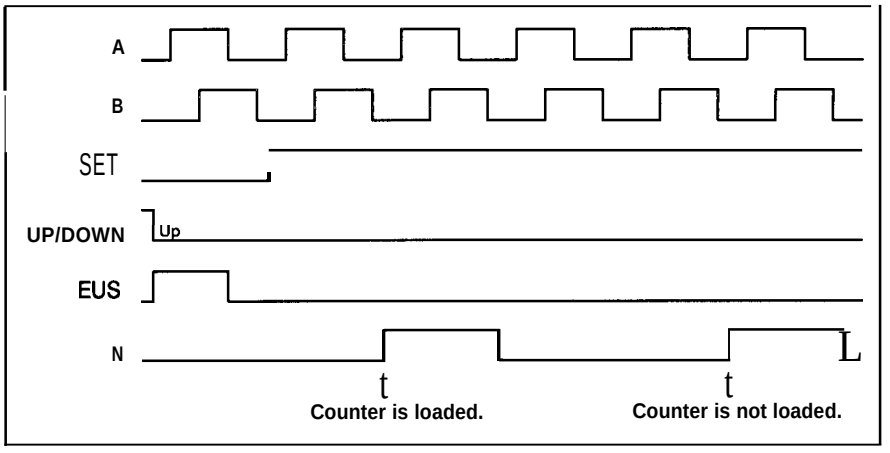
Upward counting synchronization is performed at the rising edge of the zero pulse under the following conditions.

– Enabling has been performed by the EUS control bit.
– The external SET signal is on high level.
– The counter is counting up.

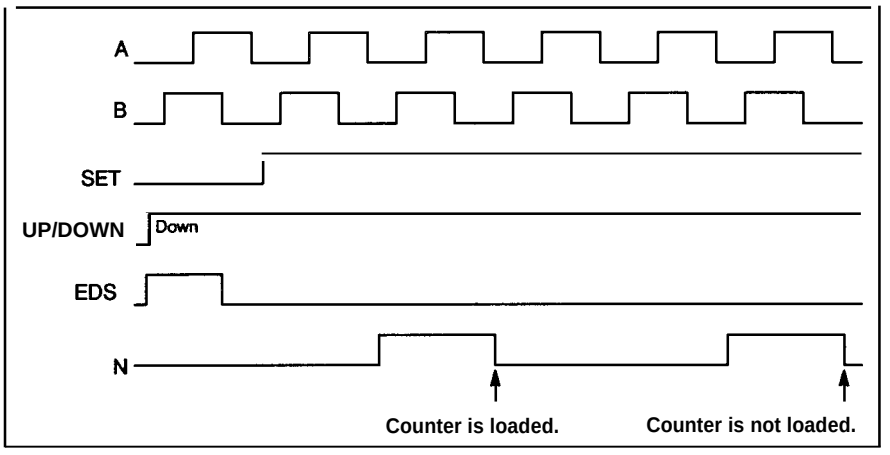
Downward counting synchronization is performed at the failing edge of the zero pulse under the following conditions.

– Enabling has been performed by the EDS control bit.
– The external SET signal is on high level.
– The counter is counting down.

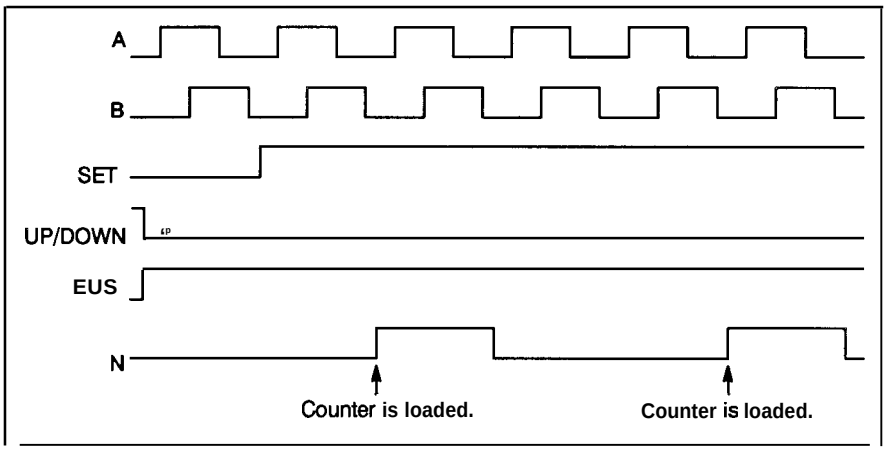
One–time, counting upward, synchronization



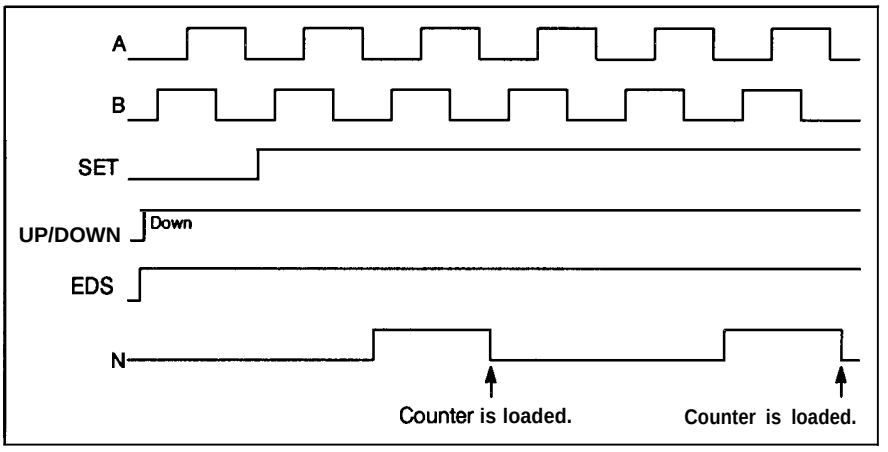
One–time, counting downward, synchronization



Multiple, counting upward, synchronization



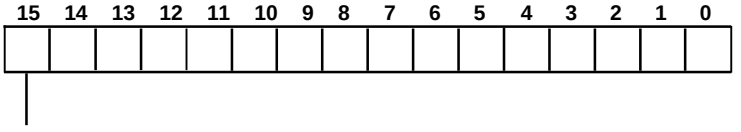
Multiple, counting downward, synchronization



Parameter register

The selection of one–time or multiple synchronization is made in parameter register 1/2 for the respective counter.

Parameter register 1/2

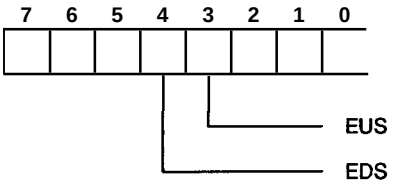


O: One–time synchronization
1: Multiple synchronization

Control register

The EUS bit must be set in control register 1 /2 for upwardcounting synchronization and the EDS bit for downward counting synchronization.

Control register 1/2



One–time: The applicable bit must beset (O → 1 edge required) before the zero pulse occurs.
Multiple: The applicable bit must beset during the entire synchroniza–tion time period.

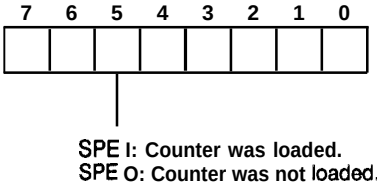
SET input

Synchronization requires that the external SET signal be on high level during synrchonization. The SET signal must occur before the synchronization event.

Confirmation of synchronization

After synchronization has been performed, the SPE status bit (counter loaded) is set in status register 1/2 of the respective counter. This bit is reset when the status register is read.

Status register 1/2



Caution

The digital output must be switched off (EDQ bit in control register 3) during synchronization. This prevents the counter from activating the interrupt function and thus the digital output during synchronization (loading).

6.5.1.3 External Reset of a Counter*

* Under development

6.5.2 Controlling Both Counters Synchronously

Method of operation

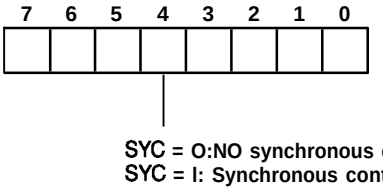
The IP 281 offers the capability of using the software gate to start and stop both counters per software simultaneously. Both software gates are controlled by control register 1.

Requirements

Synchronous control of the counters requires that the two conditions listed below be met.

- Operating mode OCSS or CCSS (any combination) must be set.
- The SYC bit must be set in control register 3.

Control register 3

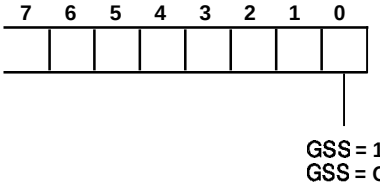


SYC = O:NO synchronous control
SYC = I: Synchronous control of both counters

Start/stop of the counter

Setting the GSS bit in control register 1 causes the software gates to be opened for both counters simultaneously. When the GSS bit is reset, the gates are also closed.

Control register 1



GSS = 1: Gates will be opened.
GSS = O: Gates will be closed.

The GSS bit in control register 2 has no function during synchronous control. The GEN 2 and GST 2 bits retain their function.

6.5.3 Raeding the Counters

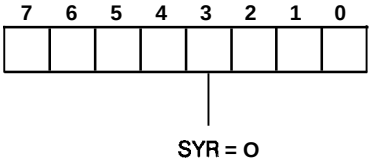
Counter 1 is read by reading counter value register 1 (CVR 1) and counter 2 by reading CVR 2 (→ section 3.5). The counters can be read both separately (asynchronously) and simultaneously (synchronously). The basic setting is asynchronous.

Reading counters asynchronously

The counters are read separately. The counter value in the respective counter value register is retained during the first read access while the read–out takes place.

The SYR synchronous bit in control register 3 must be "O" when the asyn–chronous read access takes place.

Control register 3



Reading counters 1 and 2 synchro–nously

Setting the SYR bit in control register 3 causes the counter values in both counter value registers to be retained simultaneously.

Both counter value registers can then be read.

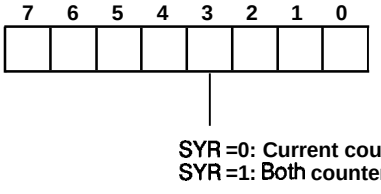
The contents of CVR 1 and 2 are retained until the SYR bit is set to "O" again.

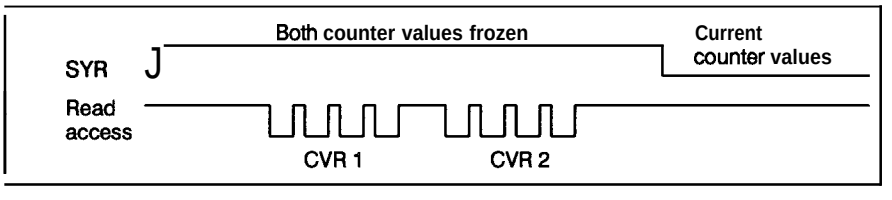
The following sequence must be adhered to for a synchronous read access.

1. **Set SYR bit to "1",**
2. **Read first counter value register.**
3. **Read second counter value register.**
4. **Reset SYR bit to "O".**

If the SYR bit is not reset, thesame value will be read again during the next read access.

Control register 3





6.6 Gate Control

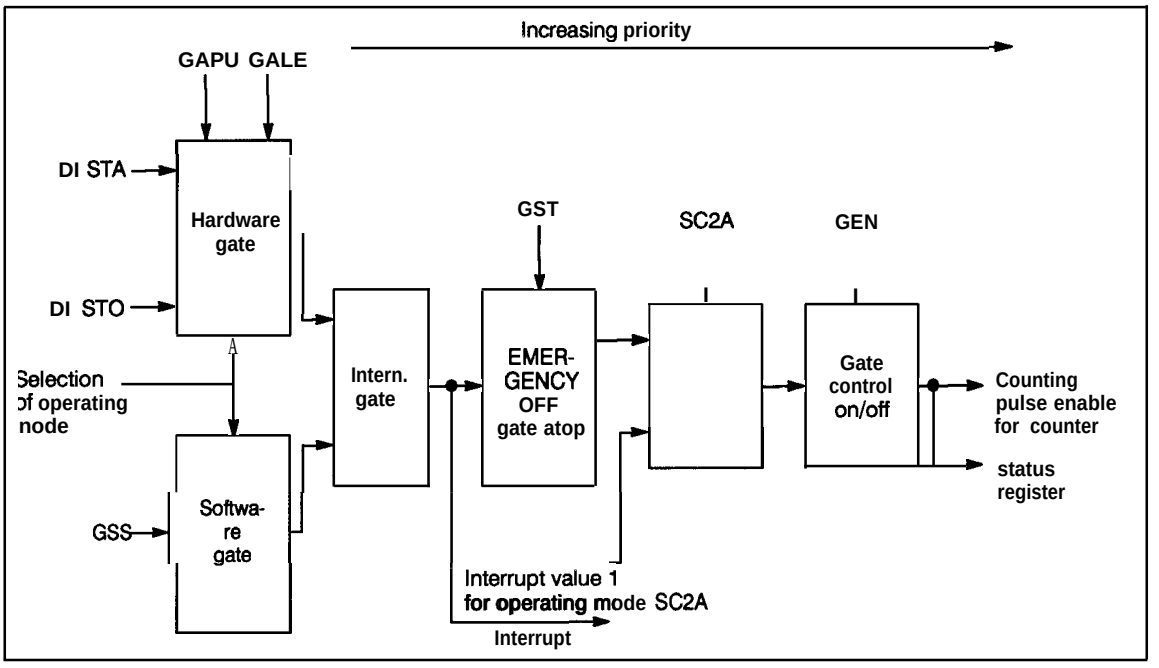
The counters are equipped with a gate control offering the following capabilities.

- **Hardware gate control by level**
- **Hardware gate control by pulse**
- **Software gate control**

The gate control is activated in control register 1/2 for the respective counter. The internal gate can be closed with an EMERGENCY OFF gate stop for all types of gate control.

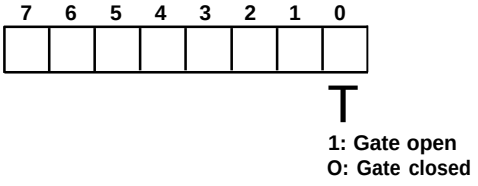
Priorities of the gate control

The following diagram shows the priorities of the gate control.



Gate status

The status of the gate is indicated in status register 1 for counter 1 and status register 2 for counter 2.



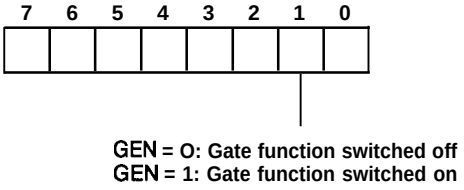
1: Gate open
O: Gate closed

6.6.1 Activating the Gate Control

After the startup of the module, the gate control is switched off (i.e., the gate is open and the counting pulses are forwarded to the counter).

The gate control is switched on/off in control register 1 for counter 1 and in control register 2 for for counter 2.

Control register 1/2

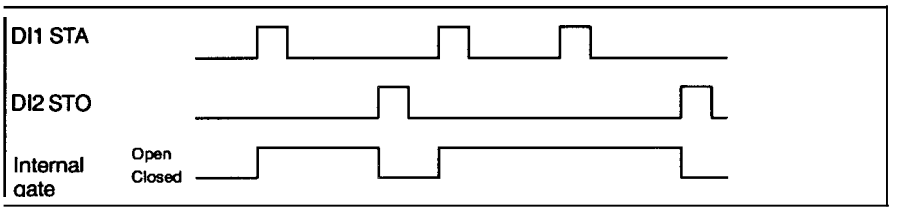


6.6.2 Hardware Gate Control with Pukes (GAPU)

Method of operation

The gate is controlled by pulses on the STA and STO digital inputs.

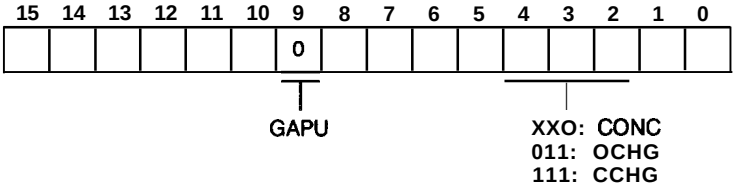
Gate start: – Pulse on the STA input
Gate stop: – Pulse on the STO input



Parameter register

The GAPU hardware gate control is parameterized in parameter register 1 for counter 1 and in parameter register 2 for counter 2.

Parameter register 1/2



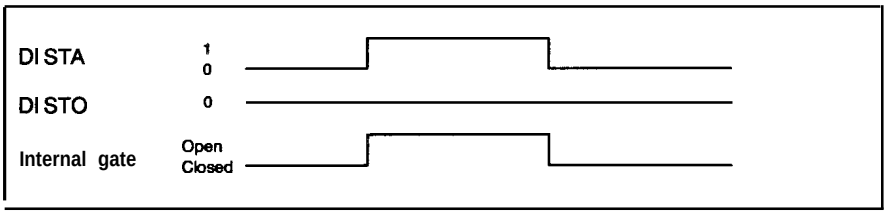
6.6.3 Hardware Gate Control with Level (GALE)

Method of operation

The gate control is performed via level on the STA digital input.

Gate start: – High level on the STA digital input
Gate stop: – Low level on the STA digital input

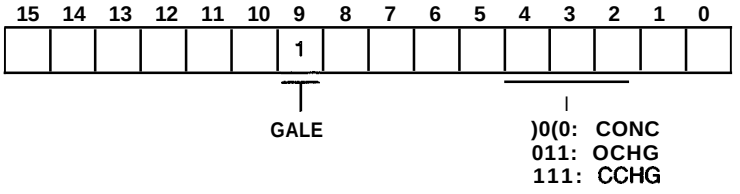
The STO digital input must be applied to 0.



Parameter register

The GALE gate control is parameterized in parameter register 1 for counter 1 and in parameter register 2 for counter 2.

Parameter register 1/2



6.6.4 Software Gate Control

Software gate control must be used when there are no hardware signals from the external system to start and stop the counters, or when this information must first be obtained from the user program in the *S5.*

Method of operation

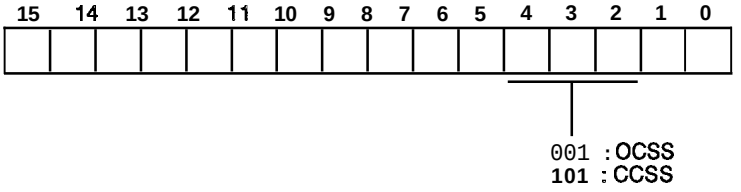
The software gate control is performed with the GSS bit in control register 1 /2.

Gate start: – Setting the GSS bit
Gate stop: – Resetting the GSS bit

Parameter register

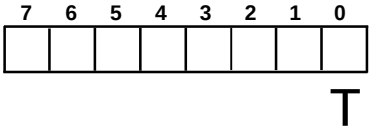
Software gate control can only be used with operating modes OCSS and CCSS. The software gate is activated by parameterizing one of these operating modes in parameter register 1/2.

Parameter register 1/2



Control register

Control register 1/2



GSS = O: Gate will be opened.
GSS = 1: Gate will be closed.

6.6.5 EMERGENCY OFF Gate Stop

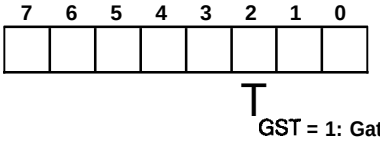
Method of operation

The hardware gate and software gate of the respective counter are closed by setting the GST bit in control register 1/2.

The EMERGENCY OFF gate stop can be used with all operating modes (except counter 2 in operating mode ZMPC) regardless of the type of gate control.

☞ **In operating modes TCLRand TCAR, the EMERGENCYOFF gate stop does not cause the load or interrupt value to be transferred. The EMERGENCY OFF gate stop also does not affect the digital outputs.**

Control register 1/2



GST = 1: Gate will be closed.
GST = O: No effect

6.7 Method of Operation of the Digital Outputs

6.7.1 Overview

Each counter is equipped with a digital output which can be used to directly trigger processes external to the IP 281 (→ section 1.4.3).

The method of operation (i.e., the conditions under which it is activated) of this digital output can be set separately for each counter in parameter register 1/2. Five possibilities are-available.

- **Digital output switched off, DQNU**
- **Digital output active in the range between the interrupt value and underflow, DQAU**
- **Digital output active in the range between the interrupt value and overflow, DQAO**
- **Pulse on the digital output when the interrupt value is reached while counting upward, DQIU**
- **Pulse on the digital output when the interrupt value is reached while counting downward, DQID**

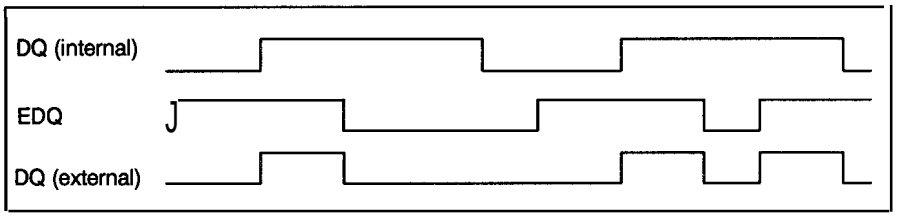
Enabling the digital outputs

The respective digital output is enabled by setting the EDQ 1/2 bit.

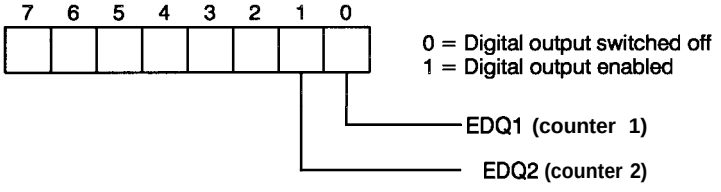
The digital output is switched off (no delay!) by resetting this bit.

Caution

The digital output becomes externally active again when the conditions for an active digital output are met (e.g., minimum pulse still exists), and the digital output is enabled with EDQ).



Control register 3



Basic setting

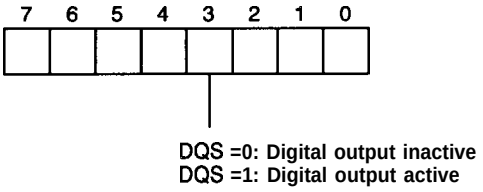
After the startup of the module, both digital outputs are switched off. This means that the following conditions exist.

- DQNU is selected.
- Bit EDQ1 and bit EDQ2 in control register 3 are "0".

Status indication

The status of a digital output (external digital output) is evaluated via the DQS bit in status register 1 or 2.

Status register 1/2



6.7.2 Digital Output Switched Off (DQNU)

Method of operation

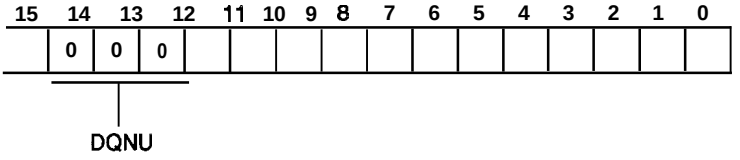
This setting switches the digital output off. This may be necessary to prevent accidental switching (e.g., during synchronization).

When this function is used, the digital output is switched to low level.

When DQNU is transferred while the digital output is active, the output remains active until the end of the minimum pulse.

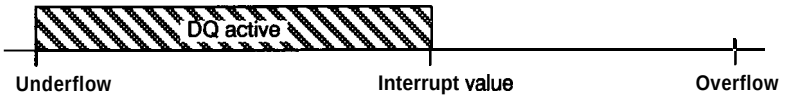
If the output is to be disabled immediately, this can be done with control bits EDQ1 and EDQ2 in control register 3.

Parameter register 1/2



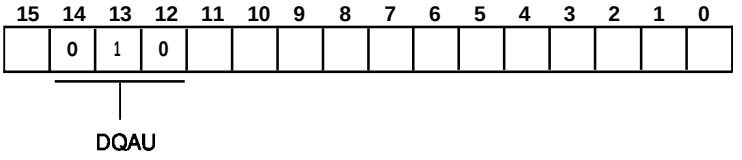
6.7.3 Digital Output Active in the Range Between the Interrupt Value and Underflow (DQAU)

Method of operation



The digital output is switched active when the counting value is in the range from interrupt value to underflow. The output remains active at least for the duration of the pulse set with a plug–in jumper (→ section 1.4.3 and section 2.3).

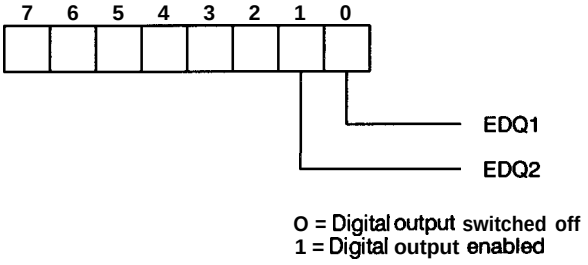
Parameter register 1/2



Control register 3

The respective digital output must be enabled with the EDQ bit in control register 3.

Control register 3



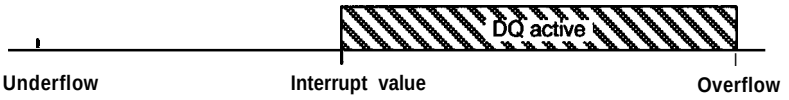
Hysteresis

The following hysteresises take effect on the limits of the active range.

Interrupt value:	Hysteresis for interrupt value (→ section 4.6)
Oveflow/underflow:	Overflow/underflow hysteresis (-t section 6.2.1)

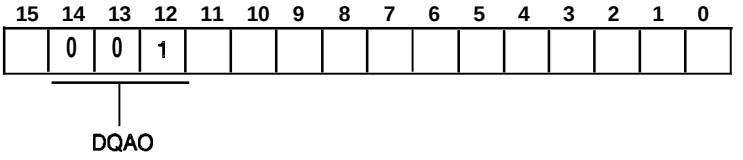
6.7.4 Digital Output Active in the Range Between the Interrupt Value and Overflow (DQAO)

Method of operation



The digital output is switched active when the counting value is in the range from interrupt value to overflow. The output remains active at least for the duration of the pulse set with a plug–in jumper (→ section 2.3).

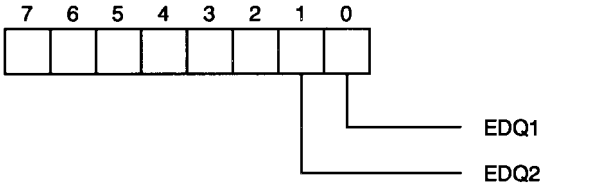
Parameter register 1/2



Control register 3

The respective digital output must be enabled with the EDQ bit in control register 3.

Control register 3



O = Digital output switched off
1 = Digital output enabled

Hysteresis

The following hysteresises take effect on the limits of the active range.

Interrupt value:	Hysteresis for interrupt value (→ section 4.6)
Oveflow/underflow:	Overflow/underflow hysteresis (→ section 6.2.1)

6.7.5 Pulse on the Digital Output When the Interrupt Value Is Reached While Counting Up (DQIU)

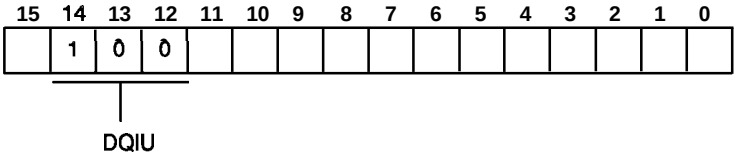
Method of operation

When the counting value reaches the interrupt value while counting up, the digital output is activated for a minimum pulse duration which can be set (10 msec, 100 msec, 500 msec → section 2.3).

The interrupt value is provided with a hysteresis of ±1(→ section 4.6).

A pulse is not triggered when the counting value reaches the interrupt value again while the digital output is still active (the time between the triggering events is less than the minimum pulse duration set). Another pulse cannot be triggered until the digital output is no longer active.

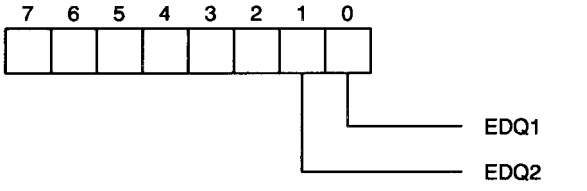
Parameter register



Control register 3

The respective digital output must be enabled with the EDQ bit in control register 3.

Control register 3



O = Digital output switched off
1 = Digital output enabled

6.7.6 Pulse on the Digital Output When the Interrupt Value Is Reached While Counting Down (DQID)

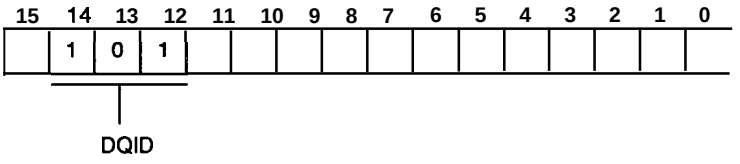
Method of operation

When the counting value reaches the interrupt value while counting down, the digital output is activated for a minimum pulse duration (10 msec, 100 msec, 500 msec → section 2.3),

The interrupt value is provided with a hysteresis of ±1(→ section 4.6).

A pulse is not triggered when the counting value reaches the interrupt value again while the digital output is still active (the time between the triggering events is less than the minimum pulse duration set). Another pulse cannot be triggered until the digital output is no longer active.

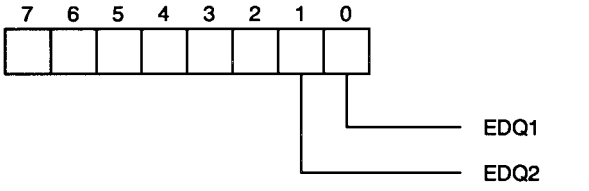
Parameter register



Control register 3

The respective digital output must be enabled with the EDQ bit in control register 3.

Control register 3



O = Digital output switched off
1 = Digital output enabled

6.8 Block Circuit Diagram

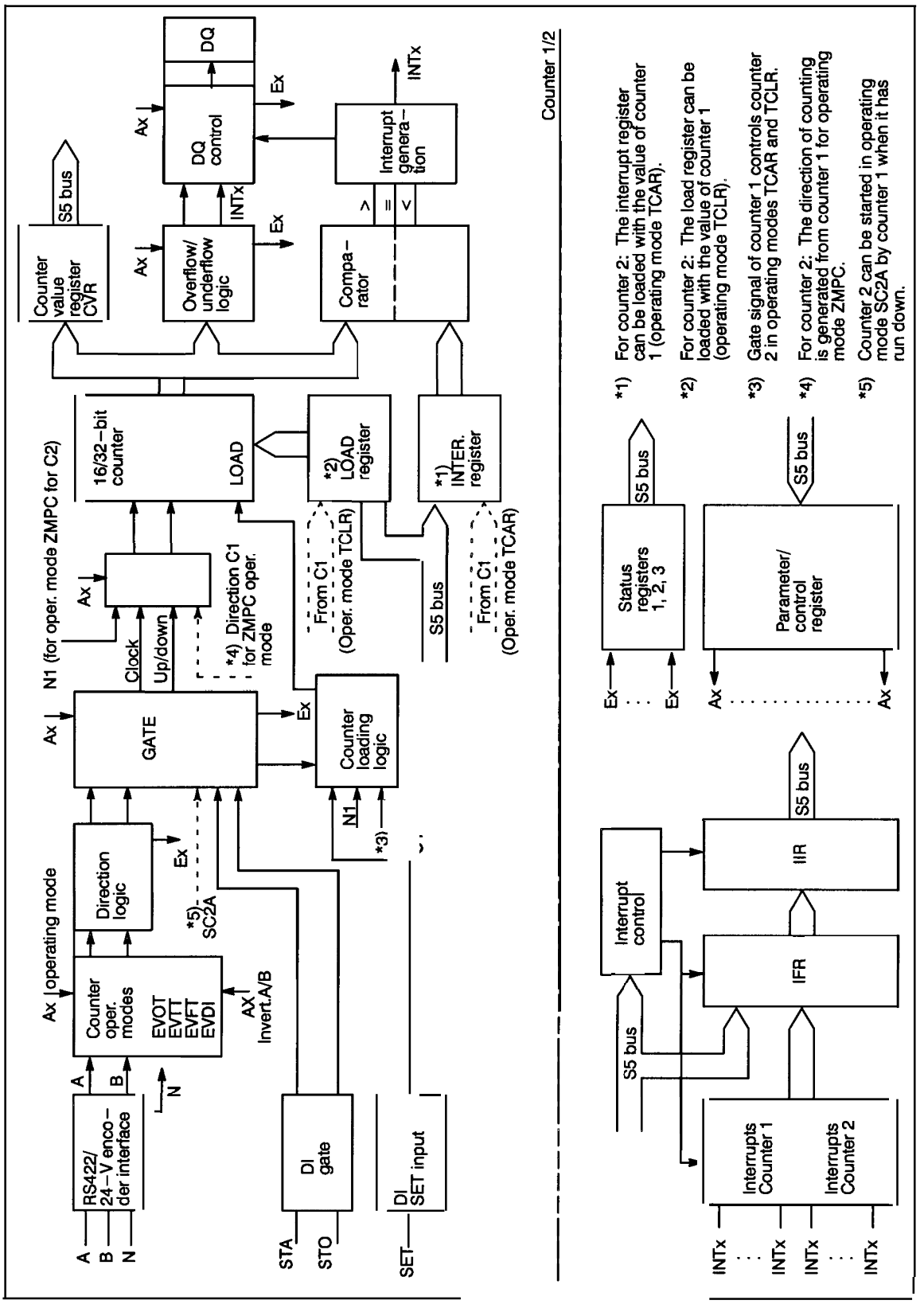


Figure 6.1: Block circuit diagram of the IP 281

7 Programming Example

7 Programming Example

7.1 General

Use

As an introduction working with the IP 281, this section contains a programming example which can be run on PLC S5–115U/S5–115H.
(OB 20 and DX O must be added to the program when PLC S5–135U or S5–155U/S5–I 55H is used.)

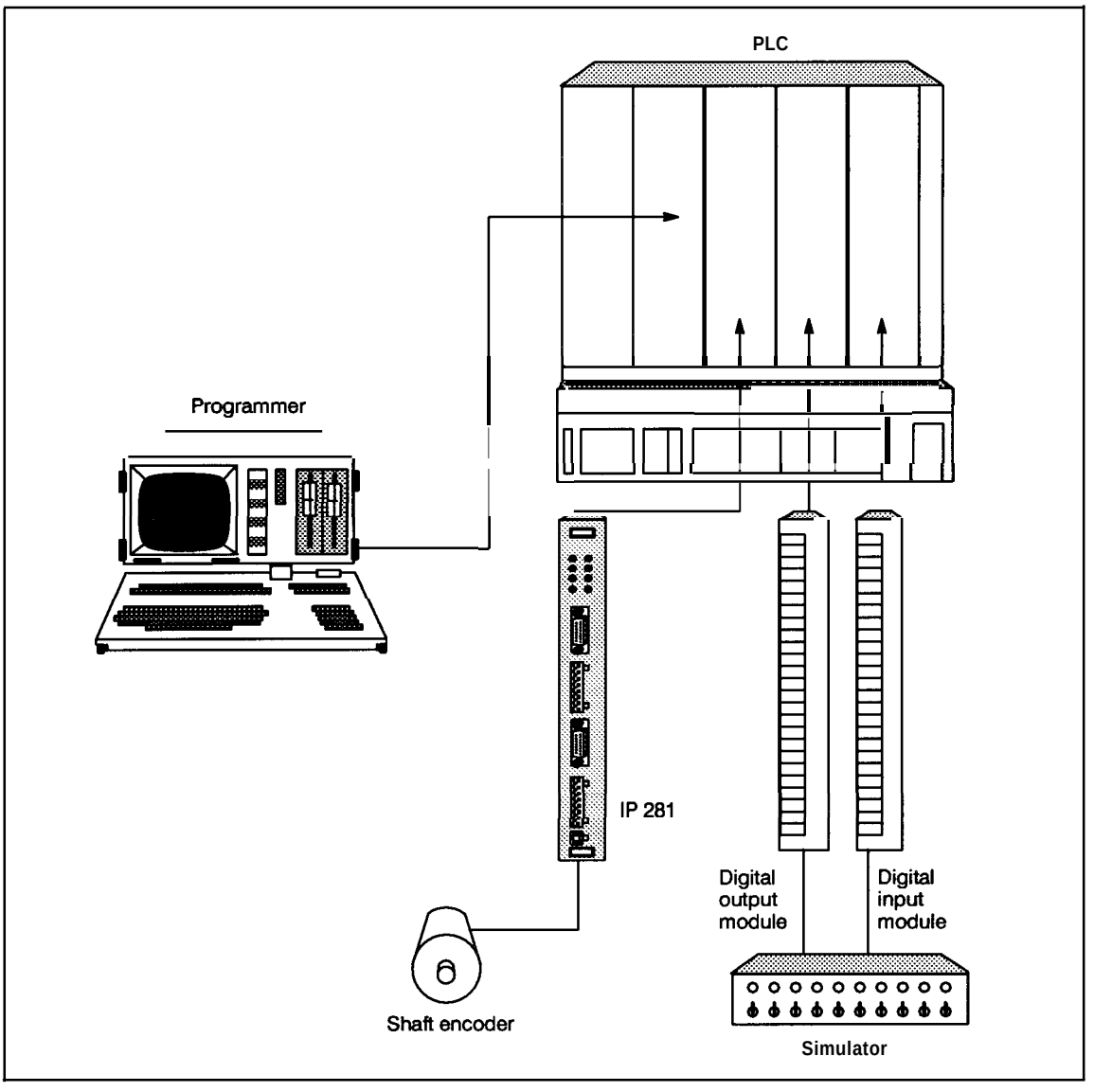
You can use this program as the basis for your own program. The individual blocks must then be adapted or supplemented to suit the application.

Block allocation

Block	Function
OB 1	Cyclic program processing
OB 2	Interrupt-controlled program processing for IRA
OB 21	Startup bahaviorfor manual power-on (STOP –> RUN)
OB 22	Startup behavior for return of voltage
FB 10	Interfaces for inputs/outputs
FB 20	Startup FB for IP 281
FB 21	Cyclic main program
FB 22	Interrupt program
DB 20	Working DB for IP 281

Device configuration

- One **of the programmable controllers listed (→ section 1.2)**
- **Programmer (e.g, PG 685, PG 750)**
- **IP 281 counter module**
- **Encoder with two pulse trains[1] displaced by 90°**
- **Digital input module (e.g.,6ES5420–4UA11)**
- **Digital output module (e.g. 6ES5 421 –4UA11)**
- **Simulator for digital inputs and outputs (e.g.,6ES5788–0LA12)**



1 **The encoder must provide signals in the upward direction or no DQ activation and no interrupt will occur.** An input signal must be inverted **if the direction of rotation is wrong.**

Hardware settings

Set basic address 128 and select interrupt line IRA on the IP 281 counter module (→ section 2.2).

When a 5.2 V encoder in accordance with RS 422 is used, the interface selection and the reference potential must also be changed (→ section 2.3).

Parameterization

The module operates in ZMPC combination mode (zero marking pulse counter). Counters 1 and 2 are parameterized as shown below (→ section 3).

Counter 1

– Gate enable, GEN = 1
– Counting mode 3
– Counting pulse evaluation EVFT
– Autonomous operating mode CCSS
– Counting inputs not inverted
– Digital output enabled
– Method of operation of the digital output, DQAO
– Interrupt at overflow enabled
– Load value: –30000
– Interrupt value: –5000

Counter 2

– Gate enable, GEN = 1
– Counting mode 3
– Counting pulse evaluation EVDI
– Autonomous operating mode CCSS
– Counting inputs not inverted
– Digital output enabled
– Method of operation of the digital output, DQAU
– No interrupt enabled
– Load value: O
– Interrupt value: 50

Method of operation of the counters in the program example

Counter 1 is loaded with load value –30000. When interrupt value –5000 is reached, the digital output is activated (active until overflow). An interrupt is triggered at overflow.

Counter 2 counts the zero marking pulse crossings. It is loaded with the load value O if it reaches the value 100.

The digital output is active from the load value to the interrupt value.

The counting procedure is continually repeated.

7.2 Startup

The module must be parameterized during startup, The module is not equipped with a buffer. Since the parameterization is lost when a power failure occurs or the module is switched off, the parameterization data must be transferred to the IP 281 each time a new start or restart is performed.

OB 21

OB 21 is processed during a manual new start (PG selection and operating mode switch STOP → RUN). It calls startup block FB 20 and working (parameterization) data block DB 20.

OB 22

OB 22 is processed when a restart is performed due to return of voltage (power-on). It is identical to OB 21.

FB 20

The following is performed in the startup FB.

- The register addresses (basic address +0 to basic address +7) are calculated and stored in DB 20 to simplify addressing in the cyclic program.
- The parameter register and control register aretransferred from DB20to the IP 281.
- The parameterization bit is set.

Keep the following in mind.

- Control register 3 must be transferred after parameterization (set parameterization bit).
- When setting the autonomous operating modes (except CONC), the GEN bit must first be set in control register 1/2 for the gate enable, and then the parameter register. Otherwise the ERROR LED goes on.
- When CPU 944A/B is used, the correct addressing sequence must be adhered to.

DB 20

DB 20 is used as parameterization DB and working DB. The addresses (128 +0 to 128 +7) calculated during startup are entered in DW O to DW 7.

In addition, the register contents are stored for the startup in DB 20 (DW 8 to DW 12),

All other register accesses (read and write accesses) are also performed via this DB (DW 13 to DW 30).

DW31 is the storage location for saving the register set address during read and write accesses. The interrupt program accesses this location to update the register set selection again after an interrupt is processed.

7.3 Cyclic Program

Function blocks FB 21 and FB 10, and working data block DB 20 are called by OB 1 in the cyclic program.

FB 21

FB 21 contains the main cyclic program for the IP 281.

The structure of the segments makes it easy to handle the individual program parts (e.g., when setting up your program).

During cyclic operation, the programmed functions are selected one after another. The individual functions (load, read write, etc.) can be made dependent (software links and digital input signals) on certain events.

Keep the following in mind when programming.

- **When the counter value registers are read, the interrupts must be disabled with 1A before the register set is called, and enabled again with RA after the read access.**
- **The selected register set must be saved for all other (not interrupt–disabled) accesses. It must be stored in DW 31 after selection.**
- **If control register 3 is to be transferred, a check in status register 3 must be made before to determine whether the parameterization bit is still set to"1" (parameterization exists), The parameterization bit must then be setto 1 with the OW instruction. If the parameterization bit in status register 3 is set to "O", a new start or restart must be performed to restore the parameterization.**

DB 20

All accesses (read and write) are performed via working data block DB 20.

FB 10

FB 10 provides the allocation to the inputs and outputs. It is only required when a simulator is used.

7.4 Interrupt Processing

OB *2* is called when an interrupt is triggered via IRA. OB 2 calls function block FB 22 and working data block DB 20.

FB 22

The interrupt information register is read in the interrupt program, and at the end of interrupt processing, the register set present before the interrupt arrived is restored again, (The register set address is stored in DW 31 of DB 20.)

The interrupts must be disabled with 1A while the IIR is being read, and then enabled again with RA.

7.5 Program

```
OB 1                                  B: PROBEIST.S5D                    LEN=13

SEGMENT 1                    0000     CYCLIC PROGRAM
0000          :JU    FB     21                    Call FB with cyclic program
0002 NAME     :CYCLIC
0004 DBNR     :      DB     20                    Working data block
0006
0008          :JU    FB     10                    Interface to inputs/outputs
000A NAME     :I/Q
000C
000E          :BE
```

```
OB 2                                  B: ST.S5D                          LEN=9

SEGMENT 1                    0000     INTERRUPT OB FOR IRA
0000          :JU    FB     22                    Call FB with interrupt program
0001 NAME     :INTERUPT
0002 DBNR     :      DB     20                    Working data block
0003          :BE
```

```
OB 21                                 B: PROBEIST.S5D                    LEN=10

SEGMENT 1                    0000
0000          :JU    FB     20                    Call startup FB
0001 NAME     :START-UP
0002 ADR      :      KF     +128                  Basic address
0003 DBNR     :      DB     20                    Working data block
0004          :BE
```

```
OB 22                                 B: PROBEIST.S5D                    LEN=10

SEGMENT 1                    0000
0000          :JU    FB     20                    Call startup FB
0001 NAME     :START-UP
0002 ADR      :      KF     +128                  Basic address
0003 DBNR     :      DB     20                    Working data block
0004          :BE
```

```
FB 10                                 B: PROBEIST.S5D                    LEN=25

SEGMENT 1                    0000     INTERFACE TO INPUT/OUTPUTS
NAME : I/Q

000A          :C     DB     20                    Working data block
000C          :L     DR     24                    Status register 1
000E          :T     QB     8
0010          :L     DR     25                    Status register 2
0012          :T     QB     9
0014          :L     DR     26                    Status register 3
0016          :T     QB     10
0018
001A          :L     IB     4                     Control register 1
001C          :T     DR     8
001E          :L     IB     5                     Control register 2
0020          :T     DR     9
0022          :L     IB     6                     Control register 3
0024          :T     DR     10
00            :BE
```

```
FB 20                              B: PROBEIST.S5D                    LEN=77

SEGMENT 1                  0000    STARTUP FB FOR IP 281
NAME  :START-UP
Decl  :ADR          I/Q/D/B/T/C:  D  KM/KH/KY/KS/KF/KT/KC/KG: KF
Decl  :DBNR         I/Q/D/B/T/C:  B

000B          :DO   =DBNR                          Open working DB
000C          :L    KH  0000                       Calculate addresses and
000E          :T    FW   20                        store in working DB
000F          :LW   =ADR
0010          :T    FW   22
0011    M001  :L    FW   22
0012          :DO   FW   20
0013          :T    DW   O
0014          :L    FW   20
0015          :I         1
0016          :T    FW   20
0017          :L FW      22
0018          :I         1
0019          :T    FW   22
001A          :TAK
001B          :L    KF   +7
001D          :<=F
001E          :JC   =M001
001F
0020          :L    KH   0000                      Select register set O
0022          :DO   DW   O                         Basic address (byte +0)
0023          :T    PY   O
0024          .
0025          :L    DR   8                         Write control register 1
0026          :DO   DW   1                         Address byte +1
0027          :T    PY   O
0028
0029          :L    DR   9                         Write control register 2
002A          :DO   DW   2                         Address byte +2
002B          :T    PY   O
002C
002D          :L    DL   11                        Write parameter register 1
002E          :DO   DW   4                         Address byte +4
002F          :T    PY   O
0030          :L    DR   11                        Address byte +5
0031          :DO   DW   5
0032          :T    PY   O
0033
0034          :L    DL   12                        Write parameter register 2
0035          :DO   DW   6                         Address byte +6
0036          :T    PY   O
0037          :L    DR   12                        Address byte +7
0038          :DO   DW   7
0039          :T    PY   O
003A
O03B          :L    KH   0000                      Select register set O
003D          :DO   DW   O                         Basic address (byte +0)
O03E          :T    PY   O
O03F
0040          :L    DW   10                        Set "parametrization" bit in
0041          :L    KM   0000000000000100          control register 3
0043          :Ow
0044          :DO   DW   3                         Write control register 2
0045          :T    PY   O                         Address byte +3
0046          .
0047          :BE
```

```
FB 21                          B: PROBEIST.S5D                    LEN=208
                                                                  Sheet 1
SEGMENT 1                 0000   MAIN CYCLIC PROGRAM OF THE IP 281
Name :CYCLIC
Decl :DBNR          I/Q/D/B/T/C: B

0008        :***

SEGMENT 2                 0009   READ COUNTER VALUE REGISTER
0009        :DO   =DBNR                          Open working DB
000A        :IA                                  Disable interrupts
000B        :L    KH    0001                     Select register sat 1
000D        :DO   DW    O                        Basic address (byte +0)
000E        :T    PY    0
000F
0010        :DO   DW    O                        Read counter value register 1
0011        :L    PY    0                        Address byte +0 (reg. byte 3)
0012        :T    DL    27
0013        :DO   DW    1                        Address byte +1 (reg. byte 2)
0014        :L    PY    0
0015        :T    DR    27
0016        :DO   DW    2                        Address byte +2 (reg. byte 1)
0017        :L    PY    0
0018        :T    DL    28
0019        :DO   DW    3                        Address byte +3 (reg. byte O)
001A        :L    PY    0
001 B       :T    DR    28
001C
001D        :DO   DW    4                        Read counter value register 2
001 E       :L    PY    0                        Address byte +4 (reg. byte 3)
001 F       :T    DL    28
0020        :DO   DW    5                        Address byte +5 (reg. byte 2)
0021        :L    PY    0
0022        :T    DR    28
0023        :DO   DW    6                        Address byte +6 (reg. byte 1)
0024        :L    PY    0
0025        :T    DL    30
0026        :DO   DW    7                        Address byte +7 (reg. byte O)
0027        :L    PY    o
0028        :T    DR    30
0029        :RA                                  Enable interrupts
002A        :***

SEGMENT 3                 00     READ STATUS REGISTERS 1,2,3
002B        :L    K H   0000                     Select register set O
002D        :T    DR    31                       Store register set
002E        :DO   DW    O                        Basic address (byte +0)
002F        :T    PY    0
0030
0031        :DO   DW    2                        Read status register 1
0032        :L    PY    0                        Address byte +2
0033        :T    DR    24
0034        :DO   DW    3                        Read status register 2
0035        :L    PY    0                        Address byte +3
0036        :T    DR    25
0037        :DO   DW    4                        Read status register 3
0038        :L    PY    0                        Address byte +4
0039        :T    DR    26
003A        :***

SEGMENT 4                 003B   WRITE CONTROL REGISTER
003B        :L    KH    0000                     Select register sat O
003D        :T    DR    31                       Store register set
003E        :DO   DW    0                        Basic address (byte +0)
003F        :T    PY    0
0040
0041        :L    DR    8                        Write control register 1
0042        :DO   DW    1                        Address byte +1
0043        :T    PY    0
0044        :L    DR    9                        Write control register 2
0045        :DO   DW    2                        Address byte +2
0046        :T    PY    0
0047
0048        :DO   DW    4                        Read status register 3
0049        :L    PY    0                        Address byte +4
```

FB 21 B: PROBEIST.S5D LEN=208
Sheet 2

```
004A        :T    DR   26
004B        :TB   D    26.2          Module still parameterizad?
004D        :JC   =CONT               If yes: continue. If no:
004E        :STS                      Stop! New atart required
004F        .
0050 CONT   :L    DW   10           Set "parameterization" bit
0051        :L    KM   0000000000000100  in control register 3
0053        :OW
0054        :DO   DW   3            Write control register 3
0055        :T    PY   0            Address byte +3
0056        .
0057        .***

SEGMENT5          0058   WRITE LOAD REGISTER
0056        :L    KH   0001         Select register set 1
005A        :T    DR   31           Store register set
005B        :DO   DW   0            Basic address (byte +0)
005C        :T    PY   0
005D
005E        :L    DL   15           Write load register 1
005F        :DO   DW   4            Address byte +4 (rag. byte 3)
0060        :T    PY   0
0061        :L    DR   15           Address byte +5 (reg. byte 2)
0062        :DO   DW   5
0063        :T    PY   0
0064        :L    DL   16           Address byte +6 (reg. byte 1)
0065        :DO   DW   6
0066        :T    PY   0
0067        :L    DR   16           Address byte +7 (rag. byte O)
0068        :DO   DW   7
0069        :T    PY   0
006A        .
006B        :L    KH   0003         Select register set 3
006D        :T    DR   31           Store register aat
006E        :DO   DW   0            Basic address (byte +0)
006F        :T    PY   0
0070
0071        :L    DL   17           Write load register 2
0072        :DO   DW   4            Address byte +4 (reg. byte 3)
0073        :T    PY   0
0074        :L    DR   17           Address byte +5 (rag. byte 2)
0075        :DO   DW   5
0076        :T    PY   0
0077        :L    DL   18           Address byte +6 (rag. byte 1)
0078        :DO   DW   6
0079        :T    PY   0
007A        :L    DR   18           Address byte +7 (reg. byte O)
007B        :DO   DW   7
oo7c        :T    PY   0
007D        .***

SEGMENT 6         007E   WRITE INTERRUPT REGISTER
007E        :L    KH   0002         Select register set 2
0080        :T    DR   31           Store register aat
0061        :DO   DW   0            Basic addreas (byte +0)
0062        :T    PY   0
0063        .
0064        :L    DL   19           Write interrupt register 1
0065        :DO   DW   4            Address byte +4 (reg. byte 3)
0066        :T    PY   0
0067        :L    DR   19           Address byte +5 (reg. byte 2)
0088        :DO   DW   5
0069        :T    PY   0
008A        :L    DL   20           Address byte +6 (reg. byte 1)
008B        :DO   DW   6
008C        :T    PY   0
008D        :L    DR   20           Address byte +7 (reg. byte O)
008E        :DO   DW   7
008F        :T    PY   0
0090
0091        :L    KH   0004         Select register set 4
0093        :T    DR   31           Store register set
0094        :DO   DW   0            Basic address (byte +0)
0085        :T    PY   0
```

```
FB 21                          B: PROBEIST.S5D                    LEN=206
                                                                  Sheet 3
0086        .
0097        :L    DL   21                    Write interrupt register 2
0098        :DO   DW   4                     Address byte +4 (reg. byte 3)
0089        :T    PY   0
008A        :L    DR   21                    Address byte +5 (reg. byte 2)
009B        :DO   DW   5
009C        :T    PY   0
009D        :L    DL   22                    Address byte +6 (reg. byte 1)
009E        :DO   DW   6
009F        :T    PY   0
00A0        :L    DR   22                    Address byte +7 (reg. byte O)
00A1        :DO   DW   7
00A2        :T    PY   0
00A3        .***

SEGMENT 7             00A4    WRITE INTERRUPT ENABLE REGISTER
00A4        :L    KH   0001                  Select register set 1
00A6        :T    DR   31                    Store register set
00A7        :DO   DW   0                     Basic address (byte +0)
00A8        :T    PY   0
00A9
00AA        :L    DR   13                    Write IR enable register 1
00AB        :DO   DW   3                     Address byte +3
00AC        :T    PY   0
00AD
00AE        :L    KH   0003                  Select register set 3
00B0        :T    DR   31                    Store register set
00B1        :DO   DW   0                     Basic address (byte +0)
00B2        :T    PY   0
00s3
00B4        :L    DR   14                    Write IR enable register 2
00B5        :DO   DW   3                     Address byte +3
00B6        :T    PY   0
00B7        .***

SEGMENT 8             00B8    LOAD COUNTER 2 AT CERTAIN VALUE
0086        :L DW      30                    Load counter value 2
00B9        :L    KF   +100
00BB        :<F
00BC        :BEC
00BD        :L    KH   0000                  Select register eat O
00BF        :T    DR   31                    Store register set
00C0        :DO   DW   0                     Basic address (byte +0)
00C1        :T    PY   0
00C2
00C3        :L    DR   9
00C4        :L    KM   0000000000100000      Load counter 2 (once)
00C6        :OW
00C7        :DO   DW   2                     Address byte +2
00C8        :T    PY   O
00C9        .***

SEGMENT 9             00CA
00CA        :BE
```

```
FB 22                                B: PROBEIST.S5D                    LEN=33

SEGMENT 1                  0000      INTERRUPT PROCESSING
NAME :INTERUPT
Decl  :DBNR          I/Q/D/B/T/C:  B

0008          ·***

SEGMENT2                   0009      INTERRUPT INFORMATION REGISTER
0009          :DO    =DBNR                          Open working DB
000A          :IA                                   Disable interrupts
000B          :L     KH  0 0 0 0                    Select register set O
000D          :DO    DW  O                          Basic addreea (byte +0)
000E          :T     PY  o
000F
0010          :DO    DW  O                          Read IR information register
0011          :L     PY  o                          Address byte +0 (counter 2)
0012          :T     DL  23
0013          :DO    DW  1                          Address byte +1 (counter 1)
0014          :L     PY  o
0015          :T     DR  23
0016          :RA                                   Enable interrupts
0017          ·***

SEGMENT 3                  0018      LOAD STORED set
0018          :L   DR    31                         Load register set (restore)
0019          :DO   DW   O                          Basic address (byte O)
001A          :T   PY    O
001B          :BE
```

```
DB 20                                B: PROBEIST.S5D                    LEN=46

                                     WORKING DB FOR IP 281
 o:    KF = +00000;                                Byte +0 Basic address
 1:    KF = +00000;                                Byte +1 Addresses are calculated
 2:    KF = +00000;                                Byte +2 during startup and
 3:    KF = +00000;                                Byte +3 stored in DW O to DW 7
 4:    KF = +00000;                                Byte +4
 5:    KF = +00000;                                Byte +5
 6:    KF = +00000;                                Byte +6
 7:    KF = +00000;                                Byte +7
 8:    KM = 0000000000000010;                      (DR 8) Control register 1
 9:    KM = 0000000000000010;                      (DR 9) Control register 2
10:    KM = 0000000000000111;                      (DR 10) Control register 3
11:    KM = 0001000001010110;                            Parameter register 1
12:    KM = 00100001 11110110;                           Parameter register 2
13:    KM = 0000000000000100;                      (DR 13) IR enable register 1
14:    KM = 00000000 00000000;                     (DR 14) IR enable register 2
15:    KH = 0000;                                  Load register 1      Bytes 3 & 2
16:    KF = -30000;                                Load register 1      Bytes 1 & O
17:    KH = 0000;                                  Load register 2      Bytes 3 & 2
18:    KF = +00000;                                Load register 2      Bytes 1 & O
19:    KH = 0000;                                  Interrupt register 1 Bytes 3 & 2
20:    KF = -05000;                                Interrupt register 1 Bytes 1& O
21:    KH = 0000;                                  Interrupt register 2 Bytes 3 & 2
22:    KF = +00050;                                Interrupt register 2 Bytes 1 & O
23:    KM = 0000000000000000;                      IR Information register (2 & 1)
24:    KM = 0000000000000000;                      (DR 24) Status register 1
25:    KM = 0000000000000000;                      (DR 25) Status register 2
26:    KM = 0000000000000000;                      (DR 26) Status register 3
27:    KH = 0000;                                  Counter value reg. 1 Bytes 3 & 2
28:    KF = +00000;                                Counter value reg. 1 Bytes 1 & O
29:    KH = 0000;                                  Counter value reg. 2 Bytes 3 & 2
30:    KF = +00000;                                Counter value reg. 2 Bytes 1 & O
31:    KH = 0000;                                  Store register set
32:    KH = 0000;                                  Use as desired
33:    KH = 0000;                                  Use as desired
34:    KH = 0000;                                  Use as desired
35:    KH = 0000;                                  Uee as desired
36:    KH = 0000;                                  Use as desired
37:    KH = 0000;                                  Use as desired
38:    KH = 0000;                                  Use as desired
39:    KH = 0000;                                  Use as desired
40:    KH = 0000;                                  Use as desired
41:
```

8 Technical Specifications

8 Technical Specifications

8.1 Counter Inputs

Overview 01 Counters 1 and 2	
Number of incremental encoder inputs	per counter
Number of STA digital inputs	par counter
Number of STO digital inputs	par counter
Number of SET digital inputs	par counter
Potential isolation – Between encoder inputs and digital inputs – Between input and output – Between input and S5 bus	 Yes Yes Yes

8.1.1 Incremental Encoder Inputs

24 V Encoder Inputs	
Nominal input voltage	24 V
Input voltage for signal "O"	–3 v to 4.5 v
Input voltage for signal "1"	13 Vto 30 v
Signal status for unconnected inputs	Low
Input current (M–switching encoder)[1] O V to 13 V to 30 V	–11 to –4 to 4 MA
Input current (P–switching encoder)[1] O V to 13 V to 30 V	O to 7.5 to 26 mA
Input current (MP–switching encoder)[1] O V to 13 V to 30 V	O to 7.5 to 26 mA
RS 422 Encoder Inputs	
Maximum differential voltage	5.5 v
Minimum differential voltage	1.4 v
Common mode voltage	Maximum ±7 V
Line termination	150 Ω
Potential isolation – Between 2 differential inputs – Between 2 differential inputs and S5 bus – Between differential input, digital output and digital input	 No No Yes
Maximum line length for maximum frequency and wire break monitor switched on	100 m at 0.2 mm^2 wire cross section

1 Required: Encoder type described in section 1.4.1.1

8.1.2 Digital Inputs

Nominal input voltage	24 V
Input voltage for signal "O"	–3 Vto 4.5 v
input voltage for signal "1"	13 v to 30 v
Signal status for unconnected inputs	Low
Input resistance	1.8 KΩ (average)
Input current for signal "1" (nominal voltage 24 V)	12 mA (average)
Input current (13 V to 30 V)	2.5 MA to 15 mA

8.1.3 Digital Outputs

Number of outputs	1 per counter
Output voltage for signal status "1"	$\geq U_{24Vext}$ –2.5 V
Output voltage for signal status "O"	< 3 V
Nominal output current	500 mA
Maximum output current	600 mA
Maximum delay time, switch on (low –> high)	120 µsec
Maximum delay time, switch off (high –> low)	120 µsec
Limit frequency	≤ 50 Hz
Short circuit proof	Yes
Overload protection	Yes
Pulse duration, can be set	10 msec/100 msec/500 msec
Enable digital outputs*	S5 BASP signal = O and U_{5Vint} within the tolerance range
Potential isolation – Between 2 digital outputs – Between digital output and S5 bus, digital input and 5.2 V encoder supply	 No Yes
Free wheeling diode for inductive loads (relay) required (circuitry → section 1.4.3)	

* ☞ BASP function can bewitched off (→ section 1.4.3).

8.2 Counting Frequencies

This information applies to all counting and digital inputs.	
Maximum counting frequency	250 kHz

8.3 Power Supply

5 V Supply Voltage via Basic Plug Connector XI	
Nominal value	5V
Lower limit	4.65 v
Upper limit	5.25 V
Maximum current consumption	600 mA
24 V Supply Voltage via Front Plug Connector X3	
Static limits (including ripple) – Lower limit – Upper limit	 20V 30 V
Dynamic limits – Lower limit value Duration Recovery time – Upper limit Value Duration Recovery time	 14.25 V 5 msec 10 sac 35V 500 msec 50 sac
Ripple	$\leq$ 3.6 V_{ss}
Maximum current consumption (depends on the output circuitry)	2.5 A
Overcurrent protection	Yes
Voltage monitoring	No
5.2 V Encoder Supply (Option)	
Nominal output voltage	5.2 V
Average output voltage at O A load current	5.20 V
Average output voltage at 350 mA load current	5.15 v
Average output voltage at 700 mA load current	5.10 v
Maximum output current	700 mA (350 mA/counter)
Short circuit proof	Yes
Potential isolation	Yes: from DI,DQ end encoder supply
24 V Encoder Supply	
Nominal output voltage	24 V
Minimum output voltage	17 v
Maximum output voltage	30V
Maximum output current	300 mA
Short circuit proof	Yes
Potential isolation	Yes: from DI, S5 bus and encoder supply

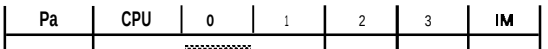
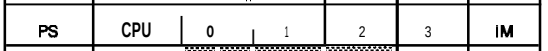
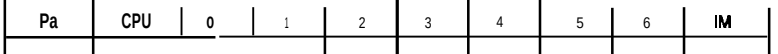
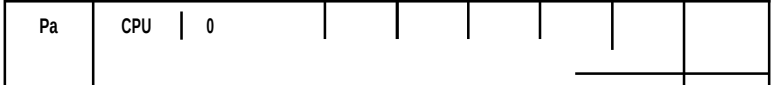
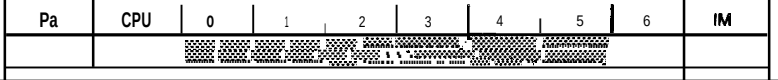
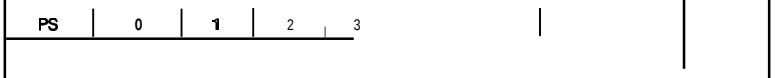
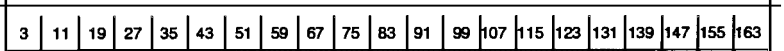
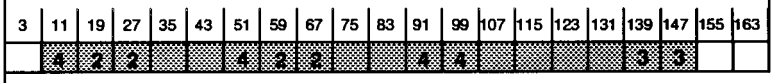
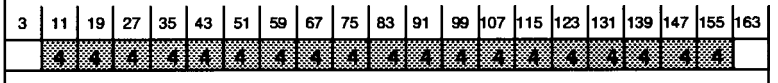
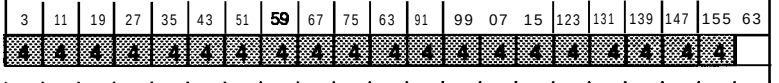
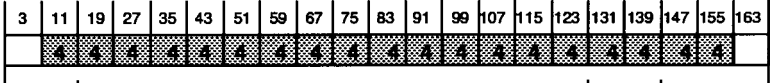
8.4 Environmental Requirements

Climatic Requirement	
Temperature	
– Operation	0" C to 55" C Temperature change 10 K/h Condensation not permitted
– Storage and transportation (in original packaging)	–40" C to 70" C Temperature change 20 K/h
Air pressure	
– Operation	Minimum 660 kPa (= 1500 m. a,s. I.) Maximum 1060 kPa Over this: Limited cooling capacity
– Storage and transportation (in original packaging)	Minimum 660 kPa (= 3500 m. a.s. i.) Maximum 1060 kPa
Mechanical Requirements	
Vibration stress during operation	In accordance with DIN IEC 66-2-6 10 Hz to 56 Hz: 0.075 mm displacement 56 Hz to 500 Hz: 9.8 $msec^{-2}$ (= 1 g)
Transportation stress of device (packed for transportation)	in accordance with DIN IEC 66-2-6 5 Hz to 9 Hz: 3.5 mm displacement 9 Hz to 50 Hz: 9.8 $msec^{-2}$ (= 1 g)
Topple/drop of device (not packaged)	In accordance with DIN IEC 66-2-31 Fall height 50 mm
Falling over (packaged)	in accordance with DIN IEC 66-2-31
Electromagnetic Compatibility	
Radio suppression (interference emission)	In accordance with VDE 0671, limit value class A
Interference immunity against line–conducted interferences on direct current supply and signal lines leaving the device	in accordance with IEC 801 –4 (burst): 1 kV
Interference immunity against static electricity discharge	in accordance with IEC 601 –2: 8 kV
Interference immunity againat HF radiation	In accordance with IEC 601 –3: to 3V/m
Protective and safety Measures	
Protection class	In accordance with VDE 0106–1 (IEC 536) class III (safety extra low voltage)
Degree of protection	
– IP 281 in S5 subrack	IP 20
– IP 281 not installed	IP 00

A fan subassembly is not required.

8.5 In Which Slots Can the Counter Module Be Operated?

The CPUS which can be used are listed in section 1.2.

Programmable Controller in Module **Subrack**		Slot Designation ▒ ≙ IP 281 can be operated in this slot.
Central controller S5-115U	CR 700-0LA	
S5-115u/ S5-115H	CR 700-OLB	
S5-115U	CR 700-1	
S5-115u/ S5-115H	CR 700-2	
S5-115U/ S5-115H	CR 700-3	
Expansion unit	ER 701-3'	
	ER 701-3LH	
Central controller	S5-135U	
Central controller	S5-155U/ S5-155H	
Expansion unit S5-183U		
Expansion unit S5-184U[6]		
Expansion unit S5-185U		
Expansion unit S5-186U		

The IP 281 counter module cannot be installed in expansion units ER 701 –1, ER 701–2 and EU 187U.

1) **Starting with release status 6ES5 701–3LA13, interrupt processing can be used in the expansion unit using optical fiber coupling 6ES5307–3UA1 1 and6ES5317–3UA11.**
2) **Only one interrupt line each available (→ equipment manual of the PLC)**
3) **Only after jumpers on the bus PCB are changed**
4) **Functionality very restricted since interrupt lines are not available.**
5) **Interrupts are only connected via IM307/IM317.**
6) **Only via interface 300–5/312–5 since EU 184U is not equipped with a power supply.**

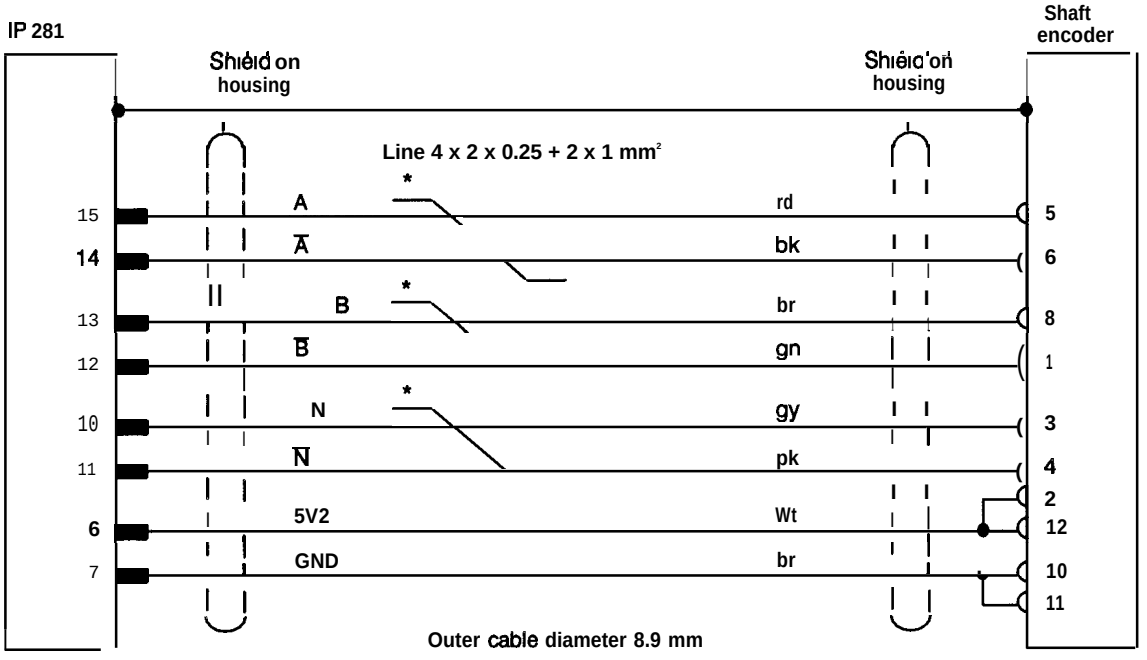
8.6 Connection Cables for Incremental Encoders

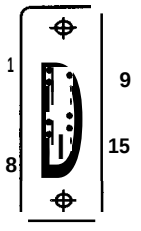
8.6.1 Connection Cable for Siemens Incremental Encoder 6FC9320 (RS 422 with 5.2 V Supply Via IP 281)

Order no: 6ES5 703–1□□□□e ST52.3/54.1 catalog.), max. length 32 m

O Cable exit: bottom
1 Cable exit: top

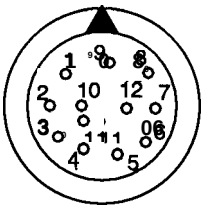
BFO: 5 m
CBO: 10 m
CCO: 20 m
CC5: 25 m
CD2: 32 m





Sub D plug connector
15–way pin (crimp)
Connection side
Metallized housing with screw lock
6FC9 341–IHC

Round plug connector
12–way socket
Connection side
Siemens
6FC9 431–IFD

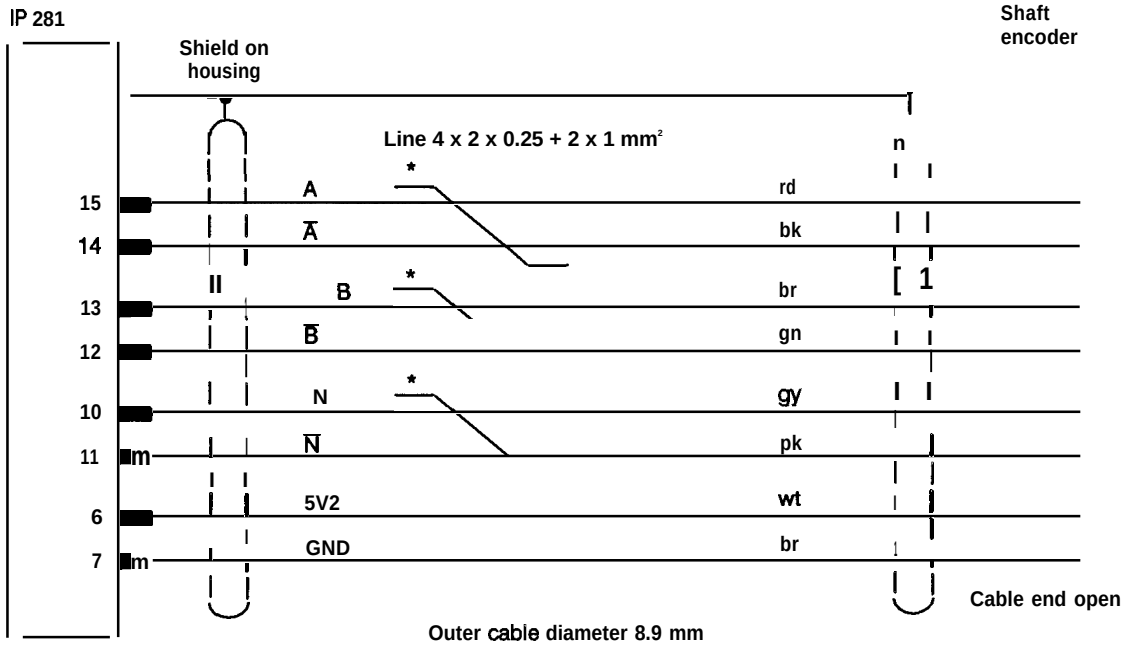


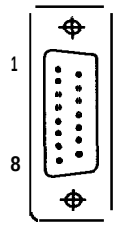
8.6.2 Connection Cable for Incremental Encoder in Accordance with RS 422 (5 V Signals; 5.2 V Supply Via IP 281)

Order no: 6ES5 703–20000 (See ST52.3/54.1 catalog.), max. length 32 m

0 Cable exit: bottom
1 Cable exit: top

BFO: 5 m
CBO: 10 m
CC0: 20 m
CC5: 25 m
CD2: 32 m





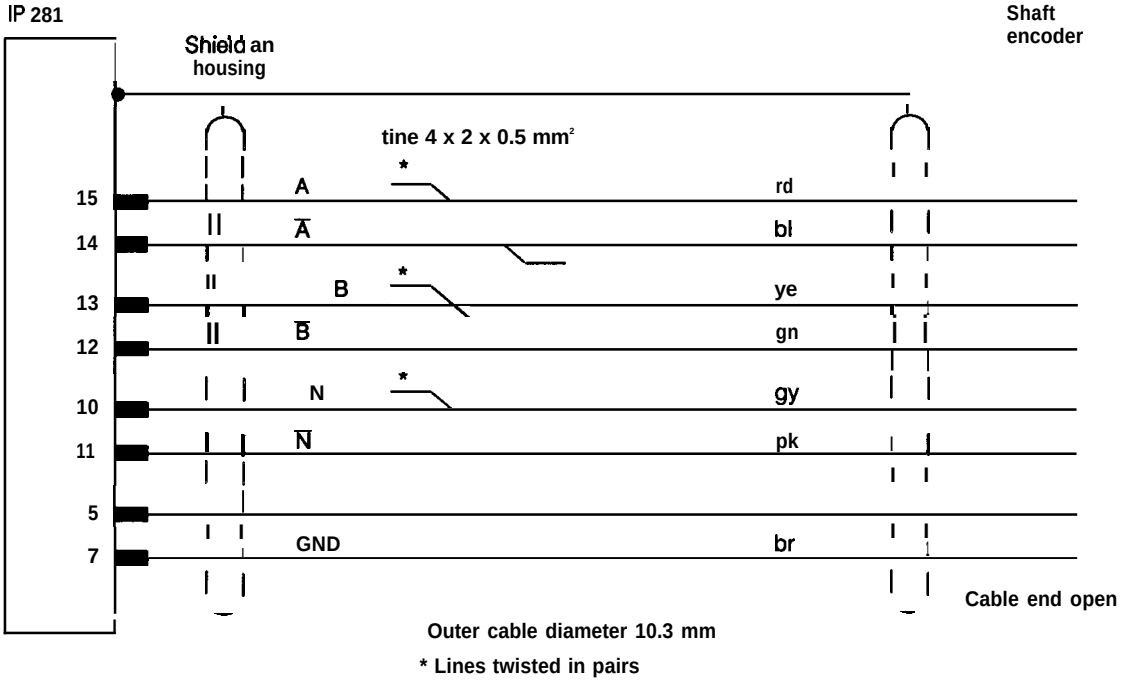
Sub D plug connector
15-way pin (crimp)
Connection side
Metallized housing
with screw lock
6FC9 341–IHC

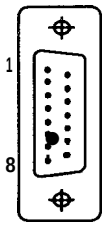
8.6.3 Connection Cable for Incremental Encoder in Accordance with RS 422 (5 V Signals; 24 V Supply Via IP 281)

Order no: **6ES5703–31XIIZU** (See ST52.3/54.1 catalog.), max. length 32 m

O Cable exit: bottom
1 Cable exit: top

BFO: 5 m
CB0: 10 m
CCO: 20 m
CC5: 25 m
CD2: 32 m





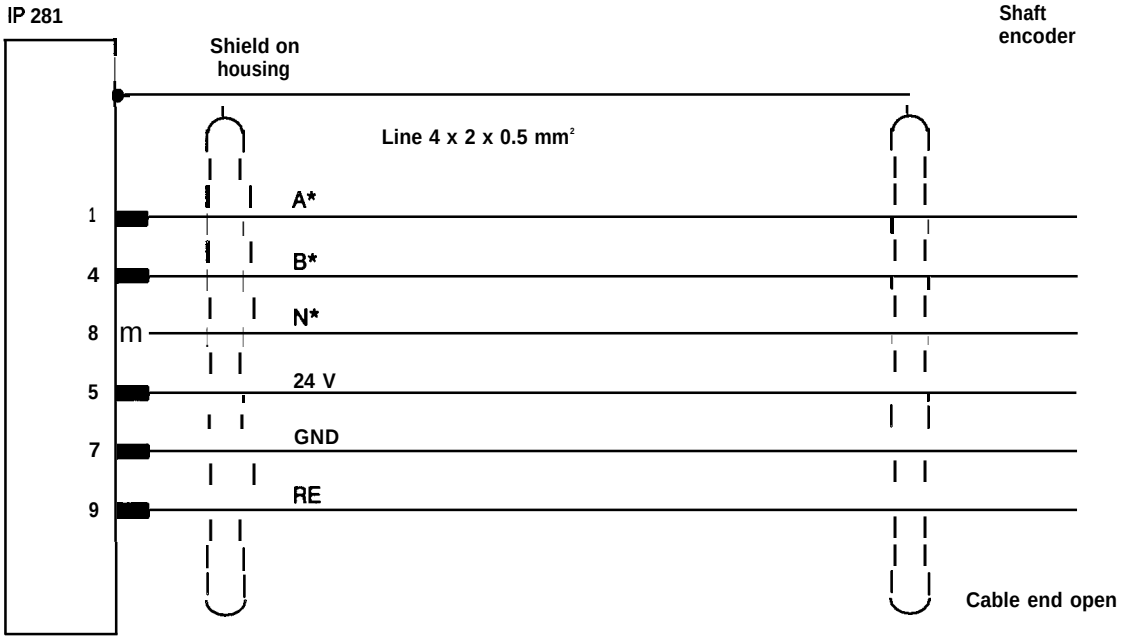
Sub D plug connector
15-way pin (crimp)
Connection side
Metallized housing
with screw lock
6FC9 341-1 HC

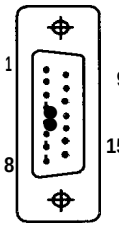
8.6.4 Connection Cable for 24 V Incremental Encoder (24 V Signals; 24 V Supply Via IP 281)

Order no: 6ES5 703–4□□□□e ST52.3/54.1 catalog.), max. length 100 m

O Cable exit: bottom
1 Cable exit: top

BF0: 5 m
CBO: 10 m
CC0: 20 m
CC5: 25 m
CD2: 32 m





Sub D plug connector
15–way pin (crimp)
Connection side
Metallized housing
with screw lock
6FC9 341–IHC

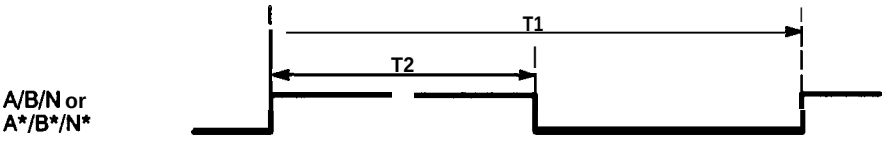
8.7 Requirements on the Input Signals

Precise functioning of the module requires that the input signals on the encoder inputs and digital inputs meet definite specifications with regard to puke width and time in relation to one another.

8.7.1 Pulse Widths of the Encoder Inputs

Counting signals

The input signals on the encoder inputs must have the following minimum puke widths.



24 V encoder

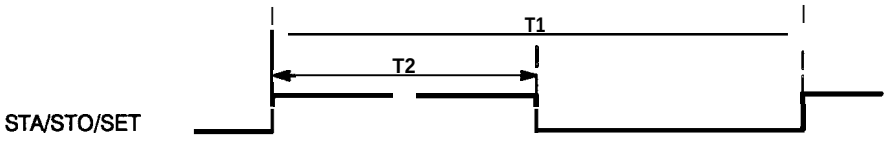
Maximum Counting Frequency	T1min	T2min
250 kHz	4 µsec	1.6 µsec
50 kHz	20 µsec	8 µsec
1 kHz	1 msec	400 µsec

Encoder in accordance with RS 422

Maximum Counting Frequency	T1min	T2min
	4 µsec	1.6 µsec

Signals on digital inputs

The input signals on digital inputs STA, STO and SET must have the following minimum pulse widths.

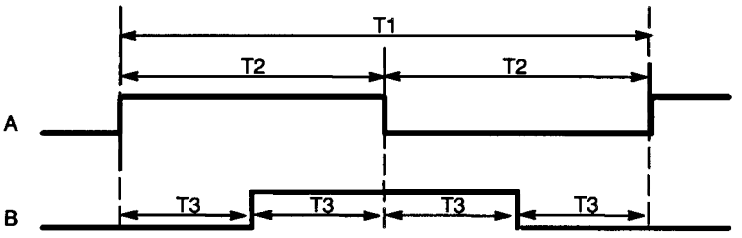


Digital inputs

Maximum Signal Frequency	T1min	T2min
250 kHz	4 µsec	1.6 µsec
25 kHz	40 µsec	16 µsec
0.1 kHz	10 msec	4 msec

8.7.2 Time Relationships Between Counting Signals A and B/A* and B*

The input signals on encoder inputs A and B must meet the following requirements.



Times for encoder inputs

Max. Counting Frequency	T1min	T2min	T3min
250 kHz	4 µsec	1.6 µsec	0.8 µsec
50 kHz	20 µsec	8 µsec	4 µsec
1 kHz	1 msec	400 µsec	200 µsec

8.7.3 Time Tables for Encoder Inputs and Digital Inputs

These tables are the basis for the calculation of time relationships in the following sections.

Times for 24 V encoder inputs

Max. Counting Frequency	Min. Delay, Emin	Max. Delay, Emex
250 kHz	0.5 µsec	1.4 µsec
50 kHz	2.5 µsec	7 µsec
1 kHz	125 µsec	400 µsec

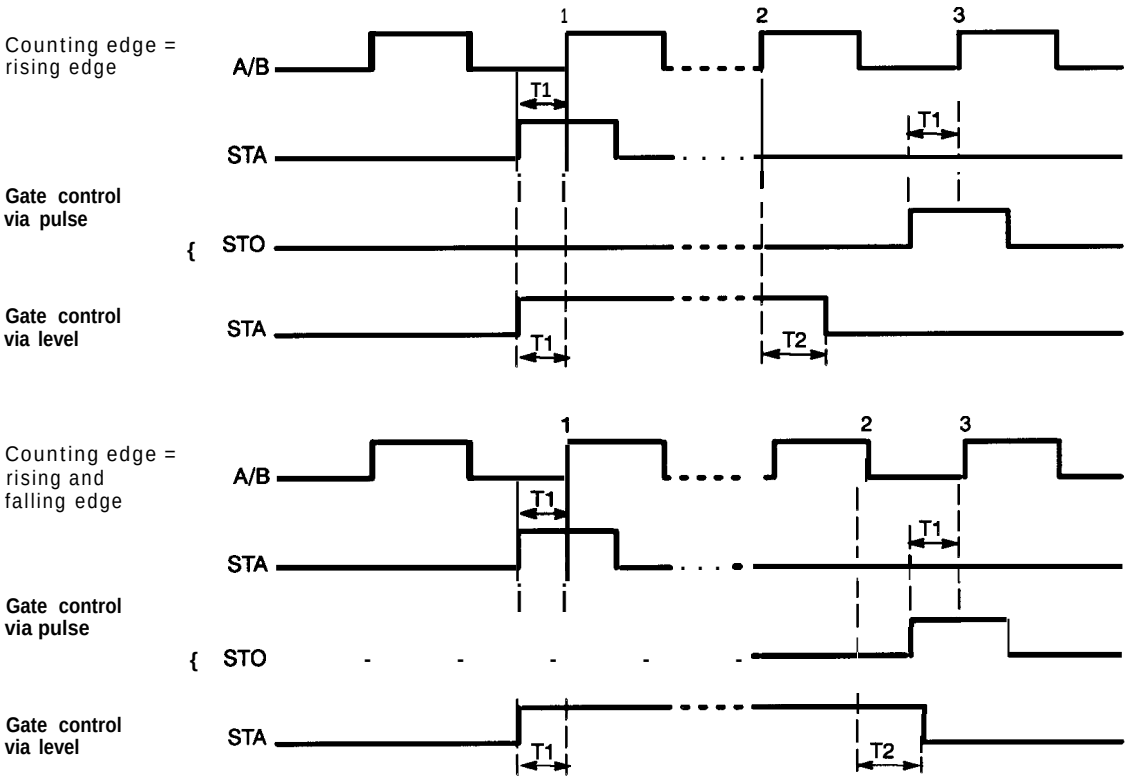
Times for RS 422 encoder inputs

Max. Counting Frequency	Min. Delay, Emin	Max. Delay, Emax
250 kHz	0	300 nsec

Times for digital inputs

Max. Counting Frequency	Min. Delay, DImin	Max. Delay, DImax
250 kHz	0.6 µsec	1.9 µsec
25 kHz	5 µsec	14 µsec
0.1 kz	1.4 msec	3.5 msec

8.7.4 Time Relationships for HW Gate Control



1 = First pulse to be counted
2 = Last pulse to be counted
3 = First pulse not to be counted

T1 min = DImax – Emin + 0.4 µsec
T2min = Emax – DImin + 0.6 µsec

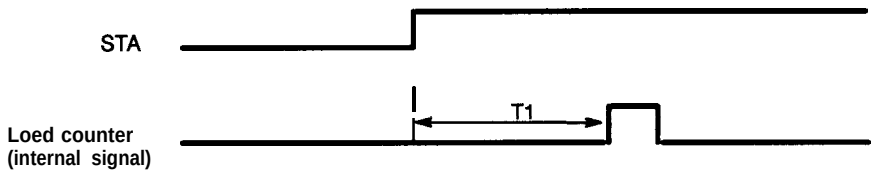
The tables in section 8.7.3 apply.

Although non–adherence to the time relationships will not cause undefined states on the module, the munter may deviate by 1 (more than 1 for high frequencies on the encoder input and large filter constants on the DI).

8.7.5 Time Relationships for Load Procedures

Loading the counter via STA

Operating modes OCHG and CCHG

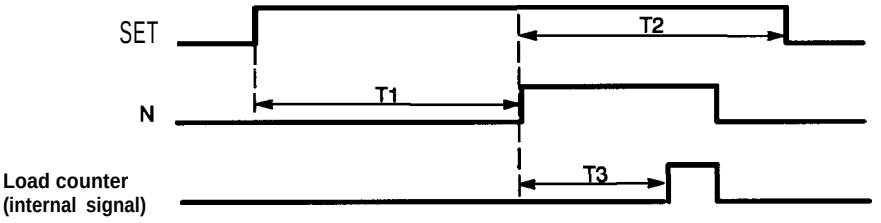


TImin = DImin + 0.7 µsec
TImax = DImax + 0.7 µsec

The time table for DI in section 8.7.3 applies.

Loading the counter via zero pulse (synchronization)

Loading in upward direction

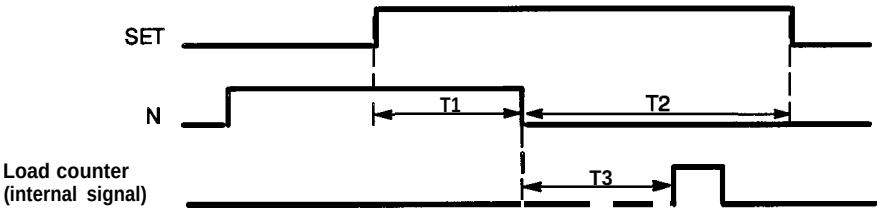


T1 min = DImax – Emin + 0.4 µsec
T2min = Emax – DImin + 0.4 µsec
T3min = Emin + 0.4 µsec
T3max = Emax + 0.4 µsec

The time table in section 8.7.3 applies.

T1 and T2 must be adhered to ensure that the counter is loaded.

Loading in downward direction



T1 min = DImax – Emin + 0.4 µsec
T2min = Emax – DImin + 0.4 µsec
T3min = Emin + 0.4 µsec
T3max = Emax + 0.4 µsec

The time table in section 8.7.3 applies.

T1 and T2 must be adhered to ensure that the counter is loaded.

Definition of Terms

BASP	Disables command output. This signal is sent when the central module goes into stop status. The signal disables the digital outputs.
CCHG	Cyclic counting procedure with hardware gate start, an autonomous operating mode
CCSS	Cyclic counting procedure with software gate start, an autonomous operating mode
CONC	Continuous counting, an autonomous operating mode
CPU	Central processing unit
CRS	Counter running status, the last position of the counter
CVR	Counter value register
DB	Data block
DI	Digital input
DQ	Digital output
DQAO	DQ active from alarm value (i.e., interrupt value) to overflow, a method of operation of the digital output
DQAU	DQ active from alarm value (i.e., interrupt value) to underflow, a method of operation of the digital output
DQID	DQ active for an adjustable impulse duration when the alarm value (i.e., interrupt value) is reached – counting down, a method of operation of the digital output
DQIU	DQ active for an adjustable impulse duration when the alarm value (i.e., interrupt value) is reached – counting up, a method of operation of the digital output
DQNU	DQ not used, a method of operation of the digital output
DQS	DQ status
DW	Data word
EDQ	Enable digital output
EDS	Enable downwards setting
ESD	Electrostatic sensitive devices/modules
EUS	Enable upwards setting
EVDI	Directional evaluation
EVFT	Four–time evaluation

EVOT	One–time evaluation
EVTT	Two–time evaluation
FB	Function Mock
GALE	Level gating (i.e., hardware gate control with level)
GAPU	Pulse gating (i.e., hardware gate control with pulse)
GEN	Gate enable
GFS	Gate function selection (i.e., select type of gate control)
GSS	Gate–start-stop
GST	Gate stop (i.e., EMERGENCY OFF gate stop)
IFR	Interrupt enable register
IIR	Interrupt information register
IOM	Illegal operating mode
IP	Intelligent peripheral (1/0) module
IR	Interrupt
LED	Light emitting diode
LOS	Load per software
OB	Organization block
OCHG	One–time counting procedure with hardware gating (i.e., one–time counting with hardware gate start), an autonomous operating mode
Ocss	One–time counting procedure with software start (i.e., one–time counting with software gate start), an autonomous operating mode
OVF	Overflow, upper counting range limit exceeded
PLC	SIMATIC S5 programmable controller
RESET	Reset pulse for the module
SC2A	Start counter 2 when alarm value (i.e., interrupt value) in counter 1 is reached, a combination operating mode
SEP	Standard slot
SET	Digital SET input
SPE	Setting performed (synchronization)
STA	Digital start input
STEP 5	Programming language used to program the SIMATIC S5 family

STO	Digital stop input
SYC	Synchronous control
SYR	Synchronous read
UNF	Underflow. Lower counting range limit has been passed below.
TCAR	Transfer counting value to alarm register (i.e., interrupt register), a combination operating mode
TCLR	Transfer counting value of counter 1 to load register of counter 2, a combination operating mode
ZMPC	Zero marking pulse of encoder 1 to counter 2, a combination operating mode

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To:
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