SIEMENS

SIMATIC S5

S5-155H
Programmable Controller
(CPU 948R / CPU 948RL)

Volume 1/2

Manual

This manual is part of the documentation package with the order number:
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Edition 06

Safety Guidelines

This manual contains notices which you should observe to ensure your own personal safety, as well as to protect the product and connected equipment. These notices are highlighted in the manual by a warning triangle and are marked as follows according to the level of danger:

Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

Caution

indicates that minor personal injury or property damage can result if proper precautions are not taken.

Note

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

The device/system may only be set up and operated in conjunction with this manual.

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground, and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

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Geschaeftsgebiet Industrie Automatisierungssysteme
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Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

SIEMENS

SIMATIC S5

S5-155H
Programmable Controller
(CPU 948R / CPU 948RL)

Instructions
(S5-155H, Part I)

C79000-B8576-C197-06

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Siemens Aktiengesellschaft C79000-B8576-C197

Preface (How to Use This Manual)

This manual (Volume 1) describes the hardware, startup procedures and functions of the S5-155H programmable controller with CPU 948R or CPU 948RL (R standing for redundant).

Volume 2 of this manual covers programming of the S5-155H, including the writing of the user program, and provides information regarding status, interrupt and error handling, latching functions and debugging aids.

The S5-155H differs from the standard version of the S5-155H programmable controller because of its fault tolerance, which allows it to be operated at a higher level of availability. The ”H” indicates that it has a higher degree of availability than standard systems.

The S5-155H programmable controller system is distinguished by the ”redundancy” of its central controller modules and, depending on how it is configured, of its I/O modules. The I/Os may even have triple redundancy. If a redundant system component fails during a process, the process can still be controlled.

The S5-155H is a 1-out-of-2-system. The system has two CPUs. Faults are specifically defined, thus making it impossible for a given fault to be transported from one subsystem to another. In order to attain a particularly high degree of availability, the input/output area should also be configured for redundancy.

Warning

The S5-155H programmable controller (H system) is not a failsafe system, despite its high availability, fault tolerance and reaction-free design.

It must not be used in installations in which dangerous operating conditions – and thus danger to persons or the environment – could occur as a result of a fault in the programmable controller (for example the highly improbable total failure of both central controllers).

In the case of such safety-related automation tasks, either a failsafe programmable controller (such as an S5-115F which has been type-tested by the TÜV (German Technical Inspectorate) must be used, or the S5-155H must be equipped with suitable interlock controls or protective systems capable of preventing the occurrence of dangerous operating conditions.

Target Group

This manual is intended for engineers, programmers and maintenance personnel with a basic knowledge of SIMATIC S5 systems. If you have any questions that are not answered in the manual, please contact your local Siemens representative.

Notes on the Contents

The following information on the contents of the various chapters is intended to simplify the use of this part of the manual.

Note

The following restrictions apply to the S5-155H programmable controller:

The S5-155H does **not** have multiprocessor capabilities.

When writing your STEP 5 user program for the S5-155H, refer to Section 2.2 for information on avoiding errors or problems on initial startup. If you are careful to observe the restrictions listed there, you will be able to use all STEP 5 user programs which can run on the S5-155U on the S5-155H as well.

Chapter 1: Introduction: System Description

Chapter 1 gives you an overview of the main functions and characteristics of the S5-155U, and outlines its principles of operation. You will find more detailed information in Chapter 2.

Chapter 2: H-Specific System Functions

Chapter 2 presents detailed information on typical characteristics and individual functions of the S5-155H, particularly on operating states and restart types. Additional topics covered in this chapter include ”event-controlled” synchronization and the system self-test for localizing hardware failures. The information on some topics goes into quite a bit of detail, so limit your reading as your necessity or interest dictates.

Chapter 3: CPU 948R / 948RL

Chapter 3 discusses the hardware and technical specifications for the CPU 948R and CPU 948RL central processing units. Some specific topics are the modules' installation, configuration, control elements and indicators.

Chapter 4: I/O Modes and Permissible Modules

Chapter 4 deals with the possible I/O modes in the S5-155U (redundant, switched, one-sided) and the modules which may be used in each case.

If you want to use redundant I/Os, you will find the module connections you require in Section 4.2. Section 4.2 also contains information on standard function blocks FB 40 and FB 43, which are used for analog value input, and on standard function block FB 41, which is used for analog value output.

Be sure to observe the instructions in this chapter when configuring and operating your I/O modules!

Chapter 5: Operating CPs/IPs in the S5-155H

Chapter 5 discusses the use of communications processors (CPs) and intelligent I/Os (IPs) in the S5-155U. It also contains all possible configurations for redundant CP operation.

Chapter 5 also discusses special features regarding the use of data handling blocks for the S5-155H, illustrating their usage in several sample STEP 5 programs.

Chapter 6: Installation and Startup

Chapter 6 discusses the procedures for installing the central controllers and I/Os as well as the IM 304/IM 324R parallel link and IM 304/IM 314R interface modules. It provides step-by-step instructions on configuring and starting your S5-155H using your COM 155H programmer software.

Chapter 6 also describes the jumper settings on the IM 304, IM 314R and IM 324R.

Chapter 7: Time Characteristics of the S5-155H

Chapter 7 deals with the S5-155H's time characteristics, most specifically those instruction execution and system program runtimes which exceed those of the S5-155U due to the S5-155H's fault tolerance.

Chapter 8: Error Diagnostics

Chapter 8 describes all available error diagnostics options for the S5-155H. It contains details on the structure of the error data block (F-DB), in which the system program enters all recognized errors, as well as a list of error codes and their meanings. It also discusses the meaning of the H flag word, from which you can read out information on the status of your PLC or enter instructions for its control.

Chapter 9: Dynamic Response to Faults, Repairs, Replacements and Upgrading

This chapter describes the response of the various modules to faults and failures and shows you how to proceed when making the necessary repairs in order to avoid interrupting operation.

Section 9.6 tells you how you can use certain on-line functions to replace or change your user program on the memory card during operation.

Chapter 10: Typical Applications

Chapter 10 contains sample applications for S5-155H configurations with all three types of I/Os. By implementing these examples, you will have a fault tolerant (H) system that you can use and expand to meet all your requirements.

Chapter 11: Technical Specifications IM 314R/IM 324R

Chapter 11 contains all the major technical specifications for the IM 314R and IM 324R interface modules and the exact pinouts of the backplane and front connectors. You will also find specifications in this chapter on the readback delay which you should take into account when configuring your digital input/output modules.

Chapter 12: Glossary

The glossary defines 155H-specific terms.

Index

The alphabetical index at the end of the manual will help you locate the most important terms in the manual.

Remarks Form

The remarks form at the very end of the manual is provided for your comments and recommendations.

Training

Consult your local Siemens representative for information on training courses to aid you in becoming familiar with this product.

Note

This manual cannot cover all details and types of configuration for the programmable controller, nor can it cover all situations which can occur in installation, operation and maintenance.

If you require further information or have questions on your specific application which are not answered sufficiently here, please contact your local Siemens representative.

Reference Material

It is recommended that you have the following reference material that supports the S5-155H system:

- Catalog ST 54.4: S5-135U, S5-155U and S5-155H Programmable Controllers (Order No. E86010-K4654-A111-A6) *
- S5-135U/155U System Manual (Order No. 6ES5 998-0SH21) *
- PG 685 Programmer (Order No. 6ES5 885-0SC21)) *
- PG 710 Programmer (Order No. C79000–G8576–C170) *
- PG 730 Programmer (Order No. C79000–G8576–C173) *
- PG 750 Programmer (Order No. C79000–G8576–C750) *
- PG 770 Programmer (Order No. C79000–G8576–C770) *
- Programming Package for PC (Order No. 6ES5 896–0SC21) *
- STEP 5 (Order No. C79000–G8576–C140) *
- S5-DOS/ST Manual (Order No. C79000–G8576–C760) *
- You will find a detailed introduction to STEP 5 programming and a description of the functions of the S5-155U programmable controller and its I/O modules in
  - *Automating with the SIMATIC S5-155U* by Hans Berger, Siemens AG, ISBN 3-8009-1561-8

***** Available from your local Siemens representative

Current Information

You can find up-to-date information about SIMATIC products on the Internet under http://www.aut.siemens.de/.

Furthermore, the SIMATIC Customer Support team provides you with current information and downloads which may be useful for users of SIMATIC products:

- On the Internet under http://www.aut.siemens.de/simatic-cs
- Via the SIMATIC Customer Support Mailbox under the number (+49) (911) 895-7100

  To dial in, use a modem with V.34 (28.8 kbps) capability whose parameters you should set as follows: 8, N, 1, ANSI, or dial in using ISDN (x.75, 64 kbit).

You can reach SIMATIC Customer Support by phone using the number (+49) (911) 895-7000 and by fax using (+49) (911) 895-7002. You can also send inquiries by e-mail in the Internet or by mail to the above mailbox.

Notes on the CE Mark for SIMATIC S5

EC Directive on EMC 89/336/EEC

The following applies to the SIMATIC products described in this manual:

Products that carry the CE mark meet the requirements of EC Directive 89/336/EEC “Electromagnetic Compatibility”.

Areas of Use

The following area of use applies for SIMATIC S5 in accordance with this CE mark:

Area of Application	Requirements on	
	Noise emission	Noise immunity
Industry	EN 50081-2: 1993	EN 50082-2: 1995

Observing the Installation Guidelines

The installation guidelines and safety notes given in the S5-135U/155U System Manual must be observed during restart and operation of SIMATIC S5 systems. The following regulations for the use of certain modules must also be observed.

Work on Cabinets

To protect the modules from static discharge, the user must discharge his body’s electrostatic charge before opening a cabinet.

Notes on Individual Modules

Additional measures are required when using the following modules.

A shielded signal cable is required for the following modules:	
Order No.	**Module**
6ES5 432-4UA12	Digital input module 432
6ES5 453-4UA12	Digital output module 453-4
6ES5 457-4UA12	Digital output module 457-4
6ES5 482-4UA11	Digital input/output module 482-4 for IP 257
A filter (SIFI C, B84113-C-B30 or equivalent) is required in the module's 230 V AC load voltage supply of the for the following modules:	
Order No.	**Module**
6ES5 436-4UA12	Digital input module 436-4
6ES5 436-4UB12	Digital input module 436-4
6ES5 456-4UA12	Digital output module 456-4
6ES5 456-4UB12	Digital output module 456-4
A filter (SIFI C, B84113-C-B30 or equivalent) is required in the module's 24 V DC load voltage supply of the for the following modules:	
Order No.	**Module**
6ES5 261-4UA11	IP 261 proportioning module
6ES5 432-4UA12	Digital input module 432
6ES5 453-4UA12	Digital output module 453-4
6ES5 457-4UA12	Digital output module 457-4
6ES5 465-4UA12	Analog input module 465-4
6ES5 470-4UB12	Analog output module 470-4

Low-Voltage Directive 73/23/EEC

The products listed below fulfill the requirements of EC Directive 73/23/EEC "Low-Voltage Directive". Adherence to this EC Directive was tested in accordance with IEC 1131-2.

Name	Order Number
Central controller 188 230V/18A	6ES5 188-3UA12
Central controller 188 230V/40A	6ES5 188-3UA22
Central controller 188 24V/18A	6ES5 188-3UA32
Central controller 188 24V/40A	6ES5 188-3UA52
Expansion unit 183U 230V/18A	6ES5 183-3UA13
Expansion unit 185U 230V/18A	6ES5 185-3UA13
Expansion unit 185U 220V/40A	6ES5 185-3UA33
Expansion unit 185U 24V/18A	6ES5 185-3UA23
Expansion unit 185 24V/40A	6ES5 185-3UA43
Expansion unit 183U	6ES5 183-3UA22
Digital input module 435-4 (24-60 V AC)	6ES5 435-4UA12
Digital input module 436-4 (115-230 V AC)	6ES5 436-4UA12
Digital input module 436-4 (115-230 V AC)	6ES5 436-4UB12
Digital input module 455-4 (24-60 V AC)	6ES5 455-4UA12
Digital input module 456-4 (115-230 V AC)	6ES5 456-4UA12
Digital input module 456-4 (115-230 V AC)	6ES5 456-4UB12

Safety Requirements for Installation

The SIMATIC S5-135U/155U and 155H programmable controllers and the 155H central controller are "open type" equipment according to the IEC 1131-2 standard and therefore adhere to the EC Directive 73/23/EEC low-voltage directive and are UL/CSA certified as such.

To fulfill requirements for safe operation with regard to mechanical stability, flame retardance, stability, and shock-hazard protection, the following alternative types of installation are specified:

- Installation in a suitable cabinet
- Installation in a suitable housing
- Installation in a suitably equipped, enclosed operating area.

Installation in a cabinet is obligatory for the following listed products (reason: protection against accidental contact):

Name	Order Number
Expansion unit 184U	6ES5 184-3UA11
Expansion unit 184U	6ES5 184-3UA21
S5-135U 24V/10A	6ES5 135-3UA42

Declaration of Conformity

In accordance with the above-mentioned EC Directive, the EU declarations of conformity are held at the disposal of the competent authorities at the address below:

Siemens AG
Automation Group
AUT 14
Postfach 1963
D-92209 Amberg

Products that do not carry the CE mark fulfill the requirements and standards as specified in the S5-135U/155U System Manual in the chapter on general technical specifications.

Updated Technical Data

Contrary to the specifications in the "General Technical Specifications" of the System Manual, the specifications listed below for noise immunity and electromagnetic compatibility apply for modules which carry the CE mark.

The specifications are valid for devices which are installed in accordance with the above-mentioned installation guidelines.

Noise immunity, electromagnetic compatibility (EMC)	
RFI suppression limit value class	To EN 55011 A 2)
Conducted interference on AC supply lines (230 V AC) to EN 61000-4-4 / IEC 1000-4-4 (burst) to IEC 1000-4-5 between two lines (µs pulses) between line and ground (µs pulses)	 2 kV 1 kV 2 kV
DC supply lines (24 V DC) to EN 61000-4-4 / IEC 1000-4-4 (burst)	2 kV
Signal lines to EN 61000-4-4 / IEC 1000-4-4 (burst)	2 kV 1)
Immunity to discharge of static electricity to EN 61000-4-2 / IEC 1000-4-2 (ESD) 2)	Immunity of 4 kV contact discharge (8 kV air discharge) is ensured with proper installation (see Installation Guidelines in the S5-135U/155U System Manual)
Immunity to electromagnetic RF field 2) amplitude-modulated to ENV 50140 / IEC 1000-4-3	80 to 1000 MHz 10 V/m 80% AM (1kHz)
Immunity to electromagnetic RF field 2) pulse-modulated to ENV 50204	900 MHz 10 V/m 50% ED
Immunity to high-frequency sinusoidal to ENV 50141	0.15 to 80 MHz 10 V 80% AM

1) Signal lines which do not serve to control the process, for example, connections to external I/O devices etc.: 1 kV
2) When cabinet door is closed

Notes for Machine Manufacturers

Introduction

The SIMATIC programmable controller is not a machine in the sense of the EC Directive on machines. Therefore, there is no declaration of conformity for SIMATIC as regards the EC Directive 89/392/EEC on machines.

EC Directive 89/392/EEC on Machines

The EC Directive 89/392/EEC on machines controls machine requirements. Here, a machine is understood to be the entire sum of devices or parts involved (see also EN 292-1, paragraph 3.1).

SIMATIC is part of the electrical equipment for a machine and must therefore be included in the procedure for checking conformity by the machine manufacturer.

Electrical Equipment for Machines to EN 60204

The EN 60204-1 standard (machine safety, general requirements for the electrical equipment for machines) applies to the electrical equipment for machines.

The following table should help you with the declaration of conformity and shows which criteria apply to EN 60204-1 (as at June 1993) for SIMATIC.

EN 60204-1	Subject/Criterion	Remarks
Para. 4	General requirements	Requirements are fulfilled if the machines are assembled/installed according to the installation guidelines. See also the explanations on the previous pages.
Para. 11.2	Digital I/O interfaces	Requirements are fulfilled.
Para. 12.3	Programmable equipment	Requirements are fulfilled if the machines are installed in lockable cabinets to protect them from memory modifications by unauthorized persons.
Para. 20.4	Voltage tests	Requirements are fulfilled.

Contents

Introduction to the Installation and Operation of the S5-155H Programmable Controller

1

The S5-155H is a fault-tolerant programmable controller for machine and plant control. It is an event-synchronized master-standby system with a 1-out-of-2 structure. A data link connects line the master to the standby controller.

This introduction is intended to familiarize you with some typical characteristics of the S5-155H, and is aimed especially at those users who are already acquainted with the S5-155U. It has been assumed that the reader is familiar with the S5-155U’s functionality.

1.1 Characteristics and Functions of the S5-155H Programmable Controller

S5-155H Performance Characteristics

The S5-155H with CPU 948R is based on the S5-155H with CPU 946R/947R, but its system performance capabilities have been expanded and considerably improved:

- The most important innovations in the S5-155H with CPU 948R are
  - its expandability to as many as 192 redundant analog I/O channels,
  - its fault-tolerant analog outputs,
  - its utilization of the CPU 948's functionality,
  - higher processing speed,
  - page access to one-sided IP/CP permitted,
  - more accurate error locating of configuration errors in the list of the cyclic DB/DX,
  - the range limit for the redundant/one-sided I/O must no longer be configured, i. e. switched, one-sided and redundant I/Os can be mixed.
- Configurable redundancy enables economical solutions (one, two or three-channel I/O operation).
- Redundant operation of digital and analog I/O modules.
- NON-STOP operation of redundant I/Os in the S5-155H. The system program supports non-stop operation of redundant I/Os with extensive self-tests for detecting and localizing errors quickly.
- On-line repair of defective I/Os, thus avoiding interruptions in programmable controller operation.
- The support of the COM 155H programmer software, a special program package with its own reference manual, in system configuring and error diagnostics.

Important

The S5-155H can be operated non-stop.

This means it tolerates the first failure of each **redundant** hardware component. The failed components can be repaired without interrupting operation.

Please note that the S5-155H will fail a) partially or b) completely when the standby component fails before the original fault has been rectified.

a) A partial failure will result if; e.g., after a redundant input module fails, its standby module also fails before the original module can be repaired.

b) The system will fail completely if; e.g., after a central controller fails, the second central controller also fails before the first can be repaired.

The faster a component is repaired, the lower the risk of further failures.

1.2 S5-155H Applications

Fault-Tolerant Systems

The S5-155H can perform extensive, complex automation tasks while providing a high degree of fault tolerance.

In the majority of cases, fault-tolerant systems continue operation even when one or more faults result in failure of peripheral or central controller components.

Fault-tolerant systems should always be used when it is necessary to keep the probability of a total control system failure (for example a cooling pump control system) to a minimum.

Based on cost, applications for a fault-tolerant programmable controller system can be divided into two categories:

- High production downtime costs per unit of time. Example: Assembly line production.
- High costs even for brief production downtimes. Example: Industrial processes.

Danger

The S5-155H must never be used in plants or installations in which a programmable controller fault or malfunction could result in danger to persons, machines or the environment. Safety-related automation tasks of this nature require the use of a programmable controller which was prototype-tested by the TÜV (German Technical Inspectorate), or the programmable controller must be equipped with suitable interlocks or protective systems which prohibit the occurrence of dangerous operating states.

Fail-Safe Systems

Please note that there is a distinct difference between a fault-tolerant system and a failsafe system.

A fail-safe system also has a redundant component configuration, but enters the STOP mode (in the case of two-out-of-two redundancy) in the event of a fault.

1.3 Redundant S5-155H Configuration

Structure

The S5-155H (central controller) always has a redundant configuration. It consists of two S5-135U/155U central controllers. Three (combinable) I/O redundancy structures are possible:

- One-channel I/O module configuration (”switched”);
- Two-channel (1-of-2) I/O module configuration;
- Three-channel (1-of-3) module configuration.

One-Channel Configuration

A one-channel I/O module configuration should be used when the application requires only central controller redundancy (Figure 1-1).

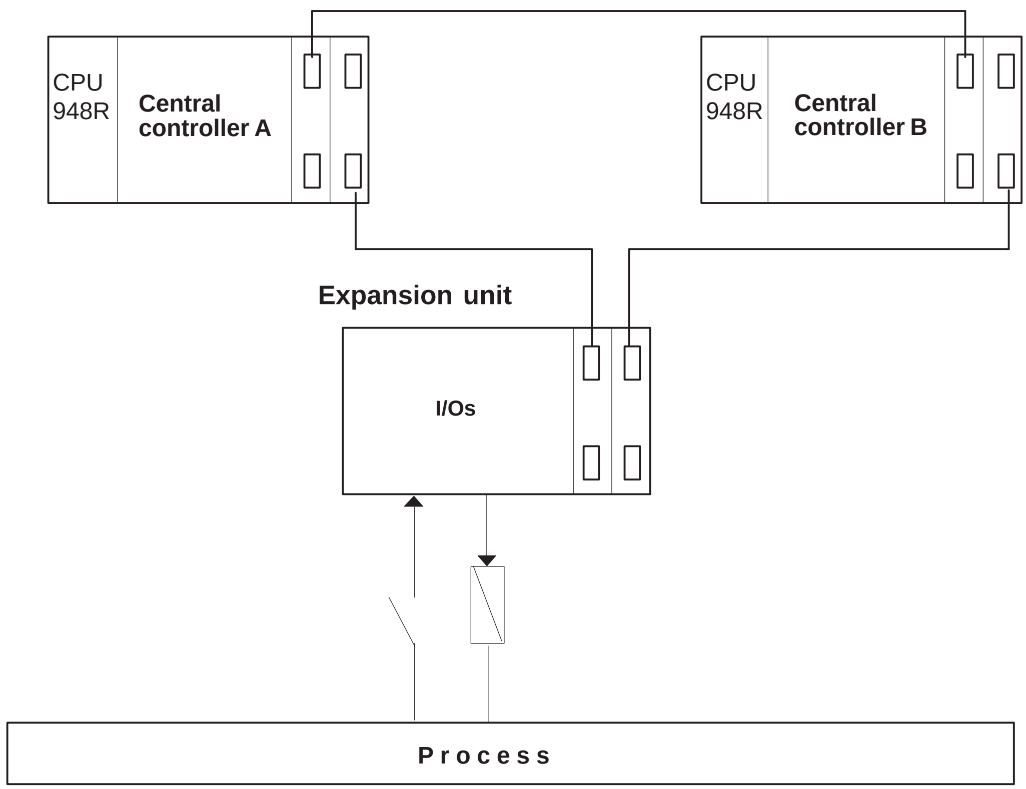


Figure 1-1 Structure of the S5-155H with One-Channel I/O Module Configuration (”Switched Mode”)

Multi-Channel Configuration

A two-channel or three-channel configuration should be implemented whenever requirements dictate that input and output modules should also have the highest possible degree of fault tolerance (Figures 1-2 and 1-3).

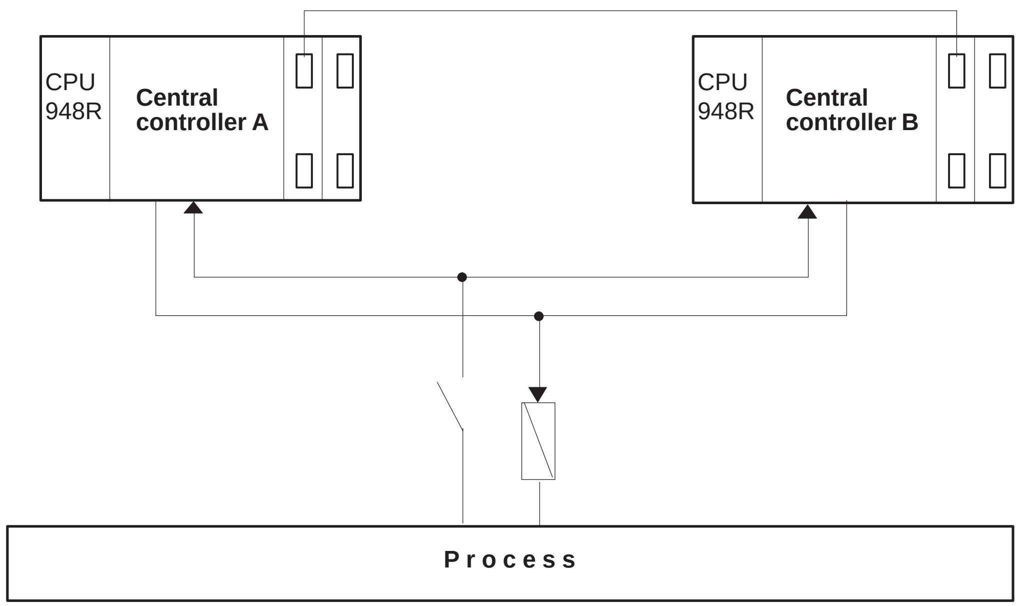


Figure 1-2 Structure of the S5-155H with Two-Channel Redundant I/O Module Configuration

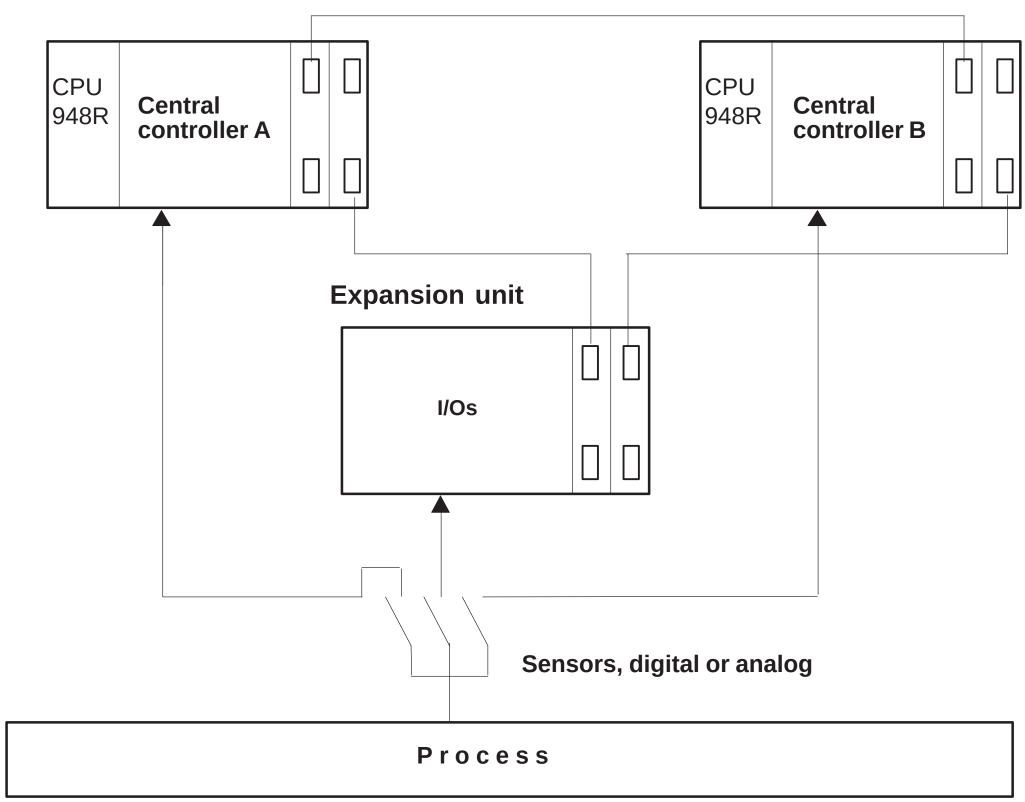


Figure 1-3 Structure of the S5-155H with Three-Channel Redundant Module Configuration

Hybrid Configuration

The three configurations can be combined as needed, thus making it possible to create configurations tailored to meet the fault-tolerance requirements of any given application.

For those parts of a plant which do not require fault tolerance, expansion units (EUs) can be interfaced to each of the central controllers on a 1-out-of-1 basis (as for a one-channel S5-155U).

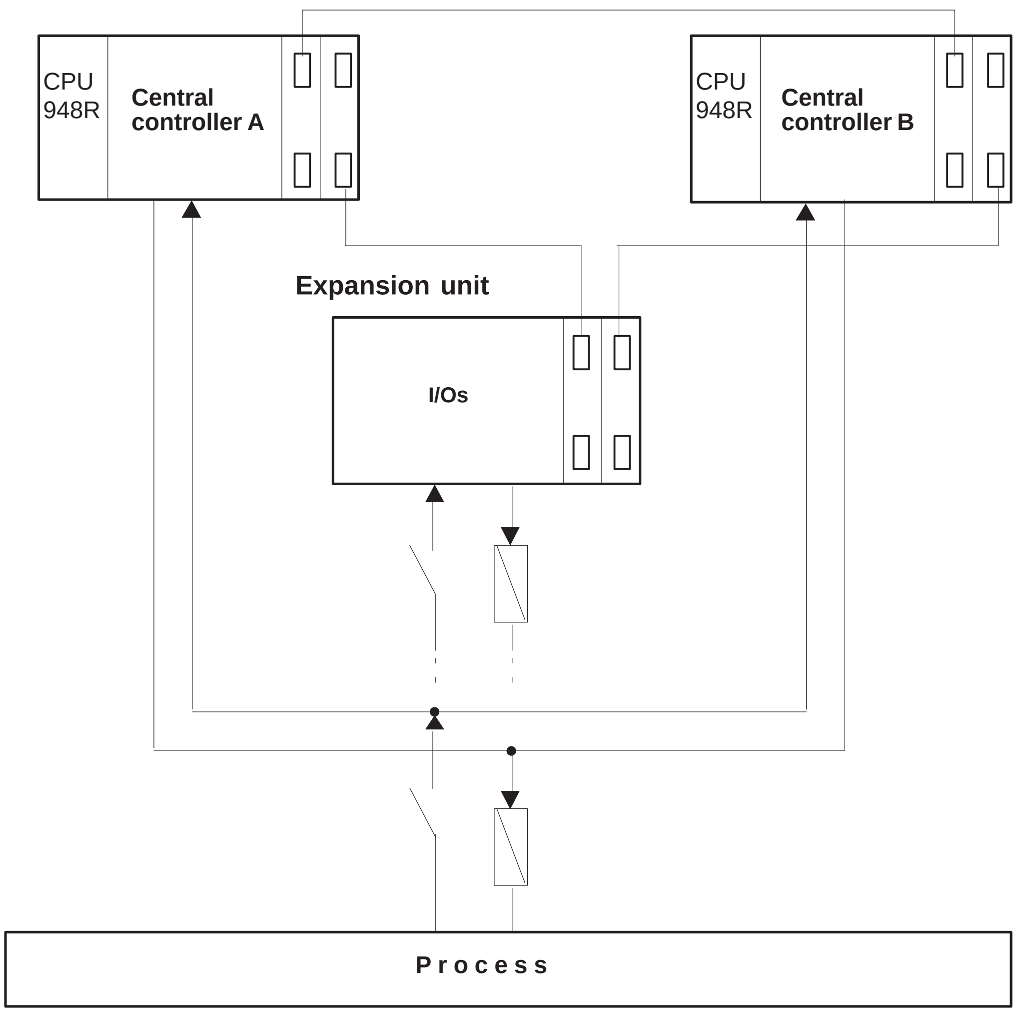


Figure 1-4 Structure of the S5-155U with One-Channel and Two-Channel Redundant I/O Module Configuration (Hybrid Configuration)

1.4 Method of Operation of the S5-155H

S5-155H-Specific Functions

Each of the two central controllers (the master and the standby) contains a CPU 948R central processing unit whose firmware autonomously handles all functions specific to the S5-155H. The most important of these are:

- Event-controlled synchronization of the two central controllers
- Self-tests for memory, processors, central controller link and S5 bus
- Switching from master CC to standby CC
- Error handling and
- Processing of operator entries on the programmer (automatic transfer of data to the other central controller).

The central controller which was powered up and successfully performed its self-test first assumes the role of master CC.

The overview below briefly describes master-standby operation of the S5-155H for one-channel and two-channel configurations of the I/O.

Operation for **one-channel** ('switched') configuration:

Master CC	Standby CC
• Reads the input signals (PII)	
• Passes the input signals to the standby CC at the beginning of each cycle	• Receives the input signals from the master CC
• Scans the user program as per the synchronization points	• Scans the user program as per the synchronization points
• Compares the process output images (PIQs) and	• Compares the process output images (PIQs)
• Generates output signals	

PII = Process input image, PIQ = Process output image

Operation for **two-channel** configuration:

Master CC	Standby CC
• Reads the input signals (PII)	• Reads the input signals (PII)
• Unifies the process input images (PIIs)	• Unifies the process input images (PIIs)
• Scans the user program as per the synchronization points	• Scans the user program as per the synchronization points
• Compares the process output images (PIQs)	• Compares the process output images (PIQs) and
• Generates output signals	• Generates output signals

Operating States and Operating Principles of the S5-155H

The master controller in a fault-tolerant S5-155H programmable controller system can assume the following states while controlling a process:

- **Solo mode**

  The master controller controls the process alone; the standby is inactive.

- **Activation of the standby**

  The master transfers the current data and the current program to the standby.

- **Redundant mode**

  The master controls the process and the standby runs concurrently in an ”updated” state, always ready to take over.

- **Error search mode**

  The master controls the process and the standby executes the self-test.

The figure below illustrates the principle of operation, and in particular the interaction between the S5-155H’s subunits.

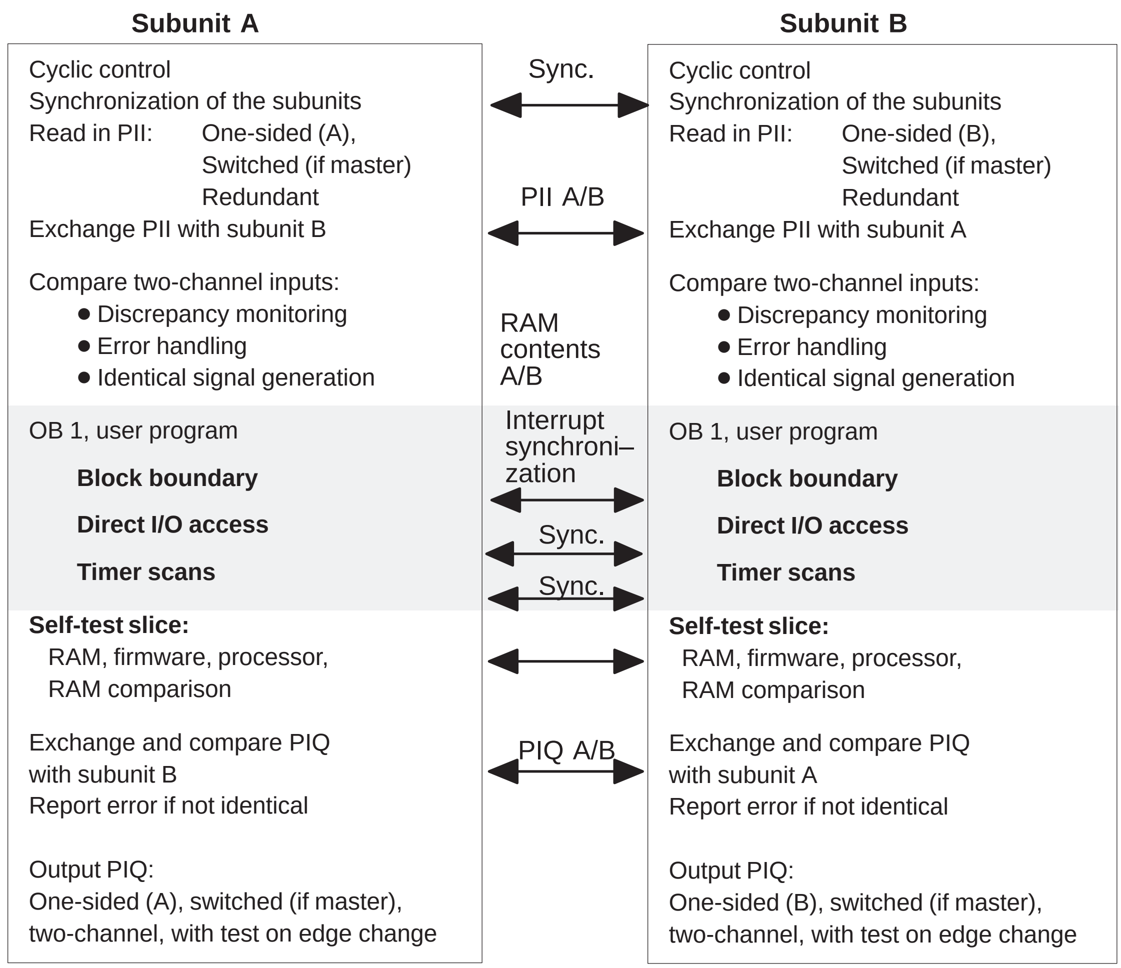


Figure 1-5 S5-155H Principle of Operation

The following is typical of S5-155H operation:

- In a one-channel (switched) configuration, only the master is active.
- In a two-channel configuration, the master and the standby are both active (parallel operation).

The operating system also ensures an ordered functional sequence when using a hybrid configuration (one-channel or multi-channel).

Programming

Essentially, the S5-155H is programmed in the same way as an S5-155U. With the exception of the operations for multi-processor mode, all STEP 5 operations are allowed.

The programmer (PG) is used in exactly the same way as for the S5-155U. In redundant systems, it is connected to only one of the central controllers, and the data entered on it are passed automatically to the second CC.

Program Processing

In addition to normal cyclic scanning of the process images in the subunits' CPUs, additional functions for synchronization and for the interchange and comparison of data and, where applicable, of status information are required during processing of the user program in the S5-155H.

Event-Synchronous User Program Processing

The same user programs run in both subunits (master and standby). Master and standby execute in **event-driven synchronism**. The 155H system program ensures that both subunits work with identical data (see Section 2.3, ”Event-Driven Synchronization”).

Process Input Image (PII)

At the beginning of each cycle, master and standby read the process images of the one-sided and redundant inputs assigned to them. The process image of the switched inputs is read in only by the master. The two subunits then exchange the entire process input image.

Discrepancy Monitoring

The 155H's system program uses a separate timer for each redundant input. These timers are used to monitor discrepancies. If a specific input signal differs between the master and the standby, this discrepancy is tolerated for the period of time programmed by the user (10 ms to 320 s). These **discrepancy timers** are updated once per cycle, following exchange of the PII. If the two input signals are still not the same when the set time has elapsed, the defective input in the master or standby is located and entered in the error data block.

Self-Test Functions

To detect errors as quickly as possible, the 155H's system program executes self-test functions during restart and cyclic program processing. These functions test the contents and state of memory, processors and I/Os, and make comparisons between the subunits. The functions are processed cyclically in ”test slices”. The number of test slices may be configured by the user. Please note that the normal scan time of your STEP 5 program is increased by the execution time of the test slices.

Process Output Image (PIQ)

When the user program in OB 1 has been completely processed, the master and the standby exchange and compare **process output images**. If there is a discrepancy, an error is reported. The standby controller enters the ”Error search” mode and the master continues in ”Solo” mode. The process output images are output to the I/Os.

Scan Cycle Time

The S5-155H has a longer scan time than the S5-155U due to the 155H-specific auxiliary functions. Some of the reasons for the increased scan time are listed below:

- The self-test; the user can configure the required time between 2 ms and 38 ms per cycle.
- The time the 155H operating system needs to process the process images (approx. 15 ms) and
- The time needed by the synchronization commands to process Transfer statements.

  Example: The ’L PW’ statement is also called upon to transfer the loaded I/O word to the second CC.

  The time needed to process the Transfer statement depends on the number of synchronization commands in the user program. The typical time needed is approximately 5 % to 15 % of the S5-155U’s scan time.

Configuring and Error Diagnostics with COM 155H

The COM 155H software supports both configuring and error diagnostics via the following functions:

- Configuring of H-specific data; this includes
  - specifying which I/O modules are redundant and which are not,
  - specifying the data block in which the system is to report errors (the so-called error DB), and
  - defining the hardware configuration.
- Error diagnostics, i. e., reading out, interpreting and displaying the information found in the error DB
- Making a hardcopy printout to document the configured data
- General system handling tasks.

1.5 S5-155H Hardware Configuration

Possible CC 188 Configurations for S5-155H with the CPU 948R

The following table shows you which modules can be inserted in which slots.

Slot No. / Module Type	3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139	147	155	163
CPU 948R, UR 11, 12, 21, 22, 51		■	□																		
CPU 948R, UR 13, 23, 53		■																			
CP 5XX, CP 143, CP 5430, CP 5431[1]			■	■	■	■	■	■	■	■	■	■	■	■	■	■					
IM 300-5 IM 301-5[1]																				■	■
IM 300-3, IM 301-3 IM 304, IM 308, IM 308B, IM 308C																		■	■	■	■
IM 307[2]														■	■	■		■	■	■	□
DI, DO, AI, AO[1]	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■
IP 241USW, IP244 IP 252[1]			■	■	■	■	■	■	■	■	■	■	■	■	■	■					
IP 240, IP 241, IP 242, IP 242A, IP 242B, IP 243, IP 281[1,3,4], IP 288			■		■		■	■	■	■	■	■	■	■	■	■					
IM 304/IM 324R																	■				
IP 260, IP 261			■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■		
Load current supply –951[1]			■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	□

■ Electrical connection   □ Mechanical width

1. Note the installation width for each particular module; some may take up more slots to the right (see Catalog ST 54.1).
2. Note the jumper setting on the IM 307; interrupt transfer is only possible in slots 107 to 131.
3. Use in slots 27, 43, 59, 139 and 147 provides only a very restricted functionality as no interrupts are wired.
4. IP 243 without DA or AD converter in slots 27, 43, 59, 139 and 147.

Possible Configurations for the EU 185U

The following table shows you which modules can be inserted in which slots.

Slot No. Module Type	3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139	147	155	163
Communications Processors (CP)			■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
IM 314 R																			■	■	
IM 300-5C																					■
IM 308																			■	■	■
IM 308-B/C [1]			■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
DI, DO, AI, AO	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Signal-processing modules (IP)	See current Catalog ST 54.1 for slot numbers																				

[1] IM 308C enabled in the EG 185U only for switched I/O in H system.

Minimum Configuration

The fault-tolerant S5-155H programmable controller consists of standard components of the SIMATIC S5 range.

The S5-155H's minimum configuration consists of two S5-135U/155U central controllers (master and standby), each with

- one built-in power supply unit and
- one CPU 948R.

The two central controllers are interconnected over a parallel interface. This interface consists of an IM 304 module (in one central controller, the subunit B), an IM 324R (in the other central controller, the subunit A), and a 721 connecting cable. The parallel interface is used for data exchange between the master and the standby.

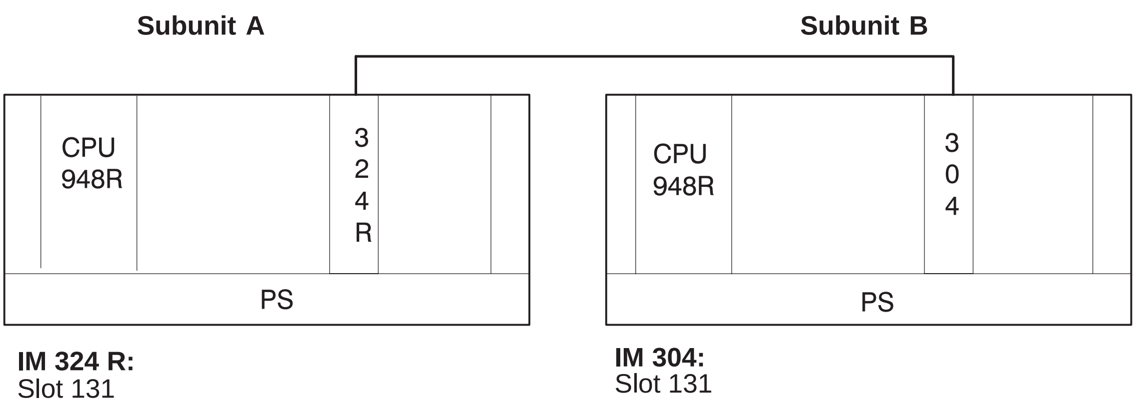


Figure 1-6 Minimum Configuration of the S5-155H

Maximum Configuration

Building on the minimum configuration, the system can be expanded by adding S5 modules:

- Digital and analog input/output modules (I/Os)
- Communications processors (CPs)
- Intelligent I/Os (IPs)

A maximum of sixteen expansion units (EUs) with up to eight I/O buses can be connected to one S5-155H.

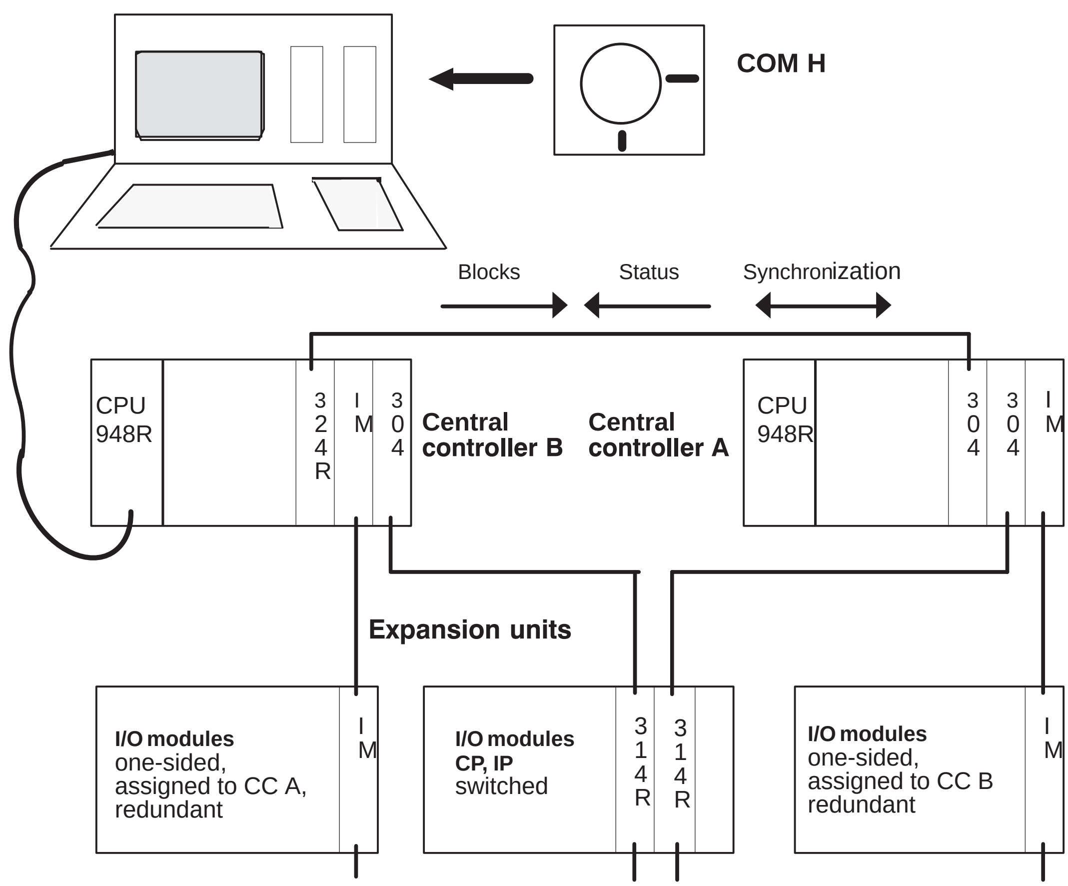


Figure 1-7 Sample S5-155H Configuration, System Structure

1.6 Software

155H System Program

The 155H system program is a modified 155U system program, expanded to include a number of redundancy-specific functions. It is an integral part of the central controller, which means that the whole program memory of the S5-155U is available for the user program.

Important

The 155H system program reserves

- the data block DX 1
- the error data block (number specified by user)
- the RAM data block (number specified by user)
- the H flag word (number specified by user)

Only those functions are listed here which have been added to the 155**H** but are not part of the 155**U** system program. These and all other functions are described in detail in the Programming Guide for the CPU 948R (Volume 2 of this manual).

The expansions and modifications in the 155H system program affect the following system characteristics and capabilities:

Function	See Chapter/Section
– Mode of operation and status	2.1
– Activating the standby controller	2.2
– Event-driven synchronization	2.3
– Switching from standby to master controller	2.4
– Self-test	2.5
– Error search mode	8.1
– Redundant I/Os	4.2, 4.3, 4.4
– Operation with the IM 314R	11.1
– Timecharacteristics	7
– Online functions	Volume II / 10
– Troubleshooting and repairs	9

The various functions are discussed in more detail in the sections indicated.

STEP 5 User Program

In the S5-155U, you can use all STEP 5 user programs that can execute in the S5-155U, provided you observe the following.

Important

The following applies to the S5-155H:

– The S5-155H can no longer be used in multiprocessor mode.

– The following integral special functions cannot be executed on the S5-155U: OB 126, OB 200, OB 202 to 205, OB 223.

– The SED and SEE operations are only for multiprocessor mode, and therefore not permissible for the S5-155H.

STEP 5 Program

In addition, please note the following when writing your user program for the S5-155H:

- Use only the STEP 5 operations LT and LCT (not LIR, TIR, LDI and TDI) for word-based access to timers.
- The parameters ”155U” (or interruptability at instruction boundaries) and ”Warm restart” must **not** be selected in DX 0. A DX 0 error resulting in this way causes the CPU to stop.
- You cannot access operating system data words RS 96 to RS 99 via the STEP 5 user program. Instead, use special-function organization block OB 121 or 151 to read or set the date and time; only in this way can you be sure that the same date/time will be entered in both subunits.
- Only the master has direct access to switched I/Os in the restart routine.

Startup

Note the following on startup:

- All DBs/DXs whose contents are changed in interrupt service routines must be entered in the interrupt DB/DX transfer data lists using COM 155H.
- All DBs/DXs whose contents are changed in the cyclic program must also be entered in the cycle DB/DX transfer data list with COM 155H.
- Unusual feature of the S5-155H as regards T PY/T PW and addressing errors:

  If a timeout (QVZ) and an addressing error (ADF) are present when the operation is executed (for unconfigured, non-existent I/Os), then only QVZ is reported in Solo mode whereas both QVZ and ADF are reported in Redundant mode.

Special Functions: OB 124, 125, 254 and 255

An error is reported when one of the following special functions is executed while the master controller is activating the standby: GDB, GXDX, OB 124 ”Delete blocks”, OB 125 ”Generate blocks”, OB 254 and OB 255 ”Transfer data blocks”. Error code ”4F”: ”Function currently impermissible because standby is being activated”, is forwarded in accumulator register 1-LL.

Differences between the CPU 948R and the CPU 946R/947R

The CPU 948R is the upwardly-compatible successor to the CPU 946R/947R. The following points should be noted:

- DX1 must be converted with the help of COM 155H V3.0.
- The structure of the error DB has been changed.
- H flag control bit 3 is disabled for the user.

H-Specific System Functions 2

This chapter describes in detail all typical system features and individual S5-155H functions.

2.1 Method of Operation and Operating States of the S5-155H

Operating States

On startup or restart, the S5-155H assumes one of the operating states shown in Figure 2-1:

Solo mode:
The master subunit alone scans the user program and controls the process; the standby subunit is inactive.

Activating the standby:
The master subunit passes the current data to the standby.

Error search mode:
The master subunit scans the user program and controls the process; the standby subunit executes the self-test.

Redundant mode:
The master subunit controls the process; the standby subunit runs in parallel (”updated” mode), and is ready to take over at any time.

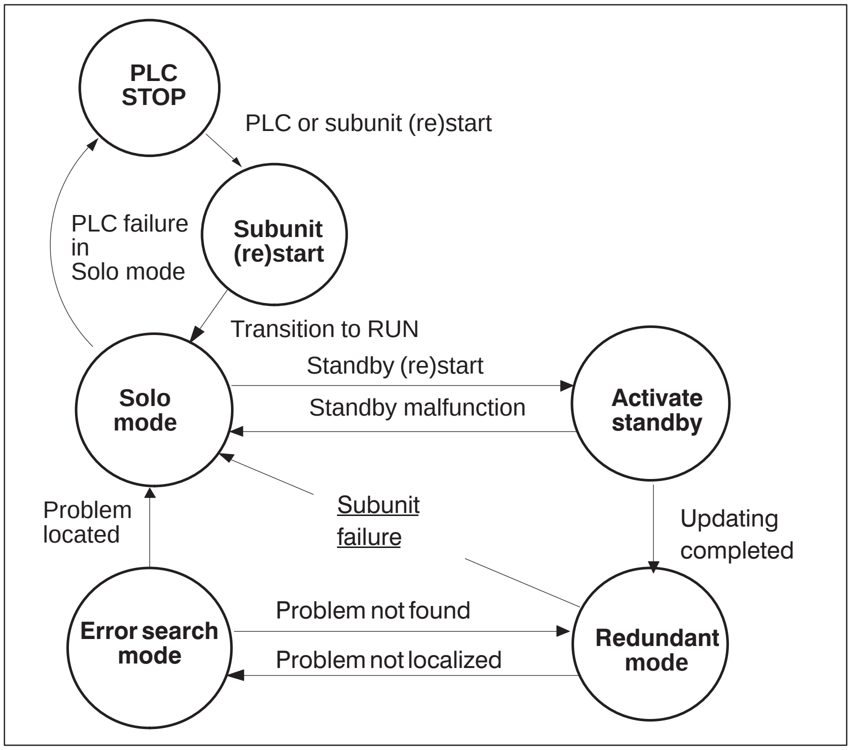


Figure 2-1 S5-155H Modes and Transitions

S5-155H Principle of Operation

In a fault-tolerant programmable controller system, identical user programs run in both subunits. The subunits are ”event-synchronized”; that is, only those events which could produce **different** internal ”states” in the two central controllers cause the controllers to be synchronized. The internal ”state” is determined by the states of the memory areas used (process image, flags, counters, timers and data blocks).

Examples of such ’events’ are:

- Direct access operations to one-sided, switched or redundant I/Os
- Timer scans
- Process interrupts and
- Timed interrupts

Processing the User Program

Figure 2-2 shows how an S5-155H with CPU 948R handles I/Os.

1. Each subunit reads the one-sided inputs assigned to it, and the redundant inputs. The ’switched’ inputs are read only by the master, which also updates the input image for both subunits and generates a unified input image.
2. One timer location is set aside for each redundant digital input, and is updated by the operating system. The CPU 948R function block sets aside one timer location per redundant analog input which is updated once per FB call. This timer is used as discrepancy watchdog for the redundant digital inputs; that is, the CPU 948R tolerates non-matching input signals for a time period defined by the user (20 ms to 320 s).
3. If a continuous signal discrepancy is ascertained, the defective input is located in subunit A or B by means of an I/O test, entered in the error DB, and passivated.

In order to increase the fault tolerance of the system, errors/faults must be detected and eliminated if possible before the redundant component fails; that is, faults/errors in the standby controller should be detected before the master controller fails. For this purpose, extensive self-test functions for memory, processors and I/Os have been integrated in the CPU 948R.

4. The S5-155H self-test functions run in their entirety every time a subunit is restarted. In cyclic mode, the tests are executed in ’slices’ whose number per cycle (scan cycle time increase) can be stipulated by the user.

   During the self-test, as during other time-consuming operating system functions, interrupts are permitted at 2 ms intervals.
5. OB 1, which, like every user program, is synchronized on an event-driven basis, is then invoked.
6. After each program pass, the two output images (PIQs) of the subunits are compared. If they are not identical, an error is reported.
7. The output images are output to the I/O. Also, in the case of two-channel digital outputs, a readback digital input uses a ”0” to ”1” edge to locate stuck at 0 errors.

The operating system synchronizes and processes system interrupts, process interrupts and timed interrupts at block boundaries. Direct access operations to **switched** I/Os are immediately synchronized and processed.

In the case of one-sided and redundant I/Os, the operating system input signals are also exchanged and compared. Timer scans are immediately synchronized and unified by copying the master's timer value to the standby.

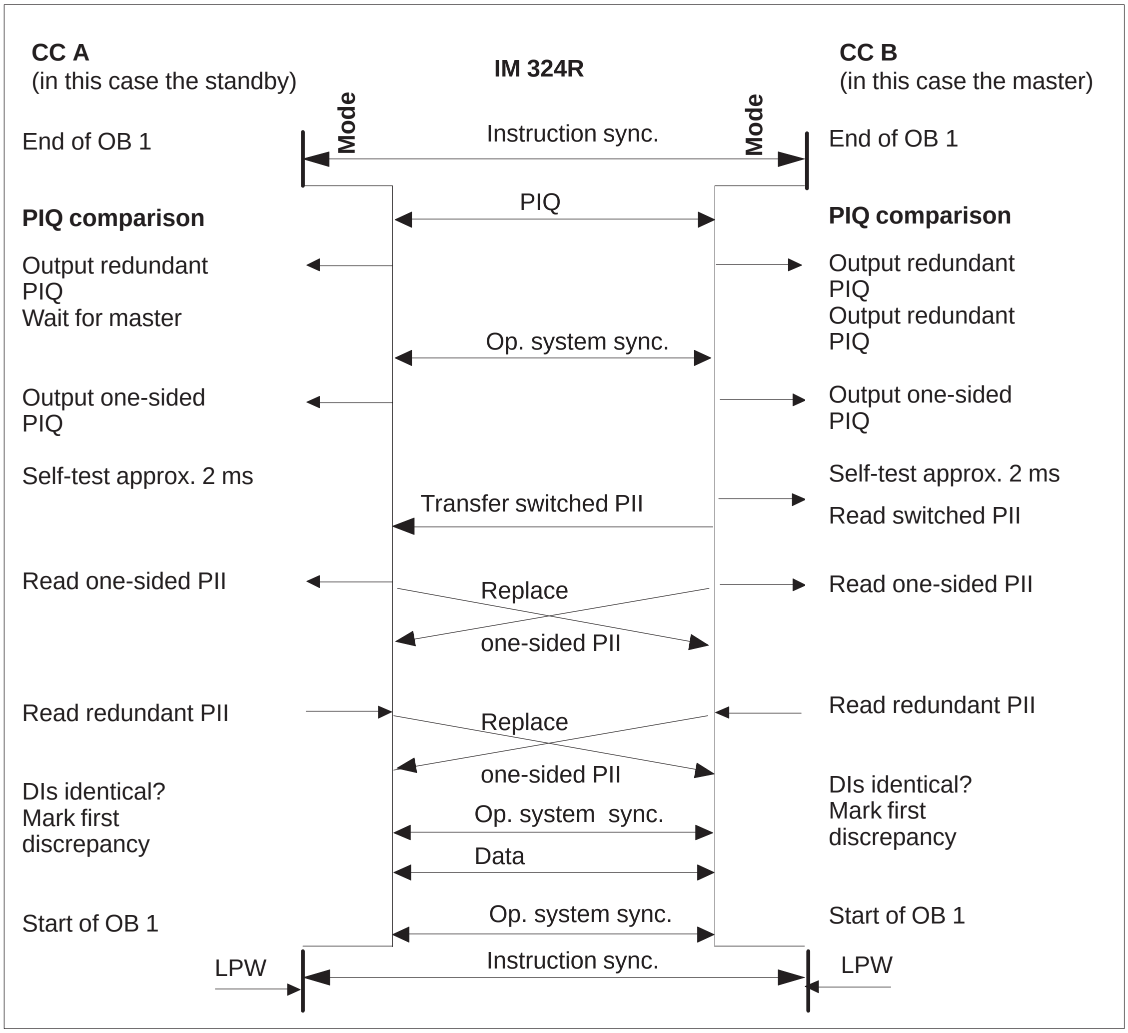


Figure 2-2 Cyclic Process Image Updating of the Inputs and Outputs

Programming the PLC Restart Routine

As regards restarts, be sure to refer to the appropriate chapter in the CPU 948R Programming Guide, (Volume 2 of this manual), where you will find information on all S5-155H restart modes:

- Cold restart: OB 20
- Manual warm restart with memory: OB 21
- Automatic warm restart with memory: OB 22

Online Function START

Activation of this online function does not restart the whole S5-155H system, but only the subunit to which the programmer is connected. The COM 155H function **”RUN SYS”**, in contrast, restarts the whole system.

2.2 Activating the Standby

Activation Process

Activating the standby means **matching the internal states** of the two subunits. After the standby has been enabled in the Restart routine, it sends an "activation request" to the master.

As soon as the request has been made, the two subunits are checked for any discrepancies. This involves checking the following to make sure that there are no differences between the two controllers:

1. The RAM capacity of the standby CPU and the master CPU are the same.
2. The operating system code in master and standby are identical.
3. The checksums of the user code chips are identical.
4. The start addresses of the STEP 5 user blocks are identical.
5. The checksums of the static user data (except for the DB and DX data blocks in cyclic and interrupt-driven program processing) are identical.
6. The checksums of the memory cards in master and standby are identical.

If there is no match in checks a., b. and f., the standby controller reports an error and stops.

If there is no match in tests c. to e., the contents of the master's CPU are copied to the standby's CPU. The activation procedure (the copying of the contents of the master controller's CPU to the standby controller's CPU) is spread over several cycles.

Restart Self-Test and Updating Process

Once the standby controller has been activated (the static data in master and standby are identical), master and standby execute an automatic depassivation routine; this procedure does not erase the error information in the error DB.

The standby controller executes its restart self-test. It then waits to be "updated"; that is, it waits for the arrival of all dynamic data from the master controller.

During the standby activation phase, the red STOP LED and the green RUN LED flash alternately on the standby CPU (at approximately 1/2 second intervals). During the restart test phase, both LEDs show a steady light.

Updating of the standby controller increases the duration of a master controller cycle **on a one-shot basis** by a specifiable amount of time. The updating instant can be chosen on a process-dependent basis; bit position "2" in the H flag word's control byte is reserved specifically for this purpose (see Section 8.5). You can disable the updating procedure by setting this bit, or enable updating by resetting it. This permits you to choose a non-critical process state for the one-shot scan cycle time increase.

Note, however, that disabling updating increases downtimes; that is, it decreases the system's availability or fault tolerance. When the bit is reset to re-enable updating, the enable becomes valid with the next cycle.

Important

Updating of the standby controller increases the duration of a master controller scan cycle on a one-shot basis by the amount of time specified in the configuration data. To minimize the scan time increase as much as possible, enter only those DB and DX data blocks during the configuring phase with COM 155H which will be modified in the user program (for example DBs in OB 1), and which must therefore be transferred within one cycle when activating the standby.

Since timed and process interrupts are not disabled when activating the standby, also specify the numbers of those data blocks modified in interrupt service routines (such as DBs in OB 13).

Updating the Standby Controller

The controller is updated as follows. The 155H system program

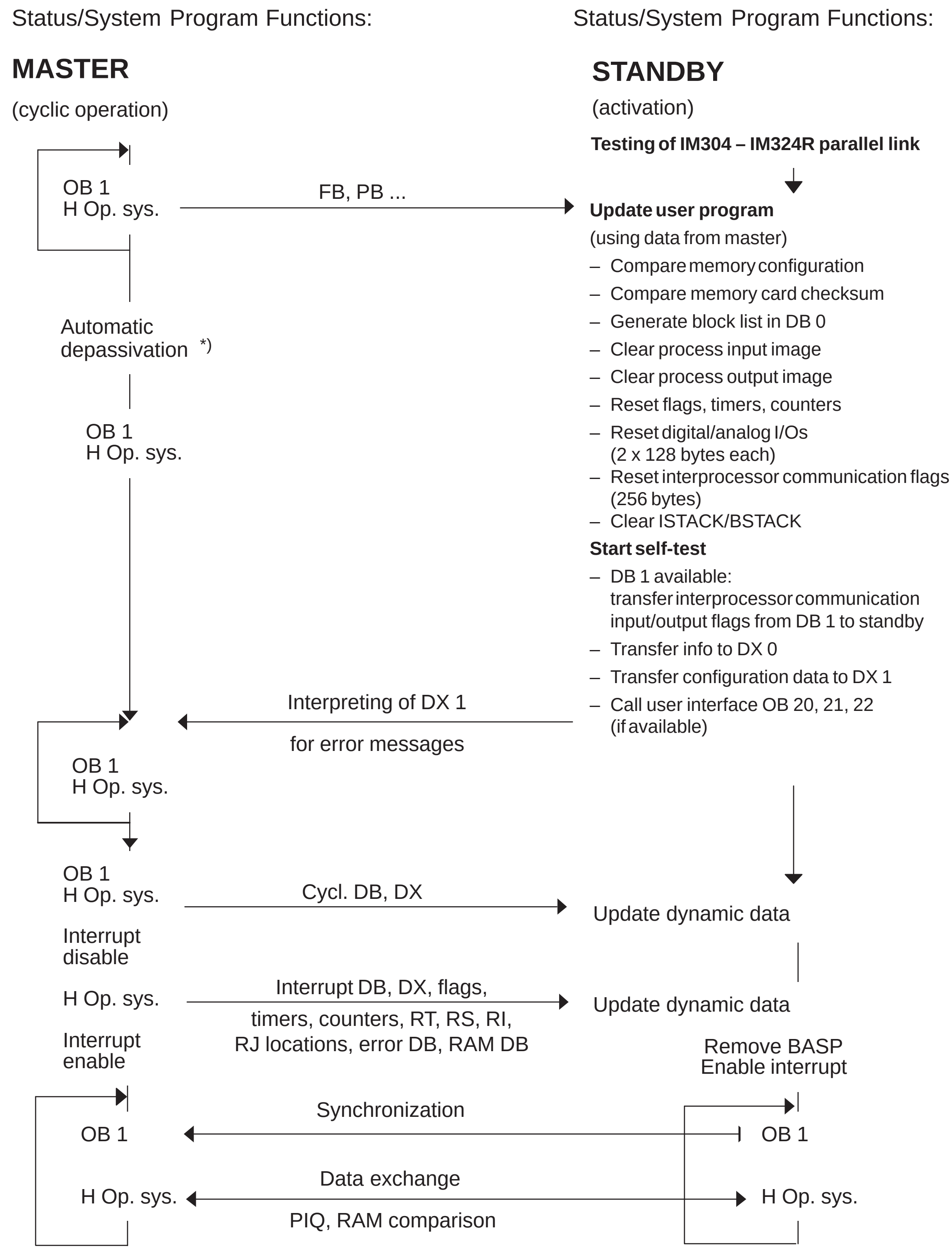
- transfers all configured ”cycle DBs/DXs”, [1)]
- disables all interrupts,
- transfers all configured interrupt DBs/DXs, [1)]
- transfers all flags, counters, timers, RS, RT, RI and RJ locations, the error DB, and the RAM DB,
- switches to ”Redundant mode” and
- enables the interrupts.

1) Data blocks processed both in the cyclic program and in an interrupt OB need be listed only once under ”interrupt DBs/DXs”.

With regard to the above, also please refer to Section 3.3 in Part III of this Volume entitled ”Initializing the Activation of the Standby”.

Once the standby has been activated and updating completed, both subunits enter the event-synchronized cyclic mode.

The following overview (Figure 2-3) summarizes the activities of the master and standby CPUs during the activation and updating process.



*) Static error image is reset. The error messages in the error DB remain unchanged. The operating system re-enters any unrectified errors in the error DB if those same errors re-occur.

Figure 2-3 Standby Activation and Updating Sequence

2.3 Event-Driven Synchronization

Switchover from Master to Standby

Both subunits are synchronized to ensure bumpless switching between master and standby at all times.

The synchronization procedure used in the S5-155H is known as ”event-driven synchronization”, which means that the subunits are synchronized whenever an event occurs which could result in the two subunits having different internal states; for example different process images, flags, timers or communications data. These events include:

- Direct access to I/Os
- Timer scans
- System interrupts
- Process interrupts
- Timed interrupts

Synchronization and Program Processing

The operating system performs subunit synchronization in order to ensure complete transparency of the user program. The user is not aware of this. This means that you can write your program in the same way as for an S5-155U in single-processor mode. The only difference is that the synchronization procedure increases the normal S5-155U execution times of the STEP 5 operations used for direct I/O access, timer scans and block changes (refer to the STEP 5 List of Operations). The execution times of the other operations are not affected.

Synchronization and Interrupt Servicing

In the S5-155H, block-granular interruptibility is the only permissible mode. This means that interrupts are serviced only between blocks. In order to prevent different ”internal states” from occurring, entry into the interrupt OB is made at the same place each time, namely, at a ”synchronization point”. In the CPU 948R, the synchronization point for interrupts is always the next block change. Input byte IB 0 can be used for process interrupts.

Synchronization and System Monitoring

In each subunit, a check is made at every synchronization point to make sure the other subunit is functioning. Depending on the result of the check, a switchover from the standby to the master controller is performed and the message ”Standby failure” output.

The synchronization procedure is timed at each synchronization point. The operating system sets the watchdog timer to 30 ms. A check is also made at each synchronization point to make sure that both subunits are executing the same statement (comparison of OP codes). If they are not, the standby controller stops and a ”synchronization error” is reported.

Process Image Updating

At the end of OB 1, the entire process output image (PIQ) in both CPU 948Rs is immediately compared and the non-passivated PIQ (redundant PIQ, switched PIQ, one-sided PIQ) output. The self-test is then run.

Following the self-test, the process input image (PII) is read in (redundant PII, switched PII, one-sided PII). The PII is exchanged and unified. OB1 is then re-called.

The required functions are described in detail in Chapter 4.

Automatic Resetting of the Standby Controller's Clock

Due to the inaccuracy of quartz timing, CMOS clocks of the two subunits may begin to show a discrepancy after a while (at a rate of approximately 1 second per day), which can cause problems when transferring from the standby controller to the master. The error codes entered in the error DB show the exact sequence of occurrences, but the time stamp could prove misleading.

For this reason, the two subunit clocks are compared cyclically, and the operating system automatically corrects the standby controller's clock when the discrepancy exceeds 0.05 seconds.

Cycle Errors

If a ZYK error occurs in Redundant mode, the standby controller always stops, while at the same time the scan cycle time in the master controller is retriggered. The subunit which continues its operation in Solo mode functions like an S5-155U; that is, the response to a subsequent ZYK error depends on OB 26.

2.4 Switchover from Standby to Master Controller

Switching Criteria

The synchronization procedure ensures bumpless switching from standby to master controller at all times. This means:

- Transfer does not affect process output signals.
- There is no loss of information in communications with CPs/IPs.
- User program processing is not affected.

Switchover from standby to master takes place in the following instances:

1. Failure of the master CC (BASP, NAU or STOP switch);
2. Initial error search of both subunit CPUs unsuccessful (see ”Error search mode”)
3. First failure of a master controller’s IM 314R when the standby controller has access to a larger number of IM 314R interface modules than the master.
4. First failure of a master controller’s I/O bus (wire break, for instance) or failure of an IM 304 when the standby controller has access to a larger number of IM 314R interface modules than the master.
5. First failure of a switched I/O module
6. User issues a software request (H flag control byte) for transfer from standby to master controller.
7. If more than 30 timeouts occur in redundant I/O bytes in the subunit of the master within one PLC cycle.

In cases c. to g., the new standby CPU does not stop, but continues functioning as standby controller.

Functional Sequence of a Switchover from Standby to Master

The standby controller checks the operational status of the master controller at each synchronization point. Failure of a master controller is detected at the hardware level by evaluating the S5 bus signals BASP and NAU in the IM 324R parallel interface module. The standby CPU’s operating system detects the failure of the master controller at the next synchronization point, and branches to a routine which executes the following functions:

- Switches over the I/O buses of all IM 314R modules;
- Switches all two-channel I/Os to single-channel operation;
- Switches the operating system to Solo mode; that is, no subunit synchronization;
- If the synchronization point is a direct I/O access operation, that operation will be retried.

Following a standby-to-master switchover, the S5-155H with CPU 948R operates in Solo mode. The H error system OB is invoked; you can program the desired response in this OB.

The following occurs with the I/Os allocated to the failed subunit:

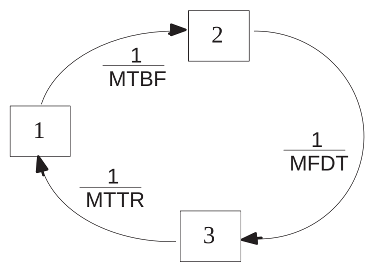
- PIQ and PII are set to zero
- No ’ADF’ error is reported when this PIQ/PII is accessed
- Timeout is reported in the event of direct access to one of these I/Os.

2.5 Self-Test

Self-Test and Fault Tolerance

Essentially, the S5-155H achieves its high degree of fault tolerance through its multi-channel capability coupled with speedy repair following detection of a malfunction. If a controller is considered to be fault tolerant only when its status is that of ”no malfunction”, it follows that the fault tolerance of an H system is increased further by its self-test (Figure 2-4).

The diagram and the formula below show that a self-test increases the fault tolerance of an automation system. The amount of time in which the controller malfunctions is reduced to a minimum.



Fault tolerance for ”No controller malfunctions” status:

$$V = \frac{MTBF}{MTBF + MTTR + MFDT}$$

Status:	Description:
1	No controller malfunctions
2	Controller malfunction
3	Controller failure

Fault rate = 1/MTBF
Repair rate = 1/MTTR
Fault detection rate = 1/MFDT, MFDT = T/2 (T= Self-test cycle)

Figure 2-4 Importance of the Self-Test to Fault Tolerance

An H system’s highest priority is fault detection and fault localization. This is required in order to control the fault. The S5-155H’s self-test routines run in both CPUs. They detect and localize hardware failures in a minimal amount of time and with little programming effort. To localize a fault, it is necessary only to find out which modules are faulty and to replace them.

Self-Test Strategy

Which self-test routines execute depends on the S5-155H’s operating status.

- **Self-test in the Restart routine**

  The entire self-test is run when a central controller is restarted. If a fault is detected at this stage, the CPU stops. An error message is entered in the error data block. Because the self-test takes longer than one minute, it can be skipped on a warm restart of the master controller (see ”H Flag Control Byte”).

  During execution of the self-test in the Restart routine, the RUN and STOP LEDs on the frontplate show a steady light. A complete self-test is run in all Restart modes.

- **Self-test in cyclic mode**

  Each time OB 1 is processed (once per cycle), part of the self-test is executed **in small slices** (2 ms test slices). The self-test therefore runs, transparent for the other software, in the background until a hardware failure is detected.

  You can configure the execution time for the self-test in increments of 2 ms. If you define a value which exceeds a test slice, the occurrence of a timed or process interrupt is queried after each test slice and the interrupt serviced **before** the next test slice. The execution time for the self-test increases in this case by the time needed to service the interrupt.

  A value of between 1 and 20 may be defined as the number of test slices to be executed per PLC cycle (refer to Chapter 3 in Part III of this Volume, entitled 'Configuring and Initializing'). These values correspond to self-test execution times of from 2 to 40 ms.

  In a test run, the CPU 948R-1 can have a maximum of 10,000 test slices, the CPU 948R-2 a maximum of 30,000 and the CPU 948RL a maximum of 5000.

Tested System Components

In the S5-155H, such important system components as CPU, memory, I/Os and communications links are continually tested and monitored.

- CPU test

  Includes testing of STEP 5 operations, timers, CMOS clock, interrupt mask and the scan time monitor.

- Firmware/RAM test

  Comparison of the RAM in both subunits and a checksum test of the OB, SB, PB, FB, FX blocks and of the constants DB/DX. Also a RAM test for all variable DB/DX.

- I/O bus test with IM 314R

  Tests for short-circuits and breaks in the 721 I/O bus cable to the IM 314R.

- I/O bus test for page addressing

  Page addressing is tested in cyclic mode once in every complete test run. The test detects the following faults:

  – A CP/IP reacts to (acknowledges) not only its own interface number, but also to the other 255 interface numbers.

  – An acknowledgement is issued by an unassigned interface number. All unassigned interface numbers are tested. The test is also executed once on each restart.

- IM 304R/IM 324R parallel interface test

  The parallel interface's dual-port RAM is tested on both subunits A and B. The purpose of this test is to locate any short-circuits or cable/wire breaks.

Locating Facilities (LF) Test

The user must configure one additional digital input and one additional digital output for each redundant digital input or output byte for which error recognition as well as error localization is to be implemented. Since these are specifically for the purpose of error localization, they are referred to as locating digital inputs (L-DIs) and locating digital outputs (L-DQs) (see Figures 4-4, 4-5 and 4-9 to 4-12).

The L-DIs and L-DQs configured for each redundant DI or DQ are referred to collectively as the locating facility (LF). The LFs are tested once every 10 hours.

The locating facilities for the redundant DIs are tested for ”stuck at 0” errors and (on restart only) for ”stuck at 1” errors. The locating facilities for the redundant DQs are also tested every 10 hours for ”stuck at 0” and ”stuck at 1”.

Self-Test in Error Search Mode

When an error is detected which, because it was found during a RAM comparison test (only valid blocks are compared), could not be allocated to a specific subunit, the standby controller enters the Error Search mode. This mode is also entered when a discrepancy is found when comparing the output images of the two subunits. In Error Search mode, the self-test is not executed in slices, but rather **in its entirety**, which takes approximately 10 to 30 seconds.

Functional Sequence in Error Search Mode

Example:

The two subunits exchange and compare the entire process output image (PIQ) at the end of each cycle. If a discrepancy is found during this cyclic PIQ comparison test, the memory locations in the PIQ are tested for ”stuck at 0” and ”stuck at 1” errors. If such an error is found, only the malfunctioning subunit stops.

If the error cannot be localized, the 155H responds as per user specifications (see Part III of this Volume, Section 3.2, ’Initializing the Operating System’). If the configured response is ”0”, the standby controller enters the ”Error Search” mode. The master controller runs in ”Solo” mode.

If the self-test locates a fault in the standby controller, the standby stops. Otherwise, the standby controller is activated and a standby-master switchover initiated. The PLC now runs in Redundant mode. Should another comparison error be found, the new standby controller enters the ”Error Search” mode while the new master continues in ”Solo” mode.

If the self-test locates an error in the new standby controller, which is now in Error Search mode, the standby controller stops and reports an error. If the self-test cannot locate an error in this subunit either, the subunit stops with ”Non-locatable error” if the second comparison error occurred within the same test cycle.

CPU 948R/948RL

3

This chapter contains the hardware description and technical specifications for the CPU 948R and CPU 948RL central processing units. In addition to comments regarding application, you will find all information and data needed for installing the modules and putting them into operation. This includes information on inserting and removing the modules as well as on control elements and indicators on the modules' frontplate.

Details on programming can be found in the Programming Guide for the CPU 948R (Volume 2 of this manual).

You can insert a memory card containing your user program into the CPU 948R and CPU 948RL.

Note

Note that only this chapter deals specifically with the CPU 948RL and that the differences between the CPU 948R and the CPU 948RL are only described in this chapter.

Where only the CPU 948R is mentioned in other chapters in this manual, the information there also applies in the same way to the CPU 948RL with the exception of the differences listed in this chapter.

3.1 Technical Specifications of the CPU 948R/948RL

Application

The CPU 948R and 948RL can be used in S5-135U/155H central controllers. Multiprocessor configurations are not possible in fault-tolerant systems.

The CPU 948R/948RL is available in the following versions:

CPU version	Internal user memory (RAM)
CPU 948RL	128 Kbyte
CPU 948R-1	640 Kbyte
CPU 948R-2	1664 Kbyte

A SIMATIC S5 flash EPROM memory card (referred to in the following simply as memory card) can be plugged into the CPU 948R and 948RL as storage medium for the user program and user data. On an overall reset, the contents of the memory card are copied to the CPU’s internal RAM.

The CPU 948R and 948RL are programmed in STEP 5 (LAD, CSF, STL, SCL). The CPU 948R/948RL processes all STEP 5 operations at a very high speed, and is also equipped with a high-speed floating-point arithmetic facility.

The following program processing levels are possible:

- Cyclic
- Time-controlled (9 different time grids, clock-controlled, delayed interrupt)
- Interrupt-driven over the S5 bus (eight process interrupts at block boundaries via IB0)
- ’Soft STOP’

Configuration

The CPU 948R/948RL’s electronics, including RAM, are on two PCBs. These PCBs have Eurocard format, and are bolted to one another. They must never be separated.

The module’s frontplate has a width of 2 2/3 standard slots, or 40 mm. The CPU 948R/948RL takes up two slots in the central controller rack.

3.2 CPU 948R/948RL Installation and Startup Procedures

Note

All jumpers on the module are required for the manufacturer's quality inspection. The jumper configuration must not be changed in any way.

Removing and Inserting the Module

Caution

Always switch off the power before removing or inserting the module.

The CPU 948R/948RL's basic board and its expansion board are a unit, and must not be separated.

Inserting the module

Proceed as follows to insert the CPU in the central controller:

Step	Procedure
1	Loosen the upper locking bar on the central controller and check to make sure that the module's locking bolt is correctly positioned (that is, with the slit in the vertical position).
2	Select the right slot (check the label on the locking bar). Insert the CPU (slot 11), aligning it to the left.
3	Push the module evenly onto the guide rail until the lever above the locking bolt is in a vertical position.
4	Press in the locking bolt on the underside of the module and turn it 90° to the right.
5	Affix the upper locking bar.

Removing the module

Proceed as follows to remove the CPU:

Step	Procedure
1	Loosen the upper locking bar on the central controller.
2	Loosen the module's locking bolt.
3	Press down on the lever and remove the module by pulling it forward and out of the controller.

Control Elements and LEDs

The control elements and LEDs are arranged in the same way on the frontplate of the CPU 948R and CPU 948RL. Figure 3-1 shows an example of the frontplate of the CPU 948R.

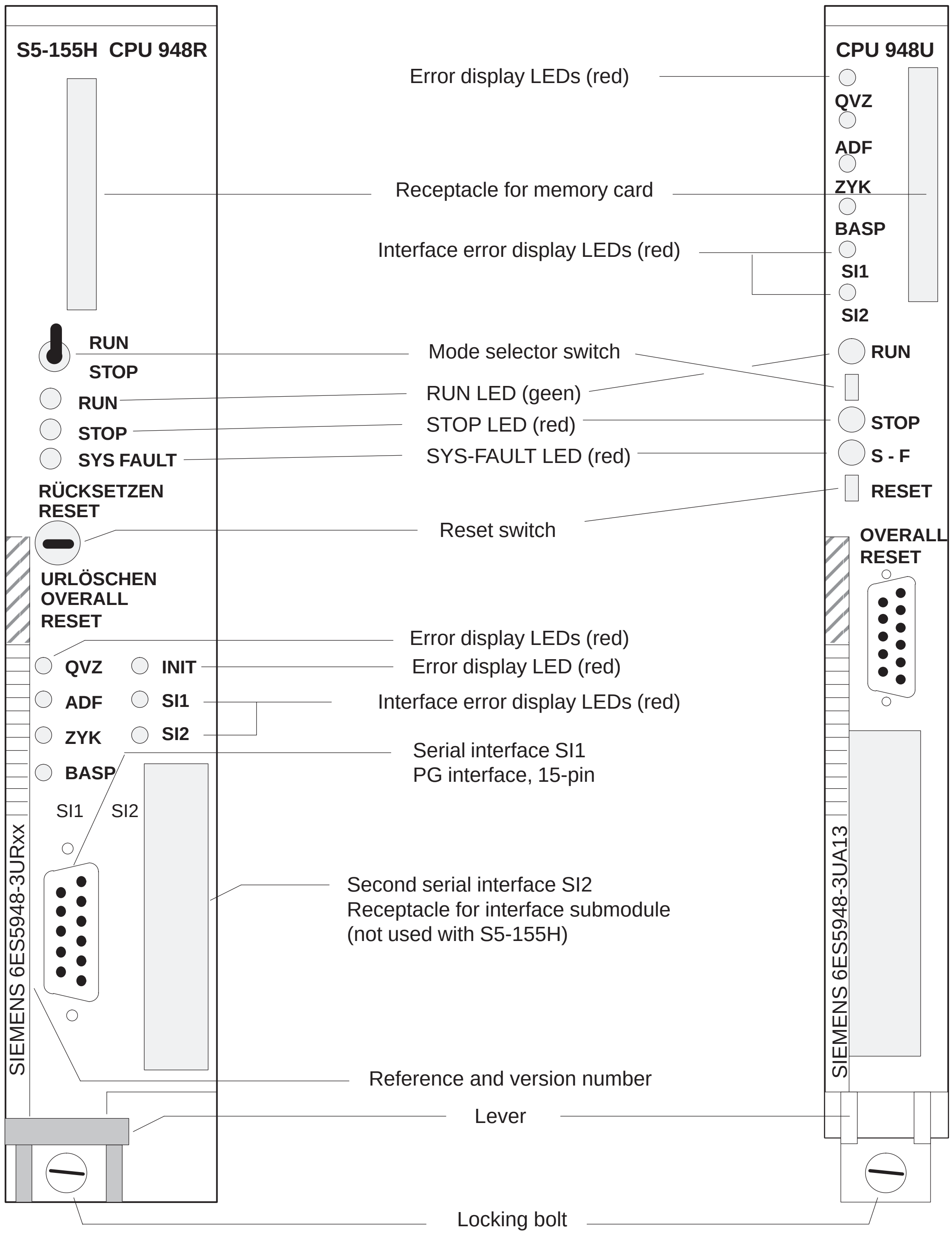


Figure 3-1 CPU 948R/948RL and CPU 948U Control Elements and LEDs

Mode Selector Switch

The mode selector switch has two positions:

- RUN

  When the mode selector switch is set to ’RUN’ and the green LED is on, the CPU 948R/948RL is processing the user program.

- STOP

  The CPU 948R/948RL goes to ’soft STOP’ when the user switches from ’RUN’ to ’STOP’. The red ”STOP” LED goes on.

Reset Switch

The restart functions ”Overall reset”, ”Cold restart” and ”Cold restart with memory” can be initiated via the mode selector switch and the reset switch:

Function	Switch position	Description
Overall reset (OVERALL RESET)	Down	An overall reset reinitializes the internal RAM (meaning any data currently in RAM are erased and the contents of the memory card, if any, are copied to internal RAM). A complete self-test is then executed.
Cold restart (RESET)	Up	A cold restart, or RESET, resets all flags, timers, counters and the process image. OB 20 is then called, and user program processing begins again.
Cold restart with memory	Middle	User program processing begins again, but all flags, timers, counters and the process image retain their current states.

Status LEDs

The following overview describes the LEDs for ”RUN”, ”STOP” and ”SYS FAULT”.

The ”STOP” LED signals a ’soft STOP’, the ”SYS FAULT” LED a ’hard STOP’.

In ’soft STOP’ mode, the CPU 948R/948RL can scan the user program (OB 39) cyclically, but the digital outputs remain disabled. In ’hard STOP’ mode, no program can run; the CPU is at a ’standstill’. This state can be exited only by switching the power off and then on again.

LED			
RUN	**STOP**	**SYS-FAULT**	**Mode**
RUN or RESTART mode			
On	Off	Off	The CPU is in RUN mode and is master (cyclic operation).
Flashes	Off	Off	The CPU is in RUN mode and is the standby (cyclic operation).
On	Flashes	Off	The CPU is master; the parallel link has failed.
On	On	On	Appears briefly when the controller is switched on.
On	On	Off	The CPU executes the self-test on startup.
Off	Off	Off	The CPU is in the RESTART mode or PROGRAM TEST.
’Soft STOP’ mode			
Off	On	Off	The CPU is in ’soft STOP’ mode. After switching on the power when the mode selector switch is at STOP and no errors occurred during initialization. A restart is possible.
Off	Flashes at high fre-quency	Off	The CPU is in ’soft STOP’ mode. An overall reset was requested via mode selector switch/reset switch or by the operating system. A restart is possible only after performing an overall reset or after eliminating the problem and then performing an overall reset.
Off	Flashes at low fre-quency	Off	The CPU is in ’soft STOP’ mode. • An error was detected during cyclic program processing. The CPU is at STOP because no appropriate error handling routine was programmed. When you move the mode selector switch from RUN to STOP, the LED will once again show a steady light as long as the error does not re-occur. • When error conditions exist, for example, selection of an illegal Restart mode, DB1/DX0 errors, and so on. • When a STOP operation (STP or STS) was encountered in the user program. • In the event of a PROGRAM TEST programmer function for this CPU. • Some programming errors and controller faults also set the ’ADF’, ’QVZ’ or ’ZYK’ LEDs.
’Hard STOP’ mode			
Off	Off	On	The CPU is in ’hard STOP’ mode. • When error-free execution of the system program is no longer possible, the CPU enters the ’hard STOP’ mode. • Reasons for a ’hard STOP’: – Timeout (QVZ) or parity error (PARE) in system RAM – ISTACK overflow – STEP 5 operation ”STW” • A ’hard STOP’ can be exited only by turning off the controller and switching it on again.
’Activate standby’ mode			
Flashes	Flashes	Off	The CPU is the standby, and the mode is ’Activate standby’.

Error LEDs

The following overview shows why and when each error LED goes on:

LED	Description
QVZ (timeout)	A module addressed by the program no longer acknowledges, although/because: • it either acknowledged in the process image (IB 0 to 127, QB 0 to 127) on a CPU 948R/948RL cold restart and was entered as available in the so-called ’9th track’ • or was entered in DB 1 (address list) and was recognized as being available on a cold restart • or was addressed in direct access mode • or no access is possible to the data handling blocks on the module. Possible causes: • Module failure; failure of the expansion unit • Module was removed during operation, while the CPU was at STOP or when the controller was switched off and there was no subsequent cold restart. • Failure of the enable voltage L+
	A timeout occurred while user memory was being accessed.
ADF On	The user program referenced an address in the process image which was not entered in DX 1.
ZYK On	The watchdog timer used for scan time monitoring responded and cyclic program processing was interrupted.
BASP On	Command output is disabled; the digital outputs are set directly to the safe state (0).
INIT On	Applies to CPU 948 UR 11/12, 21/22 and 51: This LED briefly shows a steady light during the initialization procedure which follows POWER ON, and during operation in the event of a system fault. Applies to CPU 948 R UR 13, 23, 53: INIT LED does not exist on the front plate.

A detailed description of interrupt servicing and error handling procedures can be found in the Programming Guide for the CPU 948R (Volume 2 of this manual).

Interface Error LEDs SI1 and SI2

Reasons why the interface error LEDs go on:
LED SI2 is always off unless there is a CPU fault.

LED SI1	Reason
On	No communication possible; internal error.
Off	Both interfaces are initialized and ready.

Startup

The CPU must be inserted into the correct slot in the central controller. The backup battery must be inserted and in good working order before the CPU can be put into operation.

Overall Reset

Proceed as follows:

Step	Entry/Activity	Result
1.	Set the mode selector switch to ’STOP’.	
2.	Switch on the mains power.	The following LEDs on the CPU must go on: • Red ”STOP” LED (flashes at high frequency) • Red ”INIT” LED (briefly) • Red ”BASP” LED
3.	Hold the reset switch in the ’OVER-ALL RESET’ position and move the mode selector switch from ’STOP’ to ’RUN’.	The red ”STOP” LED and the RUN LED now show a steady light.

The red ’SYS FAULT’ LED also goes on only if an error occurred during the overall reset. In this case, repeat the measures described. If necessary, switch the power off and then on again. If the LED is still on, the CPU module is defective.

Cold Restart

Continue as follows:

Step	Entry/Activity	**Result** for master
4.	Set the mode selector switch to ’STOP’.	
5.	Hold the reset switch in the RESET position and move the mode selector switch from ’STOP’ to ’RUN’.	1. The red ’STOP’ LED goes out 2. The red ’STOP’ LED and the green ’RUN’ LED go on 3. The green ’RUN’ LED goes on 4. The red ’BASP’ LED goes out The CPU is not in ’RUN’ mode, but is still without a user program.

Cold Restart with Memory Function

The reset switch allows you to execute a manual cold restart (RESET) with memory. Please refer to the Programming Guide for the CPU 948R (Volume 2 of this manual) to see when a manual cold restart (RESET) with memory is permissible.

Step	Entry/Activity	**Result** for master
1.	Move the mode selector switch from ’STOP’ to ’RUN’.	1. The red ’STOP’ LED goes out 2. The red ’STOP’ LED and the green ’RUN’ LED go on 3. The green ’RUN’ LED goes on 4. The red ’BASP’ LED goes out

For maintenance purposes or in the event of an error, the above-mentioned startup procedures, without a user program, can be used to see whether the CPU is functioning properly.

CPU 948R/948RL Interfaces

This chapter provides information on CPU 948R/948RL interfaces (ports) which can be used to connect a programmer or personal computer.

- **Programmer port SI1**

You can connect a programmer to this frontplate port regardless of the CPU's current mode.

- **Interfacing with SINEC H1 over the parallel wiring backplane**

Connecting a programmable controller with a programmer via SINEC H1 enables very-high-performance communications between the two. For example, the loading of application software into the CPU while in STOP mode is up to eight times faster than it would be if a serial port were used.

In addition to a CPU 948R/948RL, you also need a CP 143 (revision level 3), a PG 7xx programmer with SINEC H1 interface, and the STEP 5 ”Single Tasking” (version 6.3 or newer) or ”Multi-Tasking” (version 6.0 or newer) software.

Note
You cannot interface a subunit to SINEC H1 and still use the serial port.

Interfacing to SINEC H1 is discussed in detail in the Programming Guide for the CPU 948R.

Specifications

Important for use in the USA and Canada

The following approval certifications have been granted:

UL Listing Mark
Underwriters Laboratories (UL) to
Standard UL 508, Report E 85972

CSA Certification Mark
Canadian Standard Association (CSA) to
Standard C 22.2 No. 142, Report LR 63533

3.3 Technical Specifications

Common Technical Specifications

The following table contains the common technical specifications for the CPUs 948R and 948RL.

<table>
<tr><th>Characteristic/Function</th><th colspan="5">Value</th></tr>
<tr><td>Degree of protection</td><td colspan="5">IP 00</td></tr>
<tr><td>Ambient conditions
Ambient temperature during operation
Temperature change during operation
during transport and
while in storage
Relative humidity
Pollutant emissions: SO₂
H₂S
Oscillation during operation</td><td colspan="5">0 to 55 °C
Max. 10 K/h
Max. 20 K/h
Max. 95 % at 25 °C, no condensation
10 cm³/m³, 4 days
1 cm³/m³, 4 days
10 ...58 Hz (const. amplitude 0.075 mm)
58 ...500 Hz (const. acceleration 1 g)</td></tr>
<tr><td>Noise immunity, electromagnetic compatibility (EMC)
Interference suppression Limit class
Conducted interference on AC supply lines

Immunity against static discharge to IEC 801-2 (ESD)
Immunity against high-frequency radiation</td><td colspan="5">See Technical Specifications for the S5-135U/155U
A (to VDE 0871)
2 kV (to IEC 801-4 (Burst)
1 kV (to IEC 801-5) Line to line
2 kV (to IEC 801-5) Line to ground
Proper installation ensures an interference immunity of 4 kV contact discharge (8 kV atmospheric discharge).
HF current-sourcing to IEC 801-6
Limit class 3 (up to 200 MHz), corresponding to 3 V/m</td></tr>
<tr><td>Auxiliary power:
Supply voltage
Power consumption at 5 V</td><td colspan="3">948R UR11, 12, 21, 22, 51:
5 V ± 5 %
3.6 A typ.</td><td colspan="2">948R UR13, 23, 53:
5 V ± 5 %
0.5 A typ.</td></tr>
<tr><td>Backup voltage:
Backup current:</td><td colspan="5">3.4 V
10 µA (at 25 °C) typ.</td></tr>
<tr><td></td><td>P area</td><td>O area</td><td>IM3 area</td><td>IM4 area</td><td>Total</td></tr>
<tr><td>Digital inputs with process image
Digital inputs without process image
or analog inputs</td><td>max 1024
max. 1024
max. 64</td><td>–
max. 2048
max. 128</td><td>–
max. 2048
max. 128</td><td>–
max. 2048
max. 128</td><td>max. 1024
max 7168
max. 448</td></tr>
<tr><td>Digital outputs with process image
Digital outputs without process image
or analog outputs</td><td>max 1024
max. 1024
max. 64</td><td>–
max. 2048
max. 128</td><td>–
max. 2048
max. 128</td><td>–
max. 2048
max. 128</td><td>max. 1024
max 7168
max. 448</td></tr>
<tr><td>Flags</td><td colspan="5">2048</td></tr>
<tr><td>S flags</td><td colspan="5">32768</td></tr>
<tr><td>Timers</td><td colspan="5">256</td></tr>
<tr><td>Counters</td><td colspan="5">256</td></tr>
</table>

Characteristic/Function	Value	
Baud rate of the serial programmer port	9600 bps	
Number of blocks Program blocks (PBs) Sequence blocks (SBs) Function blocks (FBs) Function blocks FXs) Data blocks (DBs) Data blocks (DXs) Organization blocks (OBs)	 256 256 256 256 256, 253 of which are programmable 256, 253 of which are programmable OB 1 to 39 (interfaces to the operating system)	
Integral special-function organization blocks (OBs)	OB 121, 122, 124, 125, 131 to 133, 141 to 143, 150, 151, 153, 254, 255	
Integral serial PG port	9600 bps	
Dimensions (W x H x D)	40.6 mm x 233.4 mm x 160 mm	
Weight	948R UR11, 12, 21, 22, 51: Approx. 1 kg	948R UR13, 23, 53: Approx. 0.6 kg

Differences between CPU 948R and CPU 948RL

The following table shows an overview of the differences in performance of the CPU 948R and the CPU 948RL.

Characteristic	CPU 948R	CPU 948RL
User memory size	640 Kbytes (CPU 948R-1) 1664 Kbytes (CPU 948R-2)	128 Kbytes
Execution times	See Pocket Guide 6ES5 997-3UR21	See CPU 948R
Basic scan cycle time	approx. 5 ms	approx. 15 ms
Digital inputs	Supports following I/O types: Types 1, 2, 3 and 4	Supports following I/O types: Types 1, 2 and 3
	max. 1024 inputs with process image Types 1, 2, 3 and 4 (1-, 2- or 3-channel)	max. 1024 inputs with process image Types 1, 2 and 3 (1- or 2-channel)
	+ 3072 without process image (Types 1 and 2)	+ 1024 without process image (Types 1 and 2) + 2048 without process image (Type 2)
	+ 4096 without process image with direct memory access Type 2 (1-channel switched)	+ 4096 without process image with direct memory access Type 2 (1-channel switched)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)

Characteristic	CPU 948R	CPU 948RL
Digital outputs	Supports following I/O types: Types 8, 9, 10 and 11	Supports following I/O types: Types 8, 9, 10 and 11
	max. 1024 outputs with process image Types 8, 9, 10 and 11 (1- or 2-channel)	max. 1024 outputs with process image Types 8, 9, 10 and 11 (1- or 2-channel)
	+ 3072 without process image (Types 8 and 9, 1-channel)	+ 1024 without process image (Types 8 and 9, 1-channel) + 2048 without process image (Type 9, 1-channel)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)
Analog inputs	Supports following I/O types: Types 13, 14, 15 and 16	Supports following I/O types: Types 13, 14 and 15
	max. 192 inputs (1-, 2- or 3-channel)	max. 64 inputs (only 1- or 2-channel)
	max. 448 inputs (1-channel switched)	max. 448 inputs (1-channel switched)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)
Analog outputs	Supports following I/O types: Types 18, 19, 20 and 21	Supports following I/O types: Types 18, 19, 20 and 21
	max. 192 outputs (1- or 2-channel)	max. 64 outputs (1- or 2-channel)
	max. 448 outputs (1-channel switched)	max. 448 outputs (1-channel switched)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)
CP/IP	Supports following I/O types: Types 24 and 25	Supports following I/O types: Types 24 and 25

You will find explanations on the individual I/O types in Section 4.1

Connector Pin Assignments

Please refer to Chapter 10 of the S5-135U/155U System Manual for a list of connector pin assignments on the CPU 948R/948RL’s backplane connectors and front connector (programmer port). The pinout is the same as for the CPU 948.

I/O Operating Modes and Permissible I/O Modules

4

This chapter describes the possible I/O modes for the S5-155H (redundant, three-channel redundant, one-sided and switched) and lists the permissible modules in each case. The explanations concerning redundant I/Os in Sections 5.3 and 5.4 are of particular importance. You will also find the necessary wiring diagrams in that chapter. Standard function blocks FB 40/41 and 43 for analog value input/output are also discussed.

This chapter is vital for configuring and operating your I/O modules.

4.1 Overview

I/O Operating Modes

The S5-155H supports four different I/O operating modes:

- **Redundant I/Os**

  The module is present in **both** subunits under the **same** address. This mode offers a **high degree of fault tolerance**.

- **Three-channel redundant I/Os**

  There are three I/O modules. Two inputs are assigned to the same address and the third to either switched I/Os or to subunit A or B. However, the highest degree of fault tolerance is achieved if the third channel is assigned to switched I/Os.

- **One-sided I/Os**

  The module is assigned **exclusively** to one of the two subunits. If this subunit fails, the modules assigned to it also fail. This means that the fault tolerance of this configuration is **no higher** than that of an S5-155U.

- **Switched I/Os**

  The module can be operated by **either** of the two controllers. This mode offers **greater fault tolerance** than the S5-155U.

These modes can be combined in an S5-155H. Each I/O module can be configured individually.

Note

All four I/O modes – one-sided, switched, redundant and three-channel redundant – can be combined in one S5-155H.

I/O Types

When the digital/analog I/Os and CPs/IPs are configured with COM 155H, each process signal managed by the system program is assigned a specific type number.

The type number identifies

a) the signal type: digital, analog, input, output, CP, IP and

b) the operating mode: one-sided, switched, redundant, three-channel, redundant

The table below lists all configurable I/O types. Please also refer to the ”COM 155H” description in this manual.

Type No.	Meaning		Fault tolerance
1	DI byte	one-sided	Standard (same as S5-155U)
2	DI byte	switched	Higher
3	DI byte	2-channel redundant	High
4	DI byte	3-channel redundant	Highest
8	DQ byte	one-sided	Standard
9	DQ byte	switched	Higher
10	DQ byte	redundant	High
11	DQ byte	redundant	High (with three readback DIs)
13	AI channel	one-sided	Standard
14	AI channel	switched	Higher
15	AI channel	2-channel redundant	High
16	AI channel	3-channel redundant	Highest
18	AQ channel	one-sided	Standard
19	AQ channel	switched	Higher
20	AQ channel	redundant	High
21	AQ channel	redundant with fault locating	Highest
24	CP/IP	one-sided	Standard
25	CP/IP	switched	Higher

Configuring the I/Os

Digital I/Os are configured **by byte**, analog I/Os **by word**. This means that you can assign each I/O byte/word the attribute ”one-sided”, ”switched” or ”redundant”. When doing so, observe the following address restrictions:

I/O Type	Address Range	
One-sided digital I/Os	PY 0 ... 255	OY 0 ... 255
Switched digital I/Os	PY 0 ... 255	OY 0 ... 255
Redundant digital I/Os	PY 0 ... 127	
One-sided analog I/Os	PW 128 ... 254	OW 0 ... 254
Switched analog I/Os	PW 128 ... 254	OW 0 ... 254
Redundant analog I/Os	PW 128 ... 254	OW 0 ... 254

Switched digital and analog I/Os can also be used in other I/O areas (see Figure 4-1).

I/O Address Areas

Figure 4-1 provides an overview of the various I/O areas in the S5-155H for redundant, switched and one-sided I/Os.

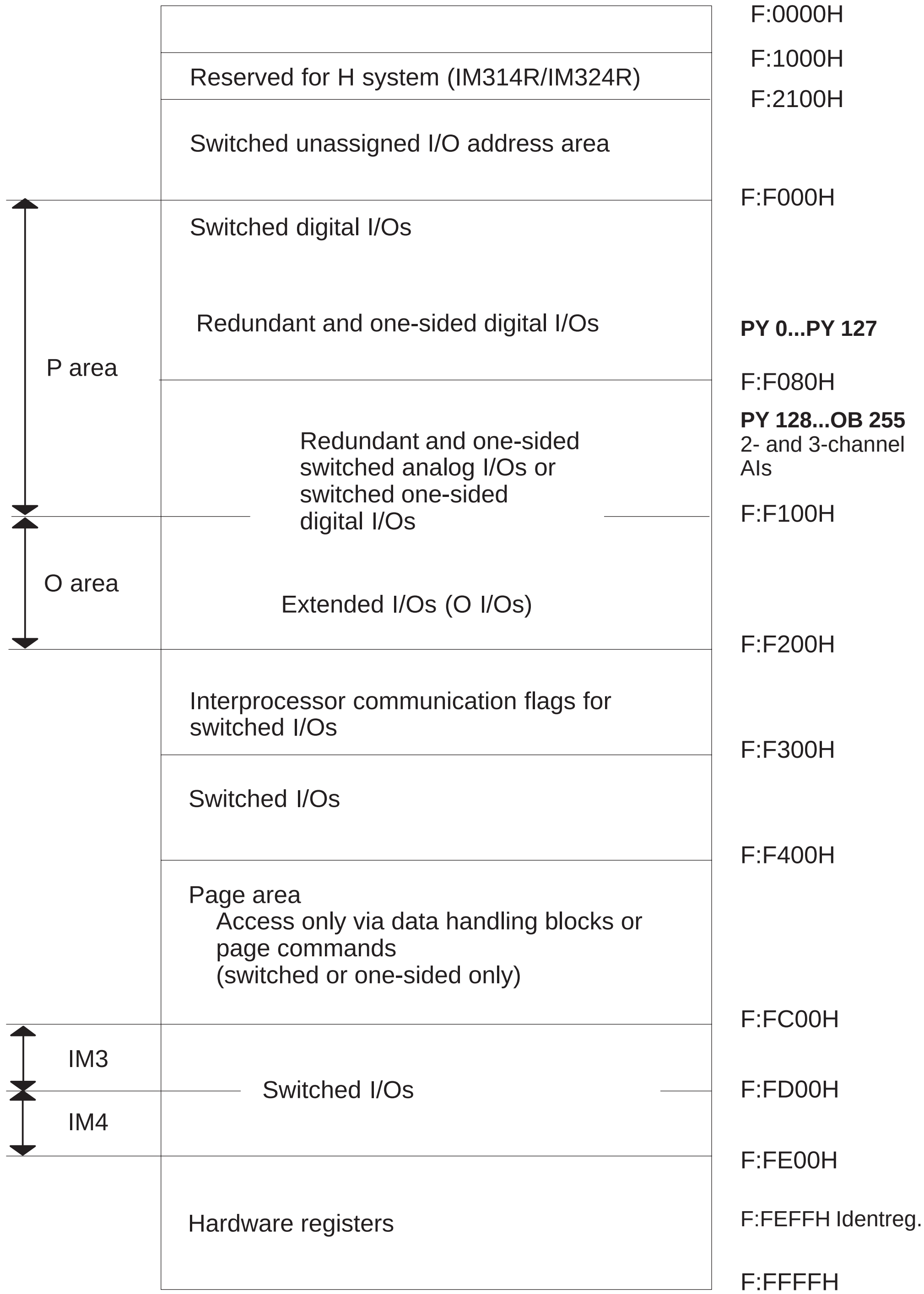


Figure 4-1 I/O Areas in the S5-155H

Updating the Process Input and Output Images

The process output image (redundant PIQ, switched PIQ, one-sided PIQ) is output after OB 1 has been processed. The S5-155H self-test then runs. This can last between 2 and 38 ms (test slice 2 ms * n), plus any time needed for interrupt servicing.

The process input image (redundant PII, switched PII, one-sided PII) is then read in. The PIIs of both subunits are exchanged and compared. OB 1 is then re-invoked (see Figure 2-2).

4.2 Redundant I/Os (Overview)

Redundant I/O (1-out-of-2)

In this mode, the input or output module has the **same** address in **both** subunits.

This mode offers the highest possible degree of fault tolerance, since failure of a central controller or an input or output module is tolerated (NON-STOP operation). The modules can be plugged into either the central controller or the expansion unit.

Figure 4-2 shows a redundant (two-channel) configuration.

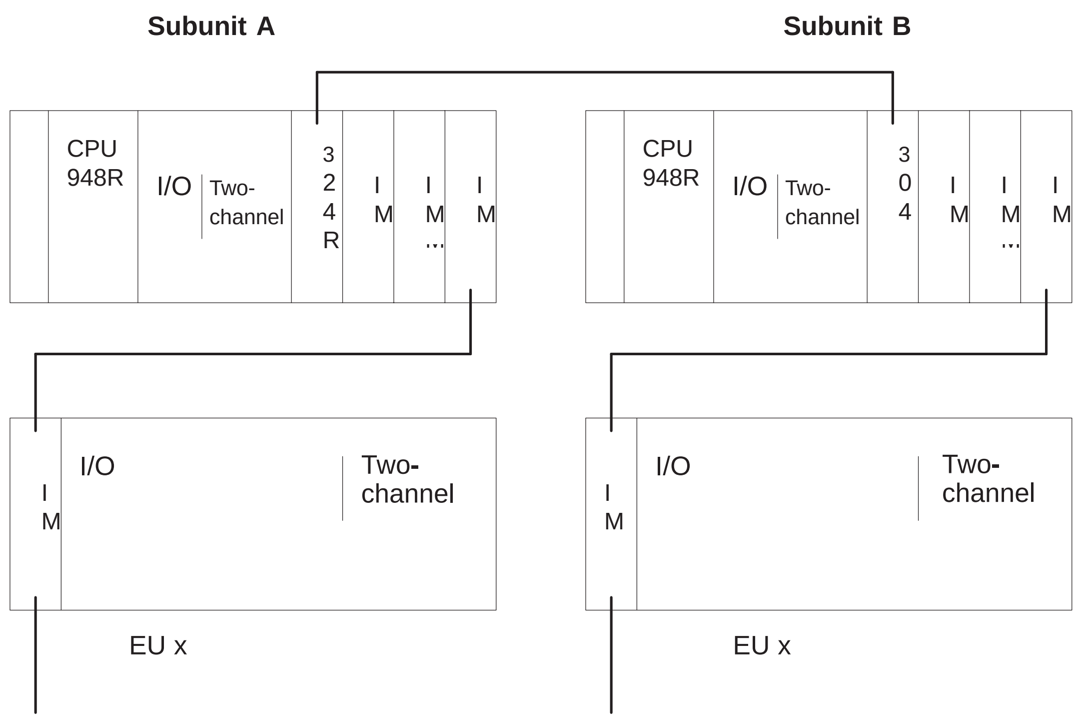


Figure 4-2 Redundant I/O Operation and Permissible Modules

Interface Modules and Expansion Units

In two-channel redundant I/O mode, the same interface modules and expansion units can be used as for the S5-155U (refer to the S5-135U/155U System Manual).

If the ET electronic terminator is being used in a redundant configuration, the following applies: If an ET 100 I/O byte must be passivated due to a timeout (QVZ), then the whole phase of this ET 100 is shut down.

Digital and Analog I/O Modules

”Redundant I/O” means the redundant input/output module in question is plugged into subunit A **and** subunit B, and both I/O modules have the **same I/O address and** have been configured with COM 155H as redundant.

All I/O modules which can be used in the S5-155U can also be used in the S5-155H.

I/Os

Redundant I/O modules are permitted in the following I/O address areas only (see Section 4.1):

- Redundant DIs/DQs: FF000 to FF07F (PY 0 to 127)
- Redundant AIs/AQs: FF080 to FF1FF (PW 128 to 254 and OW 0 to 254)

Please refer also to the configuring information for I/O modules in Section 4.1.

Note

If you want to operate specific redundant digital inputs or outputs as ”NON-STOP DIs” or ”NON-STOP DQs”, please read the information presented below in ”Locating facility (LF)”.

Locating Facility (LF)

For every redundant digital input and every redundant digital output you want to operate as a NON-STOP DI or NON-STOP DQ, you must configure a special locating facility with which the 155H system program can locate errors quickly (see Figures 4-8/4-9).

”NON-STOP DI/DQ” means that the failure of the DI/DQ and its subsequent repair have no effect whatsoever on the process.

A locating facility (LF) for a NON-STOP DI or a NON-STOP DQ consists of

- a locating digital input (L-DI) and
- a locating digital output (L-DQ).

Overview of Redundant I/O Types

This section presents an overview in the form of keywords of the characteristics of the various redundant I/O types in the S5-155H.

- **Redundant DIs without error locating**
  - Error detection: By discrepancy monitoring and edge change monitoring
  - Error locating: None
  - Passivation: Passivation of the DI byte in the subunit in which a ’stuck at 0’ error was found
- **Redundant DIs with error locating**
  - Error detection: By discrepancy monitoring
  - Error locating: By L-DQ
  - Passivation: Passivation of the defective DI byte
- **Redundant three-channel DIs**
  - Error locating: By the 2-out-of-3 method

- **Redundant DQs without error locating**

  In the case of ’stuck at 1’ errors:

  – Error detection: By cyclic comparison of PIQs and readback DIs

  – Error locating: None

  – Passivation: Passivation of the readback DI; that is, testing of 0 to 1 edge no longer possible

  In the case of ’stuck at 0’ errors:

  – Error detection:
  – Error location:
  By testing a 0 to 1 edge change

  – Passivation: Passivation of the defective DQ byte

- **Redundant DQs with error locating**

  In the case of ’stuck at 1’ errors:

  – Error detection: By cyclic comparison of PIQs and readback DIs

  – Error locating: By switching off the power supply to the group via L-DQ

  – Passivation: Passivation of the defective DQ byte and all other redundant DQs with the same group supply

  In the case of ’stuck at 0’ errors:

  – Error detection:
  – Error locating:
  By testing a 0 to 1 edge change or, at the latest, after approx. 10 hours when initial state = ”1”.

  – Passivation: None

  The defective DQ byte is reported only; access operations are not affected, and there is no further testing of the DQ byte.

- **Redundant AIs**

  – Error detection: By analog value discrepancy monitoring; minimum or maximum value may be selected on error.

  – Error locating:
  – Passivation:
  Error-dependent; see Section 4.4

- **Redundant three-channel AIs**

– Error detection:
– Error locating:
– Passivation:
By analog value discrepancy monitoring

- **Redundant AQs**

– Error detection:
– Error locating:
– Passivation:
By reading back the analog output value

Note:
More detailed information on all of the I/O types listed above, and in the same order, can be found in Sections 4.3 and 4.4.

Detecting Errors on Digital Output Modules

The table below tells you the amount of time needed to detect an error on digital output types 10 and 11.

	Error	Type 10 with Readback DI	Type 11 with 3 Readback DIs
1.	'Stuck at 1' on DQ module. When PIQ intermittent.	After two 0 → 1 edge changes	After two 0 → 1 edge changes
2.	'Stuck at 1' on DQ module. When PIQ = 0.	After TI at latest	After TI at latest
3.	'Stuck at 1' on DQ module. When process image = 1.	Through inspection	Immediately preceding the L-DQ test = every 10 hours
4.	'Stuck at 0' on DQ module or wirebreak in DQ module connection. When PIQ intermittent.	After two 0 → 1 edge changes or *) in L-DQ test = every 10 hours (fault has short-term effect[1)] on process)	After two 0 → 1 edge changes or *) immediately preceding the L-DQ test = every 10 hours
5.	'Stuck at 0' on DQ module or wirebreak in DQ module connection. When PIQ = 0.	Through inspection	Through inspection
6.	'Stuck at 0' on DQ module or wirebreak in DQ module connection. When PIQ = 1.	In the L-DQ test (= every 10 hours) (fault has short-term [1)] effect on process)	Immediately preceding the L-DQ test = every 10 hours
7.	'Stuck at 1' after decoupling diode (fault cannot be automatically rectified). When process image = 0.	After TI at latest	After TI at latest
8.	'Stuck at 1' after decoupling diode (fault cannot be automatically rectified). When process image = 1.	Through inspection	Through inspection
9.	Wirebreak in or after the decoupling diode. When PIQ intermittent.	After two 0 → 1 edge changes or *) immediately after the L-DQ test = every 10 hours (fault has short-term[1)] effect on the process)	After two 0 → 1 edge changes or *) immediately following L-DQ test = every 10 hours (fault has short-term[1)] effect on the process)
10.	Wirebreak in or after decoupling diode. When process image = 0.	Through inspection	Through inspection
11.	Wirebreak in or after decoupling diode (the wires must be redundant up to the actuator and must be run from the actuator to the readback DI). When process image = 1.	In the L-DQ test = every 10 hours (fault has short-term [1)] effect on the process)	In the L-DQ test = every 10 hours (fault has short-term [1)] effect on the process)
12.	Short-circuit to 0 after decoupling diode (fault cannot be automatically reported, but can be located). When PIQ = 1.	After TI at latest	After TI at latest

TI = 2 * T_R or 2 * PLC scan time (whichever is higher)
*) Depending on which event occurs first
1) Short-term effect on the process ('short-term' means 1 * t_R + 2 * basic clock rate for timed interrupts, without regard to the PLC scan time)
T_R = Configured readback delay time
t_R = Actual readback delay time

4.3 Redundant Digital Inputs/Outputs (DIs/DQs)

4.3.1 Redundant DIs without Error Locating Facility

Two-channel (1-of-2) DIs without error locating facility detect faults, but do not locate them. This means that these DIs **cannot** be operated as ”NON-STOP” DIs.

There is a redundant digital input in both subunit A and subunit B. The system program compares these DIs cyclically to make sure that their signal states are identical; this comparison is made during updating of the PII. If the system program discovers redundant DIs with different signal states, these DIs are flagged and the configured discrepancy timer started. As long as the timer is running, the last identical value is maintained as signal state.

If the signal states of the DIs are still different after the discrepancy time has expired, an appropriate entry is made in the error DB, and the system program waits for the next edge change. Until this edge change takes place, the last identical value continues to be retained as signal state. After the edge change, the signal state of the DI on which the edge change took place becomes the final valid signal state. The other side is passivated.

The signal states of the redundant DIs are also compared in cases of direct I/O access. In the event of a discrepancy, the last identical value is taken as signal state.

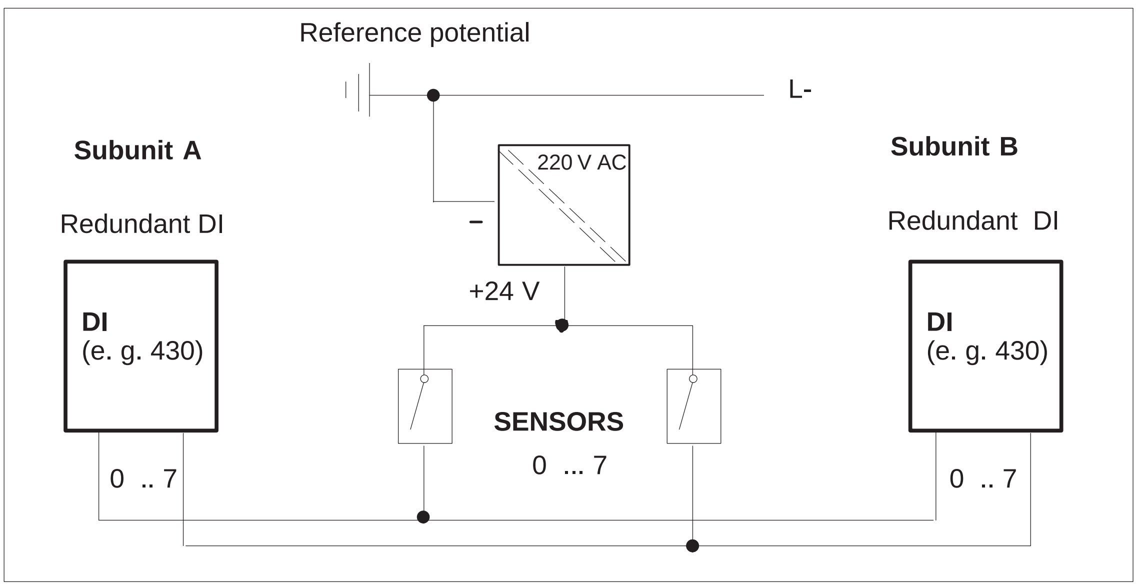


Figure 4-3 Redundant Two-Channel DIs without Error Locating Facility

4.3.2 Redundant DIs with Error Locating Facility

The 1-out-of-2 DI with LF both detects and locates faults. With the aid of the circuitry shown in Figure 4-4, the system locates the defective DI module in the event of a fault. The following sequence is then put into effect when the discrepancy time has elapsed:

- A ”0” signal is output to both L-DQs (subunits A and B), thus switching off the sensor power supply.
- A ”0” must be read back from both DIs after the specified readback delay time has elapsed. A ”1” at a DI indicates a defect in the module.
- A ”1” signal is output to both L-DQs.

The defective module is reported and the DI byte passivated; that is, this subunit’s DI byte will no longer be accessed (one-sided operation). Fault location can take several PLC cycles, depending on the configured readback delay time. During this time, the last valid process I/O image is transferred in the case of direct access to the relevant DI bytes. ”Relevant” DI bytes are all DI bytes sharing the same group power supply.

The term ”group” designates all sensors for redundant DIs or DQs supplied by the same L-DQ. The smallest possible group consists of one redundant byte, the largest possible group of all redundant DIs in an S5-155H.

Testing the Error Locating Facility

The L-DIs of the two-channel 1-out-of-2 are tested for ’stuck at 0’ and ’QVZ’ (timeout) once in each test cycle (approx. every 5 minutes).

The L-DIs and L-DQs of the two-channel 1-out-of-2 DIs are tested for ’stuck at 0’ every 10 hours by setting the L-DQs to 0 page by page. They are tested for ’stuck at 1’ only in the master’s Restart routine by setting the L-DQs to 0 in both subunits. Also refer back to the table entitled ”Detecting Errors on Digital Output Modules”.

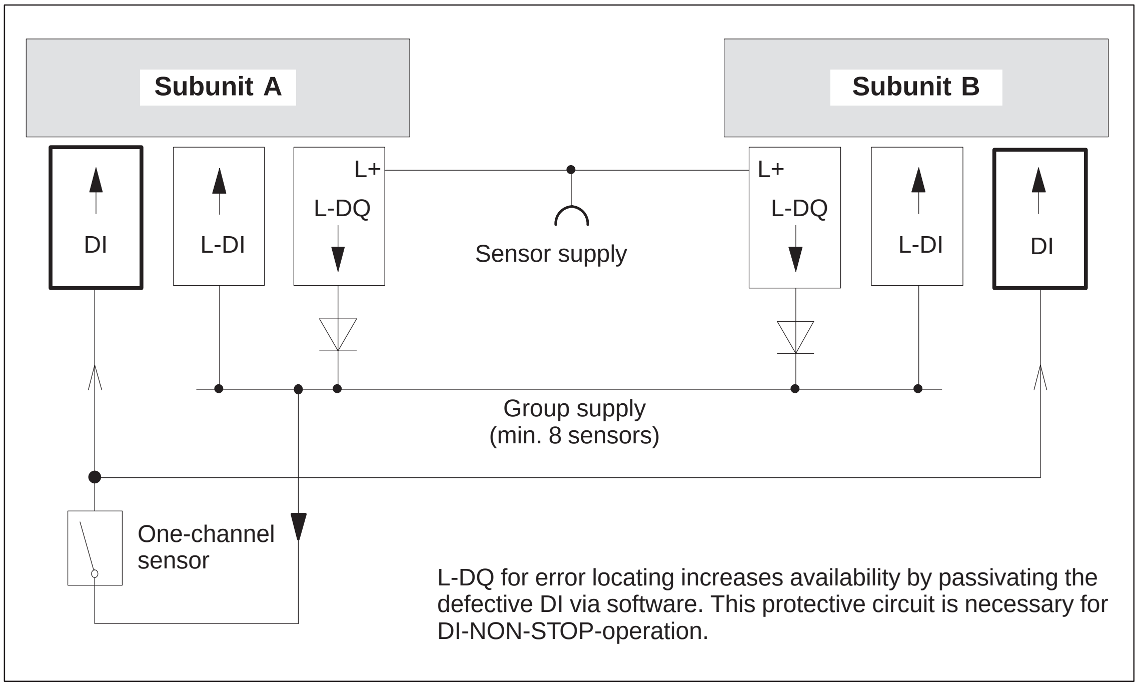


Figure 4-4 Block Diagram: 1-out-of-2 DI with Error Locating

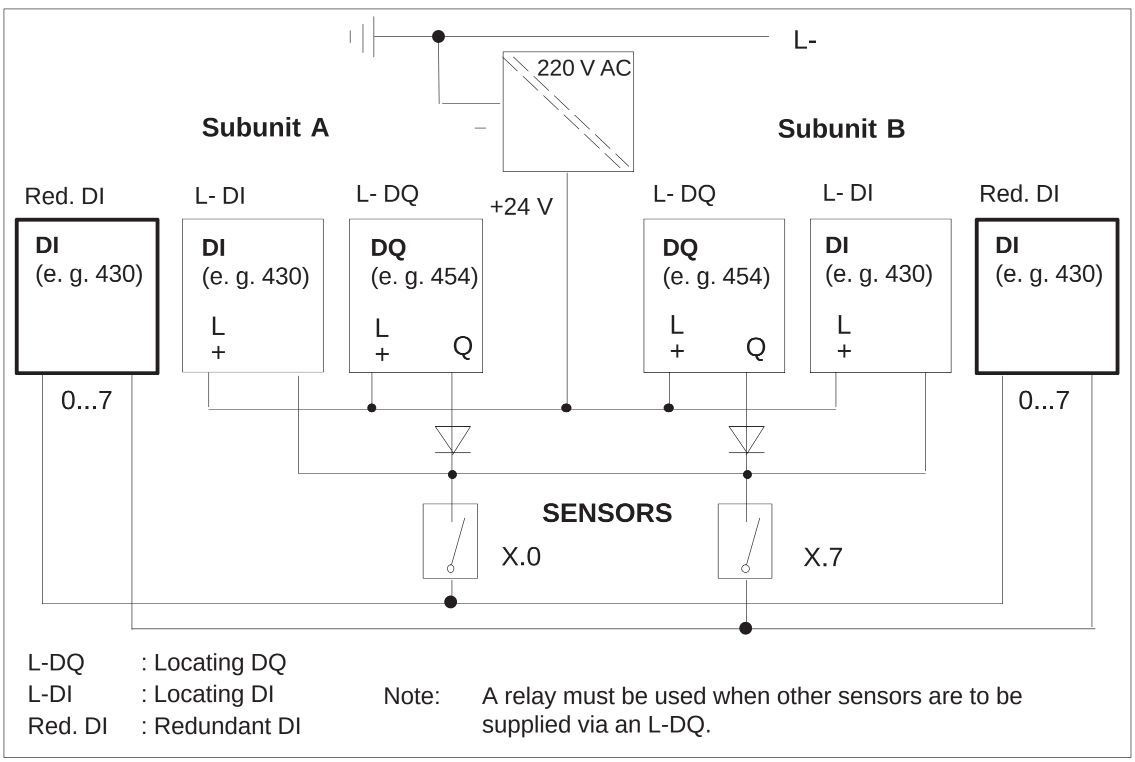


Figure 4-5 Redundant Two-Channel DI with Error Locating

4.3.3 Redundant Three-Channel DIs

Three-channel (1-out-of-3) DIs detect and locate faults. This means that these DIs can be operated as ”NON-STOP DIs”.

Each subunit is equipped with one redundant digital input, and the third is assigned to switched I/Os or to subunit A or B. Assigning the third DI to the switched I/Os provides a higher degree of fault tolerance than assigning it to subunit A or B.

The 155H system program compares the three DIs cyclically to make sure that their signal states are identical. This comparison takes place during updating of the process input image. If the system program discovers DIs with different signal states, these DIs are flagged and the specified discrepancy timer started. As long as this timer is running, the relevant standard value is taken as signal state, depending on whether one or three sensors were configured. If only one sensor was configured, the standard value is based on a 2-out-of-3 decision. If three sensors were configured, the last identical value is retained as signal state.

If the signal states of the DIs are still different after the discrepancy time has elapsed, the fault is reported. The result of the 2-out-of-3 decision is given as valid signal state. The byte is passivated. The DI continues on a 1-out-of-2 basis until the fault has been eliminated and the byte depassivated.

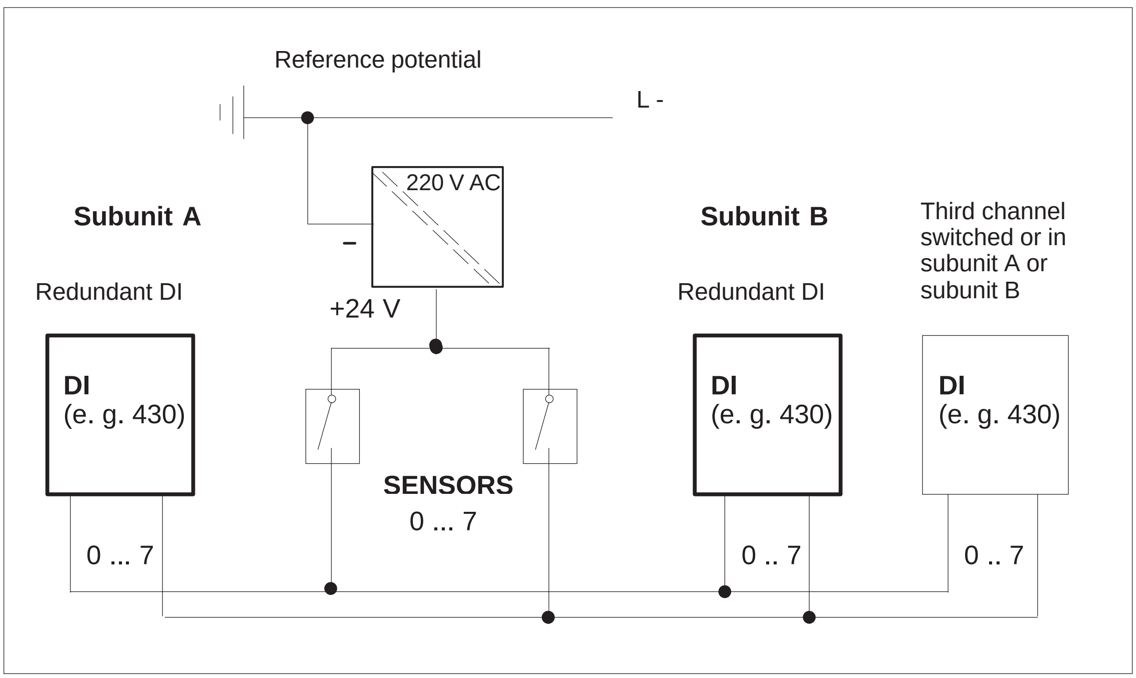


Figure 4-6 Redundant Three-Channel DI with One Sensor

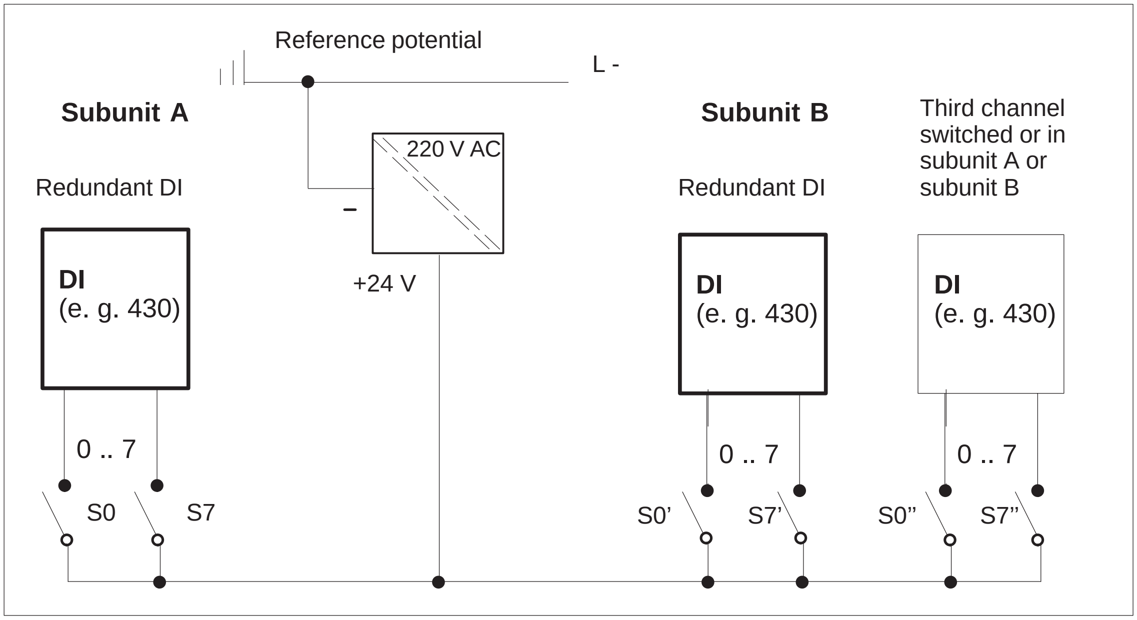


Figure 4-7 Redundant Three-Channel DI with Three Sensors

Direct I/O access to a three-channel DI is permitted.

The standardized value of the three digital inputs is supplied as the result.

The use of three sensors provides the highest possible degree of fault tolerance, as sensor faults can also be detected, located and passivated.

The maximum amount of time needed to locate a fault is:

2 x configured discrepancy time +

2 x PLC scan time.

4.3.4 Configuring Redundant Process Interrupts (DI 0)

1. Configure DI 0 as a redundant digital input without error locating (and wire accordingly).

   The system program uses the time configured for DI 0.0 as the discrepancy time for all DI 0 bits. Times specified for DI 0.1 to DI 0.7 are irrelevant.

   The maximum discrepancy time configurable for DI 0 is 1.0 s.
2. Enter ”Interrupt DI”: YES in COM 155H’s operating system form.
3. Specify ”Process interrupts:”YES and ”Timed interrupt servicing”:YES in data block DX 0. Specify 10 ms as ”Basic clock rate for timed interrupt servicing”.

Functions, Principle of Operation and Error Handling

Only the master subunit has access to DI 0. The standby subunit checks itself and the master every 10 ms for a ’stuck at 0’ or ’stuck at 1’ error.

If a ’stuck at 0’ or ’stuck at 1’ error triggers an edge on the DI, the interrupt OB is invoked as a result. An additional DI byte wired to DI 0 will allow the user to detect the ’wrong’ edge change.

The ’correct’ edge on a properly functioning DI always results in invocation of an interrupt OB. The system program thus ensures that no interrupts will be lost due to ’stuck at 0/1’ errors.

If a ’stuck at 0’ or ’stuck at 1’ error occurs in the master subunit, the system program initiates a standby-master transfer as soon as the discrepancy time has elapsed. The fault is reported, the defective DI 0 passivated, and the ’AGF’ bit (PLC fault) set in the H flag word (see Section 8.5). Thus the DI 0 in the other subunit is used to detect all process interrupts.

If a ’stuck at 0’ or ’stuck at 1’ error occurs in the standby subunit, the fault is reported, the defective DI 0 passivated and the ’AGF’ bit set in the H flag word as soon as the discrepancy time has elapsed.

Wiring DI 0

Wire DI 0 as a redundant DI without error locating. Even without error locating, ’stuck at 0’ and ’stuck at 1’ errors will be located (see above). Unused inputs must be connected to ground. The two redundant DI 0 should be plugged in the two central controllers.

If a QVZ (timeout) occurs in the master subunit, the system program carries out a standby-master transfer. The QVZ is reported, the defective DI 0 is reported as “2-way switched defective” and the DI 0 of the new master is used for the interrupt detection.

4.3.5 Redundant DQs without Error Locating Facility (LF)

Two-channel (1-out-of-2) DQs without error locating facility can only detect errors/faults, but cannot locate them, or only to a limited degree. The system treats this type of DQ as follows:

- Reading back of the digital output values, taking into consideration the configured readback delay time. This makes it possible to detect, but not locate, 'stuck at 1' errors.

'Stuck at 0' errors are detected only after the next edge change from 0 to 1:

- First, a "1" signal is output in one subunit (subunit A, for instance) while a "0" signal continues to be output in subunit B.
- After the configured readback delay has elapsed, the readback must show a "1" signal. If it does not, the error is located and reported.
- This DQ test is executed alternately in the other subunit on every edge change from 0 to 1.

Note:
When configuring with COM 155H, you must enter the DQ readback delay time, since the different digital output modules have different signal propagation times.

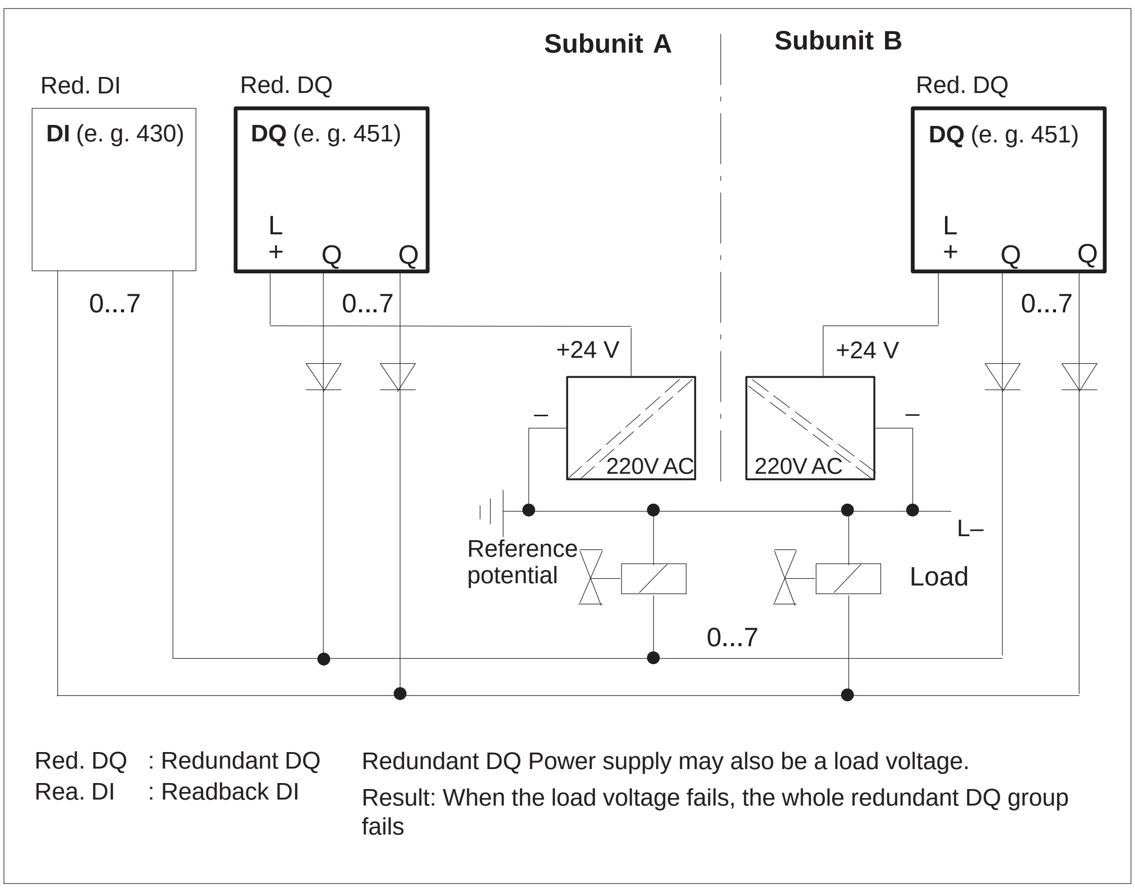


Figure 4-8 Two-Channel Redundant DQ without Error Locating

4.3.6 Redundant DQs with Error Locating Facility (DQ Type 10)

Two-channel DQs (1-out-of-2) for intermittent (frequently switched) outputs can both detect and locate faults/errors. In the event of a ’stuck at 1’ signal, a DQ of this type is passivated/isolated by the L-DQ in its controller (subunit), which outputs ”0” (shut down). In the case of a ’stuck at 0’ signal, the error is reported only. This means that this digital output can be operated as NON-STOP DQ (Figure 4-8).

The system program treats this type of DQ as follows:

- Reading back of the digital output values, taking into account the configured readback delay time. This makes it possible to detect ’stuck at 1’ errors and to localize them by shutting down the group power supply.

’Stuck at 0’ errors cannot be detected until the after the next edge change from 0 to 1:

- First, a ”1” signal is output in one of the subunits (subunit A, for instance) while subunit B continues to output a ”0” signal.
- The readback value must be ”1” as soon as the readback delay time has elapsed. Otherwise, the error is located and reported.
- This DQ test is executed alternately in the other subunit on each edge change from 0 to 1.

155H System Program Response

No further DQ tests are performed on the relevant DQ byte in the event of a ’stuck at 0’ error, nor is the L-DQ tested for ’stuck at 1’. In order to enhance the fault tolerance, the byte is not passivated, and can continue to be accessed.

In the case of ’stuck at 1’ errors, the bad DQ byte and the associated readback DI are passivated. The relevant DQ byte is no longer accessed. The group power supply is shut down via the L-DQ, which passivates all redundant DQs connected to this group supply (one-sided operation).

A ’stuck at 0’ error for an initial status of ”1” (during execution of the ”L-DQ for DQ test”) is detected a maximum of T_{test} times following the first possible readback of the ’stuck at 0’ error and the L-DQ test aborted.

T_{test} is a maximum of $3 * $ the basic clock rate for timed interrupts. In order to ensure that an error of this type affects the actuator for as brief a time as possible, the basic clock rate for timed interrupts in DX 0 should be set to $1 * 10$ ms.

When type 10 DQs are used, an error of this kind affects the actuator for a maximum period of T_{test}.

Testing the Error Locating Facility

The L-DIs and L-DQs of the two-channel 1-out-of-2 DIs are tested once per test cycle (approx. every 5 minutes) for ’stuck at 0’ and ’QVZ’ (timeout).

The L-DQs of the two-channel 1-out-of-2 DQs may and must be set to zero page by page only. ’Stuck at 1’ errors are detected every 10 hours by setting one L-DQ at a time to zero on a page-by-page basis.

Type 10 DQs with L-DQs are designed in such a way that a ’stuck at 0’ error detected during an L-DQ test affects the process for only a very brief span of time.

If a ’stuck at 0’ error is present (during an ”L-DQ for DQ test”) on a two-channel 1-out-of-2 DQ with an initial state of ”1”, it is detected no more than two basic timed interrupt clock pulses after the first possible readback of the ’stuck at 0’ error and the L-DQ test aborted. The L-DQ is then immediately set to ”1” so that the non-errored DQ will output ”1”. The ’stuck at 0’ error is reported.

Please also refer to the table entitled ”Detecting Errors on Digital Output Modules”.

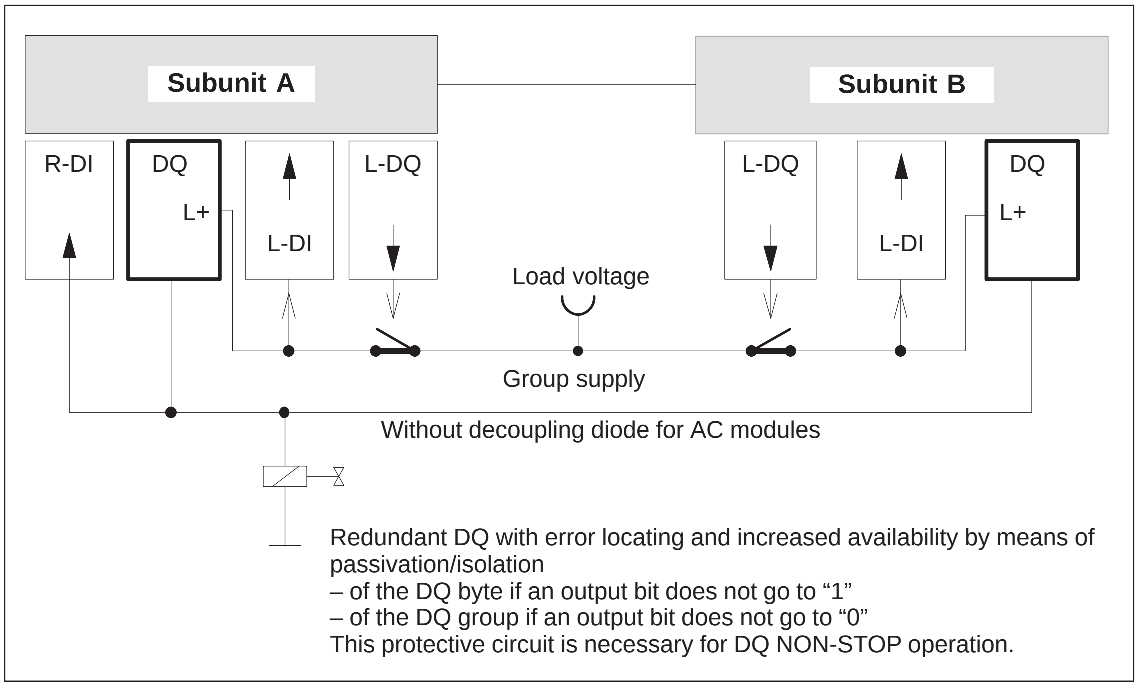
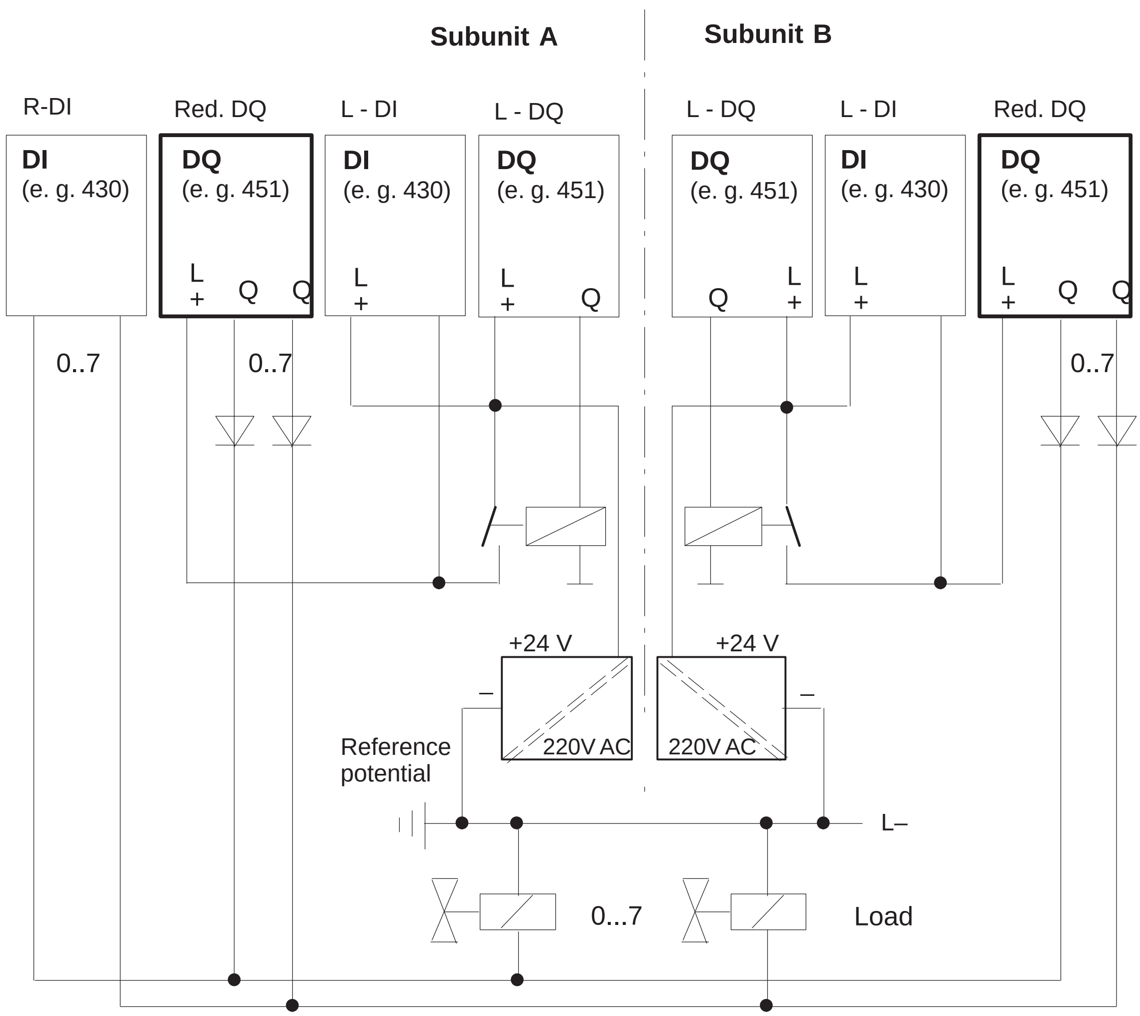


Figure 4-9 Block Diagram: 1-out-of-2 DQ with Error Locating



L-DQ : Locating DQ
L-DI : Locating DI
Red. DQ : Redundant DQ
R-DI : Readback DI

A load power supply may also be used.
Result: If the load supply fails, the entire redundant DQ group fails

Figure 4-10 Two-Channel Redundant DQs with Error Locating Facility (Type 10)

4.3.7 Redundant DQ with Error Locating Facility and 3 Readback DIs (DQ Type 11)

The two-channel (1-out-of-2) DQ for non-intermittent (infrequently switched) outputs detects and locates errors. The system program handles this type of DQ as follows:

- Readback of the digital output values, taking into account the configured readback delay time. This makes it possible to detect ’stuck at 1’ errors, and then to locate them by shutting down the group power supply.

’Stuck at 0’ errors are not detected until after the next edge change from 0 to 1:

- First, a ”1” signal is output in one subunit, (subunit A, for instance) while a ”0” signal continues to be output in the other subunit (subunit B in this case).
- The readback value must be ”1” once the configured readback delay time has elapsed. Otherwise, the error is located and reported.
- This DQ test is executed alternately in the other subunit on each edge change from 0 to 1.
- In addition, with the aid of the R-DIs in subunits A and B, the DQ is tested for ’stuck at 0’ errors every 10 hours and 5 minutes after each passivation. This makes it possible to detect a ’stuck at 0’ error in the DQ module even without an edge change.

I/O Type 11

A locating facility must be configured for type 11 (Figure 4-9). This circuit is required to allow NON-STOP operation of a non-intermittent DQ.

If a ’stuck at 0’ error is present (during execution of the ”L-DQ for DQ test”) on a DQ module with an initial state of ”1”, it is detected prior to execution of the L-DQ test and the L-DQ test is suppressed. The ’stuck at 0’ error is reported.

If, in the case of initial state ”1”, a ’stuck at 0’ error is present in or after the decoupling diode (during execution of the ”L-DQ for DQ test”), it is detected no more than T_{test} after the first possible readback of the ’stuck at 0’ error and the L-DQ test aborted.

T_{test} is a maximum of 3 $*$ the basic clock rate for timed interrupts. In order that an error of this kind affect the actuator as briefly as possible, the basic clock rate for timed interrupt should be set to 1 $*$ 10 ms in DX 0.

155H System Program Response

No further DQ tests are performed on the relevant DQ byte in the case of a ’stuck at 0’ error. To increase fault tolerance, the byte is not passivated and will continue to be accessed.

The bad DQ byte is passivated in the case of ’stuck at 1’ errors. The byte is no longer accessed. The group power supply is shut down via the L-DQ, thus passivating all redundant DQs connected to this group supply (one-sided operation).

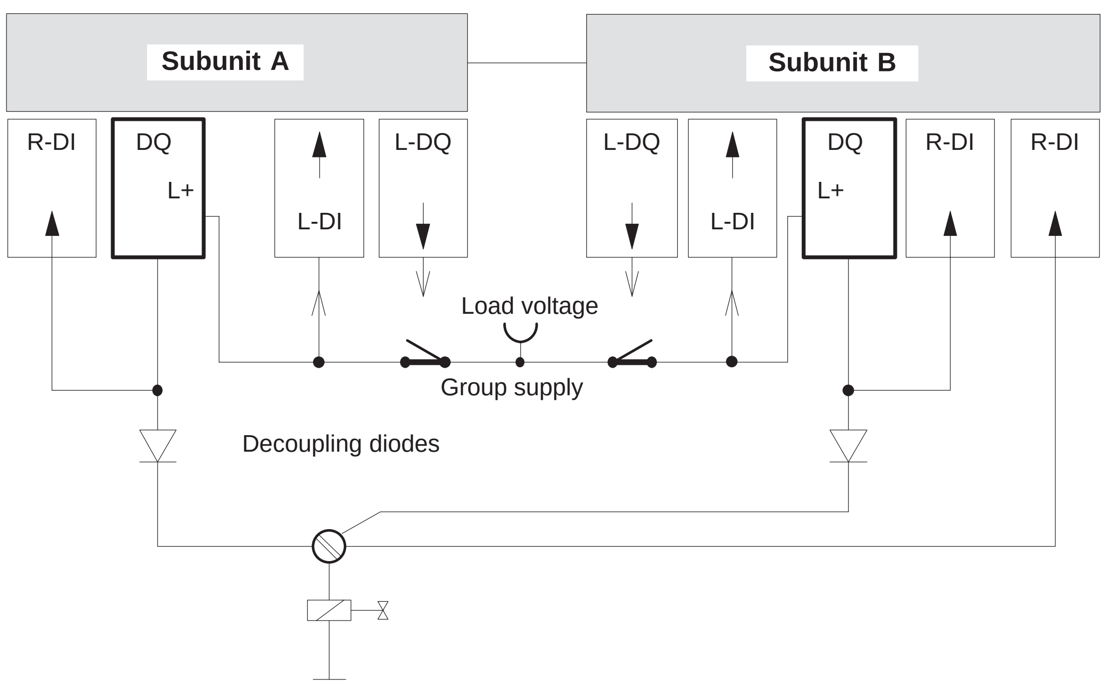
Testing the Error Locating Facility

The L-DIs and L-DQs of two-channel 1-out-of-2 DIs are tested once per test cycle (approx. every 5 minutes) for ’stuck at 0’ and ’QVZ’ (timeout).

The L-DQs of two-channel 1-out-of-2 DQs may and must be set to zero page by page only. ’Stuck at 1’ errors are detected every 10 hours by setting one L-DQ at a time to zero page by page.

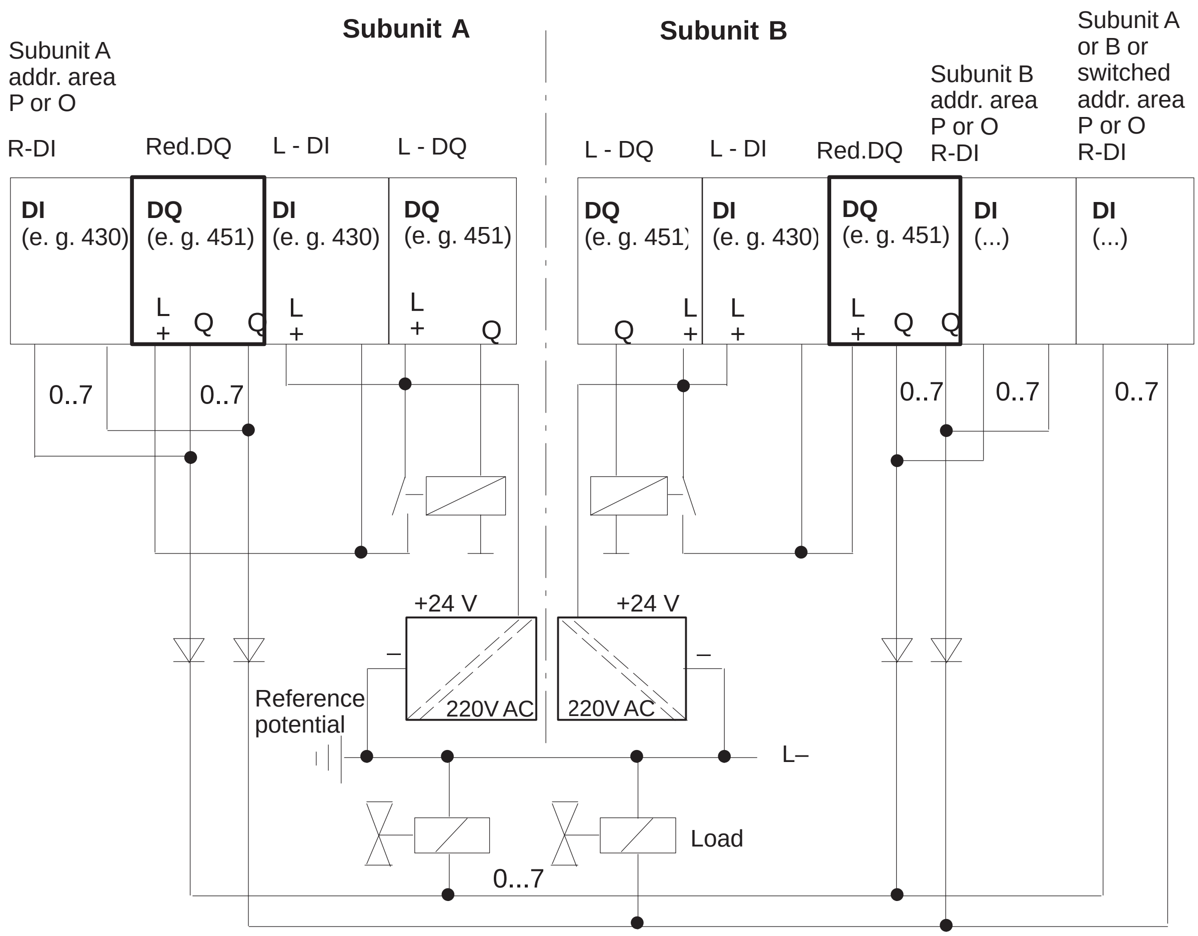
If, when the initial state is ”1”, a ’stuck at 0’ error is present **in the DQ module** (during the ”L-DQ for DQ” test), it is detected **prior to** execution of the L-DQ test and the test suppressed. The ’stuck at 0’ error is reported.

If, in the case of an initial state of ”1”, a ’stuck at 0’ error is present **in or after the decoupling diode** (during execution of the ”L-DQ for DQ test”), the error is detected no more than two timed interrupt basic clock pulses after the first possible readback of the ’stuck at 0’ error and the L-DQ test aborted. The L-DQ being tested is then immediately set to ”1” in order to reduce the duration of the effect on the process to a minimum. The ’stuck at 0’ error is reported. (Also refer to the table entitled ”Detecting Errors on Digital Output Modules”).



Redundant DQ with error locating and increased availability by means of passivation:
– of the DQ byte if an output bit does not go to “1”
– of the DQ group if an output bit does not go to “0”
This protective circuit is necessary for DQ NON-STOP-operation of a non-intermittent DQ.

Figure 4-11 Block Diagram: 1-out-of-2 DQ with Error Locating for Non-Intermittent Signals



L-DQ : Locating DQ
L-DI : Locating DI
Red. DQ : Redundant DQ
R-DI : Readback DI

A load voltage supply may also be used.
Result: If the load voltage fails, the entire redundant DQ group fails

Figure 4-12 Redundant Non-Intermittent DQ with Error Locating Facility (Type 11)

4.4 Redundant Analog Input/Outputs (AIs/AQs)

Direct I/O Access

The ”L PY” operation for redundant analog inputs is **not** permitted, and results in a Transfer error (TLAF). Redundant analog current inputs are provided only for 4-wire measuring transducers.

Direct I/O access to redundant analog inputs with the STEP 5 operation “L PW” supplies a standardized value as the result. Depending on the configuration (min./max.) this is the lower or higher **non-linearized value**.

4.4.1 Principle of the Redundant 1-out-of-2 Analog Inputs

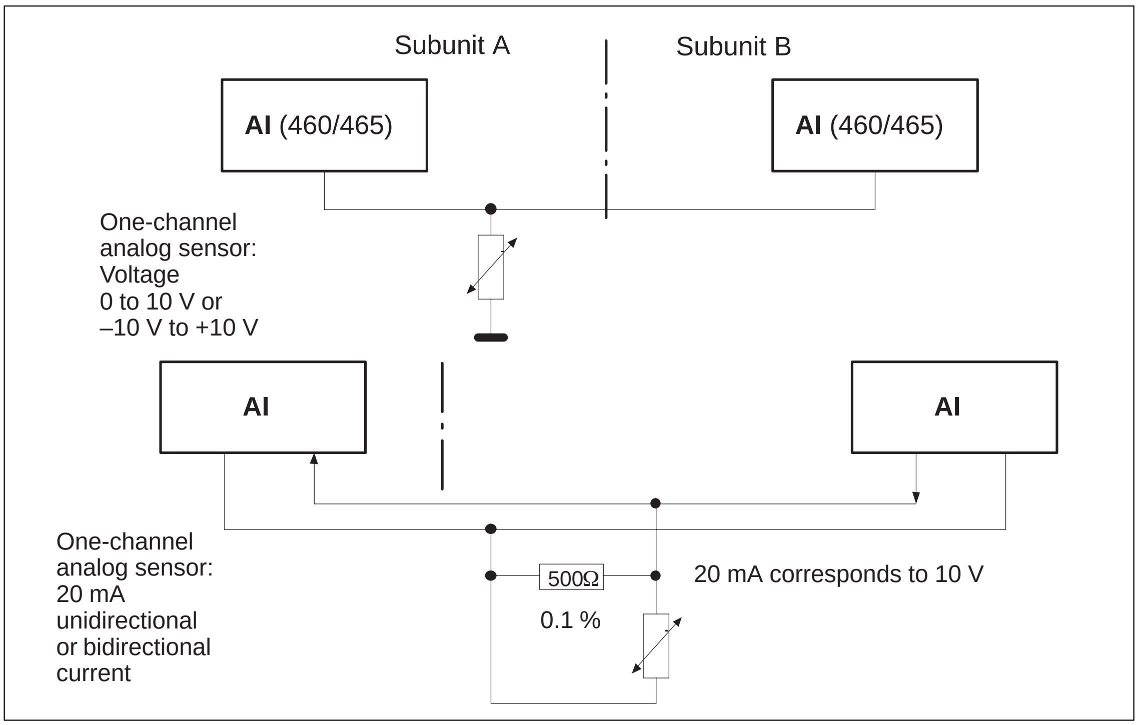


Figure 4-13 Redundant 1-out-of-2 AI, One-Channel with One or Two Sensors

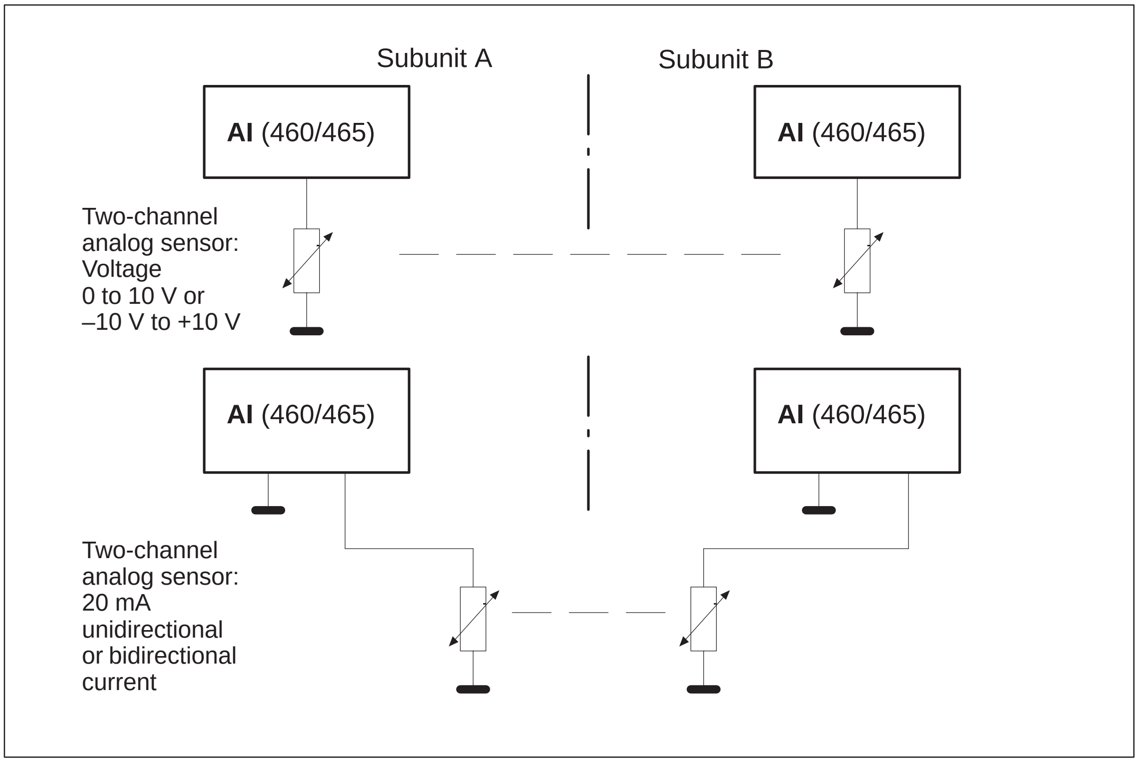


Figure 4-14 Redundant 1-out-of-2 AI, Two-Channel with One or Two Sensors

4.4.2 Redundant AI 463: FB 32

The two-channel (1-out-of-2) analog inputs (AI) detect errors, but do not always locate them.

Function block FB 32 ”2-AE:463” is provided expressly for the purpose of reading in analog values. It is part of the COM 155H package, and is on the diskette in program file S5CR70ST.S5D. All other required parameters, such as discrepancy value, discrepancy time and upper and lower limit values must be configured with COM 155H.

FB 32 can be used for AI module 463. It reads in the first two analog values and replaces the non-linearized values. Even if errors occur simultaneously, only one AI is passivated; one AI continues to work in the case of an error.

The input and output parameters for the function block are identical to those of FB 32: ”2:AE:463” for the S5-155U. In contrast, the test for range violations in modules which are configured in COM 155H as redundant takes into account the specified upper and lower range limits (refer to the table with configuration aids for COM 155H).

Note

An FB call to a non-existent and unconfigured module causes the addressing error ADF. If ADF is not acknowledged with OB 25, the standby CPU goes into STOP.

Execution Time for ”Function Blocks”

The execution times for the ”H” function block FB 33 are higher than those for standard function blocks by approx. 750 µs owing to the redundant function.

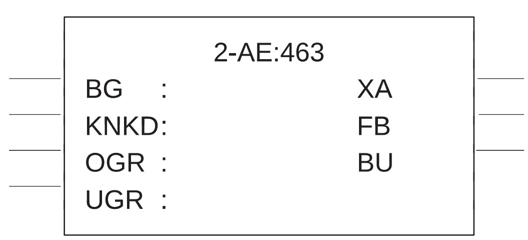
Calling the FB for 2-Channel Redundant AIs (FB 32)

Function block FB 32 reads analog value XE from two analog value inputs and, based on its nominal range, provides a proportional output value XA within the specifiable range limits UGR (lower limit) and OGR (upper limit). The analog value can be read in by the cyclic sampling method. The FB number may be changed during loading.

STEP 5 program

```
       : JU FB 32
NAME   : 2-AE:463
BG     :
KNKD   :
OGR    :
UGR    :
XA     :
FB     :
BU     :
```

Graphic representation FB 32



Description of input and output parameters

Name	Parameter Type	Data Type	Description	Remarks
BG	D	KY	I/O area and module address	In I/O area P: KY = 0.128 to 248 (4 channels) In I/O area O: KY = 1.0 to 248
KNKD	D	KY	Channel number and channel type	KY = x, y x = 0 to 3 channel number y = 20 to 21 channel type 20 unipolar (range 0 to + 1024) fixed-value representation 21 unipolar (range 256 to 1280) fixed-value representation
OGR	D	KG	Upper limit of the output value	– 1701411 + 39 to + 1701412 + 39
UGR	D	KG	Lower limit of the output value	– 1701412 + 39 to + 1701411 + 39
XA [1)]	Q	D	Output value as floating-point number	Nominal output value
FB	Q	BI	Error bit	0 = no error 1 = fewer than 192 units (for KD = 21) are read.
BU	Q	BI	Range violation	0 = no range violation 1 = range violation – if the bit ”Ü” has signal state ”1” (overflow) in the read analog value – if the nominal range is exceeded (dependent on the parameter KD)

[1)] If a data (double) word is used as the output value XA, the relevant data block must be opened before the FB 32 is called.

Note

Channel type 21 must only be selected if the measuring range 4–20 mA is set on the module in the limits 256 to 1280.

Parameter Type	Data Type	Permissible Actual Operands
I, Q	BI for an operand with bit address	I, Q, F
	D for an operand with doubleword address	ID, QD, FD, DD

Notes on Range Violation (BU) Bits

Range violation BU

In the case of modules which were configured as one-channel modules, a violation of the nominal analog value range is reported in BU. If the analog value is within the overflow range (analog value > +2047 units), the output value XA is limited to +2047 units. If the analog value lies below zero, the FB bit is set and XA displays the current value.

In the case of redundant modules, the upper and lower limit values configured with COM 155H are used to check for range violations. If these limit values are exceeded by the preferred value, the BU bit is set. When the overflow bit (BU) is set, the current value is also displayed at XA.

If the limit values configured in COM 155H lie outside the nominal range and if no discrepancy time violation occurred, the BU bit is set if the nominal range is exceeded (the preferred value is exceeded) and XA is limited to the nominal range limits.

Error Handling

If processing is performed correctly, the result of logic operation is set to ”0” on exiting the function block and accumulator 1 contains the value 0. The output XA contains the scaled value. The parameters FB and BU have the signal state ”0”.

If a value is specified in a parameter which does not lie within the defined value range, the function block reports this parameter assignment error with the RLO ”1” and with an error number in accumulator 1. The output XA is then assigned zero. The parameters FB and BU have the signal state ”0”.

Error number KF =
1: Parameter BG < 128 in P-I/O area
2: Parameter KN > 3
3: Sum of parameter BG and twice parameter KN > × 255, uneven BG addresses
4: Parameter KD not 20 or 21
5: Parameter OGR < = parameter UGR
6: 1. parameter BG > 1

If a module that does not exist or a channel that does not exist and is also not configured is selected, this causes an addressing error (ADF).

In one-sided operation, if the overflow bit BU is set, the nominal range limit value is output at output XA and the accumulator 1 contains the value 0.

Notes on Error Detection

Both analog values are checked for discrepancies. The permissible discrepancy value is calculated by adding a relative value (a percentage of the maximum value of the two analog values) to an absolute value (in units corresponding to the analog value's notation):

$$D_{perm.} = ABS + \frac{REL \times RAWV(max)}{100}$$

$D_{perm.}$:	Permissible analog value discrepancy
ABS:	Absolute component of the configured discrepancy
REL:	Relative component of the configured discrepancy
RAWV(max):	The higher of the two instantaneous analog values

Example

The following was configured with COM 155H:

ABS:	70
REL:	10%
Preferred value:	Max.

Actual analog value subunit A:	1000
Actual analog value subunit B:	980
Actual discrepancy:	D = 1000 – 980 = 20

Permissible discrepancy $D_{perm.} = 70 + \frac{10 \times 1000}{100} = 170$

It follows that the actual discrepancy lies within the permissible range. For additional calculations, the value 1000 will be used for XE.

When FB 32 is called, the analog values are read in from the two subunits, exchanged, and standardized. If a one-sided, locatable error (wirebreak or timeout) occurs, this AI is passivated; that is, it will no longer be accessed and the error is reported. The other AI continues to work in one-sided operation.

If the 155H system program detects a discrepancy error, it checks one of the subunits for an overflow or range-violated condition. If it finds one, this AI is passivated and the error reported. Otherwise, the standby controller's AI is passivated when the specified discrepancy time has elapsed.

Simultaneous occurence of an overflow or range violation on both AIs and a discrepancy leads to the standby being passivated.

Discrepancy is only recognized in the encoding range of the module to 2047 units. From this value onwards, the BU and FB bits are set. If larger analog signals are applied, the encoded value is no longer defined.

If the two modules report different errors, passivation is prioritized as follows:

1. Timeout (QVZ)
2. Wirebreak
3. Overflow
4. Range violation.

If FB 32: 2-AE:463 detected only a range violation or overflow condition but not a discrepancy, the standardized preferred value (min. or max.) is passed, together with the ”Range violation” (BU) or ”Overflow” (BU) bit.

Configuration Aids in COM 155H

Conversion if KD = 20:
100% ≙ 10V ≙ 1024 units, 0% ≙ 0V ≙ 0 units

Conversion if KD = 21:
100% ≙ 20mA ≙ 1280 units, 0% ≙ 4mA ≙ 256 units

	KD = 20			KD = 21	
Value [V]	**Upper/lower limit value**		**Value [mA]**	**Upper/lower limit value**	
1	102	10%	5.6	358	10%
2	205	20%	7.2	461	20%
3	308	30%	8.8	564	30%
4	410	40%	10.4	666	40%
5	512	50%	12	768	50%
6	614	60%	13.6	870	60%
7	717	70%	15.2	973	70%
8	820	80%	16.8	1076	80%
9	922	90%	18.4	1178	90%
10	1024	100%	20	1280	100%

4.4.3 Redundant AI 466: FB 33

The two-channel (1-out-of-2) analog inputs (AI) detect errors, but do not always locate them.

Function block FB 33 ”2-AE:466” is provided expressly for the purpose of reading in analog values. It is part of the COM 155H package, and is on the diskette in program file S5CR70ST.S5D. All other required parameters, such as discrepancy value, discrepancy time and upper and lower limit values must be configured with COM 155H.

FB 33 can be used for module 466. It reads in the first two analog values and replaces the non-linearized values. Even if errors occur simultaneously, only one AI is passivated; one AI continues to work in the case of an error.

The input and output parameters for the function block are identical to those of FB 33: ”2:AE:466” for the S5-155U. In contrast, the test for range violations in modules which are configured in COM 155H as redundant takes into account the specified upper and lower range limits (refer to the table with configuration aids for COM 155H).

Note

An FB call to a non-existent and unconfigured module causes the addressing error ADF. If ADF is not acknowledged with OB 25, the standby CPU goes into STOP.

Execution Time for ”Function Blocks”

The execution times for the ”H” function block FB 33 are higher than those for standard function blocks by approx. 750 µs owing to the redundant function.

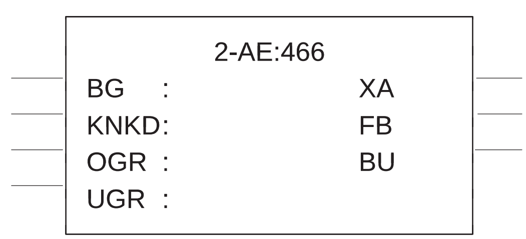
Calling the FB for 2-Channel Redundant AIs (FB 33)

Function block FB 33 reads analog value XE from two analog value inputs and, based on its nominal range, provides a proportional output value XA within the specifiable range limits UGR (lower limit) and OGR (upper limit). The analog value can be read in by the cyclic sampling method. The FB number may be changed during loading.

STEP 5 program

```
     :  JU FB 33
NAME :  2-AE:466
BG   :
KNKD :
OGR  :
UGR  :
XA   :
FB   :
BU   :
```

Graphic representation FB 33



Description of input and output parameters

Name	Parameter Type	Data Type	Description	Remarks
BG	D	KY	I/O area and module address	In I/O area P: KY = 0.128 to 248 (16 channels) In I/O area O: KY = 1.0 to 248
KNKD	D	KY	Channel number and channel type	KY = x, y x = 0 to 15 channel number y = 22 to 25 channel type 22 Fixed-point representation bipolar (nominal range -2048 to + 2048) 23 Number representation bipolar (nominal range -2048 to +2048) 24 Binary representation unipolar (nominal range -0 to +4095) 25 Fixed-point representation unipolar (nominal range +512 to +2559)
OGR	D	KG	Upper limit of the output value	– 1701411 + 39 to + 1701412 + 39
UGR	D	KG	Lower limit of the output value	– 1701412 + 39 to + 1701411 + 39
XA [1]	Q	D	Output value as floating-point number	Scaled output value
FB	Q	BI	Error bit	0 = no error 1 = fewer than 384 units are read where KD = 25
BU	Q	BI	Range violation	0 = no range violation 1 = range violation – if the bit ”Ü” has signal state ”1” (overflow) in the read analog value – if the nominal range is exceeded (dependent on the parameter KD)

1) If a data (double) word is used as the output value XA, the relevant data block must be opened before the FB 33 is called.

Parameter Type	Data Type	Permissible Actual Operands
I, Q	BI for an operand with bit address	I, Q, F
	D for an operand with doubleword address	ID, QD, FD, DD

Notes on Range Violation (BU) Bits

Range violation BU

In the case of modules which were configured as one-channel modules, a violation of the nominal analog value range is reported in BU as a range violation.

In the case of redundant modules, the upper and lower limit values configured with COM 155H are used to check for range violations. If these limit values are exceeded by the preferred value, the BU bit is set. When the overflow bit (BU) is set, the current value is also displayed at XA.

If the limit values configured in COM 155H lie outside the nominal range and if no discrepancy time violation occurred, the BU bit is set if the nominal range is exceeded (the preferred value is exceeded) and XA is limited to the nominal range limits.

Error Handling

If processing is performed correctly, the result of logic operation is set to ”0” on exiting the function block and accumulator 1 contains the value 0. The output XA contains the scaled value. The parameters FB and BU have the signal state ”0”.

If a value is specified in a parameter which does not lie within the defined value range, the function block reports this parameter assignment error with the RLO ”1” and with an error number in accumulator 1. The output XA is then assigned zero. The parameters FB and BU have the signal state ”0”.

Error no. KF =
1: Parameter BG $<$ 128 in P-I/O area
2: Parameter KN $>$ 15
3: Sum of parameter BG and twice parameter KN $> \times 255$, uneven BG addresses
4: Parameter KD not 22 or 25
5: Parameter OGR $<$ = parameter UGR
6: 1. parameter BG $>$ 1

If a module or a channel that does not exists is selected, this causes an addressing error (ADF).

When the error bit FB is set, the value zero is output at the output XA and the accumulator 1 contains the value 0.

In one-sided operation, if the overflow bit BU is set, the nominal range limit value is output at output XA and the accumulator 1 contains the value 0.

Notes on Error Detection

Both analog values are checked for discrepancies. The permissible discrepancy value is calculated by adding a relative value (a percentage of the maximum value of the two analog values) to an absolute value (in units corresponding to the analog value’s notation):

$$D_{perm.} = ABS + \frac{REL \text{ x } RAWV(max)}{100}$$

$D_{perm.}$:	Permissible analog value discrepancy
ABS:	Absolute component of the configured discrepancy
REL:	Relative component of the configured discrepancy
RAWV(max):	The higher of the two instantaneous analog values

Example

The following was configured with COM 155H:

ABS: 70

REL: 10%

Preferred value: Max.

Actual analog value subunit A: 1000

Actual analog value subunit B: 980

Actual discrepancy: D = 1000 – 980 = 20

Permissible discrepancy $D_{perm.} = 70 + \frac{10 \times 1000}{100} = 170$

It follows that the actual discrepancy lies within the permissible range. For additional calculations, the value 1000 will be used for XE.

When FB 33 is called, the analog values are read in from the two subunits, exchanged, and standardized. If a one-sided, locatable error (wirebreak or timeout) occurs, this AI is passivated; that is, it will no longer be accessed and the error is reported. The other AI continues to work in one-sided operation.

If the 155H system program detects a discrepancy error, it checks one of the subunits for an overflow or range-violated condition. If it finds one, this AI is passivated and the error reported. Otherwise, the standby controller's AI is passivated when the specified discrepancy time has elapsed.

Simultaneous occurence of an overflow or range violation on both AIs and a discrepancy leads to the standby being passivated.

Discrepancy is only recognized in the encoding range of the module to +4096 units. If larger analog signals are applied, the encoded value is no longer defined.

If the two modules report different errors, passivation is prioritized as follows:

1. Timeout (QVZ)
2. Wirebreak
3. Range violation.

If FB 33: 2-AE:466 detected only a range violation or overflow condition but not a discrepancy, the standardized preferred value (min. or max.) is passed, together with the ”Range violation” (BU) or ”Overflow” (BU) bit.

Configuration Aids in COM 155H

Conversion if KD = 22:
100% ≙ 10V ≙ 2048 units,   0% ≙ 0V ≙ 0 units

Conversion if KD = 23:
100% ≙ 10V ≙ 2048 units,   0% ≙ 0V ≙ 0 units

Conversion if KD = 24:
100% ≙ 5V ≙ 2048 units,   0% ≙ 0V ≙ 0 units

Conversion if KD = 25:
100% ≙ 5V ≙ 2560 units,   0% ≙ 1V ≙ 512 units
100% ≙ 20mA ≙ 2560 units,   0% ≙ 4mA ≙ 512 units

	KD = 24			KD = 25	
Value [V]	**Upper/lower limit value**		**Value [mA]**	**Upper/lower limit value**	
1	410	20%	5.6	716	10%
2	820	40%	7.2	921	20%
3	1229	60%	8.8	1126	30%
4	1638	80%	10.4	1331	40%
5	2048	100%	12	1536	50%
6	2458	120%	13.6	1740	60%
7	2867	140%	15.2	1945	70%
8	3277	160%	16.8	2150	80%
9	3686	180%	18.4	2355	90%
10	4096	200%	20	2560	100%

	KD = 22,23			KD = 25	
Value [V]	**Upper/lower limit value**		**Value [V]**	**Upper/lower limit value**	
1	205	10%	1.4	716	10%
2	410	20%	1.8	921	20%
3	614	30%	2.2	1126	30%
4	820	40%	2.6	1331	40%
5	1024	50%	3.0	1536	50%
6	1229	60%	3.4	1740	60%
7	1434	70%	3.8	1945	70%
8	1638	80%	4.2	2150	80%
9	1843	90%	4.6	2355	90%
10	2048	100%	5.0	2560	100%

4.4.4 Redundant AIs: FB 40

The two-channel (1-out-of-2) analog inputs detect errors, but do not always locate them.

Function block FB 40 ”H-RLG:AE” is provided expressly for the purpose of reading in analog values. It is part of the COM 155H package, and is on the diskette in program file S5CR70ST.S5D. All other required parameters, such as discrepancy value and discrepancy time, must be configured with COM 155H.

FB 40 can be used for modules 460 and 465. It reads in the first two analog values and replaces the non-linearized values. If a module reports a wirebreak, overflow or range violation, that module is passivated and the error reported. From that point on, operation is one-sided, using only the other module. The simultaneous occurrence of an overflow and a range violation does not result in passivation.

The input and output parameters for the function block are identical to those of FB 40 ”RLG:AE” for the S5-155U. In contrast, the test for range violations in modules which are configured as redundant takes into account the specified upper and lower range limits.

Execution Time for ”Function Blocks”

Depending on the operations used, the execution times for ”H” function blocks may be higher than those for standard function blocks:

FB 40 H-RLG:AE, for two-channel redundant AIs, by approx.: 750 µs

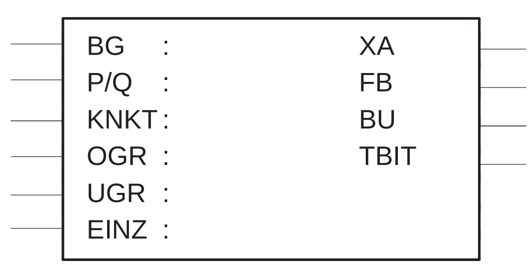
Calling the FB for 2-Channel Redundant AIs (FB 40)

Function block FB 40 reads analog value XE from two analog value inputs and, based on its nominal range, provides a proportional output value XA within the specifiable range limits UGR (lower limit) and OGR (upper limit). The analog value can be read in either by the cyclic or selective sampling method. The FB number must not be changed during loading.

STEP 5 program

```
       : JU FB 40
NAME   : H-RLG:AE
AE     :
BG     :
P/Q    :
KNKT   :
OGR    :
UGR    :
EINZ   :
XA     :
FB     :
BU     :
TBIT   :
```

Graphic representation FB 40



Description of input and output parameters

Name	Param–eter Type	Data Type	Description	Remarks
BG	D	KF	Module address	P/Q = P: BG = 128 to 240 P/Q = Q: BG = 0 to 240
P/Q	D	KS	I/O area	P/Q = P: P area P/Q= Q: O area
KNKT	D	KY	Channel number KN Channel type KT	KN = 0 to 15 KT = 3 to 6 (see Notes)
OGR	D	KG	Upper limit of the output value	–1701412+39 to +1701412+39
UGR	D	KG	Lower limit of the output value	–1701412+39 to +1701412+39
EINZ	I	BI	Selective sampling	EINZ = 0: Cyclic sampling
XA	Q	D	Address for output value XA	Scaled value between UGR and OGR (see Note)
FB	Q	BI	Bit address for ”Wirebreak” bit	0 = No wirebreak 1 = Wirebreak
BU	Q	BI	Bit address for ”Range violation” bit	0 = No range violation 1 = Range violated
TBIT	Q	BI	Bit address for ”Analog input” bit	Always 0

Parameter Type	Data Type	Permissible Actual Operands
I, Q	BI for an operand with bit address	I, Q, F
	D for an operand with doubleword address	ID, QD, FD, DD

Notes on Channel Type KT

The permissible analog input modules can provide the analog value in four different notations. You must choose the one you want by setting the KT parameter accordingly.

KT = 3 : Absolute value between 4 and 20 mA
KT = 4 : Unipolar representation
KT = 5 : Bipolar absolute value
KT = 6 : Bipolar fixed-point number

If the KT parameter is set to a value less than 3, the function block uses KT = 4; if it is set to a value exceeding 6, the function block uses KT = 6. The KT parameter must be in agreement with the method of representation set on the module itself.

Notes on Output Value XA

The input value (XE) read in from the analog input module is converted according to the formulas below depending on channel type parameter KT.

OGR	:	Upper limit value	UGR	:	Lower limit value
XE	:	Input value	XA	:	Output value

KT = 3 $XA = \frac{UGR \times (2560-XE) + OGR \times (XE-512)}{2048}$

KT = 4 $XA = \frac{UGR \times (2048-XE) + OGR \times XE}{2048}$

KT = 5/6 $XA = \frac{UGR \times (2048-XE) + OGR \times (XE+2048)}{4096}$

Notes on UGR/OGR:

Range limits for the output value

The analog value can be represented as a physical value if suitable range limits are selected.

Example:

Analog Value Range	Phys. Value	Range Limits	Resolution
0 to 10 V	2 to 150 °C	2000000+01 1500000+03	0.1 °C

Notes on Range Violation (BU) Bits

Range violation BU

In the case of modules which were configured as one-channel modules, a violation of the nominal analog value range is reported in BU. If the analog value is within the overflow range (analog value > +4096 or < –4096 units), it is limited to +4096 or –4096.

In the case of redundant modules, the upper and lower limit values configured with COM 155H are used to check for range violations. If the analog value lies within the overflow range (analog value > +4096 or < –4096), the ”Wirebreak” and ”Range violation” bits are set, and the analog value limited to + or – 4096 units.

In the case of channel type 3 (4 to 20 mA), the BU bit is also set for values from 3 to 4 mA.

Wirebreak

In the event of a wirebreak, XA is set to 0.

Addressing Error

If FB 40 is called for a channel that is not configured and not plugged, the standby CPU goes into STOP and the ADF LED on the master CPU lights up (OB 25 is not called).
The program that caused the error is displayed in the B stack in the standby CPU.

Notes on Error Detection

Both analog values are checked for discrepancies. The permissible discrepancy value is calculated by adding a relative value (a percentage of the maximum value of the two analog values) to an absolute value (in units corresponding to the analog value's notation):

$$D_{perm.} = ABS + \frac{REL \times RAWV(max)}{100}$$

$D_{perm.}$:	Permissible analog value discrepancy
ABS:	Absolute component of the configured discrepancy
REL:	Relative component of the configured discrepancy
RAWV(max):	The higher of the two instantaneous analog values

Example

The following was configured with COM 155H:

ABS:	100
REL:	10%
Preferred value:	Max.
Actual analog value subunit A:	1000
Actual analog value subunit B:	980
Actual discrepancy:	D = 1000 – 980 = 20

Permissible discrepancy $D_{perm.} = 100 + \frac{10 \times 1000}{100} = 200$

It follows that the actual discrepancy lies within the permissible range. For additional calculations, the value 1000 will be used for XE.

When FB 40 is called, the analog values are read in from the two subunits, exchanged, and standardized. If a one-sided, locatable error (timeout, wirebreak) occurs, the module is passivated; that is, it will no longer be accessed (one-sided operation).

If the 155H system program detects a discrepancy error, it checks one of the subunits for an overflow or range-violated condition. If it finds one, the module is passivated. Otherwise, the standby controller's module is passivated when the specified discrepancy time has elapsed.

If the two modules report different errors, passivation is prioritized as follows:

1. Timeout (QVZ)
2. Wirebreak
3. Overflow
4. Range violation.

If FB 40:H-RLG AE detected only a range violation or overflow condition but not a discrepancy, the configured standardized analog value is passed, together with the ”Range violation” (BU) or ”Overflow” (BU) bit. If FB 40:H-RLG AE detects a wirebreak in both modules, it sets the ”Wirebreak” bit (FB).

Direct I/O access to redundant analog inputs via STEP 5’s ”L PW” operation returns a standardized value as the result. Depending on what was specified during configuring (min/max), this value is either the lower or higher **non-linearized value**.

The ”L PY” operation may **not** be used on redundant analog inputs, and results in a Transfer error (TLAF).

4.4.5 Principle of the Redundant 1-out-of-3 AIs

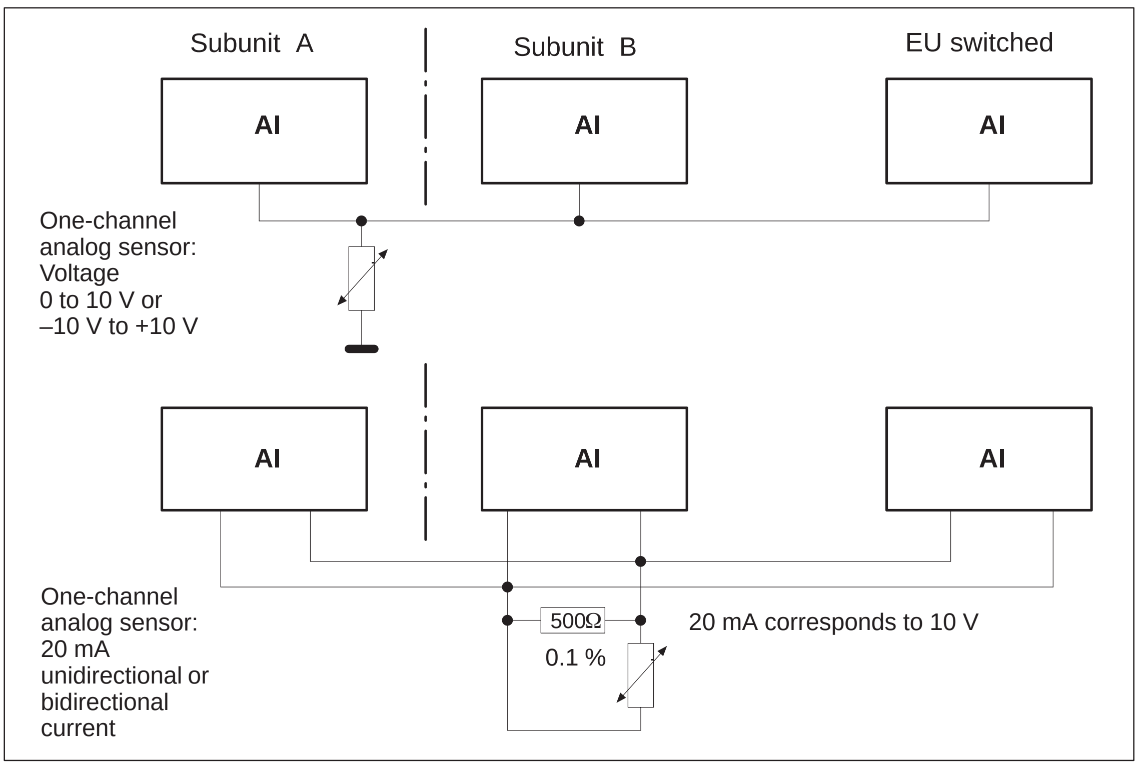


Figure 4-15 Redundant 1-out-of-3-AI, One-Channel with One Sensor

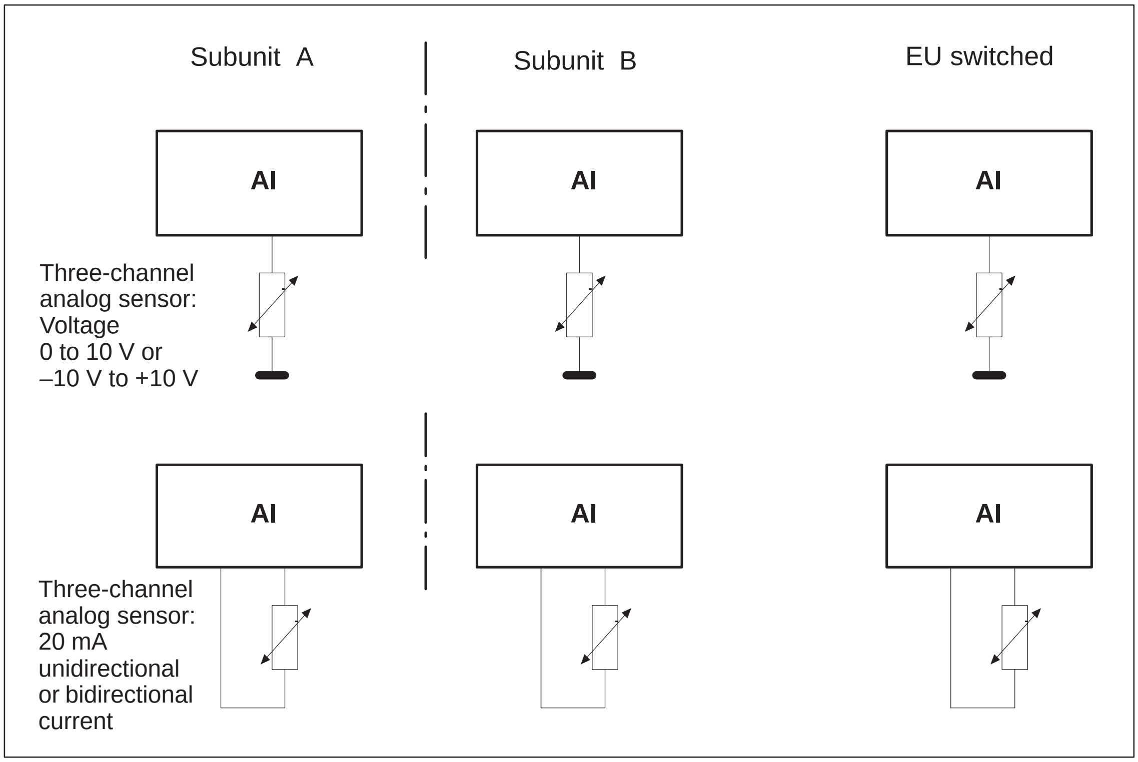


Figure 4-16 Redundant 1-out-of-3-AI, Three-Channel with Three Sensors

4.4.6 Redundant AI 463: FB 35

The three-channel (2-out-of-3 / 1-out-of-3) analog inputs (AI) always detect and locate errors.

Standard function block FB 35 ”3-AE:463” is provided expressly for the purpose of reading in three-channel analog values. It is part of the COM 155H package, and is on the diskette in program file S5CR70ST.S5D. All other required parameters, such as discrepancy value, discrepancy time, upper and lower limit value and address of the third channel must be configured with COM 155H.

FB 35 can be used for module 463. It reads in the first three analog values and replaces the non-linearized values. The value which lies in the middle of the three read values serves as the output value XA. The display value is also taken as the reference value for calculating discrepancy values. If errors occur simultaneously, only two AIs are passivated; one AI continues to work in the case of an error.

The input and output parameters for the function block are identical to those of FB 32: ”AE:463” for the S5-155U. In contrast, the test for range violations in modules which are configured in COM 155H as redundant takes into account the specified upper and lower range limits (refer to the table with configuration aids for COM 155H).

Note

An FB call to a non-existent and unconfigured module causes the addressing error ADF. If ADF is not acknowledged with OB 25, the standby CPU goes into STOP.

Execution Time for ”Function Blocks”

The execution times for the ”H” function block FB 35 are higher than those for standard function blocks by approx. 800 μs owing to the redundant function.

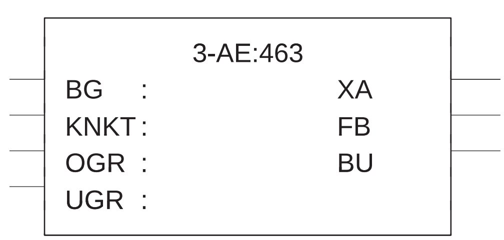
Calling the FB for 3-Channel Redundant AIs

Function block FB 35 reads three analog value XE from three analog value inputs and, based on its nominal range, provides a proportional output value XA within the specifiable range limits UGR (lower limit) and OGR (upper limit). The analog value can be read in by the cyclic sampling method. The FB number may be changed during loading.

STEP 5 program

```
        : JU FB 35
NAME    : 3-AE:463
BG      :
KNKT    :
OGR     :
UGR     :
XA      :
FB      :
BU      :
```

Graphic representation FB 35



Description of input and output parameters

Name	Param eter Type	Data Type	Description	Remarks
BG	D	KY	I/O area and module address	In I/O area P: KY = 0.128 to 248 (4 channels) In I/O area O: KY = 1.0 to 248
KNKD	D	KY	Channel number and channel type	KY = x, y x = 0 to 3 channel number y = 20 to 21 channel type 20 Fixed-point representation unipolar (nominal range 0 to + 1024) 21 Fixed-point representation unipolar (nominal range 256 to 1280)
OGR	D	KG	Upper limit of the output value	– 1701411 + 39 to + 1701412 + 39
UGR	D	KG	Lower limit of the output value	– 1701412 + 39 to + 1701411 + 39
XA [1)]	Q	D	Output value as floating-point number	Scaled output value
FB	Q	BI	Error bit	0 = no error 1 = fewer than 192 units (for KD = 21) are read
BU	Q	BI	Range violation	0 = no range violation 1 = range violation – if the bit ”Ü” has signal state ”1” (overflow) in the read analog value – if the nominal range is exceeded (dependent on the parameter KD)

1) If a data (double) word is used as the output value, the relevant data block must be opened before the FB 35 is called.

Note

Channel type 21 must only be selected if the measuring range 4–20 mA is set on the module in the limits 256 to 1280.

Parameter Type	Data Type	Permissible Actual Operands
I, Q	BI for an operand with bit address	I, Q, F
	D for an operand with doubleword address	ID, QD, FD, DD

Notes on Range Violation (BU) Bits

Range violation BU

As long as no discrepancy value violation occurred, the BU bit is set when the nominal range of the ‘middle value’ (not the mean value) is exceeded. In the case of three-way redundant modules, the upper and lower limit values configured with COM 155H are used to check for range violations. If these limit values are exceeded, the BU bit is set. When the overflow bit (BU) is set, the current value is also displayed at XA.

Wirebreak

In the event of a wirebreak of all three channels, XA is set to 0 and the FB bit is set. Only two channels are passivated and the error is reported. The third channel continues to work even with a wirebreak, an error report is made to register the error.

Error Handling

If processing is performed correctly, the result of logic operation is set to ”0” on exiting the function block and accumulator 1 contains the value 0. The output XA contains the scaled value. The parameters FB and BU have the signal state ”0”.

If a value is specified in a parameter which does not lie within the defined value range, the function block reports this parameter assignment error with the RLO ”1” and with an error number in accumulator 1. The output XA is then assigned zero. The parameters FB and BU have the signal state ”0”.

Error no. KF =
1: Parameter BG < 128 in P-I/O area
2: Parameter KN > 3
3: Sum of parameter BG and twice parameter KN >255 uneven BG addresses
4: Parameter KD not 20 or 21
5: Parameter OGR < = parameter UGR
6: 1. parameter BG > 1

If a module that does not exist or a channel that does not exist and is also not configured is selected, this causes an addressing error (ADF).

When the error bit FB is set, the value zero is output at the output XA. The accumulator 1 contains the value 0. This only applies if KD = 21 and two channels are already passivated and a wirebreak occurs at the third channel.

If the overflow bit BU is set, the nominal range limit value is output at output XA. The RLO is set to signal state ”1”; the accumulator 1 contains the value read from the module.

Notes on Error Detection

The three analog values are checked for discrepancies. The permissible discrepancy value is calculated by adding a relative value (a percentage of the maximum value of the two analog values) to an absolute value (in units corresponding to the analog value's notation):

$$D_{perm.} = ABS + \frac{REL \times RAWV(max)}{100}$$

$D_{perm.}$:	Permissible analog value discrepancy
ABS:	Absolute component of the configured discrepancy
REL:	Relative component of the configured discrepancy
RAWV:	The middle of the three instantaneous analog values

Example

The following was configured with COM 155H:

ABS: 70

REL: 10%

Actual analog value subunit A:	1000
Actual analog value subunit B:	980
Actual analog value 3rd channel:	1040
Actual discrepancy:	D1 = 1000 – 980 = 20
	D2 = 1040 – 1000 = 40

Permissible discrepancy $D_{perm.} = 70 + \frac{10 \times 1000}{100} = 170$

It follows that the actual discrepancy lies within the permissible range. For additional calculations, the value 1000 will be used for XE.

When FB 35 is called, the analog values are read in from the two subunits, exchanged, and the middle of the three analog values is used. If a one-sided, locatable error (timeout, wirebreak) occurs, the module is passivated; that is, it will no longer be accessed (1-out-of-2 operation).

If the 155H system program detects a discrepancy error, it passivates the module whose analog value shows the largest discrepancy from the other two (2-out-of-3) when the specified discrepancy time has elapsed. If two channels continue to work and a discrepancy is found, a check is made to establish whether a range violation or an overflow occurred in a channel. If so, this AI is passivated and an error is reported. Otherwise, the standby controller's channel is passivated when the configured discrepancy time has elapsed.

Discrepancy is only recognized in the encoding range of the module to 1024 units. From this value onwards, the BU bit is set. If larger analog signals are applied, the encoded value is no longer defined.

If several modules report different errors, passivation is prioritized as follows:

1. Timeout (QVZ)
2. Wirebreak
3. Overflow
4. Range violation.

If FB 35: ”3-AE:463” detected only a range violation or overflow condition but not a discrepancy at two channels, the ”Range violation” (BU) or ”Overflow” (BU) bit is set.

Configuration Aids in COM 155H

Conversion if KD = 20:
100% ≙ 10V ≙ 1024 units, 0% ≙ 0V ≙ 0 units

Conversion if KD = 21:
100% ≙ 20mA ≙ 1280 units, 0% ≙ 4mA ≙ 256 units

	KD = 20			**KD = 21**	
Value [V]	**Upper/lower limit value**		**Value [mA]**	**Upper/lower limit value**	
1	102	10%	5.6	358	10%
2	205	20%	7.2	461	20%
3	308	30%	8.8	564	30%
4	410	40%	10.4	666	40%
5	512	50%	12	768	50%
6	614	60%	13.6	870	60%
7	717	70%	15.2	973	70%
8	820	80%	16.8	1076	80%
9	922	90%	18.4	1178	90%
10	1024	100%	20	1280	100%

4.4.7 Redundant 3-Channel AI 466: FB 36

The three-channel (2-out-of-3 / 1-out-of-3) analog inputs always detect and locate errors.

Standard function block FB 36 ”3-AE:466” is provided expressly for the purpose of reading in three-channel analog values. It is part of the COM 155H package, and is on the diskette in program file S5CR70ST.S5D. All other required parameters, such as discrepancy value, discrepancy time, upper and lower limit value and address of the third channel must be configured with COM 155H.

FB 36 can be used for module 466. It reads in the first three analog values and replaces the non-linearized values. The value which lies in the middle of the three read values serves as the output value XA. The display value is also taken as the reference value for calculating discrepancy values. If errors occur simultaneously, only two AIs are passivated; one AI continues to work in the case of an error.

The input and output parameters for the function block are identical to those of FB 33: ”AE:466” for the S5-155U. In contrast, the test for range violations in modules which are configured in COM 155H as redundant takes into account the specified upper and lower range limits (refer to the table with configuration aids for COM 155H).

Note

An FB call to a non-existent and unconfigured module causes the addressing error ADF. If ADF is not acknowledged with OB 25, the standby CPU goes into STOP.

Execution Time for ”Function Blocks”

The execution times for the ”H” function block FB 36 are higher than those for standard function blocks by approx. 800 μs owing to the redundant function.

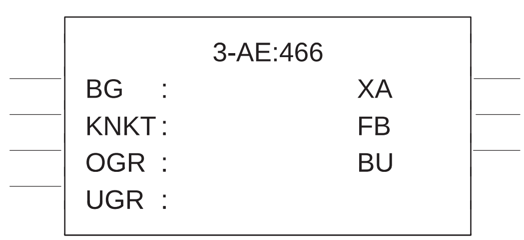
Calling the FB for 3-Channel Redundant AIs

Function block FB 36 reads three analog value XE from three analog value inputs and, based on its nominal range, provides a proportional output value XA within the specifiable range limits UGR (lower limit) and OGR (upper limit). The analog value can be read in by the cyclic sampling method. The FB number may be changed during loading.

STEP 5 program

```
        : JU FB 36
NAME    : 3-AE:466
BG      :
KNKT    :
OGR     :
UGR     :
XA      :
FB      :
BU      :
```

Graphic representation FB 36



Description of input and output parameters

Name	Parameter Type	Data Type	Description	Remarks
BG	D	KY	I/O area and module address	In I/O area P: KY = 0.128 to 248 (16 channels) In I/O area O: KY = 1.0 to 248
KNKD	D	KY	Channel number and channel type	KY = x, y x = 0 to 15 channel number y = 22 to 25 channel type 22 Fixed-point representation bipolar (nominal range -2048 to + 2048) 23 Number representation bipolar (nominal range -2048 to +2048) 24 Binary representation unipolar (nominal range 0 to +4095) 25 Fixed-point representation unipolar (nominal range +512 to + 2559)
OGR	D	KG	Upper limit of the output value	– 1701411 + 39 to + 1701412 + 39
UGR	D	KG	Lower limit of the output value	– 1701412 + 39 to + 1701411 + 39
XA 1)	Q	D	Output value as floating-point number	Scaled output value
FB	Q	BI	Error bit	0 = no error 1 = fewer than 384 units (for KD = 25) are read
BU	Q	BI	Range violation	0 = no range violation 1 = range violation – if the bit ”Ü” has signal state ”1” (overflow) in the read analog value – if the nominal range is exceeded (dependent on the parameter KD)

1) If a data (double) word is used as the output value, the relevant data block must be opened before the FB 36 is called.

Parameter Type	Data Type	Permissible Actual Operands
I, Q	BI for an operand with bit address	I, Q, F
	D for an operand with doubleword address	ID, QD, FD, DD

Notes on Range Violation (BU) Bits

Range violation BU

As long as no discrepancy value violation occurred, the BU bit is set when the ‘middle value’ (not the mean value) is exceeded. In the case of three-way redundant modules, the upper and lower limit values configured with COM 155H are used to check for range violations. If these limit values are exceeded, the BU bit is set. When the overflow bit (BU) is set, the current value is also displayed at XA.

Wirebreak

In the event of a wirebreak of all three channels, XA is set to 0 and the FB bit is set. Only two channels are passivated and the error is reported. The third channel continues to work even with a wirebreak, an error report is made to register the error.

Error Handling

If processing is performed correctly, the result of logic operation is set to ”0” on exiting the function block and accumulator 1 contains the value 0. The output XA contains the scaled value. The parameters FB and BU have the signal state ”0”.

If a value is specified in a parameter which does not lie within the defined value range, the function block reports this parameter assignment error with the RLO ”1” and with an error number in accumulator 1. The output XA is then assigned zero. The parameters FB and BU have the signal state ”0”.

Error no. KF =
1: Parameter BG $<$ 128 in P-I/O area
2: Parameter KN $>$ 15
3: Sum of parameter BG
and twice parameter KN $>$255
uneven BG addresses
4: Parameter KD not 20 or 21
5: Parameter OGR $<$ = parameter UGR
6: 1. parameter BG $>$ 1

If a module that does not exist or a channel that does not exist and is also not configured is selected, this causes an addressing error (ADF).

When the error bit FB is set, the value zero is output at the output XA. The accumulator 1 contains the value 0. This only applies if KD = 25 and two channels are already passivated and a wirebreak occurs at the third channel.

Notes on Error Detection

The three analog values are checked for discrepancies. The permissible discrepancy value is calculated by adding a relative value (a percentage of the maximum value of the two analog values) to an absolute value (in units corresponding to the analog value’s notation):

$$D_{perm.} = ABS + \frac{REL \times RAWV(max)}{100}$$

$D_{perm.}$:	Permissible analog value discrepancy
ABS:	Absolute component of the configured discrepancy
REL:	Relative component of the configured discrepancy
RAWV:	The middle of the three instantaneous analog values

Example

The following was configured with COM 155H:

ABS: 70

REL: 10%

Actual analog value subunit A:	1000
Actual analog value subunit B:	980
Actual analog value 3rd channel:	1040
Actual discrepancy:	D1 = 1000 – 980 = 20
	D2 = 1040 – 1000 = 40

Permissible discrepancy $D_{perm.} = 70 + \frac{10 \times 1000}{100} = 170$

It follows that the actual discrepancy lies within the permissible range. For additional calculations, the value 1000 will be used for XE.

When FB 36 is called, the analog values are read in from the two subunits, exchanged, and the mean of the three analog values is used. If a one-sided, locatable error (timeout, wirebreak) occurs, the channel is passivated; that is, it will no longer be accessed (1-out-of-2 operation).

If the 155H system program detects a discrepancy error, it passivates the module whose analog value shows the largest discrepancy from the other two (2-out-of-3) when the specified discrepancy time has elapsed. If two channels continue to work and a discrepancy is found, a check is made to establish whether a range violation or an overflow occurred in a channel. If so, this AI is passivated and an error is reported. Otherwise, the standby controller's channel is passivated when the configured discrepancy time has elapsed.

Discrepancy is only recognized in the encoding range of the module to 4096 units (if KD = 24). If larger analog signals are applied, the encoded value is no longer defined.

If several modules report different errors, passivation is prioritized as follows:

1. Timeout (QVZ)
2. Wirebreak
3. Range violation.

If, for all three AI modules, FB 36: ”3-AE:466” detected only a range violation but not a discrepancy, the standardized analog value is passed, together with the ”Range violation” (BU) bit or the ”Overflow” (BU) bit.

Configuration Aids in COM 155H

Conversion if KD = 22:
100% ≙ 10V ≙ 2048 units, 0% ≙ 0V ≙ 0 units

Conversion if KD = 23:
100% ≙ 10V ≙ 2048 units, 0% ≙ 0V ≙ 0 units

Conversion if KD = 24:
100% ≙ 5V ≙ 2048 units, 0% ≙ 0V ≙ 0 units

Conversion if KD = 25:
100% ≙ 5V ≙ 2560 units, 0% ≙ 1V ≙ 512 units
100% ≙ 20mA ≙ 2560 units, 0% ≙ 4mA ≙ 512 units

	KD = 24			KD = 25	
Value [V]	**Upper/lower limit value**		**Value [mA]**	**Upper/lower limit value**	
1	410	20%	5.6	716	10%
2	820	40%	7.2	921	20%
3	1229	60%	8.8	1126	30%
4	1638	80%	10.4	1331	40%
5	2048	100%	12	1536	50%
6	2458	120%	13.6	1740	60%
7	2867	140%	15.2	1945	70%
8	3277	160%	16.8	2150	80%
9	3686	180%	18.4	2355	90%
10	4096	200%	20	2560	100%

	KD = 22,23			KD = 25	
Value [V]	**Upper/lower limit value**		**Value [V]**	**Upper/lower limit value**	
1	205	10%	1.4	716	10%
2	410	20%	1.8	921	20%
3	614	30%	2.2	1126	30%
4	820	40%	2.6	1331	40%
5	1024	50%	3.0	1536	50%
6	1229	60%	3.4	1740	60%
7	1434	70%	3.8	1945	70%
8	1638	80%	4.2	2150	80%
9	1843	90%	4.6	2355	90%
10	2048	100%	5.0	2560	100%

4.4.8 Three-Channel Redundant AIs: FB 43

Three-channel (3-out-of-1) AIs always detect and locate errors.

Standard function block FB 43 ”3-RLG:AE” is provided for reading in three-channel analog values. It is part of the COM 155H package, and is on the diskette in program file S5CR70ST.S5D.

All other required parameters, such as the discrepancy value, the discrepancy time and the address of the third channel, must be configured using COM 155H.

The function block can be used for modules 460 and 465. Its input and output parameters are identical to those of standard FB 40 ”3:RLG:AE” for the S5-155U. The only difference is that the specified upper and lower limit values are used to check for range violations on those modules configured as redundant modules.

Execution Time for ”Function Blocks”

Depending on the operations used, the execution time of the ”H” function blocks may be longer than that of the standard function blocks:

FB43: 3-RLG:AE, for three-channel redundant AIs, by approx.: 800 µs

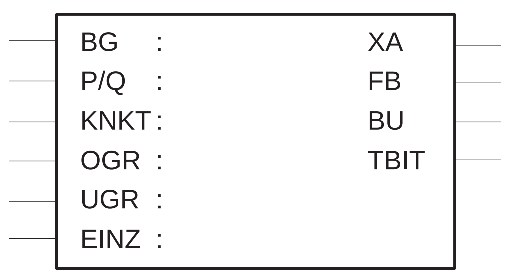
Calling the FB for 3-Channel Redundant AIs

Function block FB 43 reads three analog values XE from three analog value inputs and provides a proportional output value XA, based on its nominal range, between UGR (lower limit) and OGR (upper limit). The analog value can be read in either by the cyclic or selective sampling method. The FB number may be changed during loading.

STEP 5 program

```
      :   JU FB 43
NAME  :   3-RLG:AE
BG    :
P/Q   :
KNKT  :
OGR   :
UGR   :
EINZ  :
XA    :
FB    :
BU    :
TBIT  :
```

Graphic representation FB 43



Description of Input and Output Parameters

Name	Parameter Type	Data Type	Description	Remarks
BG	D	KF	Module address	P/Q = P: BG = 128 to 240 P/Q = Q: BG = 0 to 240
P/Q	D	KS	I/O area	P/Q = P: P area P/Q = Q: O area
KNKT	D	KY	Channel number KN, Channel type KT	KN = 0 to 15 KT = 3 to 6 (see Notes)
OGR	D	KG	Upper limit of the output value	–1701412+39 to +1701412+39
UGR	D	KG	Lower limit of the output value	–1701412+39 to +1701412+39
EINZ	I	BI	Selective sampling	EINZ = 0: Cyclic sampling
XA	Q	D	Address for output value XA	Scaled value between UGR and OGR (see Note)
FB	Q	BI	Bit address for ”Wirebreak” bit	0 = No wirebreak 1 = Wirebreak
BU	Q	BI	Bit address for ”Range violation” bit	0 = No range violation 1 = Range violated
TBIT	Q	BI	Bit address for ”Analog input” bit,	Always 0

Notes on Channel Type KT

The permissible analog input modules can provide the analog value in four different notations. You must choose the one you want by setting the KT parameter accordingly.

KT = 3 : Absolute value between 4 and 20 mA
KT = 4 : Unipolar representation
KT = 5 : Bipolar absolute value
KT = 6 : Bipolar fixed-point number

If the KT parameter is set to a value less than 3, the function block uses KT = 4; if it is set to a value exceeding 6, the function block uses KT = 6. The KT parameter must be in agreement with the method of representation set on the module itself.

Notes on Output Value XA

Input value XE from the analog input module is converted according to the following formulas, depending on channel type parameter KT.

OGR : Upper limit value UGR : Lower limit value
XE : Input value XA : Output value

$$KT = 3 \quad XA = \frac{UGR \times (2560 - XE) + OGR \times (XE - 512)}{2048}$$

$$KT = 4 \quad XA = \frac{UGR \times (2048 - XE) + OGR \times XE}{2048}$$

$$KT = 5/6 \quad XA = \frac{UGR \times (2048 - XE) + OGR \times (XE + 2048)}{4096}$$

Notes on UGR/OGR

Range limits for the output value

The analog value can be represented as a physical value if suitable range limits are chosen.

Example:

Analog Value Range	Phys. Value	Range Limits		Resolution
0 to 10 V	2 to 150 °C	2000000 +01	1500000 +03	0.1 °C

Notes on "Range Violation" (BU) Bits

Range violation BU

In the case of modules which were configured as three-channel redundant modules, the upper and lower limit values specified with COM H are used to check for range violations. If the analog value from all three modules is in the overflow range (analog value > +4096 or < –4096 units), the "Range violation" bit is set and the analog value limited to +4096 or –4096 units.

Channel type 3: 4 to 20 mA The BU bit is also set when the value is in the range from 3 to 4 mA

Wirebreak

In the event of a wirebreak on all three modules, XA is set to 0 and the 'wirebreak' bit set.

Notes on Error Detection

The three analog values are checked for discrepancies. The permissible discrepancy value is calculated from an absolute value (in units corresponding to the specified digital notation for the analog value) to which a relative value (a percentage of the maximum value of the three analog values) is added.

$$D_{perm.} = ABS + \frac{REL \times RAWV}{100}$$

$D_{perm.}$:	Permissible analog value discrepancy
ABS:	Absolute component of the configured discrepancy
REL:	Relative component of the configured discrepancy
RAWV:	The middle value of the three current analog values

Example

The following was configured with COM 155H:

ABS: 100 REL: 10%

Actual analog value, subunit A: 1000 subunit B: 980

Actual analog value, 3rd channel: 1040

Actual discrepancy: D1 = 1000 – 980 = 20

D2 = 1040 – 1000 = 40

Permissible discrepancy $D_{perm.} = 100 + \frac{10 \times 1000}{100} = 200$

It follows that the actual discrepancy lies within the permissible range.

When FB 43:3-RLG AE is called, it reads the analog values from both subunits, exchanges them, and uses the middle value of the three analog values. If a one-sided, locatable error occurs (timeout, wirebreak), the module is passivated; that is, it is no longer accessed (1-out-of-2 operation).

If the 155H system program detects a discrepancy error, the module whose analog value differs most from the other two (2-out-of-3) is passivated when the configured discrepancy time has elapsed.

If a number of modules report different errors, passivation is prioritized as follows:

1. Timeout (QVZ)
2. Wirebreak
3. Overflow
4. Range violation.

If FB 43:3-RLG AE detects only a range violation or overflow condition for all three AI modules, but no discrepancy, the standardized analog value is passed together with the ”Range violation” (BU) or ”Overflow” (BU) bit.

If FB 43:3-RLG AE detects a ”wirebreak” error in all three modules, it sets the ”Wirebreak” (FB) bit.

4.5 Redundant Analog Outputs

One-Sided Analog Outputs

All direct access operations (such as T PY, T OY and T OW), to one-sided analog outputs are allowed. Output to the I/Os is direct on two channels.

Redundant Analog Outputs

The following applies to AQs: If a STEP 5 operation (T PW, T OW) is used to output a value to a redundant channel, then the value is output to **both** subunits.

If error detection with error locating is required, you can make this possible by:

1. Implementing your own readback analog inputs

Note: When analog modules are used, the BASP signal is ignored; that is, the last analog value is retained. Remember this when wiring the redundant analog outputs.

2. Selecting the AQ type 21 which is supported by the operating system.

4.5.1 Redundant 2-Channel AQs without Error Locating Facility

The analog output (I/O type 20) has the same address in subunits A and B. No other switched or one-sided DQ or AQ may be configured under this address.

4.5.2 Redundant 2-Channel AQs with Error Locating Facility

The analog output (I/O type 21) has the same address in subunits A and B. All AQ channels are assumed to be intermittent, as no artificial value range test is executed. An active side change (relay switching every 10 hours) shows whether or not the passive AQ channel is still intact.

Fault Tolerance and NON-STOP Operation

Two-channel analog output modules may be used as NON-STOP AQs when the process is able to tolerate an AQ error output at regular intervals, which necessitates one or more FB call intervals. In the event of an error – on one side – the output to the actuator is switched, and the error thus controlled (Figure 4-13). A system with two-channel AQ will tolerate the following errors in one of the subunits:

- AQ module failure
- Failure of the rack power supply
- Failure of the load voltage in the event of redundant load voltage

The maximum duration (T_F) of an error output can be calculated as follows:

$$T_F = T_D + T_{L–DQ} + T_Q$$

TQ	Call interval for FB 41 (H:RLG:AA)
TD	Configured discrepancy time = AQ output delay + AI readback delay (rounded off to 10 ms units)
TL-DQ	Relay delay time of the L-DQ

Direct I/O Access

All direct two-address and four-address I/O access operations (such as T PW and TBGD) to two-channel AQs are permitted. When such an operation is executed, the operating system outputs the value to the two-channel AQ in **both** subunits. The readback AI is not checked. Address access operations, such as T PY, to two-channel AQs of type 21 are **not** permitted.

Subunit Failure

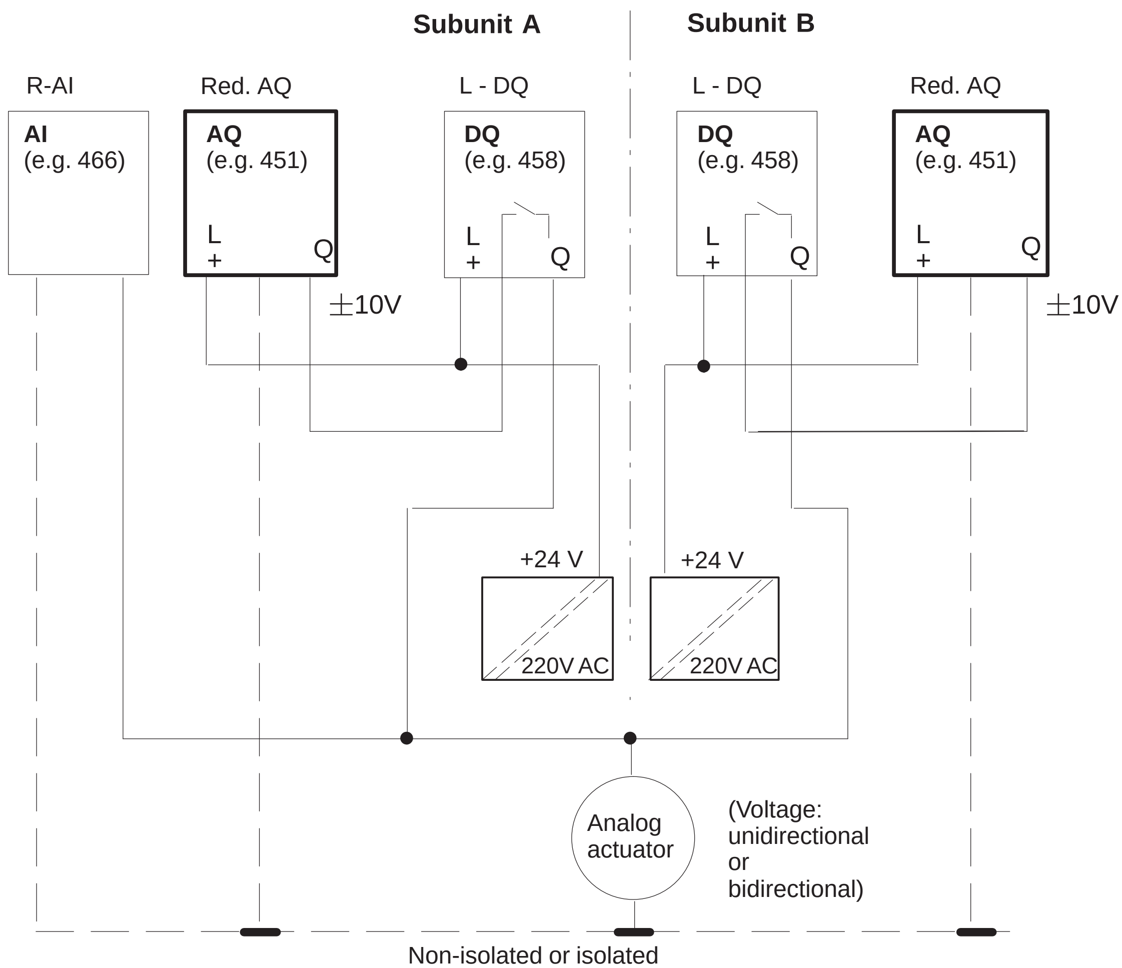
When a subunit fails, the operating system executes the switchover or decoupling routine, switching all L-DQ relay outputs in the intact subunit to ”1” (see Figures 4-13 and 4-14).

Depassivation must be initiated following repairs to a two-channel AQ. When depassivation has been completed, the two-channel AQ is once again fault tolerant.

The setting of the voltage range for AQ and R-AI must match for voltage output.

For current output, the R-AI module must be set to 1 V (1.25 V for the 466).

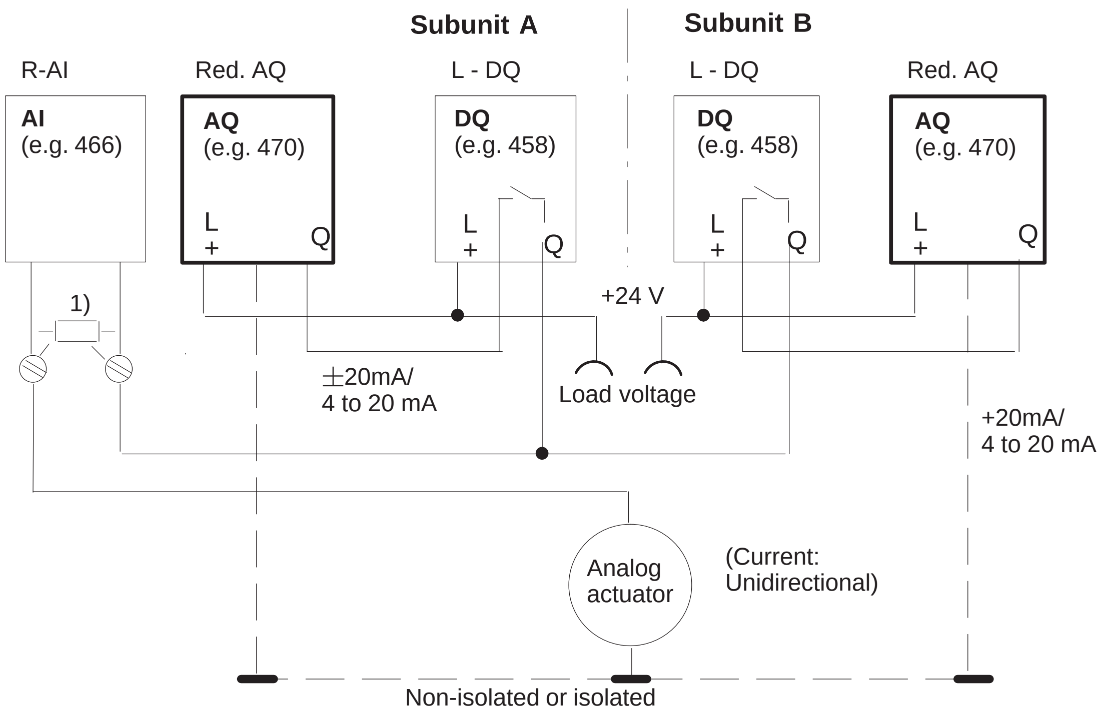
Only two’s complement number representation may be used for the setting.



L-DQ : Locating DQ
Red. AQ : Redundant AQ
R-AI : Readback AI

Use of a load voltage supply is also permitted. However, if the load voltage fails, the entire redundant AQ group fails.

Figure 4-17 Redundant (1-out-of-2) AQs with Error Locating on Voltage Output (I/O Type 21)



1) 50 Ω , 0.1 %
Setting for the AI module to 1 V. If the 466 module is used as the readback AI, 1.25 V should be set.

Figure 4-18 Redundant (1-out-of-2) AQs with Error Locating on Current Output (I/O Type 21)

At the current input, the module type 6ES5 465-... is not permitted for the R-AI. With an ET 200, ± 20 mA bi-directional is possible.

4.5.3 FB for 2-Channel Redundant AQs (FB 41)

Standard function block FB 41 ”H-RLG:AA” is provided as the means to output two-channel analog values. FB 41 is part of the COM 155H package. The FB number may be changed on loading.

The function block converts an input value XE into an output value for an analog module on the basis of nominal range limits UGR and OGR. An error is reported in the event of a range violation. The function block also processes the system’s response to the failure of a two-channel AQ component. Special configuring data must be entered with COM 155H for redundant AQs.

Execution Time of ”Function Blocks”

The execution time of the ”H” function block may exceed that of the standard function block, depending on the operations used:

FB 41 H-RLG:AA, for two-channel redundant AQs
by approx.: 750 µs

Using FB 41

FB 41 does the following:

- Both subunits still functioning properly

  FB 41 reads the readback AI and compares the value read with the corresponding value in the PIQ. If the discrepancy time elapses, the L-DQ relay is switched and and H error (”Passivation”) reported.

  The output value is output to the AQ module in both subunits and the non-linearized value stored in the PIQ.

- One I/O side has failed (CPU in redundant mode)

  FB 41 reads the readback AI and compares the value read with the corresponding value in the PIQ. If the discrepancy time elapses, an H error (”Error”) is reported. The readback AI is passivated.

  The output value is output to the AQ module and the non-linearized value stored in the PIQ.

- One subunit is operating in Solo mode

  The output value is output to the AQ module and the non-linearized value stored in the PIQ. The readback AI is not read.

Rules for the User Program

A) The channel to which the L-DQ bit is assigned must be the AQ for which FB 41 is called most often, so that the test switchover can run as quickly as possible. For example;

```
OB xx               10 ms
SEGMENT 1           0000
0000   :  L SW xx
0001   :  T PW 128  Direct access = without error detection
0002   :  L SW xy
0003   :  T PW 130  Direct access = without error detection
```

(Direct accesses are used to optimize the run time and for compatibility).

...

The output channels must be updated by the FB 41 (even if less often), as only the FB 41 executes the L-DQ switching, error detection and error localization.

```
OB 11                    10 ms
SEGMENT 1                0000
0000           :   JU FB 41
0001 NAME      :   H-RLG AA
0002 XE        :   FD 10       Input value XE (floating point)
0003 BG        :   KF + 128    Base address of the two-channel AQ
0004 P/Q       :   KS P        Area ID: P
0005KNKT       :   KY 0,0      Channel 0
...
```

```
OB 13                    100 ms
SEGMENT 1                0000
0000           :   JU FB 41
0001 NAME      :   H-RLG AA
0002 XE        :   FD 20       Input value XE (floating point)
0003 BG        :   KF + 128    Base address of the two-channel AQ
0004 P/Q       :   KS P        Area ID: P
0005KNKT       :   KY 1,0      Channel 1
...
```

The parameter value «Indic. no. of updates (1...10)» is calculated from the number of direct access operations and FB 41 calls for the chosen channel per readback delay time.

If the value calculated is greater than 10, an AI module type should be chosen which encodes quicker (for example, 463 or 466).

B) To reduce the switchover surge on the analog output when a subunit fails to a minimum time, the given instruction sequence in OB 1 and OB 37 must be implemented : (with x= H flag word)

```
OB 1
SEGMENT 1              0000
0000   :  A F x.1      Redundant mode
0001   :  S S 100.0    Any flag to signal failure of partner
...
```

OB 37

SEGMENT 1		0000	
0000	:	AN F x.1	Solo mode
0001	:	A S 100.0	and previous redundant mode
0002	:	JC FB 41	FB 41 switches all L-DQ bytes to 0FFH immediately
NAME	:	H-RLG: AA	
0003 XE	:	FD 0	Not evaluated here
0004 BG	:	KF + 0	0 means failure of partner CPU
0005 P/Q	:	KS P	Area ID: P
0006KNKT	:	KY 0,0	0,0
0007 OGR	:	KG 00000 + 0	0
0009 UGR	:	KG 00000 + 0	0
000A FEH	:	F 10.0	always 0
000B BU	:	F 10.0	always 0

...

Calling FB 41

STEP 5 program:

OB xx

SEGMENT 1

	:	JU FB 41	
NAME	:	H-RLG AA	
XE	:	FD10	Input value XE (floating point)
BG	:	KF +128	Base address of the two-channel AQ
P/Q	:	KS P	Area ID: P/Q
KNKT	:	KY 0,1	Channel number, channel type
OGR	:	KG 10000+0	Upper limit of the output value
UGR	:	KG 00000+0	Lower limit of the output value
FEH	:	F 16.0	Error bit for UGR $\leq$ OGR
BU	:	F 16.1	Error bit for XE < UGR or XE > OGR

Input/Output Parameters:

Name	Parameter Type	Data Type	Description	Remarks
XE	I	D	Address of the input value XE	Input value (floating point) in the range UGR to OGR
BG	D	KF	Module address	P/Q = P: BG = 128 to 240 P/Q = Q: BG = 0 to 240
P/Q	D	KS	I/O area	P/Q = P: P area P/Q = Q: O area
KNKT	D	KY	Channel number KN Channel type KT	KN = 0 to 7 KT = 0 unipolar KT = 1 unipolar
OGR	D	KG	Upper limit of the output value	–1701411+39 ≤ +1701412+39
UGR	D	KG	Lower limit of the output value	–1701412+39 ≤ +1701411+39
FEH	Q	BI	Bit address for error flag UGR ≤ OGR	
BU	Q	BI	Bit address for ”Range violation” bit	0 = UGR ≤ XE ≤ OGR 1 = XE ≤ UGR or XE ≤ OGR

BU : If XE lies outside the range limits UGR and OGR, the bit BU is set and the last valid value output continues to be output by the active module.

Notes on Output Value XA

The input value (XE) read in from the analog input module is converted according to the formulae below depending on channel type parameter KT.

OGR : Upper limit value   UGR : Lower limit value

XE : Input value   XA : Output value

KT = 0 $$XA = \frac{1024 * (XE–UGR)}{OGR\text{-}UGR}$$

KT = 1 $$XA = \frac{1024 * (2 * XE– [OGR–UGR])}{OGR–UGR}$$

Notes on UGR/OGR

Range limits for the output value

The analog value can be represented as a physical value if suitable range limits are selected.

Example:

Input Value XE	Range Limits UGR	OGR	Output Value XA
–5000 ... +5000	–5000000+04	+5000000+04	–1024 ... +1024

4.6 One-Sided I/Os

Configuration and Functionality

A one-sided module is always assigned to one of the two subunits. If this subunit fails, the modules assigned to it also fail. This means that this configuration provides no greater fault tolerance than the S5-155U.

The modules can be plugged into either the central controller or an expansion unit.

When using one-sided I/Os, it is of no significance which subunit is master. Both subunits receive the current signal states. If a timeout (QVZ) occurs on a one-sided I/O, the relevant I/O byte is passivated.

Figure 4-15 shows the various one-sided configurations.

Note:
If a subunit fails, the one-sided I/Os in that subunit can no longer carry out their assigned functions.

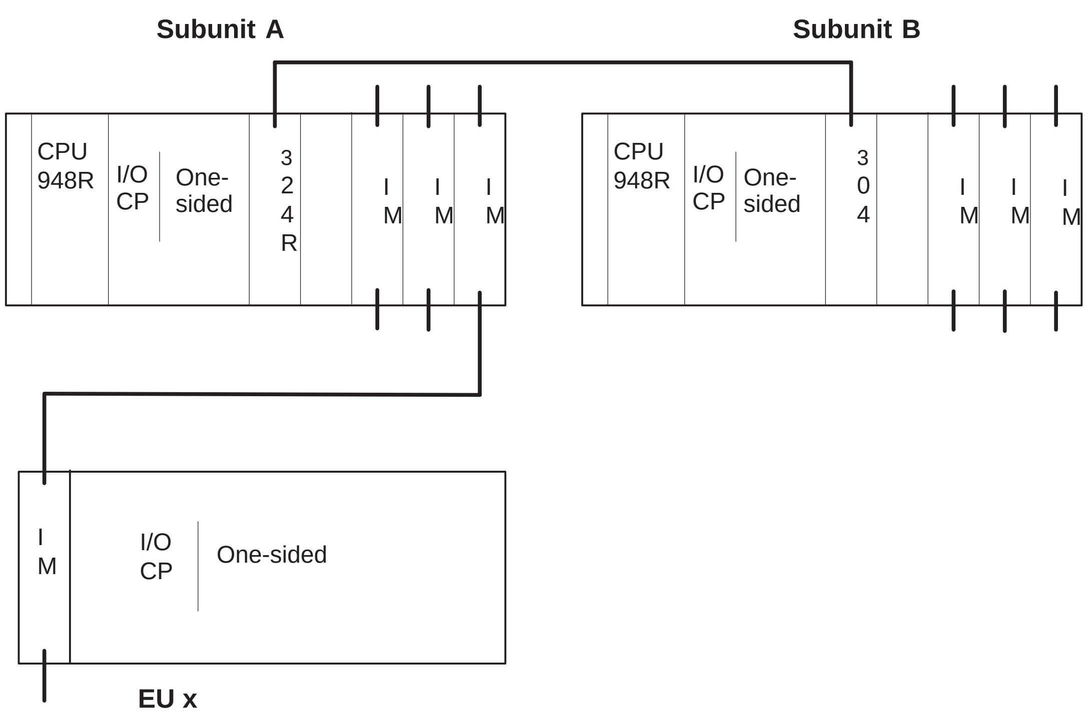


Figure 4-19 One-Sided I/O Operation and Permissible Modules

Interface Modules and Expansion Units (EUs)

The same interface modules and expansion units can be used for one-sided operation in the S5-155H as can be used in the S5-155U (refer to the S5-135U/155U System Manual, Chapter 4).

Digital and Analog Input/Output Modules

All I/O modules used in the S5-155U can be used for one-sided operation.

One-sided I/O modules should be used only for subprocesses whose failure can be tolerated in the event of a controller failure. The software for controlling these subprocesses should be implemented in blocks reserved for this purpose, and these blocks invoked conditionally; that is, only when the relevant subunit is running (see example). If this recommendation is not observed, a subunit failure will cause a continuous timeout (QVZ error), seriously affecting the scan time.

Sample program: One-sided I/Os assigned to subunit A

STL		Explanation
:O	F X.1	Flag for "PLC in redundant mode"
:		Bit 2^1 in H flag word (high-order byte)
:O	F X.4	Flag for "Central controller is
:		subunit"
:JC	FB Subproc.A	A", bit 2^4 in H flag word (high-order byte)

The subprocess runs only when subunit A is running.

Proceed in the same manner as in the sample program above for one-sided I/Os assigned to subunit B.

Sample program: One-sided I/Os assigned to subunit B

STL		Explanation
:O	F X.1	
:		
:ON	F X.4	
:		
:JC	FB Subproc.B	

Addressing

One-sided DIs or DQs may be assigned a given address once only, either in subunit A or subunit B, and the addresses used for one-sided DIs or DQs may not be used for switched or redundant DIs/DQs.

The same applies to AIs and AQs; that is, these modules may also be assigned a given address once only, and the addresses assigned to AIs/AQs may not be used for switched or redundant DIs/AIs or DQs/AQs. A one-sided third channel on a three-channel DI or AI, however, may be assigned the same address in the other subunit.

Address area:	One-sided DIs:	0FF000h to 0FF1FFh
	One-sided DQs:	0FF000h to 0FF1FFh
	One-sided AIs/AQs:	0FF080h to 0FF1FFh

All direct I/O access operations (e.g. T PY, T OY, T PW) are permitted for one-sided analog inputs/outputs.

Standard FBs

The standard FBs of the S5-155U can be used for one-sided analog I/Os.

4.7 Switched I/Os

Configuration and Functionality

The input or output module can be operated by either subunit. This provides enhanced fault tolerance compared to the S5-155U.

At least one 185U expansion unit is required to operate switched I/Os. The expansion unit is connected to both S5-155H central controllers via the IM 304/IM 314R interface modules. Up to 16 switched EUs can be operated in one S5-155H controller.

When a timeout (QVZ) occurs for a switched I/O, the byte is not passivated. On the first timeout for a switched I/O in redundant controller mode, a standby-master switchover is carried out and the "PLC fault" bit in the H flag word set.

Note

When a timeout (QVZ) occurs for digital/analog I/Os, the cycle is extended by approx. 1 ms per byte.

Figure 4-20 illustrates the various switched I/O configurations.

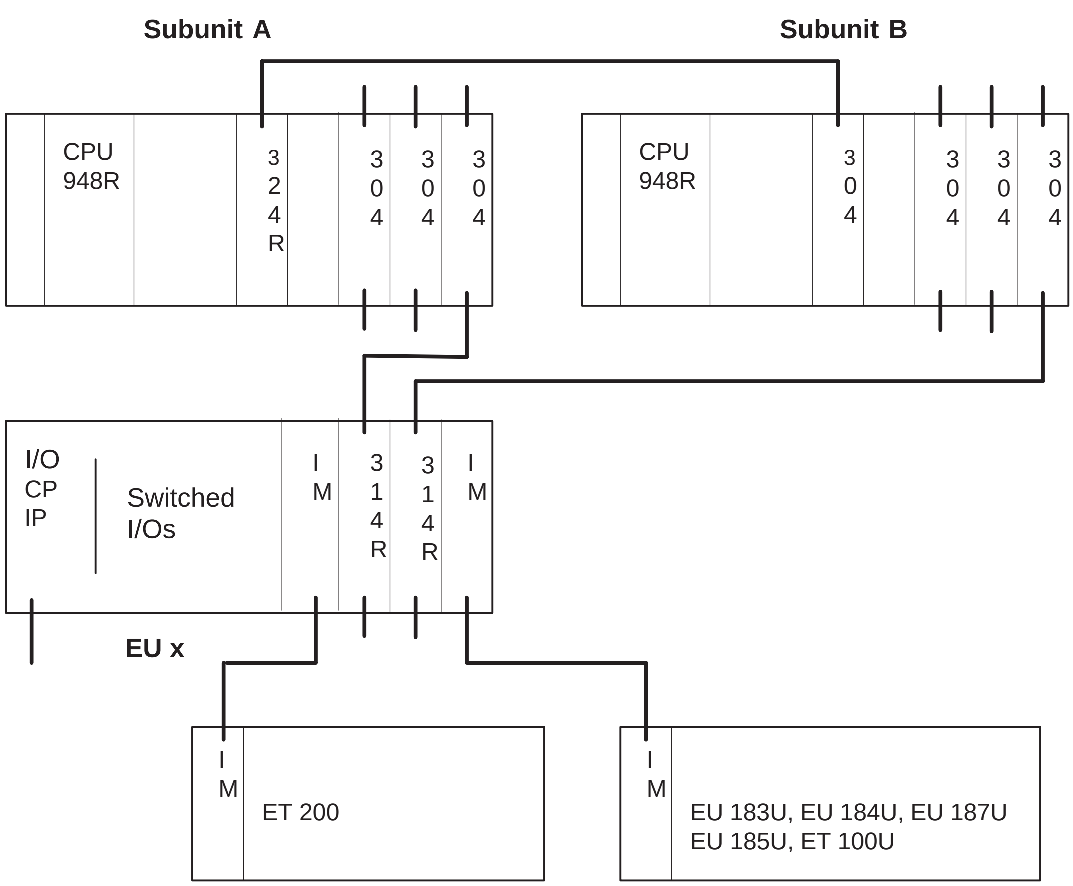


Figure 4-20 Switched I/Os and Permissible Modules

Interface Modules and Expansion Units (EUs)

At least one 185U expansion unit and the IM 304 to IM 314R interface modules are required to operate switched I/Os.

Note

If the IM 300 or IM 308 interface module is plugged into slot 163 in the expansion unit, the 183U, 184U and 187U or 185U and the ET 100U can also be operated.

In switched I/O configurations and a maximum ET 100U configuration, a time loop longer than the ET 100U configuration run (max. 4 s) must be programmed in OB 22 in both the master and standby controller.

Digital and Analog I/O Modules

All I/O modules which can be used in the S5-155U can also be used in switched I/O configurations.

Address area:	Switched DIs/DQs:	0FF000h to 0FF1FFh
		0FF300h to 0FF3FFh
		0FFC00h to 0FFDFFh
	Switched AIs/AQs:	0FF080h to 0FF1FFh
		0FF300h to 0FF3FFh
		0FFC00h to 0FFDFFh

All direct I/O access operations (T PY, T OY, and T PW, for example) are permitted for use with switched analog inputs/outputs.

Standard FBs

The standard FBs of the S5-155U can be used for switched I/Os.

4.8 Hybrid I/O Configurations

All three I/O modes (one-sided, switched and redundant) can be combined in one S5-155H.

The figure below shows possible hybrid configurations.

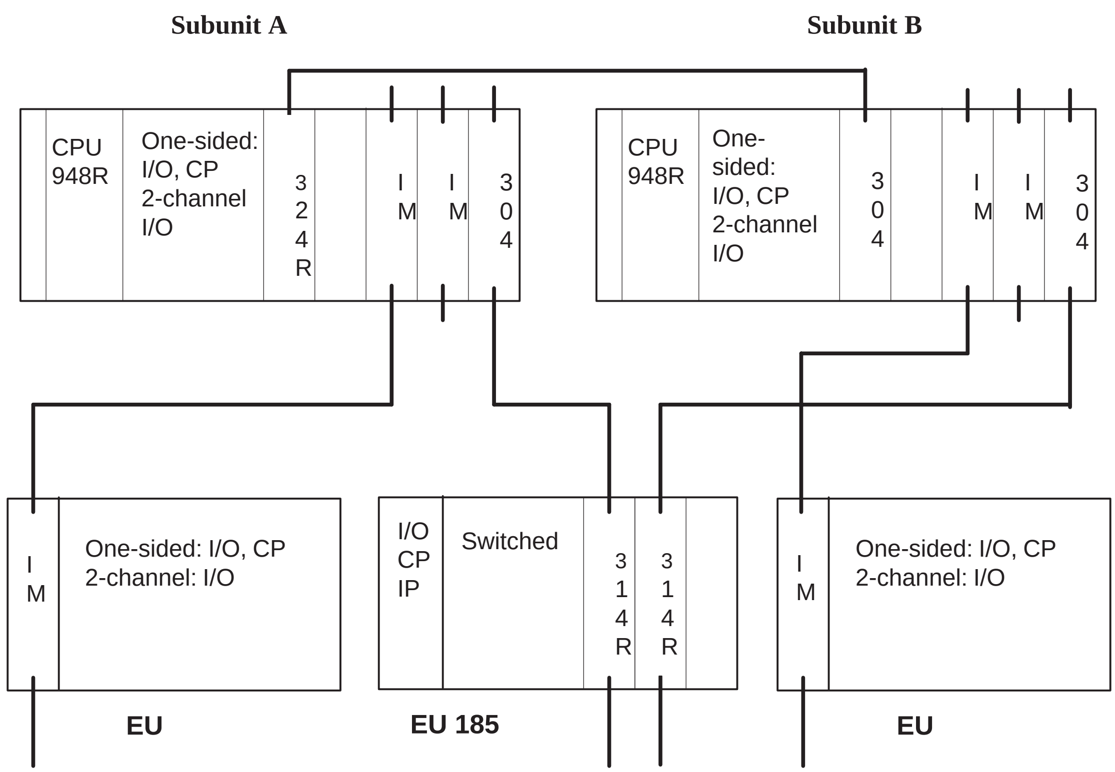


Figure 4-21 Hybrid I/O Configurations

4.9 FB 192 (IM308C-R) for Redundant and One-Sided Operation

4.9.1 General

Areas of Application

The standard function block FB 192 with the name IM308C-R is used for redundant and one-sided operation of the S5-155H programmable controller with the IM 308-C. The FB 192 IM308C-R is called in the cyclic program for the programmable controller.

For switched operation of the S5-155H programmable controller, the existing function block (FB 192 from the U system) can be used.

The function block can be used in the following address areas:

- F F000 to F F1FF
- F F400 to F F5FF
- F F600 to F F7FF
- F F800 to F F9FF (default setting)
- F FA00 to F FBFF
- F FC00 to F FDFF
- F FE00 to F FFFF

The terms ”IM area” and ”IM I/O area” are used in this manual. These refer to the above address areas.

The FB 192 IM308C-R runs on the CPU 948R and CPU 948RL in the S5-155H.

Master and slave diagnostics with the FB 192 IM308C-R are only possible from version 3.0 of the IM 308C.

Form of Supply

The standard function block is supplied together with a programming example which shows how it can be used. With an indirect configuration the parameters for the parameter assignment DB must be specified.

The files are supplied on a $3^1/_2$” disk for the operating system S5-DOS/ST (MS-DOS).

The following overview shows which files are supplied:

File Name	Valid for...	In Programmable Controller
S5ET70ST.S5D	CPU 948R / 948RL	S5-155H

4.9.2 Standard Function Block FB 192

Overview

The standard function block FB 192 with the name IM308C-R is available for communication with the IM 308-C via the IM I/O area for the S5-155H programmable controller in redundant and one-sided operation. The standard function block executes the following functions:

Function Block	Function	Call Normally in...
FB 192	Read master diagnostics Read slave diagnostics	...the cyclic program processing level

The standard function block can also be stored in an EPROM submodule. The user can change the number of the standard function block.

The diagnostic data read are structured as described in the “Distributed I/O System ET 200” manual.

Functional Description

The standard function block IM308C-R reads the diagnostic data from the master and the slave from the page number 128.

The following pages from the IM areas are used:

IM Page No.	Area on the IM 308C	Data	Remark
Page 128	IM4	Page for consistent diagnostic data	Only read by FB
Page 254	IM3	Interrupt page	Read and written by FB

The following STEP 5 memory areas are permitted: data blocks DB and extended data blocks DX.

If no interface module is located in the address area in which the FB 192 IM308C-R wants to address the IM 308-C module, this is not recognized by the function block (exception QVZ).

In FB 192 IM308C-R the programmable controller interrupt processing is disabled and enabled again if necessary.

Access Coordination in the S5-155H

The IM 308-C and the standard function block exchange their data via a page in the IM3 or IM4 area of the interface module. The data exchange must adhere to a specified access coordination so that the data can be read consistently (i.e. together). The access coordination to be adhered to is described below. The maximum wait time in the function block is set to 1 ms.

Coordinating access between the standard function block and the IM 308-C is achieved via access to the interrupt page.

The procedure is explained here based on subunit A:

1. Switch the subunits to S5-155U mode.
2. Query whether subunit A
   – Yes, continue with 3.
   – No, continue with 6.
3. In subunit A: interface to the interrupt page IRINFO of the CPU and write interrupt ID to the page
4. In subunit A: interface to the diagnostics page
5. In subunit A: read diagnostics data
6. Copy the data from subunit A to subunit B
   Receive data from subunit A
7. Switch the subunits to redundant mode again.

Calling the Function Block

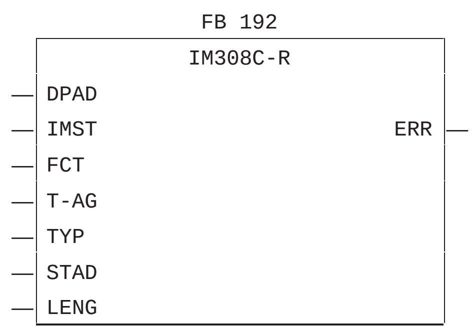
The FB 192 IM308C-R is called to read the diagnostic data in the cycle or alternatively in a time-driven program.

Block call:

STL representation

```
       :JU FB 192
NAME   :IM308C-R
DPAD   :
IMST   :
FCT    :
T-AG   :
TYP    :
STAD   :
LENG   :
ERR    :
```

LAD representation



The function block call can have direct or indirect parameter assignment.

Direct Parameter Assignment of the Function Block

With direct parameter assignment, the actual operands specified at the block apply for all parameters. The user selects direct parameter assignment by specifying a valid function (other than “XX”) at the parameter FCT.

Indirect Parameter Assignment of the Function Block

With indirect parameter assignment, the parameters must be entered in the data block currently open before the FB 192 IM308C-R is called. The user selects indirect parameter assignment by specifying the actual operand “XX” at the parameter FCT. If the parameter DB is too short, the CPU goes into STOP mode. All other errors are intercepted by the function block and output in the “parameter DB”.

Description of the Block Parameters of FB 192 IM308C-R

The following table describes the block parameters of the FB 192 IM308C-R:

Name	Param-eter Type	Data Type	Name	Permitted Assignment
DPAD	D	KH	Address	KH = x: x ∈ ×[F000, F400, F600, FA00, FC00, FE00]
IMST	D	KY	Number of the IM 308-C, station number of the slave	KY = x, y: • x ∈ ×[0, 16, 32, 48, 64, 80, 96, 112, 128, 144, 160, 176, 192, 208, 224, 240] (x = number of the IM 308) • 1 ≤ ×y× ≤ ×123 bei FCT = SD (y = station number, irrelevant if FCT = MD
FCT	D	KS	Function	KS = x: • x = ’MD’ ⇒ Read master diagnostics • x = ’SD’ ⇒ Read slave diagnostics • x = ’XX’ ⇒ Indirect parameter assignment
T-AG	D	KS	Select subunit A or B	KS = x: • x = ’A’ ⇒ Diagnostic data from subunit A • x = ’B’ ⇒ Diagnostic data from subunit B
TYP	D	KY	Type of the STEP 5 memory area	KY = x, y: • 0 ≤ ×x× ≤ ×1 0 = Data block type DB 1 = Extended data block type DX • 10 ≤ y ≤ 255 y = DB number or DX number
STAD	D	KF	Start of the STEP 5 memory area	KF = +x: • 0 ≤ ×x× ≤ ×255 x = Number of the first data word
LENG	D	KF	Number of bytes to be transferred	KF = x: • 1 ≤ ×x× ≤ ×244[1)] or x = –1 (wildcard length)[2)]
ERR	Q	W	Error word	Flag[3] output word or data word[4)]

1) The area to be transferred must lie completely within the data block.

2) The user can specify the wildcard length –1. In this case the FB transfers the number of bytes specified in the length byte 253 of the page. If the source area or destination area are not long enough, the FB does not transfer any data but outputs an error message at the parameter ERR.

3) No scratchpad flags (FY200 to FY255) must be used.
4) The data word lies in the data block open before the FB call. If the data word does not exist, the CPU goes into STOP mode.

The parameters are checked for valid limits and if an error is found, this is reported at the parameter ERR.

Function FCT=	Meaning	FB-Internal Process (Main Points)
MD	Read **M**aster **D**iagnostics	The FB transfers the number of bytes specified at the parameter LENG or the length reported back from the IM 308-C, where LENG = –1, from the IM4 area with the page number 128 to the S5 destination area (details at the parameters TYP and STAD). The station number specified at the parameter IMST is not evaluated by the FB.
SD	Read **S**lave **D**iagnostics	The number of bytes specified at the parameter LENG or the length reported back from the IM 308-C, where LENG = –1, is read from the IM4 page 128 and transferred to the S5 destination area (details at the parameters TYP and STAD).
XX	Switch to indirect parameterassignment	The FB fetches the parameter data from the data block open at the FB call (DW1 to DW8).

General Notes on Data Transfer

The function block always attempts to transfer the number of bytes specified at the parameter LENG by the used. If there are not enough bytes available on the page (LENG > length byte 253), the function block does not transfer any data. Instead, the function block outputs an error message in the parameter ERR. If the user wants to transfer fewer data than are available on the page (LENG < length byte 253), the function block does not generate an error message. If the user does not know how many data he can read out at maximum, he should specify the wildcard “–1” at the parameter LENG when he calls the function block. In this case, the function block transfers all the data bytes specified in the length byte 253. The transfer length is output in the high byte of the parameter ERR. The function block does not generate an error message (RLO = “0”, low byte of ERR = 0).

If the length byte 253 contains the value 0, the function block transfers no data, but outputs an error message at the parameter ERR.

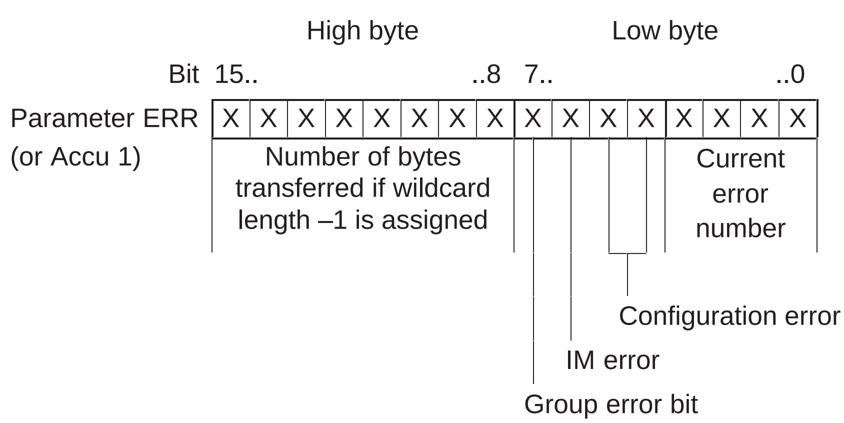
Assignment of the Parameter ERR

If an error occurs when processing the function block, the parameter ERR contains more detailed information about the cause of the error. The RLO is also set to "1".

If the function block reports a parameter error, the cause can be determined via the error number (e.g. data block does not exist or is too short).

If the function block is processed without error, the low byte of the parameter ERR contains the value zero. The RLO is also set to "0".

The high byte of the parameter ERR contains the number of bytes transferred if the function block was called with LENG = –1 (wildcard length); in all other cases "0". The low byte contains the error number if an error occurs. It has some bit assignments:



Assignment of the Parameter Data Block

The assignment of the parameter data block is only relevant for indirect parameter assignment of the FB 192 IM308C-R. With indirect parameter assignment (FCT = “XX”) the function block takes the parameter data from the parameter data block and not from the block parameters. The parameter data block must be opened and had parameters passed by the user before calling FB 192 IM308C-R. The ERR word is then always in DW 8 of the parameter DB.

The parameter data block has the following structure:

		Recommended data format
DW 0	Reserved	KH
DW 1	**DPAD**	KH
DW 2	**IMST**	KY
DW 3	**FCT**	KS
DW 4	**T-AG**	KS
DW 5	**TYP**	KY
DW 6	**STAD**	KF
DW 7	**LENG**	KF
DW 8	**ERR**	KY/KH

4.9.3 Technical Specifications

FB 192	Properties
Function block (Name)	FB 192 (IM308C-R)
Library number	P71200-S7192-A-1 CPU 948R / 948RL
Block length	532 words
Assigned flags	FY 200 to FY 255
Data area	Parameter DB to DW 8 inclusive [1)]
Nesting depth	1
Other	Disables interrupts

1) The parameter DB is only necessary for indirect parameter assignment.

4.9.4 Error Messages

Error Messages at Parameter ERR

Table 4-1 shows the error messages which can occur at the parameter ERR of the FB 192 IM308C-R.

If messages other than those listed here appear at the parameter ERR, the FB cannot address the IM 308C. Possible cause: incorrect IM 308C version.

Table 4-1 Error Messages at the Parameter ERR

LOW Byte in ERR (Hexadecimal)	Error Message
00	No error occurred
A2	Illegal IM 308-C number (parameter IMST)
A3	Illegal DP slave station number (parameter IMST)
A4	Illegal LENG parameter
A5	Illegal TYP parameter
A9	Illegal TYP parameter; the specified data block DB/DX is not available
AA	Illegal TYP parameter; the specified data block DB/DX is too short
AC	Illegal FCT parameter; FB 192 IM308C-R does not recognize the specified function
AD	Illegal STAD parameter
AE	Illegal station number (parameter IMST)
AF	LENG parameter too large. The IM 308-C does not have the required number of data bytes for the specified DP slave
B0	Timeout error; IM 308-C does not react
B1	Illegal TYP parameter; the specified DB/DX no. is invalid
B2	Illegal DPAD parameter
B4	Illegal T-AG parameter
DI	The IM 308-C is currently busy transferring data to the DP slaves. The required function could not be executed

In the case of an error, RLO = 1 is set on exiting the FB.

Operation of Communications Processors and Intelligent I/Os in the S5-155H

5

This chapter discusses the use of intelligent I/Os (IPs) and communications processors (CPs) in the S5-155H programmable controller in one-sided, switched and redundant configurations. It also covers the data handling blocks (DHBs) for the S5-155H and when and how to invoke them in the Restart routine and in the cyclic program.

5.1 Intelligent I/Os in the S5-155H

Communications

Normally, the programmable controller communicates with its intelligent I/O modules via data handling blocks (DHBs). In some cases, communication between intelligent I/Os and the user program is supported by specific standard function blocks (FBs). These FBs use the DHBs exclusively for communication between the PLC and the IPs/CPs.

In the case of other intelligent I/Os, communication between the programmable controller and the intelligent I/Os and/or communications processors is implemented by module-specific standard FBs.

The data handling blocks (DHBs) for the S5-155H are on the COM 155H diskette.

5.2 One-Sided CP/IP Configurations

Communications Processors (CPs/IPs)

In a one-sided configuration, the degree of fault tolerance is no higher than that of an S5-155H. Such a configuration may therefore be used only when a failure can be tolerated.

In one-sided CP/IP configurations, you need only configure the interface number and the module-to-subunit assignments (refer to the description of COM 155H in this manual).

Interprocessor communication flags (for CPs) may not be used in one-sided configurations.

Incoming data is forwarded to both subunits, regardless of whether the subunit containing the CP/IP is the master or the standby.

Note

One-sided CPs should be used only for subprocesses which can be sacrificed completely in the event of a PLC failure. The software for controlling these subprocesses should be implemented in separate blocks which can be invoked **conditionally** (only when the relevant PLC is functional; see example). Failure to observe this recommendation will result in a continuous timeout should a PLC fail, which in turn will greatly increase the scan time.

Sample Program

One-sided CPs assigned to subunit A:

STL		Explanation
:O	F X.1	”PLC in redundant mode” flag, bit 2^1 in the H flag word (high-order byte)
:		
:O	F X.4	Flag for ”Central controller is subunit A”, bit 2^4 in the H flag word (high-order byte)
:		
:JC	FB Subproc. A	

The subprocess is then controlled only when subunit A is operating.

One-sided CPs assigned to subunit B:

STL		Explanation
:O	F X.1	
:		
:ON	F X.4	
:		
:JC	FB Subproc.B	

The subprocess is controlled only when subunit B is operating.

5.3 Switched CP/IP Configurations

CPs/IPs

The standby-master switchover is carried out without loss of data, regardless of whether the CPs/IPs are controlled by H data handling blocks or special function blocks.

All data which the master's CPU reads from the CPs/IPs is also forwarded to the standby CPU. Only the master CPU, however, writes to the CPs/IPs; the standby CPU suppresses write operations.

Interprocessor Communication Flags

Interprocessor communication flags (address range FF200 to FF2FF) are supported only in switched CP/IP mode.

These flags must be configured in data block DB 1. All other settings in DB 1 are irrelevant in this case.

The interprocessor communication output flags are output by the master controller, while the interprocessor communication input flags are passed from the master to the standby controller. Direct I/O access to "switched I/O" IPFs is thus permissible.

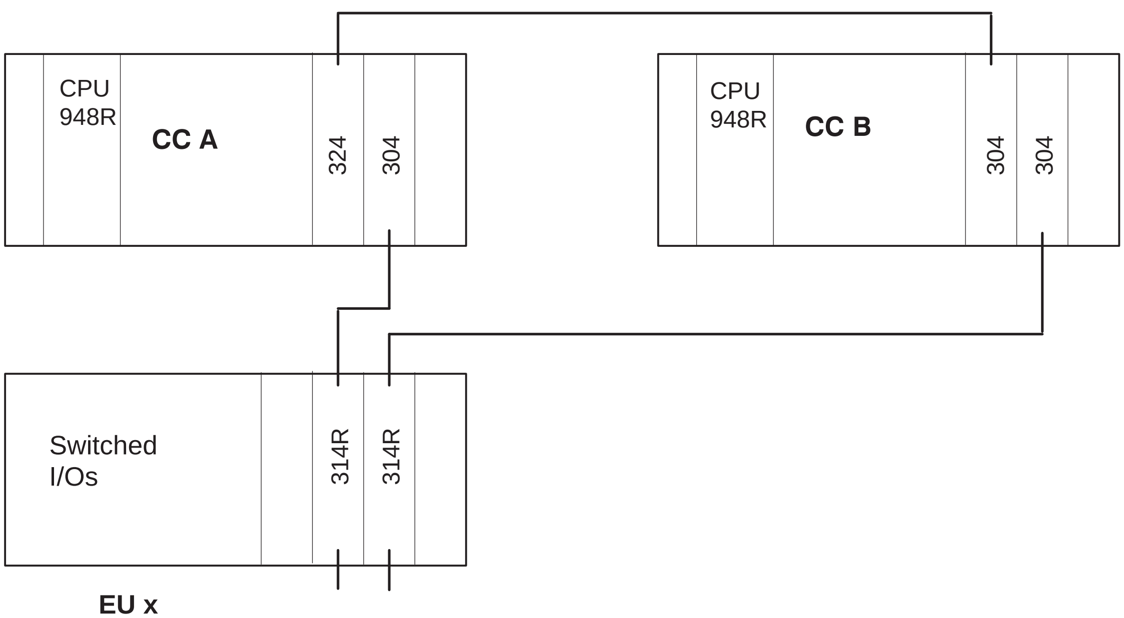


Figure 5-1 Switched I/O Configuration

5.4 Redundant Communications Processor (CP) Configurations

Configurations with Communications Processors

There are four configurations for redundant communications processors:

a) Two-channel redundant CP configuration (Figure 5-2)
b) Switched redundant CP configuration (Figure 5-3)

A single or double bus may be used.

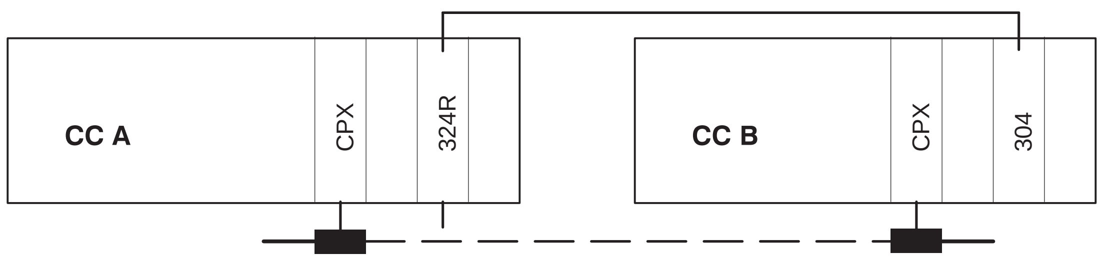


Figure 5-2 Two-Channel Redundant CP Configurations (Variant a)

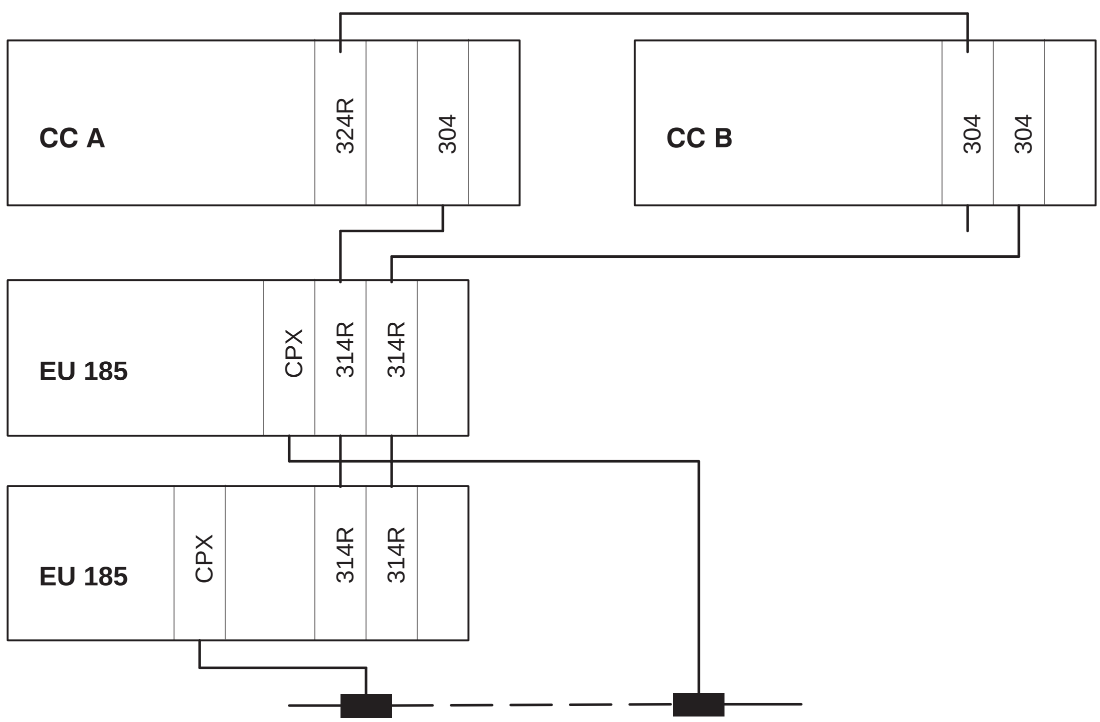


Figure 5-3 Switched Redundant CP Configurations (Variant b)

CP/IP Redundancy

CPs/IPs can also be redundant. They can be plugged into switched EUs, which is then called a ”switched redundant” configuration. The CPs can also be plugged into the two subunits, which is then called a ”two-channel redundant” configuration.

Selection criteria:

The best configuration for a given situation depends on the application.

Advantages of a switched redundant configuration:

- The CPs/IPs remain redundant even when a central controller fails
- The central controllers remain redundant even when a CP/IP fails
- Shorter scan time

Disadvantages of a switched redundant configuration:

- At least two switched EUs are required.
- While a CP/IP is being repaired, the EU into which it was plugged must be shut down. This means that all other I/O modules in that expansion unit are shut down as well.

Advantages of a two-channel redundant configuration:

- No switched EUs are required.
- CP repairs usually require that only redundant components be separated from the power supply.

Disadvantages of a two-channel redundant configuration:

- A significant increase in the scan time.

When programming, the two CPs must be regarded as independent modules. How redundancy is handled depends on the required functionality, and must be programmed by the user.

Switched Redundant CPs/IPs

If a CP/IP is to be plugged into an EU, you will need at least two EUs. A CP or IP must be plugged into each EU. When data arrives at a CP/IP, it is automatically forwarded to the other subunit.

Two-Channel Redundant CPs/IPs

In order to implement a two-channel redundant CP configuration, one CP must be plugged into each subunit. The two CPs reserve different pages, and operate independently of one another. If data arrives at one CP, it is automatically forwarded to the other subunit.

The user must program the redundancy function for a switched or two-channel redundant configuration himself. The user program must be written so as to stipulate which CP/IP is active, and must be able to detect a CP/IP fault and switch, if necessary, to the other CP/IP. The operating system ensures that the data is the same in both subunits. The two CPs/IPs must be regarded as separate, independent modules.

In contrast to redundant I/O modules, redundant CPs and IPs reserve different addresses or pages in each subunit.

Installation and Startup 6

This chapter uses examples to explain the procedures to follow when configuring and programming your programmable controller, as well as the procedures to follow to put it into operation.

Sections 6.1 to 6.5 build on one another and should therefore be read consecutively; that is, you should read the entire section even if you want to use only redundant I/Os.

The COM 155H User's Guide is also relevant to all points in this section.

6.1 Installing the S5-155H

General Remarks

The SIMATIC S5 installation guidelines apply.

To avoid confusion, the redundant central controllers should be installed in separate cabinets. This has the following advantages:

- Two redundant power supply units
- Less confusion when laying the cables
- Better visual monitoring of master and standby

Example of an Installation

S5-155H with four switched EUs:

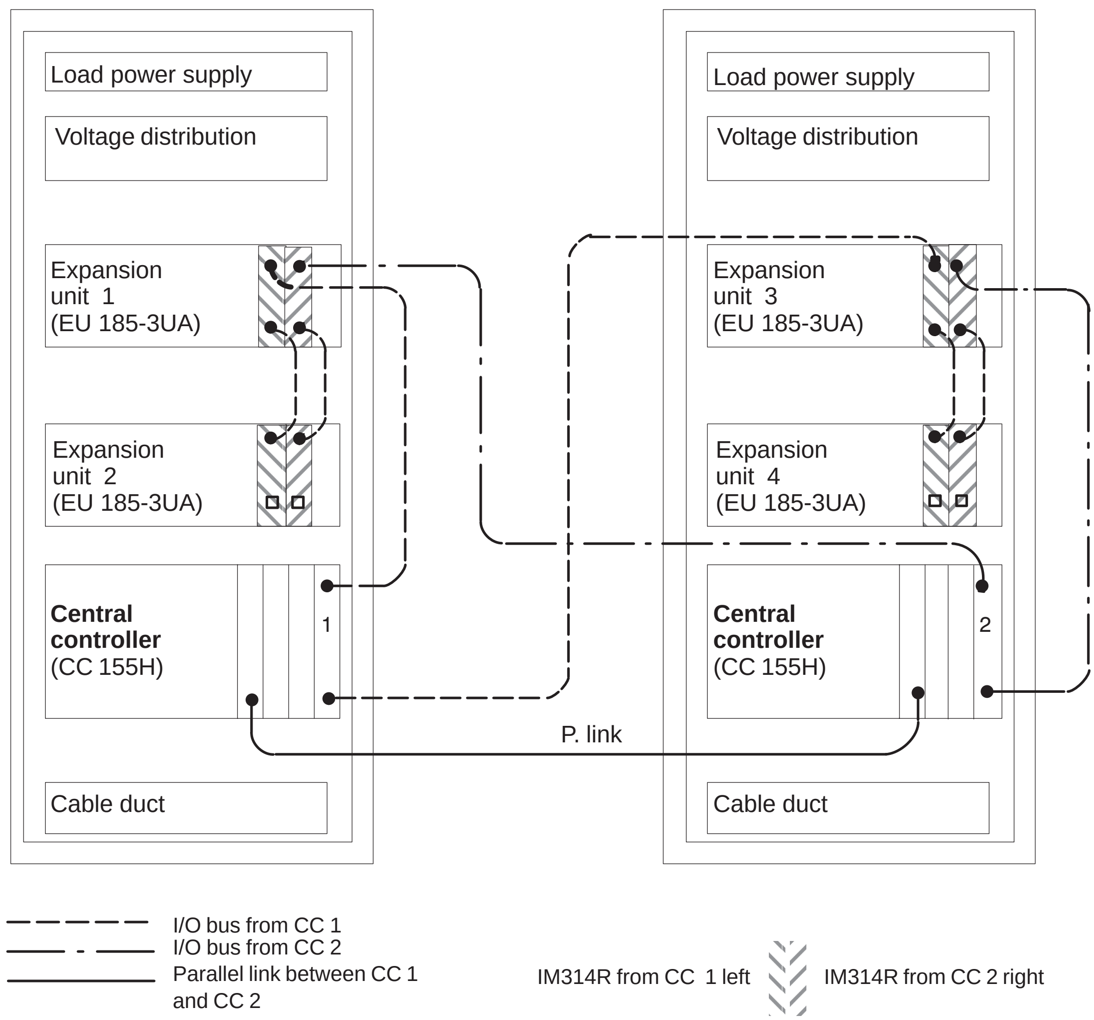


Figure 6-1 Installing an S5-155H

Recommendations and Rules for Hardware Installation

- The **central controllers'** power supply units should be fed from two separate and independent circuits.
- The power supply for the **expansion units** must have a fault-tolerant infeed (e.g. 24 V with backup batteries).

The figure below shows a possible solution:

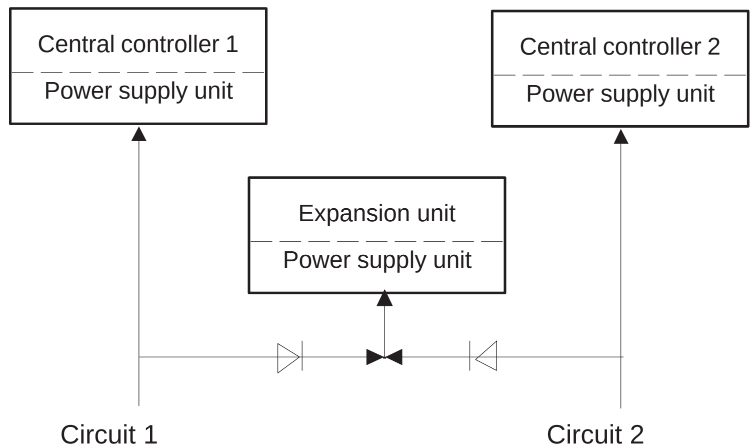


Figure 6-2 Infeed to the Power Supply Units

- It is advisable to have separate load power supplies connected to separate and independent circuits in each cabinet. They should be coupled to each other via diodes in such a way that, if one of the power supply units should fail, the other would take over. Load rating, fusing and conductor cross-section must be selected accordingly.
- If you have to run considerable lengths of connecting cables outside the cabinet, make sure the redundant cables are in separate cable ducts. This enhances fault tolerance.
- Connect all central controllers, expansion units and cabinets to an equipotential bonding conductor with a cross-sectional area of at least 10 mm^2.
- The difference in potential when linking up with cable type 721 must be < 7 V.
- To improve noise immunity, the shield of the type 721 connecting cable for the I/O buses of other EUs in a neighboring cabinet and that of the 721 cable for the IM 304/IM 314R parallel interface should be connected to the cabinet via a shield bar.
- Also make sure that the I/O buses are uniquely assigned to the central controllers and interface modules. For example:

  Central controller 1 = left interface module IM 314R

  Central controller 2 = right interface module IM 314R

Please refer to the ”Installation Guidelines” in the S5-135U/155U System Manual for additional recommendations.

955 Power Supply Block

Note

You must insert a jumper in the two 955 power supply blocks for the 135U/155U central controller to deactivate the 24 V watchdog. To do so, loosen the two screws in the power supply block, remove the entire power supply unit, and insert jumper BA-EX.

Jumper BA-EX must be open in the 955 power supplies for the expansion units. This corresponds to the factory setting.

Failure and Repair of One-Sided/ Redundant Expansion Unit

When using the IM 304/IM 314-3U... link and several expansion units in series, note that if the first expansion unit in the phase fails, all other expansion units in the phase will also fail. To increase the fault tolerance, only one expansion unit should be provided per phase.

6.2 Configuring the IM 304/IM 324R Parallel Link

Starting Point

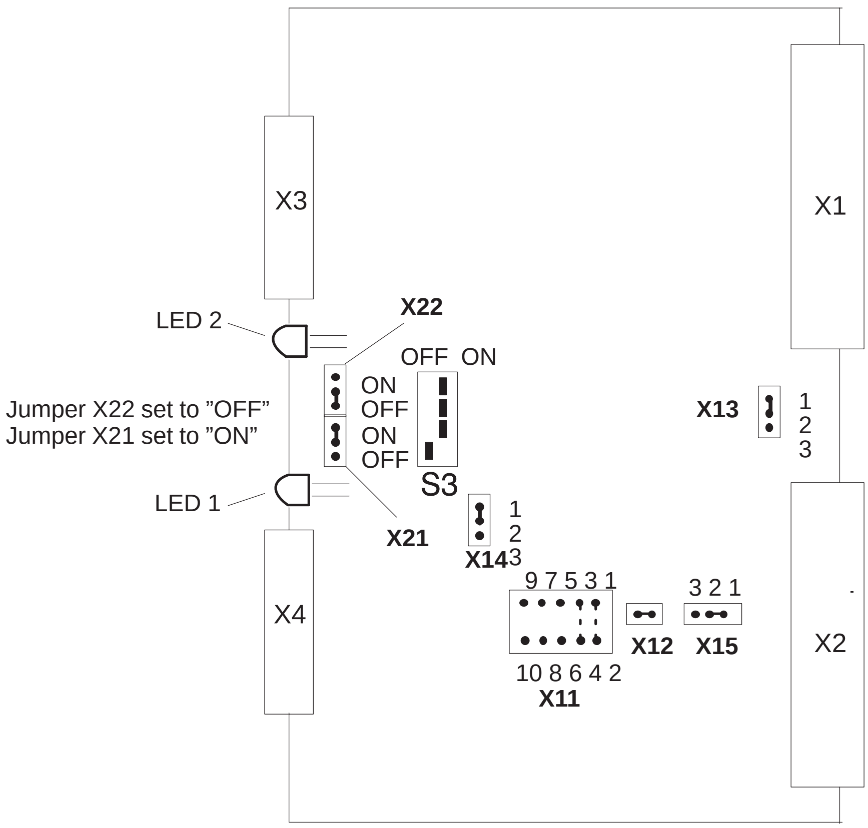
It has been assumed that a CPU 948R on which an overall reset has been performed is plugged into each subunit, and that the mains power is switched off.

Caution: Before interconnecting the two subunits via the IM 304/ IM 324R interface modules, check the jumper settings on the IM 304.

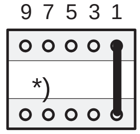
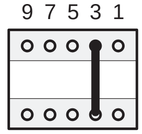
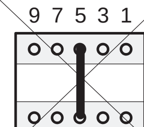
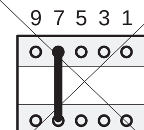
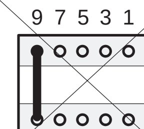
Jumper Settings on the IM 304

Jumper settings on the 6ES5304-3UB... module for a CC-to-CC parallel link via the IM 304 and IM 324R interface modules.

Caution: The IM 304 contains electrostatically sensitive components.



X11: Adaption to different cable lengths

	Jumper plug X11				
Jumper position	9 7 5 3 1  10 8 6 4 2	9 7 5 3 1  10 8 6 4 2	9 7 5 3 1  10 8 6 4 2	9 7 5 3 1  10 8 6 4 2	9 7 5 3 1  10 8 6 4 2
Cable length	Max. 10 m	10 to 100 m			

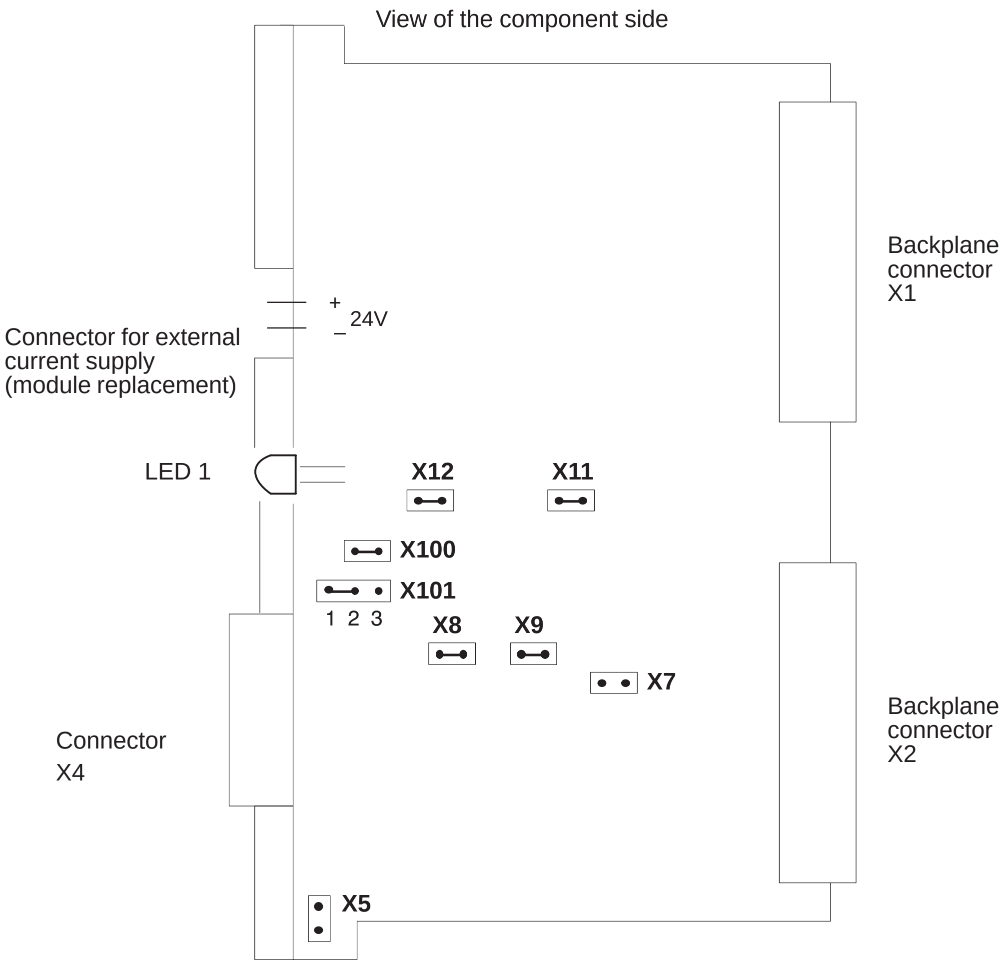
*) This setting is permissible only for the IM 304 - IM 324R link in the S5-155H. The length of the link to interface X4 determines the position of jumper X11.

Figure 6-3 Jumper Settings on the 6ES5 304-3UB** Module

IM 324R Interface Module

The IM 324R is required to establish a symmetrical 16-bit wide address/data link to a common dual-port RAM. The frontplate (lower half) is equipped with a connector for the symmetrical cable. Another connector on the top half of the frontplate is for changing modules during operation. It is used to connect an external voltage source with safe electrical isolation to VDE0160. The voltage range and current range data can be found under Technical Specifications (Section 11.2).

Caution: The IM 324R contains electrostatically sensitive components.



X101/1-2: The jumper configuration must include this jumper (distinguishes between an S5-115H and an S5-155H)

Figure 6-4 IM 324R Jumper Settings (Factory Settings)

1. Plug the IM 304/IM 324R modules into slot 131 in each subunit and connect them with a 6ES5 721-xxx cable.
2. Put the two PLCs into operation successively:

   Refer to Section 3.2 ("CPU 948R Installation and Startup Procedures").

   The green LED on the IM 324R must show a steady light (if this is **not** the case, then the IM 324R is defective).

   This allows you to operate the S5-155H in its minimum configuration:

   One subunit enters the RUN mode as master upon completion of the self-test; the RUN LED shows a steady light. The RUN LED on the other subunit flashes, showing that it is the standby.

6.3 Configuring One-Sided I/Os and Putting Them Into Operation

Starting Point

The two subunits are connected to one another via the parallel link. The CPUs have been reset (overall reset). The mains power is switched off.

- Plug the input, output or CP module you want to operate in one-sided mode into either subunit A or B or into an expansion unit assigned to either subunit A or B.
- If you plug the module into an expansion unit, be sure to use a suitable interface module.

Initializing One-Sided I/Os (COM 155H)

Switch on your programmer and start the COM 155H software (on floppy or hard disk) via the S5 command interpreter or the main menu.

Proceed as follows to configure your one-sided I/Os:

1. Choose between digital and/or analog inputs/outputs or CPs in the ”I/O Configuring” form (refer to Chapter 4 of the COM 155H User’s Guide).

   Complete the screen form for each input or output byte or word and for each CP interface.

   For digital or analog inputs/outputs, first set the byte number (invoke the ”SEARCH” function and enter the byte number), then enter the relevant type number.

   Only the following types may be specified for one-sided I/Os:

   – DI: Type 1

   – DQ: Type 8

   – AI: Type 13

   – AQ: Type 18

   You must also specify the subunit (A or B).

2. For a CP in a one-sided configuration, enter the interface number first, then the type number. In this case, you would enter CP Type 24.

   Specify the subunit to which the CP is assigned.

3. Press <RETURN> after each entry.

4. Connect your programmer to subunit A or B (Power ON). The CPUs’ mode selectors are set to ”STOP”.

5. You must now transfer your configuring data to the PLC.

Putting One-Sided I/Os into Operation

Proceed as follows:

1. Set the mode selector switch of the subunit to which the one-sided I/Os are assigned to RUN.
2. Select ”H-ERROR” in COM 155H’s basic ”DIAGNOSTICS” form. Read any entries you find there, and rectify the problems with the aid of your manual.
3. When all errors have been rectified, set the subunit back to STOP.
4. Now set the other subunit to RUN and proceed as described above. When you have once again rectified all errors, switch both CPUs to STOP and load your STEP 5 program into one of the subunits.
5. Now, configure the DB/DX numbers for your STEP 5 program and transfer DX1 to one of the subunits.
6. Execute a cold restart on that subunit.
   Following completion of the self-test (RUN LED and STOP LED both show a steady light), this subunit will enter the RUN mode as master (the RUN LED shows a steady light).
7. Execute a cold restart on the other subunit. The subunit links up to the master, receives the user program from the master, and, after completing the self-test and going through the updating procedures, it enters the RUN mode as standby (the RUN LED flashes).

6.4 Configuring Switched I/Os and Putting Them Into Operation

Starting Point

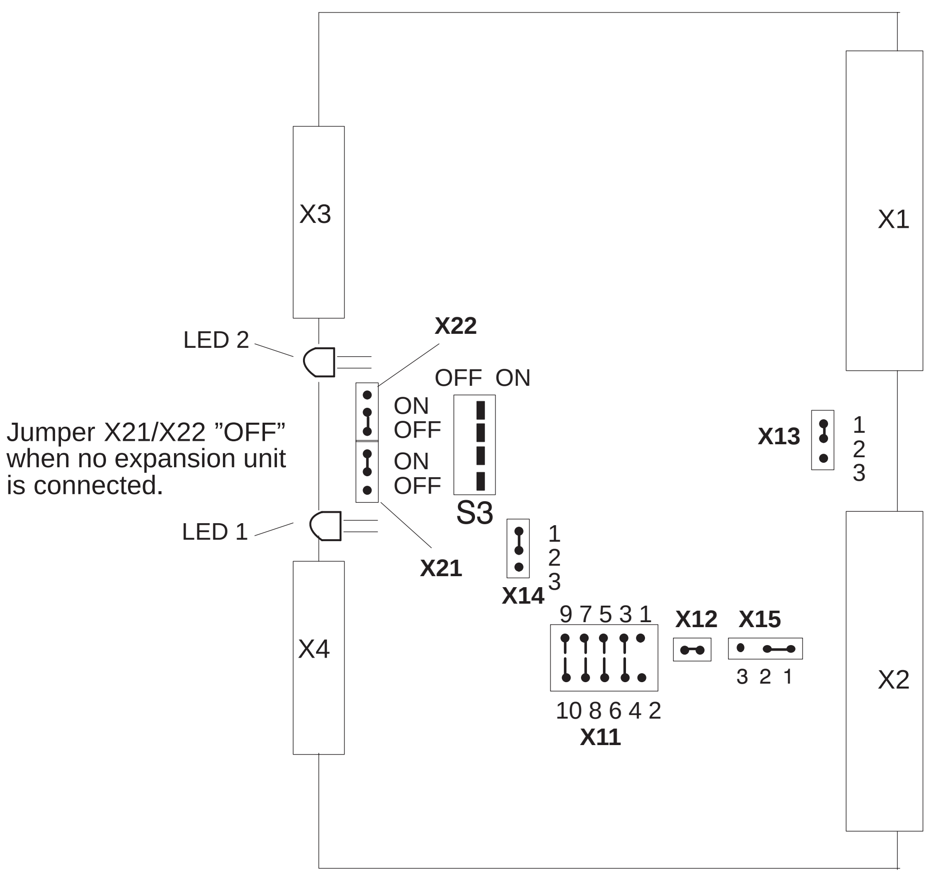
An I/O module in an EU 185 is to be operated as a switched I/O (an I/O which can be switched from bus to bus).

The expansion unit is connected symmetrically to the two subunits via an IM 304/IM 314R interface module.

1. First, check the jumper settings on the modules.
2. Plug an IM 304 into one of the last four slots in subunit A and subunit B.
3. Plug an IM 314R into slots 145 and 156 of the EU 185.

Jumper Settings on the IM 304

Jumper settings on a 6ES5304-3UB... module with a symmetrical CC-EU link via IM 304/IM 314R.



X11: Adaptation to different cable lengths

	Jumper plug X11				
Jumper position	9 7 5 3 1 *) 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2
Cable length		1 to 100 m	100 to 250 m	250 to 450 m	450 to 600 m

*) These settings are permissible for the IM 304 - IM 324R link in the S5-155H only.
The longest link to interface X3 or X4 determines the position of jumper X11.

Figure 6-5 Jumper Settings on the 6ES5 304-3UB... Module

IM 314R Interface Module

Caution: The IM 314R contains electrostatically sensitive components.

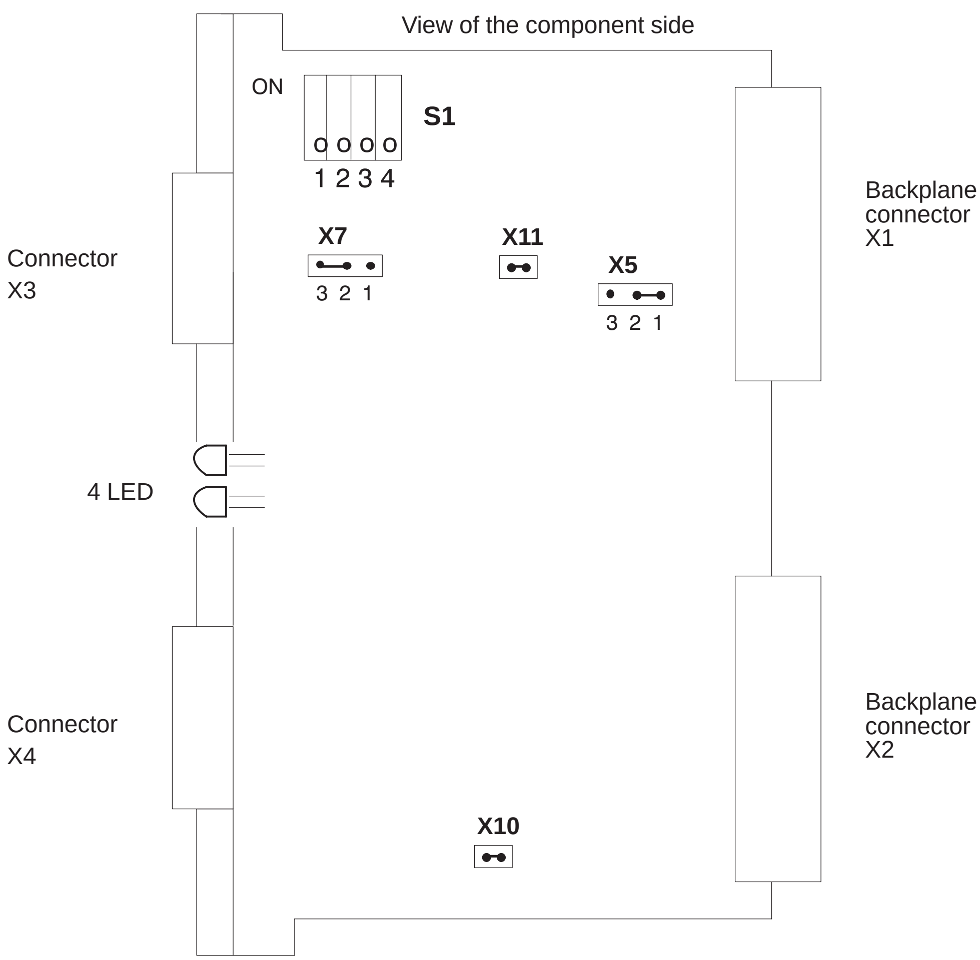


Figure 6-6 Jumper Settings on the IM 314R

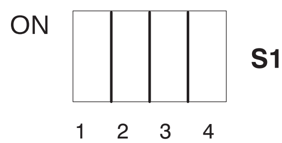
X3: Connector for the 721 cable coming directly from the subunit's IM 304 or, if several EUs are used, from the preceding IM 314R.

X4: Connector for the 721 cable to the next IM 314R or, if this is the last IM 314R on the bus, for the 760-0HA11 terminating-resistor connector.

Interfaces X3 and X4 are galvanically linked; even if the power supply to the EU 185 containing the IM 314R should fail, the bus connection remains fully intact.

Setting the EU Number

The number of the expansion unit must be set on switch S1, whereby the same EU number must be set for both IM 314Rs (you must specify a block number (see below) for this EU number during your I/O configuring session with COM 155H).



x = Switch ON
o = Switch OFF

1	2	3	4	EU No.:
o	o	o	o	00
x	o	o	o	01
o	x	o	o	02
x	x	o	o	03
o	o	x	o	04
x	o	x	o	05
o	x	x	o	06
x	x	x	o	07
o	o	o	x	08
x	o	o	x	09
o	x	o	x	10
x	x	o	x	11
o	o	x	x	12
x	o	x	x	13
o	x	x	x	14
x	x	x	x	15

LEDs on the Frontplate

The IM 314R's frontplate is equipped with four LEDs:

- The green ”F” LED lights to indicate ”Master” status
- The red ”T” LED lights to indicate ”Test”
- The red ”BF” LED lights when there is a malfunction, or when the CC stops
- The yellow ”R” LED lights to indicate ”Standby” and ”Ready to take control”

Table 6-1 LEDs on the IM 314R Frontplate

F	T	R	BF	Operational status
–	–	–	ON	CC at STOP or failed or standby is restarting
ON	ON	–	–	Master is restarting
ON	–	–	–	Master is in RUN mode
–	–	ON	–	Standby is in RUN mode
–	ON	–	–	EU not configured and associated CC is in RUN mode
–	–	–	–	Not configured and EU power OFF/ON

Command Output Disable (BASP) Signal

The IM 314R disables the expansion unit's digital outputs (BASP signal) in the following situations:

- When both subunits generate a BASP signal
- When the IM 314R is in ”Test” mode
- When both subunits are switch off or when both of an EU's I/O buses are defective

The IM 314R cannot access the EU bus as long as the EU BASP signal is present.

- Plug both IM 314Rs into the EU (slots 145 and 156). Insert the 721 cable from the subunit's IM 304 into the upper front connector X3 on the IM 314R. Connector X4 is for the 760-0HA11 terminating resistor.

Initializing Switched I/Os (COM H)

The following parameters are required to configure your switched I/Os:

1. In COM 155H's ”IM 314R” form, specify the I/O area for your EU numbers (must be identical to the setting on the IM 314R).

   This is done by entering a block number. Example:

   ”I/O area for EU No. 5: O Address area FF000H to FF0FFH”

2. Press <RETURN> after each entry.

3. Specify whether you want to operate digital and/or analog inputs/outputs or CPs/IPs in Switched mode by making the appropriate entry in COM 155H's basic ”Configuration of the I/Os” form.

   Fill out a form for each input or output byte or word and for each CP/IP interface.

   For digital or analog inputs/outputs, first set the byte number (invoke the ”SEARCH” function, then enter the byte number), then enter the type number.

   The following types may be used as switched I/Os:

   – DI Type 2
   – DQ Type 9
   – AI Type 14
   – AQ Type 19

4. For a switched CP or IP, first enter the interface number, then the type number. In this case, that would be CP/IP Type 25.
5. Press <RETURN> after each entry.
6. Transfer your configuring data to the PLC as described in the section dealing with one-sided I/Os (COM 155H ”System Handling” form).

Putting Switched I/Os into Operation

The programmer must be interfaced to either subunit A or B (power ON), and the mode selectors on both CPUs must be set to ”STOP”. Proceed as follows:

1. Set subunit A to RUN.
2. Load the error DB from the PLC into the programmer and read any entries you find there (screen COM 155H's basic ”DIAGNOSTICS” form, then call the ”H ERRORS” submenu). Rectify any errors you find with the help of your manual.
3. Switch subunit A back to STOP.
4. Repeat for subunit B.
5. Now configure the DB/DX numbers in your STEP 5 program using COM 155H's ”TRAFDAT” form.
6. When all errors have been rectified, load your STEP 5 program into one of the subunits.
7. After you have loaded the complete DX 1 configuring data block into the PLC, execute a cold restart on both subunits. Subunits A and B will then enter the RUN mode, one as master, the other as standby (the master's RUN LED will show a steady light, the standby's RUN LED will flash).

6.5 Configuring Redundant I/Os and Putting Them Into Operation

Starting Point

You must have two of every module you want to operate in a redundant configuration. One of the modules is plugged into a permissible slot in subunit A, or into an EU of subunit A, the other into subunit B, or into an EU of subunit B. The two modules must have the same address in both subunits.

The subunits are connected to each other via an IM 304/IM 324R parallel link. Each subunit has its own CPU 948R, both of which are reset (overall reset). Both subunits are at POWER OFF, and both are equipped with the same I/O module.

Initializing Redundant I/Os (COM H)

The following parameters are required to configure your redundant I/Os:

1. You must make the following entries in COM H's "Initialize operating system" form:
   - Standard discrepancy time
   - Readback delay
   - IB 0 as redundant interrupt DI byte (yes or no)
2. When you have entered all parameters, press <RETURN>.
3. Specify in COM 155H's basic "Configuration of the I/Os" form whether you want to configure digital or analog I/Os or CPs.
4. Fill in a form for each redundant input or output and for each redundant CP:

   For digital or analog inputs/outputs, specify the byte number first ("SEARCH" function: Enter byte number), then enter the Type number.

   Only the following types can be used as redundant I/Os:
   - DI Types 3 and 4
   - DQ Types 10 and 11
   - AI Types 15 and 16
   - AQ Types 20 and 21
5. Fill out the right field in the bottom half of the screen in each form by making the following entries:

   Redundant DIs
   - An L-DI
   - An L-DQ

     $\}$ for DIs **with** error locating facility
   - Discrepancy times for the individual DI bits (confirm or change)

Redundant DQs

– An L-DI
– An L-DQ

for DQs **with** error locating facility

– A Readback DI
– Type specification for the R-DI (one-sided in subunit A or B, switched in the P or O I/O area)

Redundant AIs

– The absolute discrepancy value
– The relative discrepancy value
– The preferred discrepancy value for an AI
– The lower limit of the analog value
– The upper limit of the analog value
– The discrepancy time (confirm or change)

Redundant AQs

– An L-DQ for AQs with error locating facility
– An R-AI
– The absolute discrepancy value
– The discrepancy time (confirm or change)
– The number of updates within the discrepancy time

6. Press <RETURN> after completing the configuration of the I/O.

Putting Redundant I/Os into Operation

The programmer is connected to subunit A or B (power ON). The mode selector switches on both CPUs are at ”STOP”.

1. Transfer your configuring data to the PLC as described in the section on one-sided I/Os (COM 155H’s basic ”System Handling” form).
2. Set subunit A to RUN.
3. Load the error DB from the PLC into the programmer and read any entries you find (COM 155H’s basic ”Diagnostics” form, ”H ERRORS” submenu). Rectify any errors you find with the help of your manual.
4. Switch subunit A back to STOP.
5. Repeat the above for subunit B.
6. Now configure the DB/DX numbers for your STEP 5 program in the ”TRAFDAT” form.
7. When all errors have been rectified, load your STEP 5 program into the S5-155H.
8. When the complete DX 1 configuring data block has been loaded into the PLC, execute a cold restart on both subunits. Subunits A and B then enter the RUN mode, one as the master, the other as standby (the master’s RUN LED will show a steady light, the standby’s RUN LED will flash).

Note:
To document your configuring data on paper, have COM 155H print an overview (do so by invoking the ”Print” menu in the ”System Handling” form).

6.6 S5-155H Responses to Faults/Errors

Sample Program

The example below illustrates how the S5-155H responds to a fault.

FB 37 scans the newest error block for error code YY. If this error/fault is present, the controller can respond accordingly.

STL	Explanation
OB 37	
SEGMENT 1	
:JU FB37 NAME :ERR–EVAL :BE	

STL	Explanation
FB 37	
SEGMENT 1 0000	
NAME :ERR–EVAL	
0005 :MBA	**Address of error DB**
0006 :LRW +1	**Pointer to current error block**
0008 :+D	
0009 :MAB	
000A :LRW +0	**Load –**
000C :L KB 255	**error code**
000D :AW	
000E :L KB YY	**Error code YY**
000F :!=F	**?**
0010 :JC= M001	
0011 :JU =BE	
0012 M001 :	**Program the response**
0013 :	**to error code YY here**
0014 :	
0015 BE :	
0016 :BE	

7 Time Characteristics of the S5-155H

The S5-155H programmable controller's dynamic response differs in a number of ways from that of the S5-155U. This applies to

- Statement execution times
- System program runtimes
- Restart time
- Standby activation
- Function blocks
- On-line programmer functions

7.1 Statement Execution Times for the S5-155H

General Remarks

The majority of STEP 5 statements take the same amount of time to execute in the S5-155H as they do in the S5-155U. The STEP 5 statements which require master-standby synchronization, however, are an exception.

- Direct I/O access operations to a
  - one-sided/two-channel (1-out-of-2) DI approx. 300 µs
  - three-channel (1-out-of-3) DI approx. 400 µs
  - one-sided/two-channel (1-out-of-2) DQ approx. 200 µs
- Direct access to switched I/Os

Statement Execution Times for Access to Switched I/Os

Note:

These execution times depend on

- the length of the cables and
- the modules used (acknowledgement time).

7.2 System Program Runtimes

Increased S5-155H Runtimes

The 155H system program's runtime is longer by the value DT than the 155U system runtime; DT is composed of the following:

- **Self-test slice: T1**

  The self-test slice time can be configured with COM H in increments of 2 ms.

- **I/O test and process image update: T2**

  The purpose of this test is to unify and monitor redundant I/Os, and is executed for those modules only. The increase in the scan time for updating the process image of redundant I/Os is as follows:

  – Per switched digital input byte: 25 µs
  – Per one-sided digital input byte: approx. 40 µs
  – Per two-channel digital input byte: approx. 60 µs
  – Per three-channel digital input byte: approx. 120 µs
  – Per switched digital output byte: 5 µs
  – Per one-sided digital output byte: approx. 20 µs
  – Per two-channel digital output byte: approx. 40 µs
  – Per interprocessor communication input flag: 25 µs
  – Per interprocessor communication output flag: 5 µs
  – Basic load 2 ms

- **155H system program: T3**

  An almost constant time increase of approximately 5 ms per cycle is needed for bus management, link requests, EU failures and the like.

  In a best-case situation, the scan time increase as compared with the S5-155U is thus

  DT = T1 + T2 + T3

S5-155H Restart Time

The S5-155H restart routine includes a full-scale self-test, thus significantly increasing the S5-155H's restart time as compared with the S5-155U.

The restart time (TA) is as follows:

- For CPUs with 640 Kbytes approx. 8 s
- For CPUs with 1664 Kbytes approx. 20 s

7.3 Dynamic Response on Standby Activation

”Activation” Time

During standby activation, the self-test is inhibited so as not to load the cycle even more. The standby controller is activated in two phases:

- **Phase 1**

Updating of the user program and the constants (see Section 3.3).

During this phase, the self-test is inhibited so as not to load the cycle even more.

Time needed for phase 1:

– With CPU 948R I: 180 PLC cycles

– With CPU 948R II: 436 PLC cycles

– With CPU 948RL: 36 PLC cycles

- **Phase 2**

Updating of the dynamic data

The amount of time this phase adds to the cycle (on a one-shot basis only, however) depends on several factors:

– Transfer time for flags, counters, timers and RS data

This is a constant value: T7 = approx. 25 ms

– Transfer time for configured data blocks

This is an approximate value: T8 = approx. 4 µs / word

The one-shot increase in the scan time caused by standby activation procedures is:

TK = T7 + T8

7.4 Interrupt Response Time

The minimum interrupt response time allowed by the 155H system program is determined by

- the self-test (**Ts**)
- the I/O test (**Te, Ta** and **Tg**).

The time value is calculated from the maximum value for the following four formulas:

1. Ts = 2 ms
2. Te = (n $*$ T-DIr) + (m $*$ T-DIe) + (l $*$ T-DI3) + 1.0 ms
3. Ta = (p $*$ T-DQr) + (q $*$ T-DQe) + 0.5 ms
4. Tg = r $*$ T-DIg

where l, n, m, p, q, r = number of bytes in the process image

T-DI3	=	120	µs	Time for three-channel DIs
T-DIr	=	60	µs	Time for redundant DIs
T-DIe	=	40	µs	Time for single-sided DIs
T-DIg	=	25	µs	Time for switched DIs
T-DQr	=	40	µs	Time for redundant DQs
T-DQe	=	20	µs	Time for single-sided DQs

Normally, the interrupt response time is thus 5 ms, but can increase to as much as 20 ms (128 three-channel DI bytes).

S5-155H Error Diagnostics 8

This chapter discusses all error diagnostics facilities for the S5-155H programmable controller. It describes in detail the structure of the error data block, the block in which the 155H system program enters all errors that are detected, and it also provides a list of error numbers and explains what these codes mean. In addition, it describes in detail the H flag doubleword, error OB 37, and the structure of the H flag word.

8.1 Troubleshooting and Error Handling in the S5-155H

All troubleshooting, error diagnostics and error handling facilities provided for the S5-155U are also available to you in the S5-155H. In addition, the S5-155H provides a number of different options for error identification and error handling. Table 8-1 contains an overview of available facilities.

Automatic error identification and error locating facilities for the S5-155H function better when **no** Block End (BE) operation is programmed in OB 26.

Error Recovery

S5-155H-specific error messages

- The causes of errors reported via COM H must be eliminated in ascending order so that secondary error reports do not make troubleshooting more difficult.
- The elimination of the causes of errors in ascending order is important in an S5-155H system for the following reason:

  A number of errors (PEU, for instance) would cause the S5-155U to stop, but would ”only” be reported in an S5-155H system so as not to jeopardize fault tolerance unnecessarily; yet these errors are also critical and must be eliminated as soon as possible.

Table 8-1 Troubleshooting and Error Handling in the S5-155H

	PLC	Brief Description	Error Diag-nostics	Error Hand-ling
Fault LED	155U + 155H	Specific combinations of the STOP/SYSFAULT/INIT/ADF/QVZ and ZYK LEDs on the CPU's frontplate are indicative of specific causes of interruption.	X	
Control bits	155U + 155H	These bits provide information on the current operating status, and report all errors which have occurred up to that point.	X	
ISTACK	155U + 155H	Contains the point of interruption, the bits currently set, the contents of the accumulators, and the reason for the interrupt.	X	
BSTACK	155U + 155H	Lists all blocks which were invoked prior to the STOP but not yet completely processed.	X	
COM 155H ”DIAGNOS TICS”	155H only	You can read out all errors which have occurred in the system and user programs up to that point, including point of interruption and time stamp, with the programmer (error DB is output in plaintext).	X	
Error DB	155H only	The 155H system program uses this block to enter all errors detected during the self-test and during program processing, complete with error class, error no. and the date. The block also contains a static error image of all inputs and outputs and all CP/IP interfaces.	X	
Error FBs 19 to 34	155U + 155H	In some cases, the system program invokes the relevant OBs before going into STOP; you can program appropriate responses to errors in these OBs.		X
Error OB 37	155H only	The system program invokes OB 37 each time it detects an error which requires an entry in the error OB; you can program an appropriate response in this OB.		X
H flag doubleword	155H only	This flag doubleword (FD) provides data for the time stamp in the error DB. You can use this flag doubleword to program identifiers helpful in diagnosing errors.	X	
H flag word	155H only	The H flag word's status byte contains important information on the PLC status. You can initiate specific requests in the STEP 5 program via the control byte.	X	

8.2 Error Data Block (E-DB)

Entries in the Error DB

You must choose a number between 3 and 255 for this block when you are configuring the system (COM 155H):

:

H error DB number (3 to 255): 10

:

The 155H system program than generates the error DB automatically in the RESTART routine, normally with a length of 2 Kwords.

The following entries are of particular importance should an error occur:

- **Entry in the error image**

A static error image is stored in the error DB which is organized in such a way that each repairable unit (I/Os, CPs, IPs, IM 314R EU) is assigned its own bit. These bits are arranged in ascending order of addresses or interface numbers. A distinction is also made between repairable units assigned to subunit A and those assigned to subunit B.

All bits in the image are initially set to ”0”. When the system program detects an error, the appropriate bit is set to ”1”.

You will find an example under ”DW 6 to DW 279: Static Error Image”.

- **Entry in the status word**

Each error is also assigned to a specific error group (”Parallel link errors”, ”I/O errors”, and so on). One bit is reserved in the status word for each group. Each of these group error bits remains at ”1” as long as the error image shows at least one error belonging to that group. The error groups assigned bits in the status word are listed under ”Status Word (DW 3)”.

- **Entry in the error record**

Each error detected by the system program is entered in a so-called error record. An error record comprises eight data words. The exact format of an error record is described in detail under ”Structure of an Error Record”.

As a rule, every error detected is entered only **once** in the data block.

IMPORTANT

Each time an error is entered in the error DB, the 155H system program invokes error OB 37; you can evaluate the error and program an appropriate response in this OB.

Structure of the Error DB

DW	15 High 8		7 Low 0		
DW 0	Error counter				
DW 1	Write pointer				
DW 2	Unassigned				
DW 3	Status word				
DW 4	Address of the 1st error record (400)				
DW 5	Reserved				
DW 6 ..13	Static error image	DI	0..127	Subunit A	
DW 14 ..21	Static error image	DI/AI	128..255	Subunit A	
DW 22 ..29	Static error image	DI	0..127	Subunit B	
DW 30 ..37	Static error image	DI/AI	128..255	Subunit B	
DW 38 ..45	Static error image	DI	0..127	Switched	
DW 46 ..53	Static error image	DI/AI	128..255	Switched	
DW 54 ..69	Error image of the O area	I	0..255	Switched	
DW 70 ..85	Error image of the IPC flags	I	0..255	Switched	
DW 86 ..93	Static error image	DQ	0..127	Subunit A	
DW 94 ..101	Static error image	DQ/AQ	128..255	Subunit A	
DW 102 ..109	Static error image	DQ	0..127	Subunit B	
DW 110 ..117	Static error image	DQ/AQ	128..255	Subunit B	
DW 118 ..125	Static error image	DQ	0..127	Switched	
DW 126 ..133	Static error image	DQ/AQ	128..255	Switched	
DW 134 ..149	Error image of the O area	Q	0..255	Switched	
DW 150 ..165	Error image of the IPC flag	Q	0..255	Switched	
DW 166 ..181	CP/IP interface error image		0..255	Subunit A	
DW 182 ..197	CP/IP interface error image		0..255	Subunit B	
DW 198 ..213	CP/IP interface error image		0..255	Switched	
DW 214	Static error image of EU (IM 314R) Subunit A				
DW 215	Static error image of EU (IM 314R) Subunit B				
DW 216 ..231	Static error image	DI/AI	0..255	Subunit A	Q
DW 232 ..247	Static error image	DI/AI	0..255	Subunit B	Q
DW 248 ..263	Static error image	DQ/AQ	0..255	Subunit A	Q
DW 264 ..279	Static error image	DQ/AQ	0..255	Subunit B	Q
DW 280 ..399	Reserved				
DW 400	E. location	E. class	Error code		1st error record
	Additional info 1				
	Additional info 2				
	Additonal info 3				
	Prog. number		Ascending number		
	Time stamp, second (BCD)		Time stamp, minute (BCD)		
	Time stamp, hour (BCD)		Time stamp, day (BCD)		
	Time stamp, month (BCD)		Time stamp, year (BCD)		
DW 408	2nd error record				
	and additional error records				

Data Word DW 0: 'Error Counter'

All errors are tallied in this counter. The counter stops when it reaches 32767. It is reset during a cold restart and on depassivation.

Data Word DW 1: 'Write Pointer'

The write pointer always points to the beginning (the first data word) of the current error record. The current error record is the record in which the most recent error was entered. The write pointer is '0' as long as the error DB contains no errors.

Data Word DW 2: Unassigned

This data word is available to the user.

Data Word DW 3: 'Status Word'

H system errors can be divided into specific groups. Each bit in the status word is reserved for one of these groups, and stays set to '1' as long as the error image shows at least one error for that group.

Data word DW 3 in the error DB is reserved as status word; this word has the following format:

2^{15} … 2^{0}

UMK		MLD	GER	HW	SYS	HAN	PRJ	CP	PER	PEB	PK	ANW		CPU	

2^0	:		Unassigned
2^1	:	**CPU**	Group error bit for CPU errors
2^2	:		Unassigned
2^3	:	**ANW**	Group error bit for user memory errors (memory card)
2^4	:	**PK**	Group error bit for parallel link errors (IM 304 - IM 324R)
2^5	:	**PEB**	Group error bit for I/O bus errors (IM 304 - IM 314R)
2^6	:	**PER**	Group error bit for I/O errors
2^7	:	**CP**	Group error bit for CP/IP errors (page area)
2^8	:	**PRJ**	Group error bit for configuring errors
2^9	:	**HAN**	Group error bit for data handling errors
2^{10}	:	**SYS**	Group error bit for system errors
2^{11}	:	**HW**	Group error bit for hardware errors (defective CPU, for example)
2^{12}	:	**GER**	Group error bit for device errors (EU power OFF, for example)
2^{13}	:	**MLD**	Message
2^{14}	:		Unassigned
2^{15}	:	**UMK**	'Error DB full' identifier

Bit 15 : 'Error DB full' identifier

This bit is set when all of the data block's error records are full and subsequent entries start again with the first error record (ring method).

DW 4: Address of the 1st error record

DW 4 contains the start address of the first error record in the error DB: Data word number ”400”.

DW 5: Reserved

DW 6 to DW 279: Static error image

The image in these data words shows which I/Os or CP/IP interfaces are defective.

Example: Static error image of the digital outputs (DQs) assigned to subunit B.

	2^{15}															2^{0}
DW 102	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DW 103	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DW 109	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112

Digital outputs DQ 30 and DQ 22 in subunit B are bad when bits 14 and 16 in data word DW 103 are ”1”.

If more than one timeout (QVZ) occurs during updating of the process image (or of the interprocessor communication flags), the byte number with the lowest address is entered **immediately** ; the remaining byte numbers are entered within the next 32 PLC cycles.

Beginning DW 400: Error records

The error records begin in data word DW 400. Each record comprises eight data words.

An error record is filled out for each new error the system program detects during the cycle. When all error records are full, the next error is entered in the first error record (which begins with DW 400) and the ’Error DB full’ identifier (bit 15 of the status word) is set to ”1”.

If several errors are detected during the transfer of the process image to switched I/Os, only one error record entry is made. The other bad addresses are entered in the error image within the next 32 PLC cycles.

Structure of an Error Record

15		8 7	0
E. location	E. class	Error number	
Additional info 1			
Additional info 2			
Additional info 3			
Prog. number		Ascending number	
Time stamp, second (BCD)		Time stamp, minute (BCD)	
Time stamp, hour (BCD)		Time stamp, day (BCD)	
Time stamp, month (BCD)		Time stamp, year (BCD)	

Error Location and Error Class

7	6	5	4	3	2	1	0
B	A	RES	MA		PAS	WST	HST

Bits 0 to 3 contain the error response (default is the standard response):

Bit 0 :	**HST**	Hard STOP (CPU error, for example)
Bit 1 :	**WST**	Soft STOP (signature error in user program, etc., for example)
Bit 2 :	**PAS**	Passivation (on timeout, discrepancy error, etc., for example)
Bit 3 :		Unassigned
Bits 0 to 3=0:	**MESSAGE**	

7	6	5	4	3	2	1	0
B	A	RES	MA		PAS	WST	HST

Bits 4 to 7 describe the error location:

Bit 4 : **MA** Error occurred in master controller

Bit 5 : **RES** Error occurred in standby controller

Bit 6 : **A** Error occurred in subunit A

Bit 7 : **B** Error occurred in subunit B

If, for example, bits 4 and 7 are ”1”, it is apparent that the error occurred in subunit B, which is currently controlling the process as master.

This produces the following possible combinations:

Bit 6/7 and bit 4/5	= 1: Error occurred in one of the subunits
Bits 6 and 7	= 1: Error occurred in both subunits
Bit 5	= 1: Error occurred in the IM304/IM324R parallel link
Bit 4	= 1: Error occurred in the switched I/Os
Bits 4 and 5	= 1: Comparison error (the Error Search Mode is entered)

Error Number

The error number is a consecutive number between 1 and 255; each error number is assigned to a plaintext.

Example: CPU fault, DI module fault, CP/IP fault, etc. (refer to the table ”Structure of an Error Record” on the previous page).

Error Location (Additional Information)

The error location informs the user where a specific error has occurred. The information is contained in up to three data words.

Example: Module address, interface no. etc.
(refer to the table ”Structure of an Error Record”)

Program Number and Consecutive Number for the Service Specialist

The number of the system program OB to be executed when an error occurs and a consecutive number (= OB subtask) are entered here.

Time Stamp

The current date and time (from the CPU's system data area) are entered here in the event of an error.

Second (tens)	Second (units)	Minute (tens)	Minute (units)
Hour (tens)	Hour (units)	Day (tens)	Day (units)
Month (tens)	Month (units)	Year (tens)	Year (units)

You can also use the first two data words to store the contents of a specific flag doubleword whose number you specify with COM 155H. Refer also to ”H Flag Doubleword” in Section 8.3.

Note

When several timeouts occur in the switched I/Os during updating of those I/Os (or of the IPC flags), only **one**, i.e., the one with the lowest byte number, is entered in the error record.

The other byte numbers are entered in the static error image.

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
2	CPU 948R failure (MPU)	Hardware fault on CPU or CC power supply unit's load voltage monitor not disabled	Check the jumper setting of the load voltage or replace the CPU 948R or phone for maintenance.
3	Message from CPU 948R	System error	
4	Clock error (CPU 948R) or battery failure		
7	System error		Phone for maintenance.
8	BASP error		Replace the CPU 948R.
10	I/Os not connected or not ready	I/Os not ready. An EU or I/O bus (721 I/O cable) has failed. If a switched EU has failed, consult the static error image.	

Table 8-2 Error List

Error No.	Description	Cause of Error	Remedy
11	Standby failed to activate successfully	Standby stopped again while being activated. The preceding error usually indicates the reason for this error.	Examine the reason why the standby went into STOP by viewing the contents of the ISTACK and the error DB.
13	DX 1 configuring block invalid		Generate or modify DX 1 only via COM 155H.
14	DB 1 invalid. **info 1:** DB 1 ID (ref.) **info 2:** DB 1 ID (act.)		Generate or correct DB 1 via screen form.
15	Master stopped during standby activation	When the master stops during activation, the standby also stops, as the latter has not yet received the current data (flags, for instance).	
16	”Standby STOP” bit set in H flag word	User (program) has set the H flag bit for ”Standby has stopped”.	
17	I/Os ready again	This message enables you to read or log the time of a repair or to initiate depassivation.	
18	One master stopped because partner also master.	Parallel link error	
19	Old standby performs warm restart as master.	This subunit stopped as standby; other subunit was master on last system STOP. The ex-master has the current process data, but is still at STOP.	a) Always use ”Cold restart without memory”. b) If this is not possible and standby activation is not required, scan OB 37 for this error no. and set the subunit to STOP.
20	Memory module error. **info 1:** Address (page) **info 2:** Address (low)	Memory defective.	Replace CPU.
21	RAM comparison error. **info 1:** Block type/block no. **info 2:** Relative address	A user RAM location does not match in the two subunits, which is not permissible in a redundant system. Assuming there has been no hardware fault, the reason for the RAM comparison error is always one of the following user errors: a) No interrupt DB/DX specified with COM H. b) Illegal access operation to a bit or a word in the system data area (TBRS n.m., LRS n) executed (see list in Section 2.4).	The error can usually be rectified if the specified DB / DX is entered in the list of interrupt DBs/DXs with COM H (see COM H User’s Guide).

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
22	Checksum error in block. **info 1:** Sum (ref.) **info 2:** Sum (act.) **info 3:** Block type/block no.	Contents of the STEP 5 logic block (OB, PB, SB, FB, FX) illegally modified, via OUTPUT ADDR or via the user program.	STEP 5 logic blocks may be modified by the programmer (output block) or OB 124/125 to ensure that the block checksum is correctly entered in DB 0.
23	Error search without result.	Error search found no hardware errors.	Evaluate error code 21 or 24 in the error DB for additional details.
24	PIQ comparison error. **info 1:** Address (page) **info 2:** Address (low)	The PIQ is not the same in both subunits. Possible reasons: - Parallel link error - User programming error; for example, illegal access to system RAM in order to change the PIQ.	
25	Operating system EPROM failure.	Bad operating system EPROM.	Replace the CPU 948R.
26	PIQ RAM error **info 1:** Address (page) **info 2:** Address (low) **info 3:** Faulty bit no.		
27	Memory configuration incompatibility.	In a redundant system, the subunits may not have different memory configurations.	Check the SPAUS to see where the difference in the memory configuration lies and upgrade the standby accordingly. After executing an overall reset on the standby, it can be reactivated (see error no. 21 for further details).
28	System program incompatibility.	In a redundant system, the subunits may not have EPROMs with different contents.	Activating the standby when the subunits are using two different operating system versions is permissible only when the standby is the one with the newer version. Prior to activation, the COM H ”UPGRADE” parameter must be set to ”CPU 948R”. The standby can then be activated, and takes over as master. The other subunit stops and must then be upgraded.
29	Different user program code.	The subunits cannot be operated with different user memory cards (the block sequence must also be the same!).	Generate two identical memory cards and activate the first using COM 155H’s ”UPGRADE”, ”MEMCARD” function (see Chapter 9, ”Upgrading”).

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
30	Standby-master switchover due to master failure **info 1:** Instruction code **info 2:** Absolute SAC (high) **info 3:** Absolute SAC (low)	The master failed during user program processing.	
31	Standby failure. **info 1:** Instruction code **info 2:** Absolute SAC (high) **info 3:** Absolute SAC (low)	Standby controller failure during user program processing.	
32	Synchronization error (master-standby) in the user program. **info 1:** Instruction code **info 2:** Absolute SAC (high) **info 3:** Absolute SAC (low)	A subunit waited at this synchronization point until the waiting time elapsed. One reason for this error might be differences in the program scan in master and standby caused by discrepancies in DB contents.	All DBs (DXs) whose contents have been changed in an interrupt handling routine must be reconfigured as interrupt DBs/DXs.
33	Parallel link error (IM 304 / IM 324R)	IM 304, IM 324R or parallel link cable failed.	
34	Synchronization error (master-standby time) in the operating system	For maintenance purposes.	Print out the error DB, the ISTACK and the BSTACK and phone for maintenance.
35	Standby-master switchover due to master failure	Master failed while the operating system was processing.	
36	Standby failure	Standby failed while the operating system was processing.	
37	Standby-master switchover due to I/O error. **info 1:** QVZ address (page) **info 2:** QVZ address (low)	A standby-master switchover is carried out automatically in the event of a timeout (QVZ) on a switched I/O because the operating system assumes that an I/O bus has failed. The subsequent error message(s) and the static error image show what it was that failed (an EU, for instance). Any additional timeouts occurring prior to the next passivation do not cause another transfer.	Rectify the I/O error. Fault-tolerance is restricted because the master's bus failure prevents a standby-master switchover.
38	Synchronization error (master-standby location) in the user program. **info 1:** Instruction code **info 2:** Abs. address (high) **info 3:** Abs. address (low)	A subunit has recognized that its peer is waiting at another synchronization point. See error no. 32 for the cause of error and suitable recovery measures.	

Table 8-2 Error List

Error No.	Description	Cause of Error	Remedy
39	Synchronization error (master-standby location) in the operating system.	For maintenance purposes	Print out the error DB, ISTACK and BSTACK and phone for maintenance.
40	I/O bus error (IM 304 / IM 314R) **info 1:** EU number	EU power supply or IM 314R / IM 304 module or I/O bus cable failure.	Check to see if more than one error with no. 40 was entered in the same cycle. Following repairs, H flag bit DPA (depassivation) must be set.
50	Timeout (QVZ) on input module **info 1:** QVZ address **info 2:** (Instruction code)	Module fault or EU failure. Is sometimes reported together with error no. 40 or 10, which might be the cause of error.	
51	Timeout (QVZ) on output module **info 1:** QVZ address **info 2:** (Instruction code)	See error no. 50.	
52	Timeout (QVZ) when accessing IB 0 (process interrupt active) **info 1:** QVZ address **info 2:** Instruction code	See error no. 50.	
53	Timeout (QVZ) on input communication flag **info 1:** QVZ address **info 2:** Instruction code	Incorrect jumper setting on CPs/IPs or EU failure or module fault. See error no. 50.	
54	Timeout (QVZ) on output communication flag **info 1:** QVZ address **info 2:** Instruction code	See error no. 53.	
55	Configured DI byte not found (timeout) **info 1:** DI address	Configuring error or incorrect jumper setting, module fault or EU failure.	
56	Configured DQ byte not found (timeout) **info 1:** DQ address	See error no. 55.	
57	Configured AI byte not found (timeout) **info 1:** AI address	See error no. 55.	
58	Configured AQ byte not found (timeout). **info 1:** AQ address	See error no. 55.	

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
59	DQ group passivation (L-DQ or DQ error) **info 1:** DQ address	When a locating digital output (L-DQ) fails, the DQ modules assigned to it in the same subunit are passivated.	First, check to see if error code 71, 73 or 74 has been entered in the error DB.
60	DI error (stuck at ”0” or ”1”) **info 1:** Bit no. / byte no.	The DIs still do not match although the discrepancy time has elapsed. The error info includes the subunit containing the bad module.	
61	DQ error (stuck at ”0” or ”1”) **info 1:** Bit no. / byte no. **info 2:** 0: stuck at 0 1: stuck at 1	The readback digital input (R-DI) did not read back the anticipated value although the readback delay had expired.	If the same error is reported at the same time (immediately before or after) for the other controller, it is indicative of an external error. The R-DI is subsequently passivated.
62	AI error (wirebreak) **info 1:** AI address	In addition to an error bit (wirebreak, for example), this error is also reported by function block ”H-RLG:AE”.	
63	AI error (range violation) **info 1:** AI address	See error no. 62.	
64	AI error (overflow) **info 1:** AI address	See error no. 62.	
65	AI error (discrepancy error) **info 1:** AI address	See error no. 62.	
66	AQ error **info 1:** Byte no.		
68	DI error on 3-channel DI. **info 1:** Bit no. / byte no. **info 2:** 0: stuck at 0 1: stuck at 1	The DIs still do not match although the discrepancy time has elapsed. The error info specifies the side on which the problem was detected. The problem may be a wirebreak, a DI module fault or a sensor fault.	
69	Discrepancy timeout for DI bit – no signal changed. **info 1:** Bit no. / byte no.	A discrepancy error was detected on a 2-channel DI without error locating facility; the error could not yet be located. Error locating begins with the next edge change at this input.	
70	Error in locating circuit for DI. **info 1:** Bit no. / byte no. of L-DI **info 2:** Bit no. / byte no. of L-DQ **info 3:** Stuck at 0 or stuck at 1 error	This error no. is indicative of a wiring or module fault on the L-DI or L-DQ module. The error info includes the byte number and the bit number of the L-DQ and the L-DI, as the fault could be on **either**.	

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
71	Error in locating circuit for DQ. **info 1:** Bit no. / byte no. of L-DI **info 2:** Bit no. / byte no. of L-DQ **info 3:** Stuck at 0 or stuck at 1 error	See error no. 70. Error in the error locating facility for redundant DQs.	
72	Timeout (QVZ) on ”error locating DI”. **info 1:** Byte number of L-DI	L-DI module defective or failure of the EU containing the L-DI module.	
73	Timeout (QVZ) on ”error locating DQ”. **info 1:** Byte no. of L-DQ	L-DQ module defective or failure of the EU containing the L-DQ module.	
74	Stuck at 0 error of an L-DQ for redundant DQs. **info 1:** Bit no. / byte no. of the L-DQ	L-DQ bit defective or wiring fault.	
75	Readback error. **info 1:** Byte no. of R-DI **info 2:** Byte no. of associated DQ	If error 61 is reported at the same time (just before), it has priority. Error no. 75 only indicates that the R-DI is no longer in use. Otherwise, this error no. means only that there is a problem with the R-DI or the wiring.	
76	Timeout (QVZ) on readback DI. **info 1:** Byte no. of R-DI **info 2:** Byte no. of associated DQ	R-DI module defective or failure of the EU containing this R-DI.	
77	Stuck at 1 – redundant readback DI. **info 1:** Bit no. / byte no. **info 2:** Byte no. of the associated redundant DQ	The readback input detected signal state ”1” although the redundant output is supposed to output ”0”.	
78	Timeout (QVZ) in redundant readback DI. **info 1:** Byte no. causing the timeout **info 2:** Byte no. of the associated redundant DQ	Module or EU failure.	
79	Stuck at 0 in redundant readback DI or in redundant DQ. **info 1:** Bit no. / byte no. **info 2:** Byte no. of the associated redundant DQ	Output or readback input defective.	
80	CP/IP interface error. **info 1:** Interface no. (page number)	CP/IP was not configured or CP/IP acknowledges with more than one interface number.	

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
81	CP/IP does not acknowledge (timeout). **info 1:** Interface no. (page number)	CP/IP fault or failure of the EU containing the CP/IP.	
85	Input communication flag not available. **info 1:** Address (F page)	Module fault, PLC failure or configuring error. The interprocessor communication input flag configured in DB 1 does not exist. In contrast to the 155U, the 155H allows a cold restart/warm restart without IPC flag.	
86	Output communication flag not available. **info 1:** Address (F page)	See error no. 85.	
90	Cannot locate configured DB/DX. **info 1:** High: 0 = Cyc DB 1 = Cyc DX 2 = Interr. DB 3 = Interr. DX Low: DB/DX number	Configuring error. Note: This error increases the length of the activation cycle.	
91	I/O communication flag ID set more than once in DB 1. **info 1:** Illegal identifier	DB 1 not generated via screen form.	Generate DB 1 via screen form.
92	Area ID (I/O comm. flag) missing in DB 1.	See error no. 91.	
93	I/O communication flag byte no. > 255 (DB 1) **info 1:** IPC input/output flag ID **info 2:** Illegal byte number	See error no. 91.	
94	> 255 I/O communication flag bytes (DB 1). **info 1:** IPC input/output flag ID	See error no. 91.	
95	DI module not configured. **info 1:** DI address	Some of the modules being used have not been configured, or a module was incorrectly addressed or acknowledges for more than one address.	
96	DQ module not configured. **info 1:** DQ address	See error no. 95.	
97	AI module not configured. **info 1:** AI address	See error no. 95.	
98	AQ module not configured. **info 1:** AQ address	See error no. 95.	

Table 8-2 Error List

Error No.	Description	Cause of Error	Remedy
99	DB/DX not configured in TRAFDAT list. **info 1:** Low: DB/DX number High: 0 = DB, 1 = DX	This DB/DX is modified by the user program.	Check to see whether DB/DX is modified in the cyclic program or in an interrupt service routine, and configure the DB/DX in the appropriate list.
101	Prog. attempted illegal I/O access. **info 1:** Instruction code **info 2:** Abs. SAC (high) **info 3:** Abs. SAC (low)	This programming error is detected in redundant systems only, and means that one of the following was not observed: a) Block transfers to I/Os must not involve the address area for redundant/one-sided I/Os; refer to the information provided on initializing operating system parameters. b) Read access by byte to a redundant AI is not permitted; redundant AIs must be accessed by word in order to enable result-matching.	
105	GDB error in the user program.	The interval required between block deletion and block generation was not observed.	
110	Internal CPU 948R communication error.	Interrupts disabled too long.	
121	CPU 948R data bus error.	CPU 948R hardware fault.	Replace CPU 948R.
122	CPU 948R addr. bus error.	CPU 948R hardware fault.	Replace CPU 948R.
123	CPU 948R EPROM error.	CPU 948R hardware fault.	Replace CPU 948R.
124	CPU 948R RAM error.	CPU 948R hardware fault.	Replace CPU 948R.
125	CPU 948R CPU error.	CPU 948R hardware fault.	Replace CPU 948R.
130	Timeout (QVZ) on 3rd DI channel **info 1:** Byte no. reporting the timeout. **info 2:** No. of the associated byte in A and B		
132	Discrepancy error in 3rd DI channel. **info 1:** Byte no. for discrepancy. **info 2:** No. of ass. byte in A and B **info 3:** DL: Permanent 1/0 DR: Bit no.	DIs still do not match although discrepancy time has elapsed. Error info includes the subunit containing the bad module.	

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
136	Discrepancy error in 3rd AI channel. **info 1:** AI address **info 2:** No. of the associated channel in A and B	The third AI channel differs from the other two channels for a longer period than that defined by the discrepancy time.	
137	Wirebreak in 3rd AI channel. **info 1:** AI address **info 2:** No. of the associated channel in A and B		
138	Overflow in 3rd AI channel. **info 1:** AI address **info 2:** No. of the associated channel in A and B		
139	Range violation in 3rd AI channel. **info 1:** AI address **info 2:** No. of the associated channel in A and B		
140	Timeout (QVZ) in readback analog input. **info 1:** Readback AI address **info 2:** Associated AQ address	Module or EU failure.	
141	Wirebreak in readback analog input. **info 1:** Readback AI address **info 2:** Associated AQ address	Wirebreak.	
142	Discrepancy in readback analog input. **info 1:** Readback AI address **info 2:** Associated AQ address	The second analog output has already been passivated or the PLC is running in Solo mode. If a discrepancy on this analog channel was reported within 5 minutes, it is not the AQ, but rather the AI, that is defective.	
143	Discrepancy: AQ value too high. **info 1:** AQ address **info 2:** Actual discrepancy value	The readback analog input reads a higher value than the one to be output to the analog output.	Check/re-measure output value and replace defective module.

Table 8-2 Error List

Error No.	Description	**Cause of Error**	**Remedy**
144	Discrepancy: AQ value too low. **info 1:** AQ address **info 2:** Actual discrepancy value	The readback analog input reads a lower value than the one to be output to the analog output.	Check/re-measure output value and replace defective module.
145	Timeout (QVZ) in locating DQ for redundant AQ. **info 1:** L-DQ address **info 2:** Address of the associated AQ in A and B	Module or EU failure.	
150	DB/DX too short or list of dyn. DB/DX unequal. **info 1:** Block length in master controller **info 2:** Block length in standby controller **info 3:** Block number / identifier in master controller	The user program on the standby controller's new MEMCARD differs from the master controller's user program, and this difference is not permitted.	Copy DB/DX block to a new MEMCARD or increase block length.
151	Depassivation due to standby activation.	The master executed automatic depassivation as part of the standby activation phase. This error is entered in the error list only when at least one fault/error is reported in the master controller.	
152	Depassivate without deleting the error records.	H flag control bit X.1 set.	

Explanation of Additional Information

Interface no.: Interface number for CP/IP errors

SAC: STEP address counter. The STEP address counter points to the absolute address +1 in the program memory of the last operation executed.

Block type/block number: This block was the last one processed.

Block type	Block number
2^{15} ... 2^{8}	2^{7} ... 2^{0}

Block type			Block number
1	=	DB	0 to 255
2	=	SB	
4	=	PB	
5	=	FX	
8	=	FB	
12	=	DX	
16	=	OB	

IMPORTANT

The error DB is erased **in its entirety**

– when a cold restart is performed on the master controller

– when you request depassivation by setting the appropriate bit in the H flag word.

Notes on Error Diagnostics

Not all error numbers are reserved.

Avoid RAM comparison errors (error search mode) by

- configuring all DBs/DXs which are modified in an interrupt OB (OBs 2 to 18) as **interrupt** DBs/DXs (refer to the COM 155H User's Guide).

Evaluating the Error Data Block

You can evaluate the error DB in various ways.

a) **Evaluating the error DB on the programmer with COM 155H:**

Using the COM 155H ”DIAGNOSTICS” function, you can have the errors in the error data block output in plaintext. You can scroll up and down through the error records on the screen.

b) **Evaluating the error DB with STEP 5:**

Since the system program automatically invokes the OB 37 user interface when an entry is made in the error DB, it is easy to evaluate the contents of the error DB in OB 37 as part of the STEP 5 program in that organization block (with the aid of error counters, read and write pointers, status word, and so on) and then to respond suitably to that error (refer to the sample program in Section 6.6).

c) **Evaluating the error DB on the programmer using online functions:**

Using a series of on-line functions, you can read out the error data block as a data field right directly on the programmer.

Error Messages from the CP 523

The example in this section shows you how to use OB 37 to output the operating system error messages via CP 523

Preparing the CP 523

1. Plug the memory card into the programmer.
2. Insert the COM 155H diskette in the disk drive and copy the following blocks from file DB523DST.S5D to the memory card.
   – DB 1 Parameter initialization DB (parameters for page length, etc.; refer to the CP 523 manual).
   – DB 194
   – DB 195
   – DB 196
3. Insert the memory card into the receptacle on the CP 523.
4. Set the required module address on the CP 523 (refer to Chapter 5 in the CP 523 manual).

Note

Data block DB 1 contains the printer configuration. The following parameter default values are already set:

- V.24; 9600 bps; 2 stop bits; 7 data bits; 1 start bit; no parity (corresponds to the programmer defaults).
- Number of lines: 72.
- If you want a different configuration, you must modify the relevant parameters in DB 1.

Outputting Error Messages

Error information is passed to the CP 523 via an ”Error message block”; FB 48 (which is part of the COM 155H package and stored as file ”S5CR70ST.S5D”), which you must call in OB 37.

Calling parameters in OB 37:

```
STL                         Explanation
OB 37
       :JU    FB 48         Standard error messages CP 523
NAME   :CP 523 STF
BADR   :KF    +128
P/Q    :KS    O
STDA   :KS    24
CPUZ   :KS    JJ
FEWO   :FW    195
       :BE
```

Name	Para-meter Type	Data Type	Description	Remarks
BADR	D	KF	Module address	P/Q = P : BADR = 128 .. 248 P/Q = Q : BADR = 0 .. 248
P/Q	D	KS	I/O area	P/Q = P: P area P/Q = Q: O area
STDA	D	KS	Hour representation	STDA = 24 : 24-hour representation (German) STDA = 12 : 12-hour representation (US)
CPUZ	D	KS	PLC clock or CP clock as time source	CPUZ = JJ : The PLC clock is used as time source, making the COM H FM time and the printer time the same. Each error reported resets the CP clock. CPUZ = NN : The CP clock is used as the time source. The COM H error message time and the printer output time may differ.
FEWO	Q	FW DW	Value address for error word	All errors detected by FB 48 during parameter initialization and processing

Note:
Even when set to the O address area, the CP can be plugged into an EU 185 which is set for the P address area.

Description of the Error Word (FEWO) in FB 48

FY n								FY n+1							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Status of the CP 523 module in printer mode; refer to the CP 523 manual

No error DB
Illegal error code
Invalid I/O area identifier
Base address BADR out of range
Printer port not ready
Invalid hour representation identifier (STDA)
Unassigned
Unassigned

Sample Printout

```
                           :
10.05.91  11:03:01   SUBUNIT B STANDBY SOFT STOP E-NO.: 020
                     MEMORY MODULE FAULT
                     ADDRESS:  0003  0001  H
10.05.91  11:03:01   SUBUNIT A STANDBY PASSIVATION E-NO.: 061
                     DI ERROR (STUCK AT 0 OR STUCK AT 1)
                     BIT NO./BYTE NO.  005,003
                     STUCK AT 001 ERROR
```

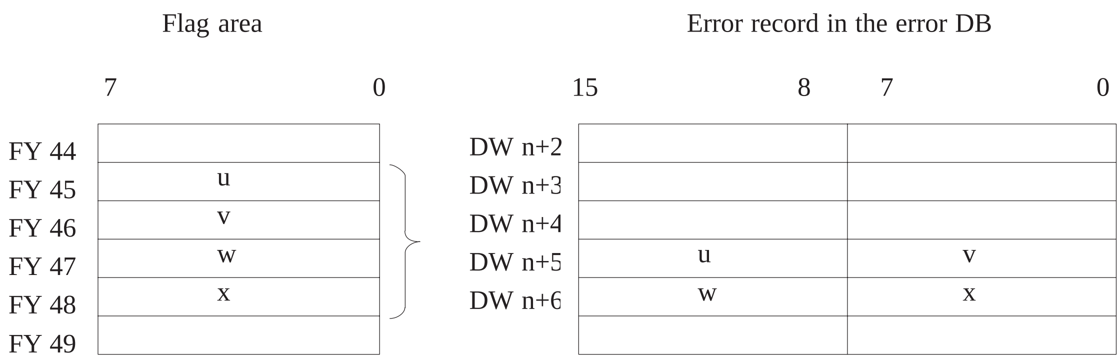
8.3 H Flag Doubleword

Using the H Flag Doubleword

The contents of this flag doubleword, whose number you yourself may choose and stipulate in a COM H run, supplies the time stamp (in the 6th and 7th data word of each error record) for all error messages in the error data block.

You can, for example, use the bits in this doubleword for information useful in error diagnostics (cycle counter or sequencer status).

Example for flag doubleword FD 45:



If, when configuring the system with COM 155H, you do **not** specify a number in the line

```
:
Time stamp flag doubleword (SEC/0..252):SEC
:
```

(see ”SEC” parameter) the internal CPU time is automatically stored in the time stamp in the event of an error (provided the real-time clock has been set). This ensures that every error entry is provided with the exact time (second, minute, hour) and date (day, month, year).

8.4 Error Organization Block OB 37

Tasks Performed by OB 37

As soon as the 155H system program detects an error (during execution of the self-test, for example) and enters it in the error data block, it invokes organization block OB 37.

OB 37 is the block in which you can program the desired responses to errors; for example to output an error message via the CP 523 and/or set the PLC to STOP.

If more than one new 155H-specific error occurs in the STEP 5 program which makes up OB 37, only the first error is entered as error record.

8.5 The H Flag Word

The H flag word contains important information about the status of your programmable controller (such as ”PLC in Error Search Mode”), which you can also evaluate in OB 37.

You may select the number for the H flag word yourself, and specify it during your configuring session with COM H:

```
:
H system flag word     (0..254):   0
:
```

Format of the H Flag Word

The H flag word consists of a status byte and a control byte.

The control information can be set bit by bit in the STEP 5 user program.

The information provided in the status byte is read out in the user program.

Status Byte (High-Order Byte of FY 0)

7	6	5	4	3	2	1	0
AGF	ADL	AMA	ZGA	ANK	MAS	RED	SOL

Bit 0 : **SOL**
”Solo mode”
”1” : PLC is in ”Solo mode”
”0” : in all other cases

Bit 1 : **RED**
”Redundant mode”
”1” : PLC is in ”Redundant mode”
”0” : in all other cases

Bit 2 : **MAS**
”Master”
”1” : CC is master
”0” : CC is standby
} In redundant mode this bit is always 0

Bit 3 : **ANK**
”Standby activation”
”1” : PLC is in ”Standby activation” mode
”0” : in all other cases

Bit 4 : **ZGA**
Central controller is subunit A/B
”1” : CC is subunit A
”0” : CC is subunit B
} In redundant mode this bit is always 0

Bit 5 : **AMA**
Subunit
”1” : Subunit A is master
”0” : Subunit B is master

Bit 6 : **ADL**
Updating in progress
”1” : Standby is being updated
”0” : in all other cases

Cyclic DBs/DXs are transferred.
The system program automatically resets this bit when updating has been completed. The bit can be evaluated only in interrupt OBs.

In order to keep the number of interrupt DBs/DXs to a minimum, this bit can be scanned in interrupt service OBs in order to avoid modifications to the contents of DBs for this brief period of time.

Bit 7 : **AGF**
Note: **No** automatic switchover possible
”1” : PLC fault in switched I/Os
”0” : No faults

(PLC faults are, for example, I/O bus failure, DI 0 failure in one subunit, timeout for switched I/O, etc. An automatic switchover is no longer possible should a secondary fault occur)

Control Byte (Low-Order Byte, e.g. FY 1)

7	6	5	4	3	2	1	0
	RST	AUM	DPA		ARE	DPO	OAT

Bit 0 : **OAT** (No Restart test)
Suppress Restart test
”1” : Restart master without test
”0” : Restart master with test

The system program resets this bit after cold restarts and overall resets.

Bit 1 : **DPO** (Depassivation without deleting)
Depassivate without deleting error records

Bit 2 : **ARE** (Update standby)
Disable updating of the standby controller
”1” : Updating of the standby controller disabled
”0” : Updating of the standby controller enabled (= default)

Bit 3 : Reserved

Bit 4 : **DPA** (Depassivation)
Revoke passivation
”1” : Revoke passivation
”0” : in all other cases (default)

Important:
This bit **must** be set using signal edge evaluation; that is, it may be set once only, and may not be set again until the system program has reset it. The system program resets the bit after passivation has been revoked. This bit may not be reset in the user program.

Bit 5 : **AUM** (Switchover request)
Switchover requested
”1” : Switchover requested ”0” : in all other cases (default)

The system program resets this bit after the switchover has taken place.

Bit 6 : **RST** (Standby STOP)
Set standby controller to STOP
”1” : Set standby controller to STOP
”0” : in all other cases (default)

The system program resets this bit after setting the standby to STOP.

Bit 7 : Unassigned

Dynamic Response to Faults, Repair, Replacement and Upgrading

9

This chapter discusses the S5-155H's dynamic response to faults and to module, expansion unit and cable failures, and recommends repair procedures.

It also explains how to replace the memory card and update the CPU.

9.1 Failure and Repair of the CPU and Parallel Links

Replacing the Central Processing Unit

If you have to replace a CPU 948R because of a defect, you will also have to replace the other CPU 948R if it is not running the same version of the operating system. To replace a CPU 948R without interrupting operation, proceed as described in Section 9.6.

Replacing the Interface Modules (IMs)

Should the parallel link between subunit A and subunit B fail, because of a wirebreak or a module defect, for example, the master controller continues in Solo mode and the standby controller stops (only when a switched EU is present; otherwise refer to the CPU 948R Programming Guide, Section 4.5.1, Cyclic Program Execution "Special Situation: Operation Without Connected EU").

Proceed as follows to replace a component:

- First, replace the 721 cable that connects the IM 304 with the IM 324R and start the standby controller.
- If the link fails again, set the standby controller to "STOP". Switch off the power. Replace the standby controller's IM 304 (or IM 324R) interface module. Reconnect the IM 304 and the IM 324R and start the standby controller.
- If the link fails again, proceed exactly as described below, for only then will you be able to process your program in NON-STOP mode.

1. Set the standby controller to "STOP" and switch off the power.
2. Remove the IM 304 or IM 324R from the standby controller and plug in a functional IM 304.
3. Case-basis decision:

   A If the master is equipped with an IM 324R, go to 4.

   B If the master is equipped with an IM 304, it must not be removed; an IM 304 cannot be inserted/removed while the controller is in operation (the master would stop). **A slot (27 to 123) must be available for the new IM 324R**. (After repairs, the IM 304 and the IM 324R will each be in the opposite subunit, but this does not affect the subunit identification). Now go to 5.
4. Connect the 24 V supply and ground to the appropriate terminals on the frontplate of the IM 324R. You can use the 24 V output of your central controller's power supply unit for this purpose. **Now remove this IM 324R**.
5. Connect the 24 V and ground to the appropriate terminals on the frontplate of the IM 324R (you can use the 24 V output of your central controller's power supply unit for this purpose). Plug the IM 324R into the controller that is currently the master.

6. Remove the 24 V source (including ground). The green LED on the IM 324R's frontplate goes on. Reconnect the IM 304 and the IM 324R.
7. Switch the standby controller on and start it up.

After repairs have been completed and the standby controller has been activated, the S5-155H is once again fault-tolerant.

Replacing the IM 30x Interface Modules in the CC (Excepting those used for the Parallel Link)

The relevant central controller must always be at STOP and its power switched off.

Replacing the IM 30x – IM 31x Connecting Cable

In one-sided/redundant systems, the expansion unit must be switched off when replacing the 721 cable connecting an IM 30x and an IM 31x.

In switched configurations, only the standby's 721 cable may be replaced when it connects an IM 304 and an IM 314R. Before doing so, always set the standby to STOP.

9.2 Failure and Repair of Expansion Units (EUs)

Cycle Extension

The cycle monitoring time must be set accordingly for the S5-155H to tolerate an EU failure: per digital/analog I/O byte, the cycle extension amounts to 1 ms + runtime of the user program in OB 37.

One-Sided EUs

A ”wirebreak” or ”EU power failure” is reported in the form of one of more error messages. You can evaluate the timeout information for the relevant I/O modules. The I/O addresses of these modules are passivated, as otherwise there would be a continuous timeout. The S5-155H tolerates the failure of all one-sided EUs; that is, both CCs continue operation even without EUs.

When an expansion unit has been repaired, you must depassivate that unit (by setting the ”DPA” bit in the H flag word). The modules plugged into that unit are then once again entered in the process image. Following activation, the S5-155H is once again fault-tolerant.

Switched EUs

If an IM 304 (in the master) or IM 314R (in an expansion unit) fails because of a wirebreak (plug pulled), for instance, the 155H system program switches to the standby. The current master becomes the standby, and reports a fault.

When an EU fails, an ”I/O bus fault” is reported (error no. 40); the user can then evaluate the fault information.

The S5-155H tolerates the failure of all switched expansion units; that is, both controllers continue to operate, even without EUs. If one of the two controllers in a switched configuration fails, the other continues in Solo mode.

When a switched EU has been repaired, it is automatically activated in the next PLC cycle. The modules in that EU are updated.

Redundant EUs

When an EU fails, the central controller continues to run. The fault is reported and entered in the error data block.

For information on repairs, see ”One-sided EUs”.

Following depassivation, the S5-155H is once again fault-tolerant. The one-sided I/Os are updated.

9.3 Failure and Repair of I/O Modules

Replacing an I/O Module

When an I/O module fails, the failure is detected in the S5-155H

- through a timeout (QVZ) or
- during the self-test.

The module failure is reported.

You can replace the module during operation if you

1. Use the enable input and
2. Remove the front connector before changing the module.

When the I/O module has been repaired and is back in the subrack, it is not activated until it has been depassivated (by setting the ”DPA” bit in the H flag word). The module is once again entered in the process image. When the activation phase has been completed, the S5-155H is once again fault-tolerant.

9.4 Failure and Repair of CP/IP Modules

Replacing a CP/IP

In the S5-155H, the failure of a CP/IP module is detected because of a timeout (QVZ). The module failure is reported. ”CP/IP does not acknowledge” is entered in the error DB (a timeout (QVZ) has error no. 81).

1. Switch off the power to the subrack (EU or possibly the CC) containing the defective CP/IP module before removing it for repairs or replacing it with another module.
2. Once the CP/IP has been replaced, you must revoke its passivation (by setting the ”DPA” bit in the H flag word). You must also call the ”SYNCHRON” function block (FB 125), which prepares the module for reinclusion.

   The module is then activated. Once the activation phase has been completed, the S5-155H is once again fault-tolerant.

Sample Program

```
STL                         Explanation
        :                   Program for CP 1
        :O F   10.0         F 10.0 must be set when CP 1
        :L KT  150.2        is repaired
        :SE T  1            Depassivation takes max. 15 sec.
        :O(
        :L     FY 8         PAFE byte for CP 1
        :L KH  0000
        :><F
        :)
        :O F   10.0         F 10.0 must be set when the
        :R F   10.0         CP 1 is repaired
        :=F    11.0

        :JC    FB 125
NAME    :SYNCHRON
SSNR    :      KY0.0        Page no. for CP 1
BLGR    :      KY0.6
PAFE    :      FY 8
        :A F   11.0         Depassivation requested?
        :A T   1            Have 15 seconds elapsed yet?
        :BEC                Yes –> BE, as only one CP
        :                   may be depassivated at a time
        :A F   11.0         Have 15 seconds elapsed?
        :R F   11.0
        :JC    FBxx         Error reported; CP 1 cannot
        :L KB 0             be depassivated
        :T FY 8
```

(Continued on next page)

STL		Explanation
	:	
	:	**Program for CP 2**
	:O F 10.1	F 10.0 must be set when
	:L KT 150.2	CP 2 is repaired.
	:SE T 1	Depassivation takes max. 15 seconds
	:O(	
	:L FY 9	PAFE byte for CP 2
	:L KH 0000	
	:><F	
	:)	
	:O F 10.1	F 10.1 must be set when CP 2 is repaired.
	:R F 10.1	
	:=F 11.1	
	:JC FB 125	
NAME	:SYNCHRON	Page no. for CP 2
SSNR	: KY0.2	
BLGR	: KY0.6	
PAFE	: FY 9	Only one CP may be
	:A T 1	depassivated at a time
	:BEC	
	:	
	:A F 11.1	
	:R F 11.1	Error reported; CP 2 cannot
	:JC FBxx	be depassivated
	:L KB 0	
	:T FY 9	
	:	**Program for CP 3**
	:	

9.5 Standby-Master Switchover

Switchover Criteria

During operation, a standby-master switchover results in the current master becoming the standby and the current standby becoming the master. Such a switchover takes place when

a) the master fails (BASP, NAU or mode selector set to ’STOP’)

b) the first error search (see Section 2.5) on the standby was unsuccessful

c) an IM 314R fails

d) an I/O bus to a switched EU fails

e) a switched I/O module fails

f) the user requests a switchover at the software level (by setting a bit in the H flag word or via COM 155H).

In situation a), the standby controller enters the Solo mode. In case b), the **new** standby enters the Error Search mode while the ”old” standby continues in Solo mode. In cases c) to f), the **new** standby controller does not stop, but continues on as standby.

Standby-Master Switchover when the Master Fails

Via the IM 324R parallel link module, the standby controller checks at every synchronization point to see if the master is ready. If the standby ascertains that the master has failed, it takes the following actions:

- The I/O buses of all IM 314Rs are switched.
- The two-channel I/Os are switched to one-channel operation.
- The ”switchover mode” is entered; that is, the subunits are no longer synchronized.
- If the synchronization point is a direct I/O operation to a switched I/O, the operation is repeated.

Example

Standby-Master Switchover

```
OB 1 in the master CC                              OB 1 in the standby CC
                          Synchronization
   :T   QB  z   <------------------------------>     :T   QB z
   :L   DW x                                         :L   DW  x
   :L   KB  1                                        :L   KB 1
   :+F                                               :+F
 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   (:T  DW x)              Master failure            :T   DW  x
   (:AW     )                                        :AW
   (:.      )                                        :.
   (:.      )                                        :.
   (:.      )                                        :.
   (:L  PW y)   <---------------------------         :L   PW  y
                 Standby wants to synchro-           :T   FW
                 nize, recognizes that the           :A   F x.y
                 master has failed, and
                 switches over and becomes
                 the master
```

One-Sided I/Os in the Failed Subunit

The one-sided I/Os assigned to the failed subunit are treated as follows:

- The process output image (PIQ) is set to ”0”.
- The process input image (PII) is set to ”0”.
- A timeout (QVZ) is reported in the event of a direct access operation to these I/Os or this PII/PIQ.

Note

One-sided I/Os should be used only for **independent subprocesses**, which are completely passivated in the event of a PLC failure. The software for controlling these processes should be stored in separate blocks and called only **conditionally**; that is, only when the respective subunit is operating.

Bumpless Switchover

Event-driven synchronization ensures bumpless standby-master switchover whenever necessary; such a switchover has no effect whatsoever on process output signals, and there is no loss of information during communication with the CPs/IPs.

Switchover Time

The switchover time is the once-only increase in scan time caused by a standby-master switchover. From the instant at which the fault/error (synchronization error, for example) is detected, the switchover itself takes no more than 30 ms (full configuration).

The switchover takes up to 3 ms in the event of a CC power supply failure or total CPU failure, or when a request for a switchover is made via H flag (full configuration).

9.6 Replacing the Memory Card During Operation

Conditions and Upgrading Sequence

Modifications to the user program in the flash EPROM memory card must be made known to the operating system via the ”software modification” parameter. When the standby is activated, this parameter prevents a comparison between the 32-bit checksums of the controllers’ memory cards, and the master CPU’s user program is **not** transferred to the standby CPU.

All data blocks in the standby must come from the memory card. The new data blocks may be longer, but not shorter than those in the master.

The contents of the data blocks in the COM H list, timers, counters, flags and system data are transferred at one synchronization point. Upon completion of the activation phase, a standby-master switchover is executed and and CPU which is now the standby stops. The ”software modification” parameter is reset.

Once again, in this situation the standby CPU must not create any blocks when starting up.

Operator Input Sequence

The following entries are required:

1. Using COM 155H, set the ”PLC memory card upgrade function” parameter. This effects deactivation of Restart functions ”DB 0 comparison” and ”Block transfer”.
2. Set the standby controller to STOP.
3. Replace the standby CPU 948R’s memory card.
4. Execute an overall reset on the standby controller.
5. Execute a cold restart by setting the standby controller to RUN.

   This restarts and updates the standby controller. It also initiates an automatic standby-master switchover and sets the ”old” master to STOP. The ”software modification” parameter is automatically reset.
6. Replace the ”old” master’s memory card.
7. Execute an overall reset and a cold restart with activation of the CPU 948R as standby.

The above sequence makes possible interruption-free software modification (changing of the user program) simply by replacing the memory card.

IMPORTANT

A bumpless switchover from standby to master can only be guaranteed if the use of the dynamic data is not changed.

9.7 Upgrading the CPU 948R's RAM or Version Number

Conditions and Upgrading Sequence

Upgrading of the CPU 948R's RAM capacity must be made known to the operating system via the "CPU 948R upgrade" parameter. The CPU's new user RAM capacity must be the same as, or higher than, the old one. The user program in the master CPU is transferred to the standby CPU. All data blocks in the master's RAM are transferred to the same locations in the standby's RAM.

The contents of the data blocks in the COM H list, timers, counters, flags and system data are transferred at one synchronization point. Upon completion of the activation phase, a standby-master switchover is initiated and the CPU which is now the standby stops. The "CPU 948R upgrade" parameter is reset.

Operator Input Sequence

Proceed as follows to upgrade the S5-155H without shutting down the system:

1. Using COM 155H, set the "PLC upgrade CPU 948R function" parameter in the master controller. This causes deactivation of Restart function "DB 0 comparison".
2. Set the standby controller to STOP.
3. Switch off the controller that is now at STOP.
4. Replace the CPU 948R in the standby controller with a CPU that has more RAM or a newer version number.
5. Switch the power back on.
6. Execute an overall reset.
7. Execute a cold restart by setting the standby's CPU to RUN.

   This restarts and updates the standby controller. The cold restart is followed by an automatic standby-master switchover, after which the "old" master stops. The "CPU 948R upgrade" parameter is automatically reset.
8. Replace the CPU 948R on the "old" master as described in steps 3, 4, 5 and 6.
9. Execute an overall reset and a cold restart with activation of the CPU 948R as standby.

Observing this sequence makes possible interruption-free upgrading of the RAM memory or of the CPU itself. Downgrading (installing lower-capacity RAM or a CPU with a lower version number) is not possible during operation.

Typical Applications 10

This chapter contains sample applications for various configurations of an S5-155H system. When you have worked through these examples, you will have an H system you can use for any purpose and expand to meet your specific requirements.

10.1 Task and Required Resources

Problem Definition

The steps making up the overall application should be carried out in the following order:

- First, you put the hardware into operation.
- Next, you add switched I/Os.
- Then you add one-sided I/Os to the switched I/Os.
- Finally, you add redundant I/Os with error locating facilities.

Hardware

The following hardware is required for our sample application:

- Two S5-135U/155U central controllers, each with a CPU 948R
- One IM 324R interface module
- Three IM 304 interface modules
- Three 721 interface cables
- One EU 185U expansion unit
- Two IM 314R interface modules
- Three 430 digital input modules
- Two 451 digital output modules
- Two 760-0HA11 terminators

Software

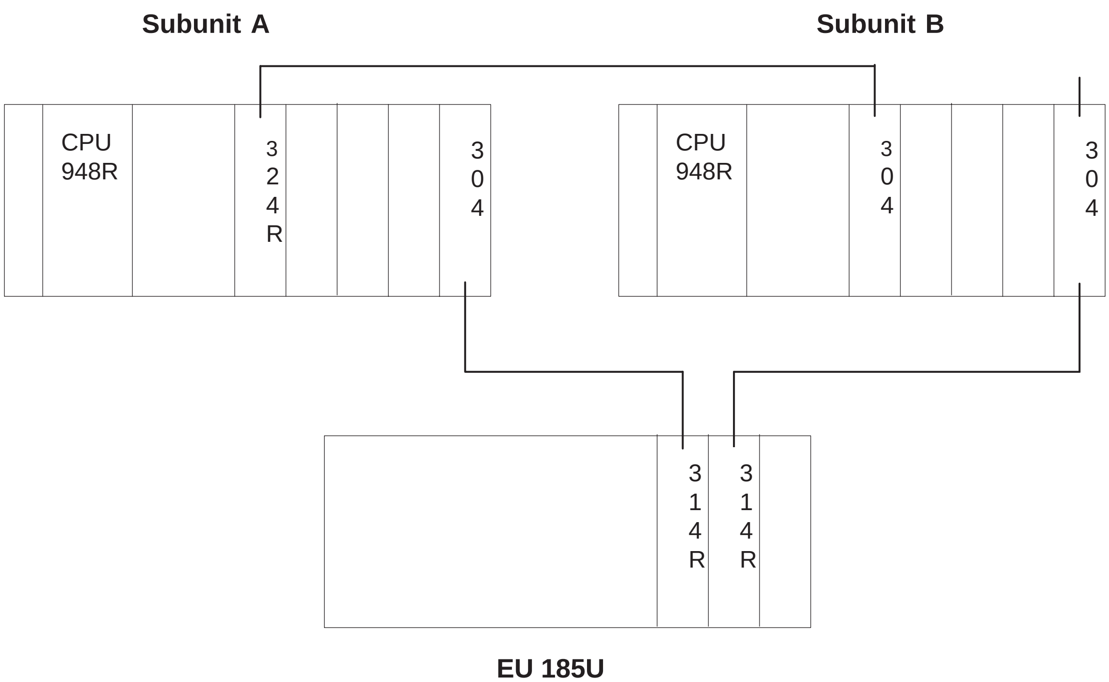
You require the following software:

- COM 155H (version 3.0 or newer)
- STEP 5 basic package, level 5

10.2 Installing the Hardware

System Configuration

You are going to install and configure an S5-155H system as shown in the diagram below.



Establishing a CC-to-CC Parallel Link

The purpose of this step is to establish the parallel link between the two CCs via the IM 324R and IM 304 (6ES5 304-3UB11) interface modules.

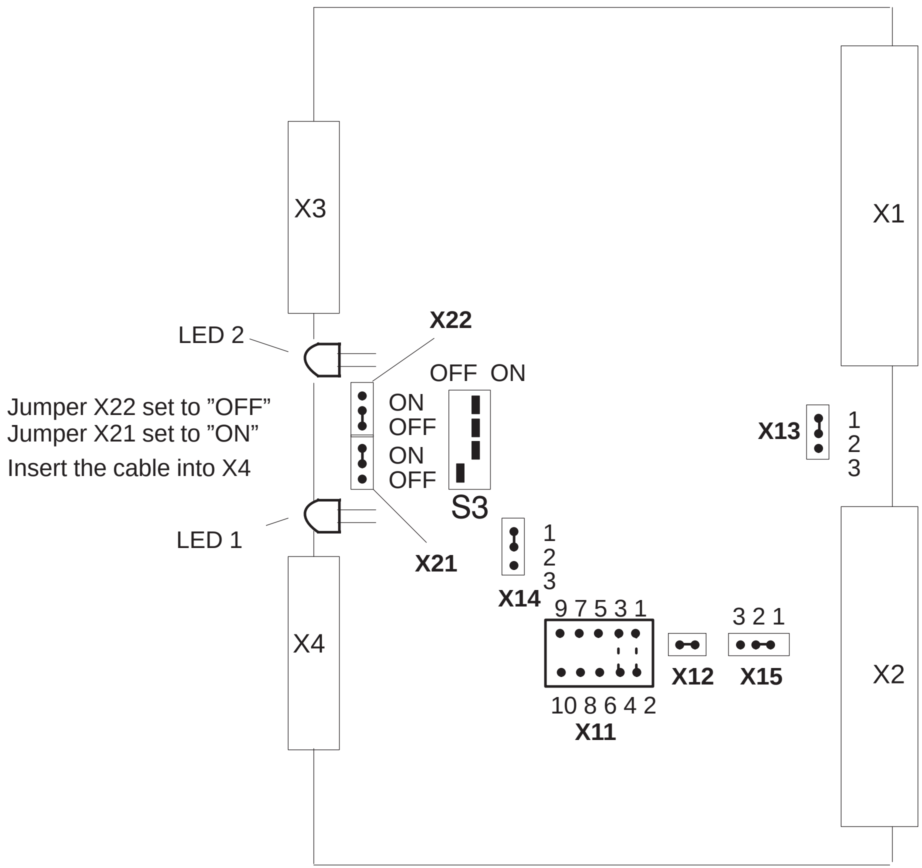
No changes to the jumper settings on the IM 324R are necessary (see Section 4.2). You must change the jumper settings on the 6ES5 304-3UB.. as shown in the diagram on the next page.

Plug the IM 324R into slot 131 in one of the subunits. This subunit will be referred to as subunit **A**.

Jumper Settings on the IM 304

Configure the jumpers on the IM 304 (module 6ES5 304-3UB11) as shown in the diagram below.

The setting for X11 may not exceed 100 m.



X11: Adaption to different cable lengths

	Jumper plug X11				
Jumper position	9 7 5 3 1 *) 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2
Cable length	Max. 10 m	10 to 100 m			

*) These settings are only allowed for interfacing the IM 304 and IM 324R in an S5-155H system.

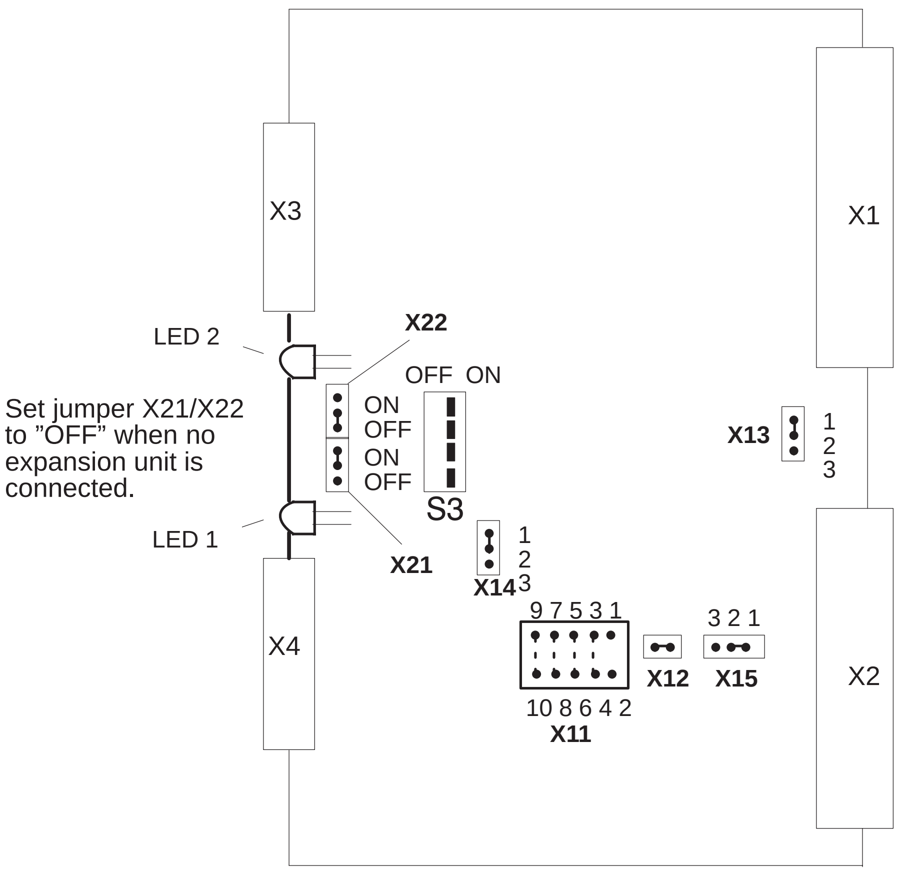
The length of the link to interface X4 determines the position of jumper X11.

Installing the I/O Bus

The purpose of this step is to establish the symmetrical link between the CC and the EU via the IM 304 (6ES5 304-3UB11) in subunits A and B and the two IM 314Rs in the expansion unit.

Jumper Settings on the IM 304

Set the jumpers on the IM 304 (module 6ES5 304-3UB11) as shown in the diagram below.



X11: Adaption to different cable lengths

	Jumper plug X11				
Jumper position	9 7 5 3 1 *) 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2	9 7 5 3 1 10 8 6 4 2
Cable length		1 to 100 m	100 to 250 m	250 to 450 m	450 to 600 m

*) These settings are permitted only for interfacing the IM 304 and the IM 324R in an S5-155H system.

The length of the link to interface X3 or X4 determines the position of jumper X11.

10.3 Configuring Switched I/Os

This section shows you how to configure four output bytes (bytes 8 to 11) and three input bytes (bytes 8 to 10) in switched I/Os.

1. Insert the input and output modules with the relevant settings (DI = address 8, DQ = address 8) and readback module into the EU 185U. Connect your programmer to the CPU in subunit A.

Calling COM 155H

2. Call up the Package Selection form on the programmer monitor with ”S5”. Position the cursor to the ”COM 155H” line and press function key F1 to call the COM 155H programming software.
3. After entering the name of the program file and choosing the ”ON” mode, press F6 <EXEC>.

The COM 155H ”Main Menu” form for STEP 5, level 5, appears on the screen.

COM 155H Main Menu COM 155H / PEC16

CPU FIRMWARE	:nn	PROGRAM FILE	: @@@@@ST.S5D
SYMBOLS	:NO	SYMBOLS FILE	:
FOOTER	:NO	FOOTER FILE	:
PRINT WIDTH	:NORMAL	PRINTER FILE	:
OP MODE	:ON (MOD IN CYCL)		
PATH NAME	:	PATH FILE	:

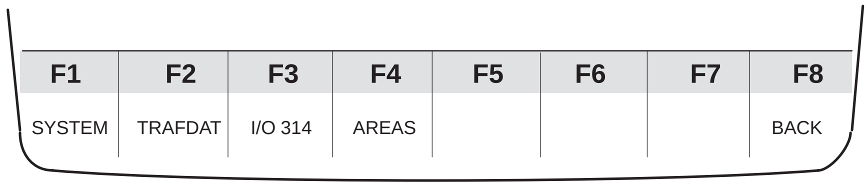
F1	F2	F3	F4	F5	F6	F7	F8
CONF PLC	CONF FD	CONF PG	PLC FCT	DIAGN.	DEFAULTS	SYSHAN	BACK

4. Press function key F2 <CONF FD> to select the S5-155H configuring form.

Configuration (DX 1) has been loaded

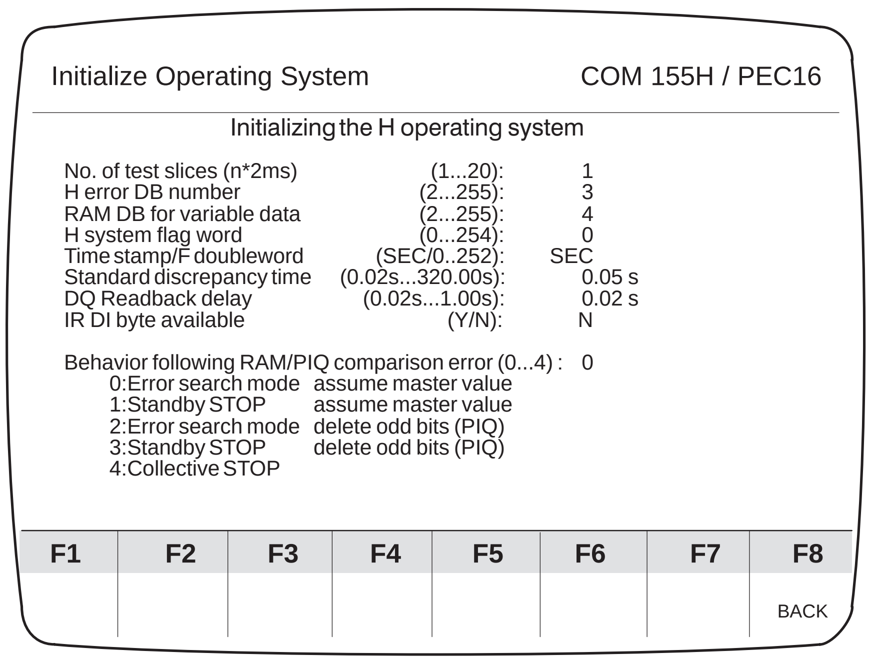
F1	F2	F3	F4	F5	F6	F7	F8
OS	IOCONF		DELETE				BACK

5. Press function key F1 <OS> to screen the softkey menu for ”Initialize Operating System”.



6. Press function key F1 <SYSTEM>.

Initializing the Operating System (COM 155H)



7. Enter ”198” as H flag word. Confirm the default values for all other parameters. Press F8 <BACK> to save the parameters and return to the ”Initialize operating system” softkey menu.
8. Press function key F3 <I/O 314>.

Setting the System Size

Set System Size COM 155H / PEC16

Enter area number! ”N” means not reserved

I/O area of EU number 0	:	0	P area	FF000H–FF0FFH
I/O area of EU number 1	:	N	not reserved	
I/O area of EU number 2	:	N	not reserved	
I/O area of EU number 3	:	N	not reserved	
I/O area of EU number 4	:	N	not reserved	
I/O area of EU number 5	:	N	not reserved	
I/O area of EU number 6	:	N	not reserved	
I/O area of EU number 7	:	N	not reserved	
I/O area of EU number 8	:	N	not reserved	
I/O area of EU number 9	:	N	not reserved	
I/O area of EU number 10	:	N	not reserved	
I/O area of EU number 11	:	N	not reserved	
I/O area of EU number 12	:	N	not reserved	
I/O area of EU number 13	:	N	not reserved	
I/O area of EU number 14	:	N	not reserved	
I/O area of EU number 15	:	N	not reserved	

F1	F2	F3	F4	F5	F6	F7	F8
							BACK

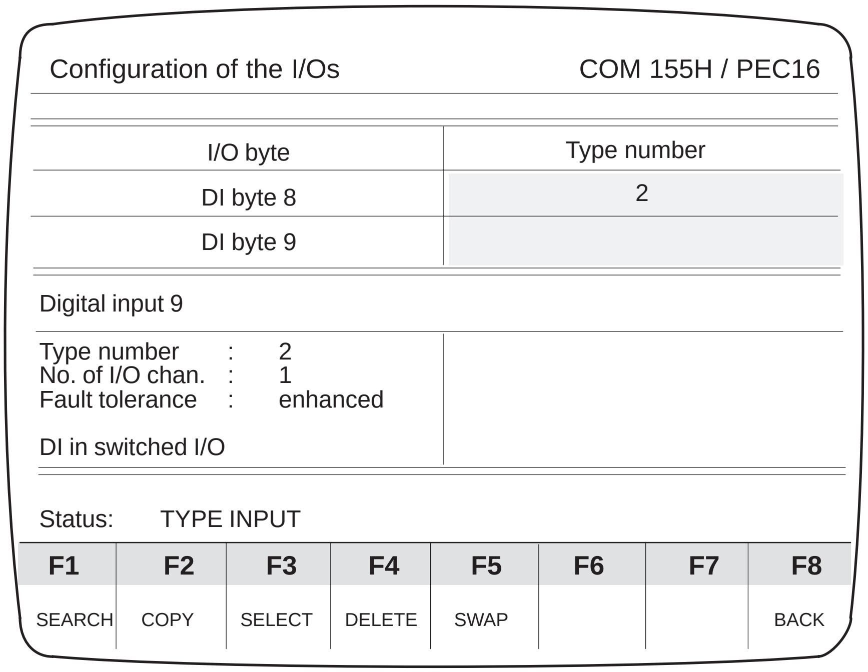
9. Since your expansion unit (EU 0) is to be operated in the P area, you must enter area number ”0” (for P area).
10. Press function key F8 <BACK> to return to the COM 155H main menu. Press function key F2 <IOCONF> to select the softkey menu for ”Configuration of the I/Os”.

Configuration (DX 1) has been loaded

F1	F2	F3	F4	F5	F6	F7	F8
DI	DQ	AI	AQ	CP/IP			BACK

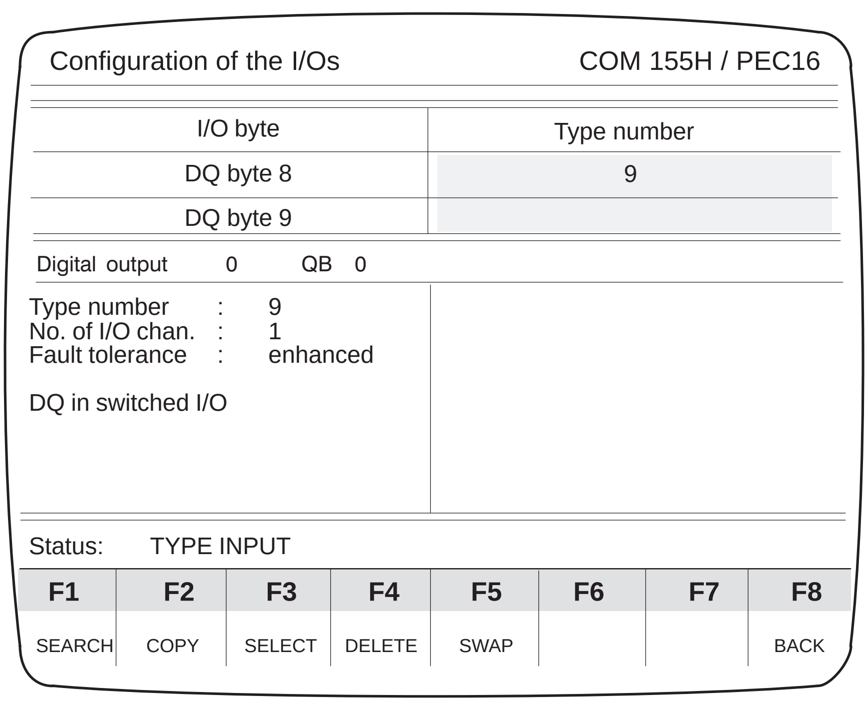
11. Press function key F1 <DI>.

Configuring Digital Inputs



12. Enter the type number ”1” (DI in switched I/O) for bytes 8 to 10, then press function key F8 <BACK>. Finally, press function key F2 <DQ> to enter the ”Configuration of the I/Os” screen.

Configuring Digital Outputs



13. Enter type number ”9” (DQ in switched I/O) for bytes 8 to 11.
14. Press function key F8 <BACK> three times in succession to select the ”OVERWRITE CONFIGURATION (DX 1) ON FLOPPY?” prompt. Press <INSERT> to return to the COM 155H main menu.

Transferring Configuring Data (DX 1)

15. Press function key F7 <SYSHAN>, then function key F3 <TRAN/LOAD> to select the softkey menu for ”I/O transfer/load”.

Configuration (DX 1) has been loaded

F1	F2	F3	F4	F5	F6	F7	F8
PLC→PG	PG→PLC	FD→PG	PG→FD				BACK

16. Transfer the new DX 1 with F2 <PG → PLC> to your subunit A.
17. Press function key F8 <BACK> three times in succession to exit COM 155H.

Starting Up the PLC

Your configuring data (DX 1) is now in subunit A.

18. Execute a cold restart on subunit A. After completion of the self-test (red and green LEDs are on), the CPU enters the RUN mode (green LED is on).

    The operating system generates the configured error data block and RAM-DB automatically.

19. Execute a cold restart on subunit B (after an overall reset has been performed).

    The program in subunit A (master) is transferred to subunit B, and subunit B is ”activated”. The red and green LEDs on subunit B flash alternately. Following termination of the self-test (red and green LEDs show a steady light), the standby’s CPU also enters the RUN mode. A flashing green LED shows which subunit is the standby.

You can now write programs just as you did for the S5-155U.

Note:
In the standby controller, direct I/O access operations must be suppressed during startup with the aid of the H flag word (status byte).

On-Line Functions

In Redundant mode, all write operations are executed on both PLCs simultaneously. Read operations in Redundant mode are the same as in the U system.

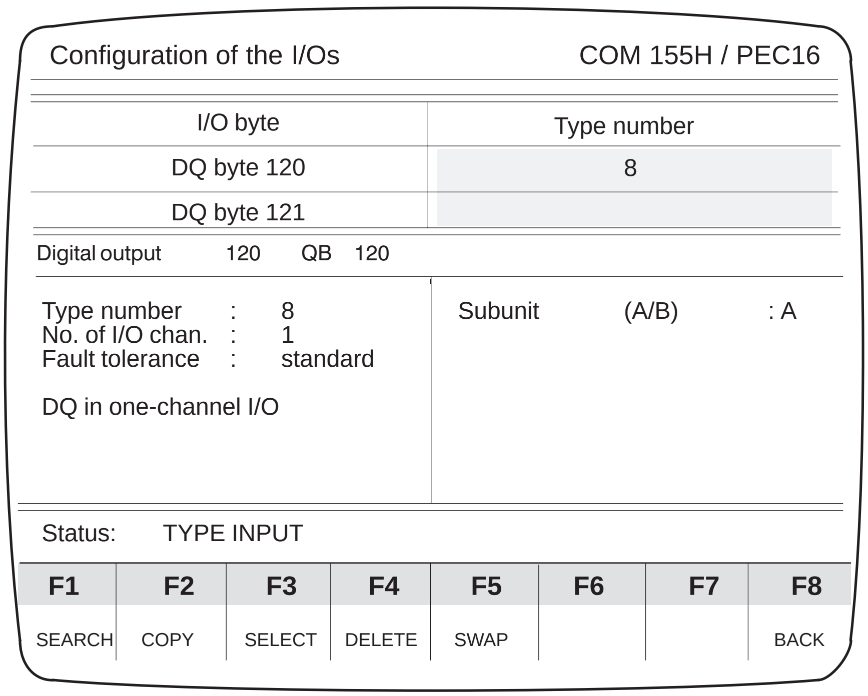
10.4 Configuring One-Sided I/Os

In this step, two output bytes (bytes 120 and 121) will be configured as one-sided I/Os in subunit A.

1. Insert the output module with the relevant setting (DQ = address 120) and readback module into subunit A.
2. Press function key F2 <CONF FD> to load DX 1 into the programmer.

Configuring Digital Outputs

3. Press F2 <IOCONF>, then F2 <DQ> to select the ”Configuration of the I/Os” screen so that you can configure your one-sided digital outputs.



4. Enter type number ”8” (DQ in one-channel I/O) and subunit ”A” for bytes 120 and 121.
5. Press function key F8 <BACK> three times in succession to return to the main menu. Transfer the new DX 1 to the PLC.

Starting Up the PLC

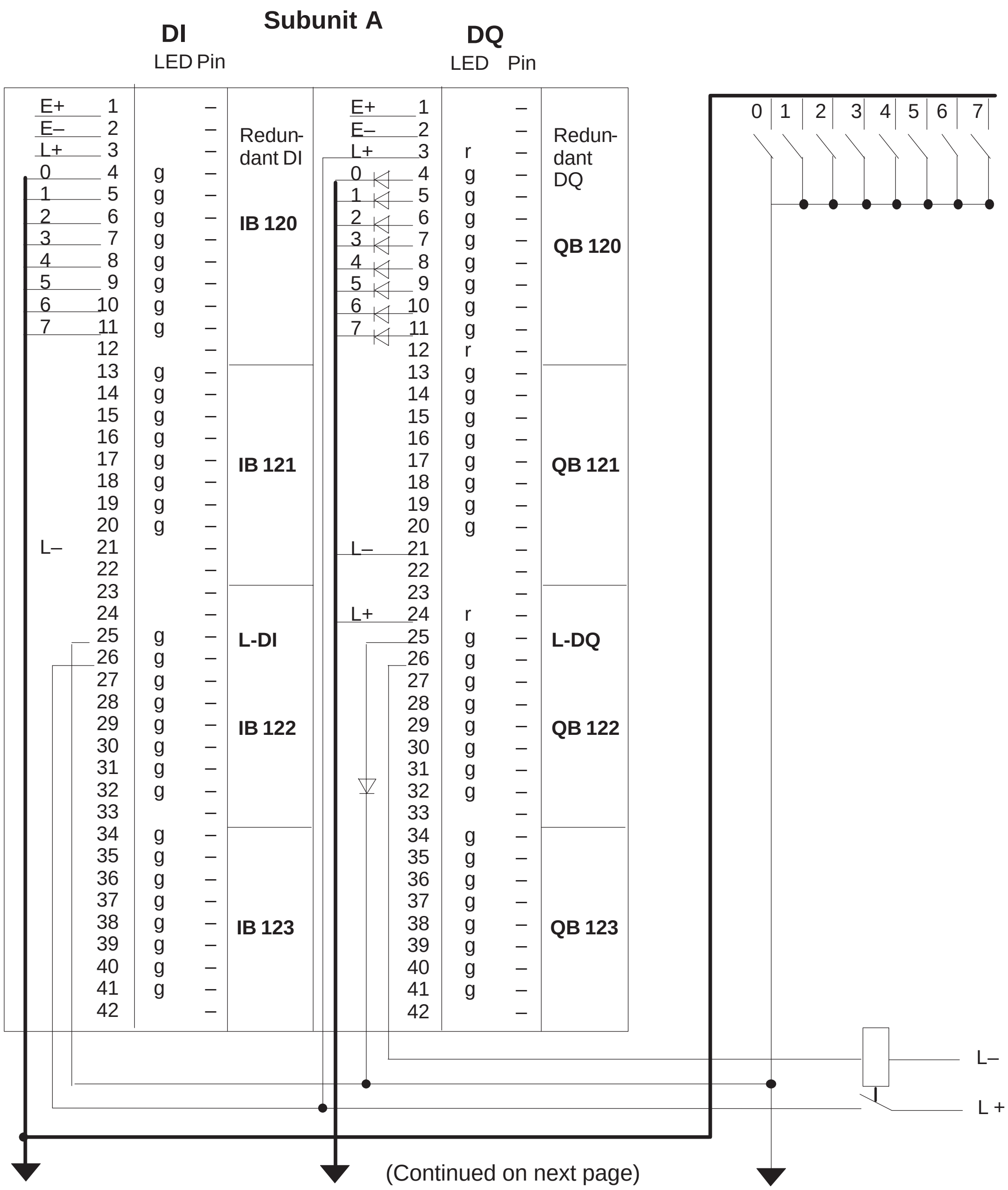
Write your programs as you would for an S5-155U. Make sure, however, that the output bytes are assigned to only one subunit. When that subunit fails, the I/O bytes assigned to it are no longer available.

10.5 Configuring Redundant I/Os

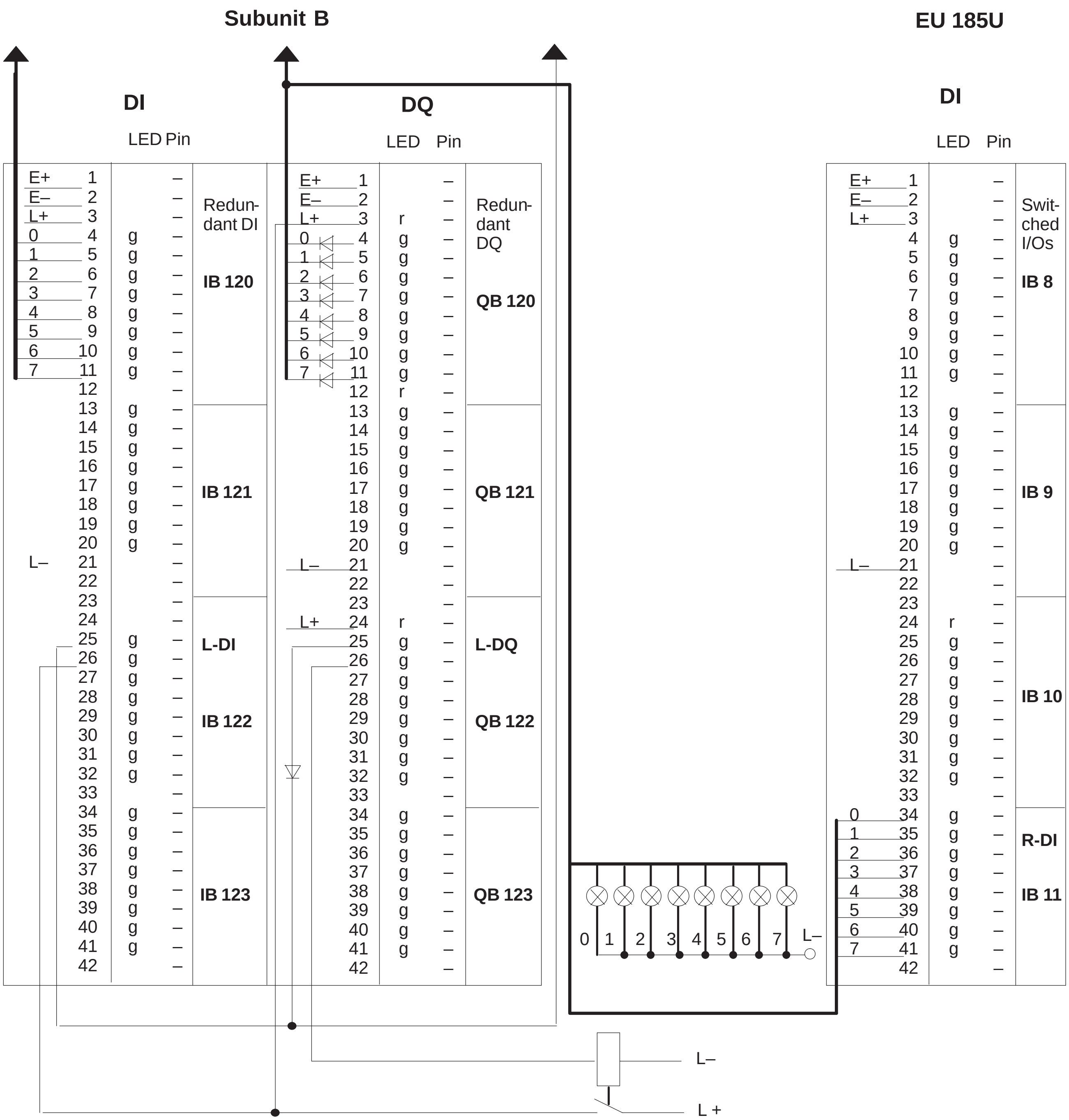
In this step, or section, which is regarded as a ”separate project”, as it were, you are going to configure one redundant input byte and one redundant output byte, each with error locating facility.

Interconnecting I/Os

1. Insert one 430 input module and one 451 output module with the module address 120 into each of the subunits. Then plug a 430 input module with the module address 8 into the switched I/O (expansion unit EU 185U).
1. Interconnect the modules as shown in the diagram below.



(Continued on next page)


Subunit B
EU 185U
DI
LED Pin
Redun-
dant DI
IB 120
IB 121
L-DI
IB 122
IB 123
DQ
LED Pin
Redun-
dant
DQ
QB 120
QB 121
L-DQ
QB 122
QB 123
DI
LED Pin
Swit-
ched
I/Os
IB 8
IB 9
IB 10
R-DI
IB 11
L–
L +

Setting the System Size

3. If you have not yet entered expansion unit EU 0 with area number ”0” (P area), do so now.

Set System Size COM 155H / PEC16

Enter area number! ”N” means not reserved

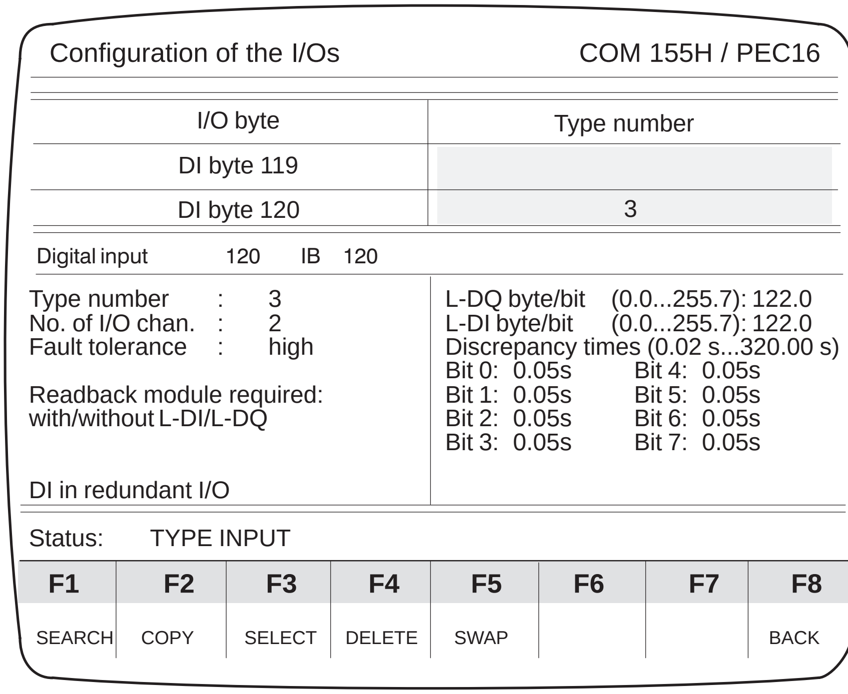
I/O area of EU number 0	:	0	P area	FF000H–FF0FFH
I/O area of EU number 1	:	N	not reserved	
I/O area of EU number 2	:	N	not reserved	
I/O area of EU number 3	:	N	not reserved	
I/O area of EU number 4	:	N	not reserved	
I/O area of EU number 5	:	N	not reserved	
I/O area of EU number 6	:	N	not reserved	
I/O area of EU number 7	:	N	not reserved	
I/O area of EU number 8	:	N	not reserved	
I/O area of EU number 9	:	N	not reserved	
I/O area of EU number 10	:	N	not reserved	
I/O area of EU number 11	:	N	not reserved	
I/O area of EU number 12	:	N	not reserved	
I/O area of EU number 13	:	N	not reserved	
I/O area of EU number 14	:	N	not reserved	
I/O area of EU number 15	:	N	not reserved	

F1	F2	F3	F4	F5	F6	F7	F8
							BACK

4. Press function key F8 <BACK> twice in succession to return to the COM 155H configuring menu.
5. Press function key F2 <IOCONF>, then function key F1 <DI> to select the ”Configuration of the I/Os” screen.

Configuring Redundant Inputs

6. Enter type number ”3” (DI in redundant I/O) for byte 120. Enter ”122.0” as L-DQ and as L-DI bit. Confirm the default values for the discrepancy times.



7. Press function key F8 <BACK>, then function key F2 <DQ> to select the ”Configuration of the I/Os” screen.

Configuring Redundant Outputs

8. Enter type ”10” (DQ in redundant I/O) for byte 120. Enter ”122.1” as L-DQ bit and L-DI bit. Enter byte ”11” in switched I/O (”3”) as R-DI (readback digital input).

Configuration of the I/Os COM 155H / PEC16

I/O byte	Type number
DQ byte 119	
DQ byte 120	10

Digital output 120 QB 15

Type number : 10
No. of I/O chan. : 2
Fault tolerance : high

Readback module required
with/without L-DI/L-DQ
with/without R-DI
DQ in redundant I/O

L-DQ byte/bit (0.0 ... 255.7): 122.1
L-DI byte/bit (0.0 ... 255.7): 122.1
R-DI byte (0... 255) : 11
R-DI in I/O : 3
(1: subunit A, 2: subunit B,)
3: P swit., 4: O swit.)

Status: TYPE INPUT

F1	F2	F3	F4	F5	F6	F7	F8
SEARCH	COPY	SELECT	DELETE	SWAP			BACK

9. Press function key F8 <BACK> twice in succession to return to the COM 155H main menu.

10. Transfer the new DX 1 to the PLC.

Printing out the Configuring Data

11. In the main menu, press function key F7 <SYSHAN>, then F4 <PRINT> to select the ”Print menu” screen.

F1	F2	F3	F4	F5	F6	F7	F8
DI	DQ	AI	AQ	CP/IP	TYPES	ALL	BACK

12. Press F1 <DI> and F2 <DQ> for the following printouts of your I/O modules.

Digital Inputs/Outputs

I/O Byte	Symbol	Type	Subunit	I/O Byte	Symbol	Type	Subunit
IB 8		2		IB 9		2	
IB 10		2		IB 11		R-DI	
IB 120		3		IB 122		L-DI	
QB 120		10		QB 122		L-DQ	

10.6 Redundant Point-To-Point Link

To establish a redundant link, you can plug the relevant CP either

- into both central controllers (for two-channel redundancy) or
- into switched expansion unis (for switched redundancy).

The H-specific special features of a two-channel redundant and of a switched redundant point-to-point connection are discussed using the CP 525 as an example.

Establishing links with other CPs, such as CP 523, CP 524, CP 530, CP 544 and CP 143, is done in the same way.

Two-Channel Redundant Point-to-Point Link

The following hardware is required:

- One S5-155H in its basic configuration
- One S5-115U with power supply unit, CPU and IM 306 as link partner
- Four CP 252s

The CP 525 in the S5-155H's subunit A is referred to as CP A_H, the CP 525 in subunit B as CP B_H. The two corresponding CPs in the S5-115U are referred to as CP A_U and CP B_U.

The system is illustrated in Figure 10-1.

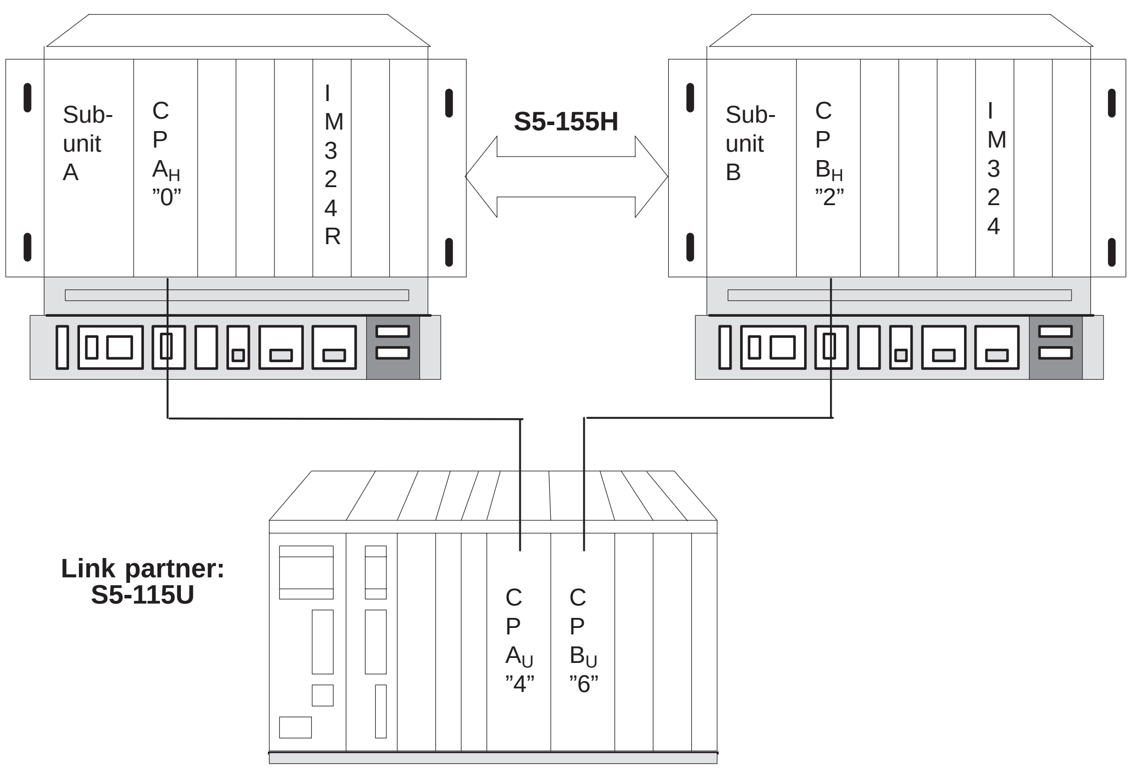


Figure 10-1 Schematic of a Two-Channel Redundant Point-to-Point Link

You must set the addresses over which the CPUs can communicate with their CPs on DIP switches located on the rear of the CPs.

- Set interface number (SSNR) 0 on CP A_H; CP A_H thus reserves pages 0 and 1.
- CP B_H is assigned page numbers 2 and 3, that is, SSNR = 2.
- CP A_U is assigned SSNR 4, CP B_U SSNR 6.

Initializing the CPs with COM 155H and COM 525

Using COM 155H, you must initialize CP A_H in subunit A and CP B_H in subunit B as one-sided CPs, and not as redundant CPs.

The COM 525 parameter initialization software is used to define how the CPs are to function. The two CPs in the U controller are configured only with the COM 525 parameter initialization software in the usual manner.

Programming

H-specific parts of the user program are:

- Restart routine
- Data interchange and
- OB 1.

These are discussed in the following sections.

Restart PLC

Because both subunits have the same user program, but the two CPs for the redundant link (CP A_H and CP B_H) have different page numbers, the SYNCHRON data handling block (DHB) must be invoked conditionally for CP A_H (:JC FB 125) in subunit A.

The same applies to CP B_H in subunit B. Because of SYNCHRON, the CPU knows that the configuration includes a CP.

If the SYNCHRON DHB is not invoked conditionally in both subunits, an error is entered in the PAFE byte (in this case in flag byte 198 or 199).

This ”feature” must be programmed in a restart FB (see Figure 10-2). You must invoke this restart FB in all restart OBs (OB 20, OB 21 and OB 22) so that it will be processed no matter what kind of restart is involved, thus avoiding errors.

STL			Explanation
FBxx			
NAME	:ANLAUF		
	:A F 0.4		CC is subunit A
	:JC	FB 125	
NAME	:SYNCHRON		
SSNR	:KY	0.0	Page no. for CP A_H
BLGR	:KY	0.6	
PAFE	:FY 198		
	:AN F 0.4		CC is subunit B
	:JC	FB 125	
NAME	:SYNCHRON		
SSNR	:KY	0.2	Page no. for CP B_H
BLGR	:KY	0.6	
PAFE	:FY 199		
	:BE		

Figure 10-2 Restart FB for S5-155H

Data Interchange

Data can be interchanged in two directions:

- S5-155H → S5-115U and
- S5-155H ← S5-115U

Data Interchange S5-155H →S5-115U

Depending on how reliable you want the interchange of data to be in a redundant link, you can check both CPs in the S5-115U controller to see if

- any data has arrived at all,
- the same amount of data has arrived in both, or
- the same data has arrived.

The more reliability you want, the more you have to program. In the example, we have kept to the simplest case, which is ”whether any data has arrived at all” (see Figure 10-3). In contrast to a ”simple” link, the user need only

- program Send requests for the CP A_H and CP B_H, and
- program the ”Data test” FB.

FB 252 is the standard FB RECEIVE. For detailed information on FB 252, please refer to Catalog ST 57. On the S5-115U, FB 252 is integrated in the operating system.

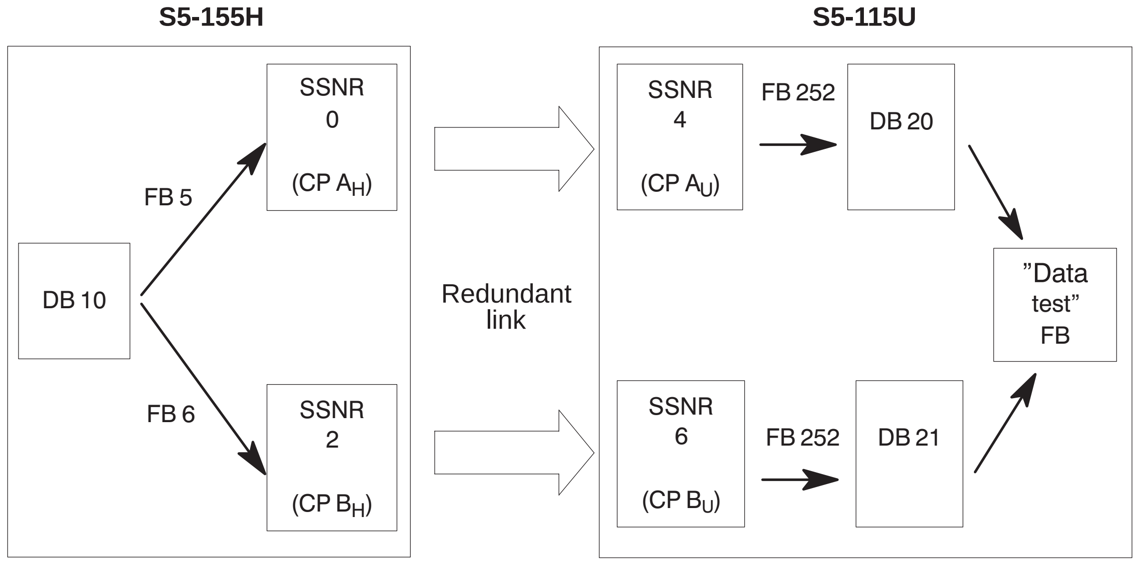


Figure 10-3 Schematic of Data Interchange S5-155H → S5-115U

Send Requests for CP A_H and CP B_H

The user must program SEND requests for CPs A_H and B_H which transfer specific data from DB 10 to the respective page. These requests must be programmed in a function block. In the example, FB 5 is used for CP A_H and FB 6 for CP B_H. In contrast to a standard computer link, the first word in DB 10 is used as frame counter. FB 5 and FB 6 must be called conditionally in the S5-155H's OB 1.

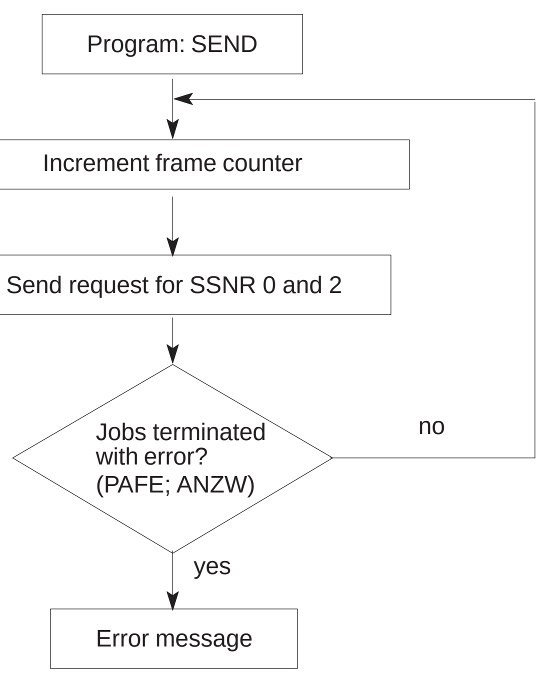


Figure 10-4 Structogram of FB 5 and FB 6

The "Data Test" FB

In the "Data test" FB, the frame counter in the first word of DBs 20 and 21 is used to ascertain whether the two U CPs have received any data at all. If a U CP is not receiving data, the "Data test" FB recognizes this fact and reports it. Figure 10-5 shows a structogram of the "Data test" FB.

You can program this FB both for S5-155H ← S5-115U and S5-155H → S5-115U.

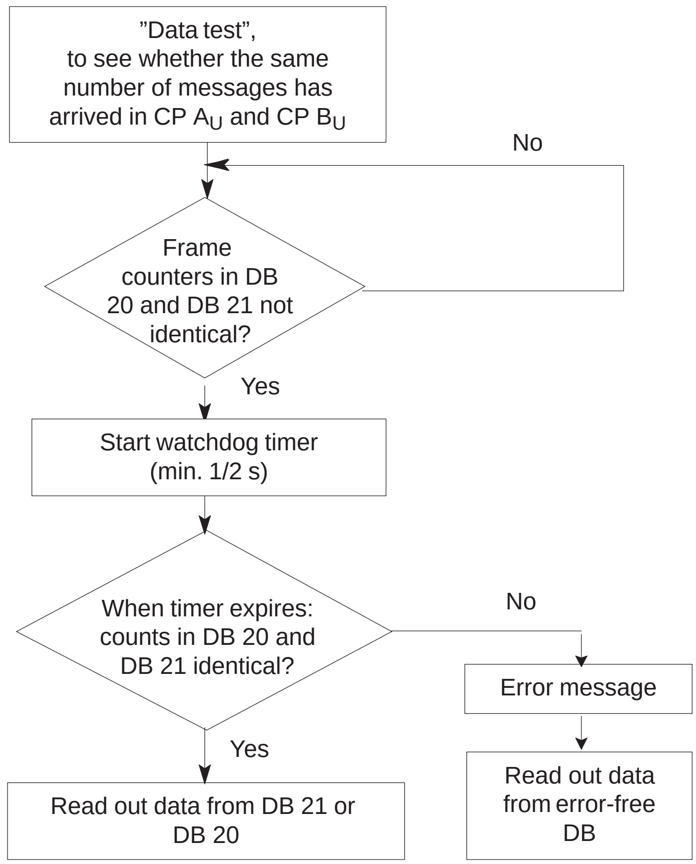


Figure 10-5 Structogram of the "Data Test" FB

Data Interchange S5-155H ← S5-115U

In this case, too, we have taken as an example the simplest case; that is, whether any data has arrived at all. As for S5-155H → S5-115U interchanges, the user must:

- program Send requests for CP A_U and CP B_U, and
- program the "Data test" FB

FB 127 is the standard FB RECEIVE. For detailed information on FB 127, see Catalog ST 57.

Send Requests for CP A_U and CP B_U

In the example (see Figure 10-6), the Send requests for CP A_U and CP B_U are in FB 15 and FB 16. The structograms for FBs 15 and 16 are the same as those for FBs 5 and 6 (see Figure 10-4). FB 15 and FB 16 must be called unconditionally in the S5-115U's OB 1.

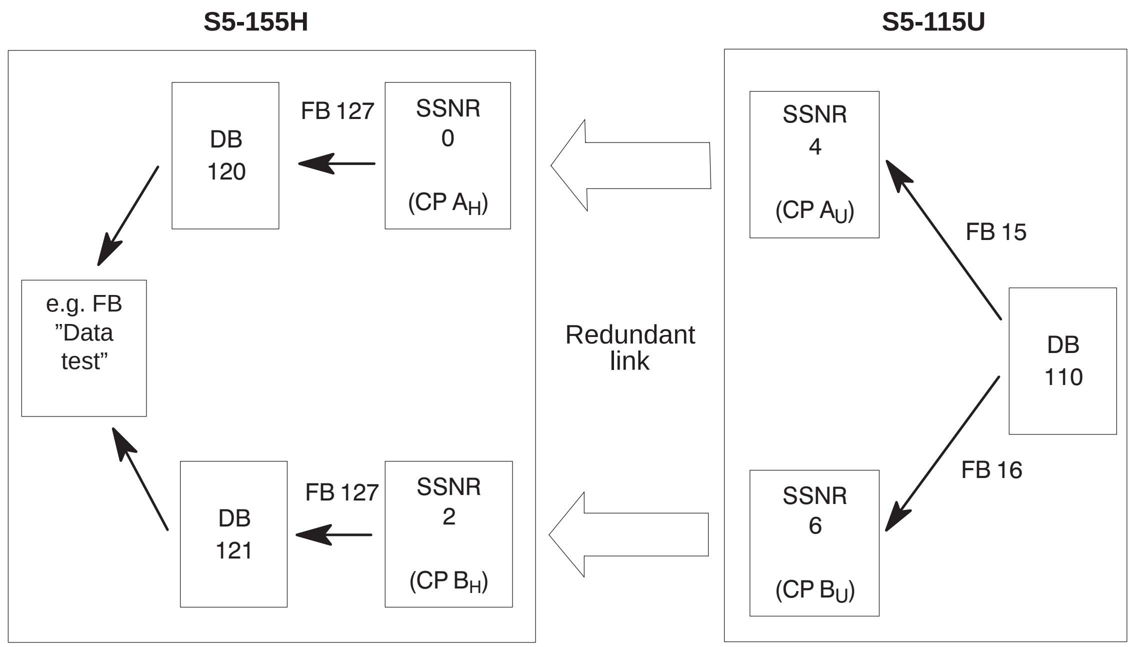


Figure 10-6 Schematic of Data Interchange S5-155H ← S5-115U

OB 1 in the S5-155H

FB 5 for CP A_H and FB 6 for CP B_H are called conditionally in the S5-155H's OB 1, depending on whether the S5-155H is in Redundant mode or subunit A or B is in Solo mode. Figure 10-7 shows you how you can program OB 1.

```
STL                           Explanation
OB 1
...
        :A      F 0.1         PLC in Redundant mode?
        :                     PLC not in Redundant
        :O      F 0.4         mode and subunit A
        :JC FB 5              in RUN mode?
NAME    :SUBUNIT A
        :A      F 0.1         PLC in Redundant mode?
        :                     PLC not in Redundant
        :ON     F 0.4         mode and subunit B
        :JC FB 6              in RUN mode?
NAME    :SUBUNIT B
        :BE
```

Figure 10-7 Conditional Calling of the "Send Requests" in OB 1 of the S5-155H

Switched Redundant Point-to-Point Link

The following hardware is needed:

- One S5-155H in its basic configuration with two IM 304s, connecting cables and terminating resistor connectors (terminators)
- Two EU 185s with four IM 314Rs
- One S5-115U with power supply unit, CPU and IM 306 as link partner
- Four CP 525s.

  The CP 525 in EI 1 of the S5-155H (see Figure 10-8) is referred to as CP 1_H, the one in EU 2 as CP 2_H. The two corresponding CP 525s in the S5-115U are referred to as CP 1_U and CP 2_U.

  – You could also implement the link using one EU 185. Such a system would have a much lower degree of fault tolerance than one with two EUs, however, since the whole EU would have to be shut down to replace a CP.
- You must set the address (page numbers) over which the CPUs communicate with their CPs with DIP switches on the CP modules.
- Set interface number (SSNR) 0 on CP 1_H; CP 1_H thus reserves pages 0 and 1.
- CP 2_H is assigned page numbers 2 and 3; that is, SSNR = 2.
- CP 1_U is assigned SSNR 4, CP 2_U SSNR 6.

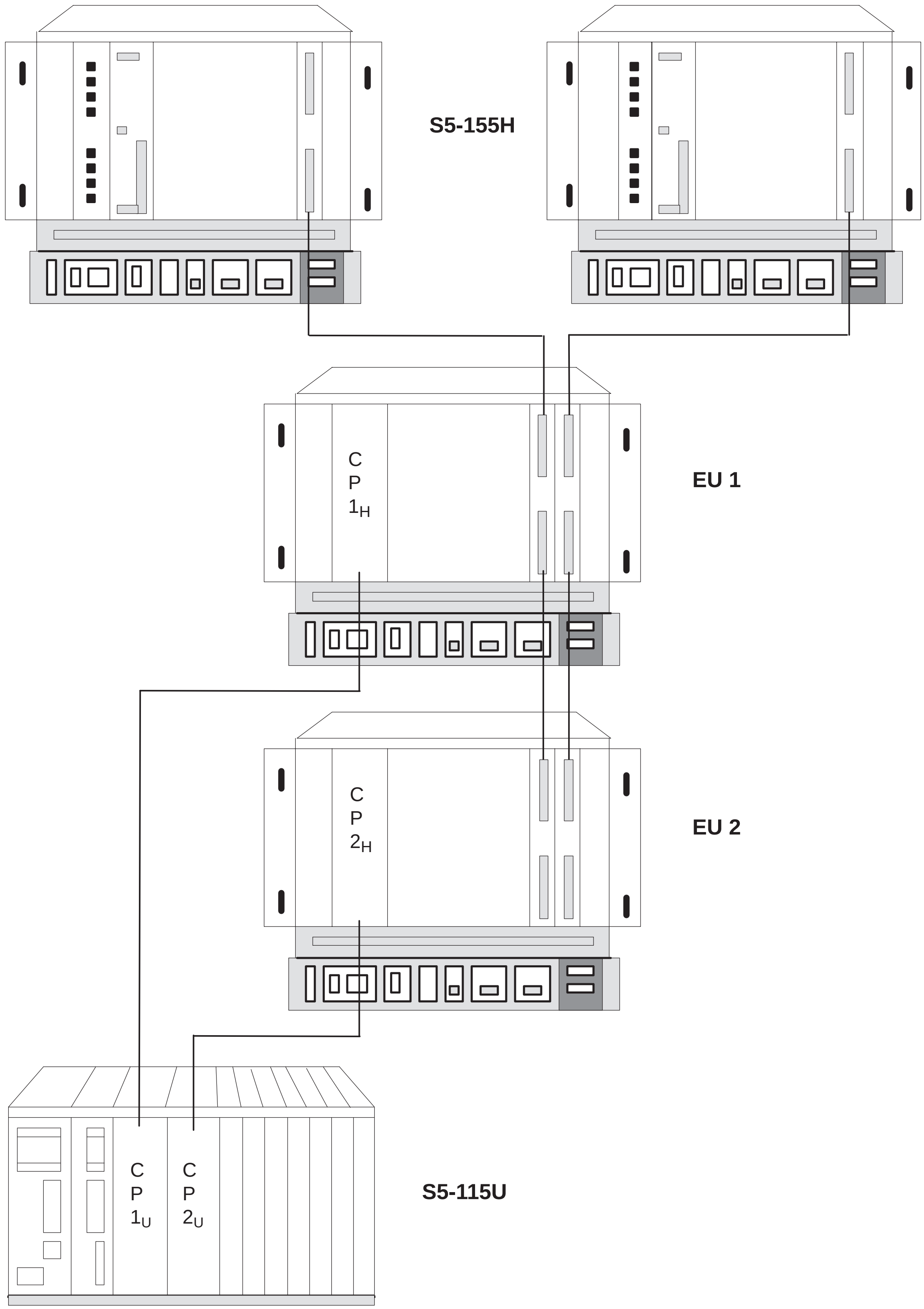


Figure 10-8 Schematic of a Switched Redundant Point-to-Point Link

Parameter Initialization with COM 155H and COM 525

Using COM 155H, CP 1_H and CP 2_H must be configured as switched CPs, not as redundant CPs. You must use the COM 525 parameter initialization software to define how the CPs are to function. The two CPs in the U-series controller are configured only with the COM 525 parameter initialization software.

Programming

H-specific parts of the user program are:

- Restart routine
- Data interchange
- OB 1 and
- Reactivation of a failed CP

PLC Restart

Both subunits have the same user program, but the two CPs for the redundant link (CP 1_H and CP 2_H) have different page numbers. Because CP 1_H and CP 2_H are plugged into switched EUs, the master subunit must be synchronized by invoking FB 125 (:JC FB 125).

If the standby controller also invokes the SYNCHRON data handling block, an error is entered in the PAFE byte (in this case flag byte 198 or 199). You must program this ”feature” in a restart FB (see Figure 10-9). This FB must then be invoked in all restart OBs (OB 20, OB 21 and OB 22) so that it will always be processed, no matter what kind of restart is involved, thus avoiding errors.

STL	Explanation
FBx	
NAME :RESTART	
:A F 0.2	CC is master
:JC FB 125	
NAME :SYNCHRON	
SSNR :KY 0.0	Page no. for CP 1_H
BLGR :KY 0.6	
PAFE :FY 198	
:A F 0.2	CC is master
:JC FB 125	
NAME :SYNCHRON	
SSNR :KY 0.2	Page no. for CP 2_H
BLGR :KY 0.6	
PAFE :FY 199	
... :BE	

Figure 10-9 Restart FB for H Controller

Data Interchange

Data interchange is exactly the same as over the two-channel redundant point-to-point link (see above).

OB 1 in the S5-155H

FB 5 for CP 1_H and FB 6 for CP 2_H are invoked unconditionally in the S5-155H’s OB 1 (see Figure 10-10). FBs 5 and 6 were discussed in detail in Section 10.6.

```
STL                           Explanation
OB 1
...
        :JU     FB 5          FB for CP 1H
...
...
        :JU     FB 6          FB for CP 2H
...
```

Figure 10-10 Absolute Call of the ”Send Requests” in OB 1 of the S5-155H

Reactivating a Failed CP (In-Cycle Synchronization)

Should CP 1_H or CP 2_H fail, it must be reincluded in the process following its repair without a cold or warm CPU restart. This, of course, means that CP synchronization must take place in the current cycle, which in turn means that you must invoke FB (see Figure 10-11) unconditionally in OB 1.

```
STL                       Explanation
        :                 Program for CP 1
        :O F 10.0         F 10.0 must be set when
        :LKT 150.2        CP 1 has been repaired
        :SE T   1         Depassivation takes max. 15 sec.
        :O(
        :L      FY 8      PAFE byte for CP 1
        :L KH   0000
        :><F

        :)                F 10.0 must be set when
        :O F    10.0      CP 1 has been repaired
        :R F    10.0
        :=F     11.0

        :JC     FB
125
NAME    :SYNCHRON         Page no. for CP 1
SSNR    :       KY0.0
BLGR    :       KY0.6
PAFE    :       FY 8      Depassivation requested?
        :A F    11.0      15 sec. elapsed?
        :A T    1         If yes, –> BE, as only one CP can be
        :BEC              activated at a time
        :                 Have 15 sec. elapsed?
        :A F    11.0
        :R F    11.0      Error CP 1 cannot be
        :JC     FBxx      depassivated
        :L KB   0
        :T FY   8
```

Figure 10-11 FB for Reactivating a Failed CP (continued on next page)

STL			**Explanation**
	:		
	:		**Program for CP 2**
	:A F	10.1	F 10.1 must be set when
	:L KT	150.2	CP 2 has been repaired
	:SE T	1	Depassivation takes max. 15 sec.
	:O(		
	:L	FY 9	PAFE byte for CP 2
	:LKH	0000	
	:><F		
	:)		
	:A F	10.1	F 10.1 must be set when
	:R F	10.1	CP 2 has been repaired
	:=F	11.1	
	:JC	FB	
125			
NAME	:SYNCHRON		Page no. for CP 2
SSNR	:	KY0.2	
BLGR	:	KY0.6	
PAFE	:	FY 9	Only one CP may be activated at a time
	:A T	1	
	:BEC		
	:		
	:A F	11.1	Error CP 2 cannot be depassivated
	:R F	11.1	
	:JC	FBxx	
	:L KB	0	**Program for CP 3**
	:T FY	9	
	:		
	:		

Figure 10-11 continued

Technical Specifications: IM 314R / IM 324R

11

This chapter contains the technical specifications of the IM 314R and IM 324R interface modules.

11.1 Technical Specifications of the IM 314R Interface Module

The electronics are accommodated on a printed-circuit board in double-height Eurocard format. There are two 48-pin connectors of range 2 to connect the module to the S5 bus of the expansion unit. The frontplate of the module is 1 1/3 standard slots wide and has two 50-pin D-type connectors for the symmetrical cable (6ES5 721-0xxx0) and four LEDs.

Supply voltage:	+ 5 V ± 5%
Current consumption:	approx. 900 mA
Timeout for internal registers:	approx. 10 µs
Max. cable length from IM 304 to the last IM 314R	600 m
Max. potential difference between H components (equipotential bonding conductor to design regulations):	5 V
Max. number of IM 314Rs on the bus:	4
Weight:	approx. 350 g
Dimensions:	160 mm x 233.4 mm
Width of frontplate:	20.32 mm
Front connector:	Two 50-pin male connectors
Backplane connector:	Two 48-pin ES 902, range 2

Ambient Conditions

Operating temperature range: (Operation without fan permissible, but natural convection must be guaranteed)	0 °C to 55 °C (32 °F to 131 °F)
Non-operating temperature:	– 40 °C to + 70 °C (– 40 °F to + 158 °F)
Max. relative humidity:	95 % at 25 °C (77 °F), no condensation
Max. operating altitude:	3500 m above sea-level

Connector Pin Assignment

Pin		Pin		Pin	
1	Shield	18	+AD 8	34	+MEMR/
2	+AD 12	19	- AD 8	35	- MEMR/
3	- AD12	20	+AD 9	36	+MEMW/
4	+AD 13	21	- AD 9	37	- MEMW/
5	- AD13	22	+AD 10	38	+ALE
6	+AD 14	23	- AD10	39	- ALE
7	- AD14	24	+AD 11	40	+BASP
8	+AD 15	25	- AD11	41	- BASP
9	- AD15	26	+AD 3	42	+AD 0
10	+AD 6	27	- AD 3	43	- AD 0
11	- AD 6	28	+AD 4	44	+AD 1
12	+AD 7	29	- AD 4	45	- AD 1
13	- AD 7	30	+AD 5	46	+AD 2
14	+PEU	31	- AD 5	47	- AD 2
15	- PEU	32	+ZGU	48	+RDY/
16	P’	33	- ZGU	49	- RDY/
17	Shield			50	Ground

Figure 11-1 IM 314R: Pin Assignment of the X3 and X4 Front Connectors

Pin	d	b	z
2	Shield	M	+5 V
4		PESP	
6	A12	A 0	CPKL/*RESET
8	A13	A 1	MEMR/
10	A14	A 2	MEMW/
12	A15	A 3	RDY/
14		A 4	D 0
16		A 5	D 1
18		A 6	D 2
20		A 7	D 3
22		A 8	D 4
24		A 9	D 5
26		A10	D 6
28		A11	D 7
30	M	BASP	
32	BASPA/	M	M

Figure 11-2 IM 314R: Pin Assignment of the X1 Backplane Connector

Pin	d	b	z
2		M	+5 V
4		SA 0	NA 0
6	(CPKL/)	SA 1	NA 1
8		SA 2	NA 2
10		SA 3	NA 3
12	+5 V		
14	+5 V		
16			
18		NAU/	
20			
22		M	M
24			
26			
28			
30			
32		M	M

Figure 11-3 IM 314R: Pin Assignment of the X2 Backplane Connector

11.2 Technical Specifications of the IM 324R Interface Module

The electronics are accommodated on a printed-circuit board of double-height Eurocard format. There are two 48-pin connectors of range 2 to connect the module to the S5 bus of the expansion unit. The frontplate of the module is 1 1/3 standard slots wide and has two 50-pin D-type connectors for the symmetrical cable (6ES5 721-....). The frontplate also has a green LED and a connector for module replacement during operation (NON-STOP mode). The module also contains MOS components that are sensitive to electrostatic charge:

Supply voltage: + 5 V ± 5%

Current consumption:	approx. 1000 mA
Memory capacity in the S5-155H:	4 x Kwords
Memory capacity in the S5-115H:	4 x Kwords
Max. access time (with one-sided RAM access:	100 ns
Response time (S5 bus): *)	approx. 300 ns
Response time (PK bus): *)	approx. 500 ns
Max. cable length from IM 304 to IM 324R:	100 m
Weight:	approx. 350 g
Dimensions:	160 mm x 233.4 mm
Front plate width:	20.32 mm
Front connector (X4, bottom):	50-pin, male connector
Backplane connector:	Two 48-pin ES 902, range 2
Frontplate connector, top (for power supply when replacing modules)	24 VDC ± 7 V 14 mA ± 6 m

Ambient Conditions

Operating temperature range: (Operation without fan permissible, but natural convection must be guaranteed)	0 °C to 55 °C (32 °F to 131 °F)
Non-operating temperature:	– 40 °C to + 70 °C (– 40 °F to + 158 °F)
Max. relative humidity:	95% at 25 °C (77 °F), no condensation
Max. operating altitude:	3500 m above sea-level

*) The response time is the time between the falling edge of the memory read (MEMR) or memory write (MEMW) signal at the IM 324R input and the falling edge of the ready (RDY) signal generated by the IM 324R, provided the RAM is not accessed by the other subunit.

Connector Pin Assignment

Note: The signals in parentheses are not transmitted via the interface.

Pin		Pin		Pin	
1	Shield	18	+AD 8	34	+MEMR/
2	+AD 12	19	- AD 8	35	- MEMR/
3	- AD 12	20	+AD 9	36	+MEMW/
4	+AD 13	21	- AD 9	37	- MEMW/
5	- AD 13	22	+AD 10	38	+ALE
6	+AD 14	23	- AD 10	39	- ALE
7	- AD 14	24	+AD 11	40	+BASP
8	+AD 15	25	- AD 11	41	- BASP
9	- AD 15	26	+AD 3	42	+AD 0
10	+AD 6	27	- AD 3	43	- AD 0
11	- AD 6	28	+AD 4	44	+AD 1
12	+AD 7	29	- AD 4	45	- AD 1
13	- AD 7	30	+AD 5	46	+AD 2
14	+(PEU)	31	- AD 5	47	- AD 2
15	- (PEU)	32	+ZGU	48	+RDY/
16	p’	33	- ZGU	49	- RDY/
17	Shield			50	Ground

Figure 11-4 IM 324R: Pin Assignment of the X4 Front Connector

Pin	d	b	z
2	Shield	M	+5 V
4			
6	A12	A 0	CPKL/*RESET
8	A13	A 1	MEMR/
10	A14	A 2	MEMW/
12	A15	A 3	RDY/
14		A 4	D 0
16		A 5	D 1
18		A 6	D 2
20		A 7	D 3
22		A 8	D 4
24		A 9	D 5
26		A10	D 6
28	DSI/	A11	D 7
30		BASP	
32	BASPA/	M	

Figure 11-5 IM 324R: Pin Assignment of the X1 Backplane Connector

Pin	d	b	z
2		M	+5 V
4		D 8	D 12
6	M	D 9	D 13
8		D 10	D14
10		D 11	D 15
12			
14			NAU/
16			
18			
20			
22			
24			
26			
28			
30			
32		M	

Spare Parts

Coding plug C79334-A3011-B11

11.3 Readback Delays

Digital Input Modules

6ES5 420	:	30 ms each
6ES5 430	:	
6ES5 431	:	
6ES5 434	:	
6ES5 435	:	
6ES5 436	:	

Digital Output Modules

6ES5 441	:	30 ms each
6ES5 451	:	
6ES5 453	:	
6ES5 454	:	
6ES5 455	:	
6ES5 456	:	
6ES5 457	:	
6ES5 458	:	
Total readback delay		60 ms

For redundant 220 V digital modules, the readback delay must be at least 100 ms.

When using the ET 100U/ET 200U, the readback delay must be at least $2t_{h\ max}$. Please refer to the manual ”ET 100U/ET 200U Distributed I/O System” for methods of calculating the value $t_{h\ max}$.

12 Glossary

The Glossary, whose contents are listed in alphabetical order, defines the most important 155H-specific terms and functions. Use the keyword index to find additional information on all terms and topics in the main body of the manual.

Configuring Block DX 1

The system program stores all configuring data entered with COM 155H during a configuring session at the programmer in data block DX 1. For this reason, DX 1 may be used for no other purpose.

An S5-155H can operate only when DX 1 has been loaded.

Depassivation

’Depassivation’ is the opposite of ’passivation’, and therefore revokes the former. The tests are also reactivated. Following repairs (module replacement), depassivation must be initiated.

Discrepancy Value

For a redundant analog input, you may configure a value to serve as the maximum amount by which analog value A (subunit A) may differ from analog value B (subunit B). The ’discrepancy value’ is composed of an absolute portion and a relative portion. Only when this value is exceeded (and the configured discrepancy time has elapsed) does the 155H system program recognize an error.

Discrepancy Time

Redundant digital or analog inputs can show different signal states or input values within a relatively short space of time. The ’discrepancy time’ is the time period during which the 155H system program will tolerate different signal states or input values. The default discrepancy time is 0.05 s, but the user may set it to a value between 0.01 and 320 s. The system program does not recognize an error until this time has elapsed.

Error Locating

Because of a series of comprehensive self-tests, the 155H system program cannot only detect errors and faults quickly, but can also locate them. With the aid of this facility, it is possible to find out which modules are defective and must be replaced.

A special error locating facility (or LF) must be configured for digital I/Os which are to be operated on a NON-STOP basis. As soon as a defective module has been located, the 155H system program automatically shuts that module down and operation from that point on is one-sided.

Error Search Mode

’Error Search’ mode is invoked when the 155H system program finds discrepancies between the RAM contents or process images in master and standby. In this mode, the master scans the cyclic user program while the standby executes the self-test to locate the problem.

Group Power Supply

A ’group’ constitutes all sensors for redundant digital inputs (DIs) or digital outputs (DQs) that are served by the same locating digital output (L-DQ). The smallest possible group consists of **one** redundant DI or DQ byte, the largest possible group of **all** redundant DIs or DQs in an S5-155H controller.

H Flag Word

The user specifies the number of the ’H flag word’ during his configuring session with COM 155H. This flag word comprise a status byte and a control byte. The system program uses the status byte to store important information on the current status of the controller. The control byte can be used for making important requests via the STEP 5 program.

H Flag Doubleword

The user specifies the number of the ’H flag doubleword’ during his configuring session with COM 155H. Its contents are of no consequence. If no number is specified for the flag doubleword, each entry in the error data block is automatically stamped with the current date and time from the internal CPU clock.

Each time it makes an entry in the error data block, the 155H system program copies the contents of the flag doubleword to the 6th and 7th data word of each error record.

Intermittent Outputs

In contrast to a non-intermittent output, an output is said to be intermittent when it changes its signal state at least once every hour.

Locating Facility (LF)

The ’locating facility’ locates errors on redundant digital input/output modules.

For each redundant digital input or output for which the 155H system program is not only to detect but also to locate errors, the user must configure one additional input and one additional output.

NON-STOP Operation

The S5-155H tolerates the first failure of each redundant hardware component. The defective components can thus be repaired or replaced without having to interrupt program processing.

Passivation

When a redundant I/O module or communications processor (CP) fails, the 155H system program, after locating the problem, shuts it down (that is, passivates it) and operation is one-sided until depassivation takes place.

When an I/O module has to be passivated, the associated group power supply sometimes has to be shut down, thus passivating all other redundant modules that share the same power supply.

Once the module goes back on line, it must be depassivated.

Depassivation is usually done in the Restart routine in response to a user request. The relevant bit is set in the H flag word (acknowledgement key).

Readback Delay

The digital readback inputs (R-DIs) detect errors in redundant digital outputs. The 'readback delay' is the amount of time by which the digital readback inputs (R-DIs) should be delayed.

This delay makes it possible to take into account the different signal propagation times of the various digital output modules. The default readback delay is 0.01 s, but the user may define a delay of from 0.01 to 1.0 s with COM 155H. If the specified readback delay is shorter than the scan cycle time, the 155H system program takes the scan time as readback delay time.

Redundant Mode

When the S5-155H operates in Redundant mode, the master controls the process. The standby is updated at each synchronization point and checks to make sure that the master is still functioning properly. If the standby controller detects a fault in the master, it simply takes over control.

Redundant I/Os

An I/O module is 'redundant' when it is 'double', i.e. when it has the same address in both subunits. If one of the two I/O modules or subunits fails, the failure is tolerated and their is no interruption in the process. The defective module is reported and can then be replaced or repaired.

Self-Test

The S5-155H supports NON-STOP operation of redundant components with a number of comprehensive self-tests. These check the contents and state of the CPUs and I/Os and make comparisons between the two subunits. The tests execute in the background, and are transparent to the other software, until a hardware failure is detected and located. Every problem detected by the self-tests is reported.

Standby Activation

When the master controller is in Cyclic mode and the standby controller is to be (re)-instated in the process, for instance during a restart or error search, the 155H system program provides the standby with all of the data from the master. If necessary, it even transfers the whole user program from the master to the standby controller (as long as the program is in RAM).

The transfer of this static data can take **several cycles**. The standby controller is then updated; that is, within one cycle, it is given the master's dynamic data (see 'Updating'). The standby activation phase is complete when the internal states of master and standby are identical.

Standby-Master Switchover

Certain events necessitate making the standby the new master, and 'demoting' the master to standby status.

In Redundant mode, for instance, when the standby detects a fault in the master controller, the standby takes control as soon as the activation phase has been completed.

The event-driven synchronization of the two subunits ensures that bumpless switchover is possible at any time.

Solo Mode

In ’Solo mode’, the master controls the process alone. The standby is at STOP or in Error Search mode, and does not participate in the process.

In Solo mode, the S5-155H is like an S5-155U; that is, the two subunits are not synchronized, but the master continues to execute the self-tests on its own.

Stuck at 0 and Stuck at 1 Errors

A certain input or output shows stuck at 0 or stuck at 1, and can no longer reacts to a signal change. The 155H system program continually checks all redundant input and outputs for stuck at 0 or stuck at 1.

Synchronization Points

Whever an event occurs which can result in the master and the standby having different internal states, the subunits are synchronized. They are, for instance, synchronized after every direct access operation, timer scan, and a process or timed interrupt. In the case of interrupts, the ’synchronization point’ is always the next block change.

The 155H system program monitors each synchronization point. A check is made to make sure that both subunits are still working and that they are both processing the same operation.

Test Slices

The S5-155H’s self-test comprises approximately 300 ’test slices’ of 2 ms duration each. The user can specify the exact number of test slices to be processed per cycle with COM 155H. The default value is one test slice per cycle, but the user may select a number between 1 and 19.

Transfer Data

’Transfer data’ are the DB and DX data blocks whose contents are modified during processing of the STEP 5 program. The 155H system program must transfer all of these blocks from the master to the standby every time the standby controller is updated in order to ensure that the two subunits always have the same data.

The numbers of the DB and DX data blocks to be transferred must be specified in a COM 155H session at the programmer.

Updating

Updating is understood to be the procedure, undertaken by the 155H system program, of copying the dynamic data from the master controller, which is in RUN mode, to the standby controller **within one cycle**.

Updating is part of ”standby activation”, and is regarded as completed when the internal states of master and standby are identical.

Abbreviations

This appendix lists and explains the abbreviations and mnemonics used throughout this manual.

A-NR	Job number
ABS	Absolute value
ADF	Addressing error
AI	Analog input
AGF	PLC error
AMA	Subunit is master
ANZW	Condition codeword
AQ	Analog output
AS	Absolute addressing
BASP	Command output disable
BCD	Binary coded decimal number
BLGR	Frame size
BS	System data area
BSTACK	Block stack
BSU	Bit slice unit
C	Counter
CC	Central controller
CP	Communications processor
CPU	Central processing unit
DB	Data block
DBNR	Data block no., DX no., no. of the address area (for IA operation)
DHB	Standard data handling block
DI	Digital input
DQ	Digital output
DW	Data word
DX	Extended data block
E-DB	Error data block
EPROM	Erasable programmable read-only memory
ESC	Escape
EU	Expansion unit

F	Flag (bit)
FB	Function block
FD	Floppy disk (diskette, drive)
FX	Extended function block
G DB	STEP 5 operation ”Generate data block”
GP	Global I/Os, virtual memory area that can be mapped to unassigned I/O areas of the individual SINEC L2 stations
HW	Hardware
I	Input module
I/O	Input/output
IB	Input byte, parameter for source/destination data of the process input image
IF	Interface
IM	Interface module
INT	Interrupt
IP	Intelligent input/output module
ISTACK	Interrupt stack
KF	Fixed-point constant
L-DI	Locating digital input
L-DQ	Locating digital output
LAN	Local area network
LED	Light-emitting diode
MAI	Memory and interface
MB	Flag area (F)
MFDT	Mean failure detection time
MTTF	Mean time to failure
MUART	Multifunction universal asynchronous receiver transmitter
NAU	Power failure
NN	No source/destination parameters at block

OB	Organization block
O-I/O	Extended I/O area (F F100 ... F F1FF)
OS	Operating system
OY	Peripheral byte (extended)
P-I/O	I/O area (F F000 ... F F0FF)
PAFE	Parameter assignment error
PARE	Parity error
PB	Parameter for source/destination data from/in I/O modules
PEU	EU power supply failure
PG	Programmer
PI	Process image
PII	Process input image
PIQ	Process output image
PLC	Programmable controller
PY	Periferal byte
Q	Output module
QANF	Relative start address within the type
QB	Output byte, parameter for source/target data of the process output image
QLAE	Number (length) of source data
QTYP	Type of data source
QVZ	Timeout
R-DI	Readback digital input
RALU	Registered Arithmetic Logic Unit
RAM	Random access memory
REL	Relative value in %
RLO	Result of logic operation
RT	Extended system data area
RW	Read/write
SAC	STEP 5 address counter
SB	Sequence block

SPS	Standard slot
SS	Interface
SSNR	Interface number
STP	Stop at end of cycle
STS	Direct stop
STUEB	Block stack overflow
STUEU	Interrupt stack overflow
SUF	Substitution error
T	Timer
TLAF	Transfer load error
XX	Type identifier for indirect parameter assignment
ZANF	Relative start address within the type
ZLAE	Number (length) of target data
ZTYP	Type of data target

Index

Note:
The page numbers following the terms and search keys of this index are preceded by a I, II or III (Roman numerals), which stands for the part of the manual containing the corresponding information.

The individual parts of the manual are separated by a red page.

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SIEMENS

SIMATIC S5

Data Handling Blocks for the CPU 948R (Standard Function Blocks)

Reference Manual
(S5-155H, Part II)

C79000-B8576-C134-05

Safety Guidelines

This manual contains notices which you should observe to ensure your own personal safety, as well as to protect the product and connected equipment. These notices are highlighted in the manual by a warning triangle and are marked as follows according to the level of danger:

Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

Caution

indicates that minor personal injury or property damage can result if proper precautions are not taken.

Note

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

The device/system may only be set up and operated in conjunction with this manual.

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground, and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

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Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

Preface (How to Use This Manual)

In SIMATIC S5 programmable controllers, specific tasks are handled by special modules such as communications processors and intelligent I/O modules. Data exchange between these modules and the CPUs is implemented by data handling blocks (DHBs).

This part contains a general introduction to, and instructions for, assigning parameters to the data handling blocks (FBs), followed by a description of how to evaluate the output parameters and detailed function descriptions of the data handling blocks for the CPU 948R (S5-155H).

Target Group

This Reference Manual is aimed at programmers with special system knowledge. If you have any questions which are not answered by the Reference Manual, please contact your local Siemens representative.

Notes on the Contents

The information below concerning the contents of the individual chapters is designed to make using this Reference Manual easier.

Chapter 1: Using the Data Handling Blocks

This chapter gives you basic information concerning the functions, possible applications and principle of operation of the CPU 948R data handling blocks. The introduction is followed by a description of the program sequence with data exchange via the data handling blocks.

Chapter 2: Assigning Parameters to the Data Handling Blocks

This chapter contains general statements concerning parameter assignment of the data handling blocks, the meaning of the parameters, methods of parameter passing and the types of parameter assignment with examples of direct and indirect parameter assignment.

The structure of the function block parameters is explained, especially the source and destination parameters, with reference to the different types of parameter assignment.

Chapter 3: Data Handling Blocks in the User Program

This chapter contains important notes for working with data handling blocks in the user program and for using data blocks in different functions.

It tells you how to calculate the available area length remaining for data transfer and also offers information on the execution time of the data handling blocks.

Chapter 4: Description: Data Handling Blocks

This chapter shows every available handling block with block diagram, parameter table and detailed functional description.

Index

The alphabetical index at the end of the manual will help you locate the most important terms in the manual.

Remarks Form

The (green) remarks form at the end of the manual is provided for your comments and recommendations.

Reference Literature

See the Preface to ”S5-155H Programmable Controller” (Part I) in this manual.

Contents

Using the Data Handling Blocks 1

This chapter contains basic information concerning the functions, possible applications and principle of operation of the data handling blocks.

1.1 Introduction

SIMATIC S5 Communications

With the SIMATIC S5 programmable controller, tasks such as operator interfacing or bus links are supported by specific modules. The CP 143, for instance, is used for linking programmable controllers to the SINEC H1 bus-type local area network (LAN). In addition to such communications processors (CPs), intelligent I/O modules (IPs) are also used, for example, for closed-loop control and positioning.

The data handling blocks enable CPU ↔ CP and CPU ↔ IP communications (see Figure 1-1), but not between the CP and/or IP. These are function blocks which can be called up and assigned their parameters by the user.

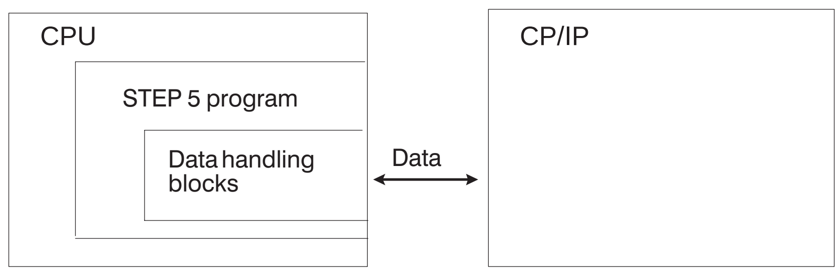


Figure 1-1 Data Communication between the CPU and the Intelligent I/Os

For reasons of simplicity, ”CPU” will often be used below to refer to the CPU 948R and ”CP” to refer to CPs and IPs using data handling blocks.

Configuration

The CPU accesses I/O modules via the S5 bus (read inputs, write outputs), using certain STEP 5 statements or instructions (L PW, T PW). Data exchange between CPU and CPs is carried out in a similar way.

The most important component of a CP module is a special memory (dual-port RAM, of which there may be several). The CPs themselves do not use the S5 bus, but fetch from the dual-port RAMs information stored there by the data handling blocks, or they store information there which is read by the data handling blocks.

The dual-port RAM itself and the hardware and/or software facilities which write data to the dual-port RAM and read data from the dual-port RAM and which establish the link with the actual CP (function) will be referred to below as the ”interface”. An interface is selected with the ”SSNR” parameter (interface number, see parameter description).

The CP function could, for example, be the editing of data which it has received via the dual-port RAM or via the interface and transferring this data to a monitor or a bus. In this case, too, ”interfaces” may possibly be used, but these should not be confused with those mentioned above!

Depending on their type, the CPs contain one or more dual-port RAMs or interfaces.

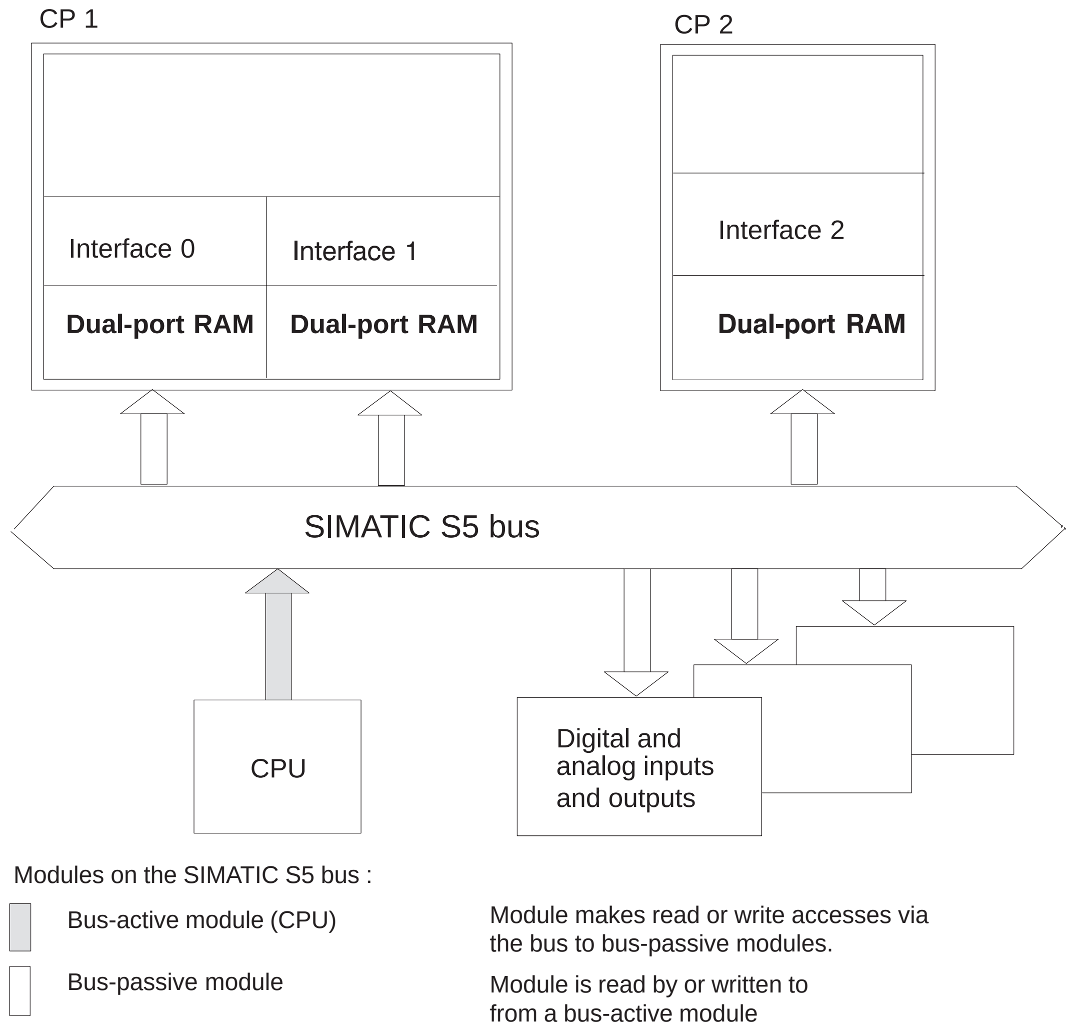


Figure 1-2 Basic Principle of a Configuration with Three CPs with a Total of Two Interfaces

The ”DHBs for CPU 948R”

All CP/IP operating modes, one-sided and switched, are possible using the programming package ”Data Handling Blocks for the CPU 948R”.

The data handling blocks for the S5-155H are included in the scope of supply of the COM 155H programmer software and are located on diskette in the program file S5CR70ST.S5D. The data handling blocks are called up and the condition codes are evaluated in the same way as for the S5-155U.

Special features of the 155H DHBs compared to the 155U DHBs

- The CPs can be synchronized both at startup (OB 20, 21, 22) **and also in the cycle** (see: Calling the DHB SYNCHRON in the cycle).
- When assigning the source and destination type parameters, the specification ”PY” (I/O (peripheral) byte) is permissible **only** for switched I/O. Both the CPs/IPs and the I/Os are then operated in switched mode.

Function Blocks

The following data handling blocks are available to the CPU 948R for the purpose of transferring data, parameters and control/status information from the CP/IP (more precisely, from the dual-port RAM) and to the CP/IP:

Function Block	Name	Function	Length
FB 120	SEND	Send data	approx. 3200 words 1)
FB 121	RECEIVE	Receive data	approx. 3200 words
FB 122	FETCH	Fetch job	approx. 1600 words
FB 123	CONTROL	Status inquiry	approx. 800 words
FB 124	RESET	Reset	approx. 600 words
FB 125	SYNCHRON	Initialize	approx. 600 words
FB 126	SEND-A	Send data	approx. 2400 words
FB 127	REC-A	Receive data	approx. 2400 words

1) 1 word = 2 bytes = 16 bits

Note:
It is possible to change the function block numbers (but not those of the FX function blocks).

Data Handling Blocks, Functions

The data handling blocks are used in the extended area of the system data (RT area) and do not call data blocks.

The handling blocks access flags or data words or other areas which are used as parameters or contain parameters or the data to be transmitted or received.

In the same way, the handling blocks influence the result bits (CC 1, RLO etc.). Once processing of a handling block is completed, all result bits except RLO (result of logic operation) are irrelevant. RLO is designed as an error bit and can be set (error) or cleared (no error).

The accumulator contents (ACCU 1, ACCU 2, etc.) can be changed by means of the handling blocks.

Addressing the Dual-Port RAMs

The information in this section will be required for the jumper setting on the CP modules. Individual CP descriptions are contained in the relevant chapters:

Addressing procedure for data handling blocks:

”Page frame” addressing; the page number is identical to the parameter ”SSNR” or interface number (see Section 2.3 Parameter Description).

1.2 Program Sequence

Data Exchange

A special coordination procedure enables different types of data/parameters to be transmitted in both directions via an interface (a dual-port RAM). This procedure is known as ”handshaking”.

The SEND, SEND-A, RECEIVE, REC-A, FETCH and RESET blocks only carry out handshaking if the control/status information read in previously requires and permits it. Otherwise, if there is no handshaking, the block is ”idling”.

The CONTROL block is restricted to the reading of status information. It does not carry out a handshake.

SYNCHRON block: see below.

Initializing an Interface

Provision must be made for interlocking the SYNCHRON DHB (FB 125) when initializing, either in one-sided or switched I/O, depending on the type of application of the CP.

Every interface must first be initialized by means of a SYNCHRON. This includes erasing/pre-programming of the dual-port RAM. This data handling block can be called up during restart; that is, during a cold restart or cold restart with memory (restart OBs: OB 20, OB 21, OB 22), and also during restart from ”soft STOP” (OB 38) and in the cycle.

The remaining SEND, SEND-A, RECEIVE, REC-A, FETCH, CONTROL and RESET handling blocks can only communicate properly with an interface if this interface has previously been initialized without error.

Cold Restart, Cold Restart with Memory

If an interrupt has occurred when processing a data handling block, the handling block will **not** be continued at the interrupt point in the case of a cold restart with memory. Instead, OB 1 is processed from the beginning. This means:

Cold restart with memory of the CPU can be used; the CPs must be re-initialized.

Passivation of CP

In the event of an error, the CP affected is passivated. It then no longer carries out data transfer.

Depassivation of the interfaces is handled as usual via the H flag control byte.

Assigning Parameters to the Data Handling Blocks

2

This chapter contains statements concerning the parameter assignment of the data handling blocks, the meaning of the parameters, the methods of parameter transfer and the types of parameter assignment with examples of direct and indirect parameter assignment.

The structure of the function block parameters is described, especially the source and destination parameters, with reference to the different types of parameter assignment. The error bits which occur in the event of errors in processing the handling blocks and the meaning of the bit values are explained.

2.1 Parameters and Function of the Data Handling Blocks

Parameters and Parameter Passing

Parameters are assigned to all the handling blocks by a uniform procedure. The function block parameters will therefore be described in detail in this chapter. These are the parameters used:

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Job number
ANZW	I	W	Condition codeword
BLGR	D	KY	Frame size
QTYP/ZTYP	D	KS	Type of data source/data destination
DBNR	D	KY	Data block number: DB no. or DX no. or number of the address area (AS operations)
QANF/ZANF	D	KF	Relative start address within the type of data
QLAE/ZLAE	D	KF	Number (length) of the source/destination data
PAFE	Q	BY	Byte for parameter assignment errors
RLO			Result of logic operation, RLO bit, is used as an additional parameter

Each data handling block carries out a specific function. The SEND block, for example, is designed for data transfer from a CPU to a CP. Parameters determine which data is to be transferred. There are different ways of passing parameters to data handling blocks:

- Parameters at the function block
  The actual parameters specified with the function block call are used immediately. This procedure is called **direct parameter assignment**.
- Parameters in the data block
  The actual parameters of the function block call point to data words in a DB/DX data block. The data handling block uses the parameters contained in these data words. This procedure is called **indirect parameter assignment**.
- Parameters from the CP
  The CP provides the data handling block with the parameters required. The actual parameters of the function block call are irrelevant.

Depending on the method of passing the parameters and on the function, only some of the actual parameters may be required at the function block. In this case, values without any relevant meaning can be assigned as dummy parameters. It is also possible to use a block call with a reduced number of parameters (see SEND-A, REC-A).

Rule:
Parameters and/or flag words/data words which are completely irrelevant may contain any values. Parameters and/or flag words/data words which only contain the information of one byte must have ”0” in the high-order byte.

2.2 Direct and Indirect Parameter Assignment

Parameter Assignment Types

As the table below shows, assignment of the function block parameters to the data handling blocks is clearly divided into three sections (parameter assignment groups).

	Data Handling Block									
FB Parameter	**SEND**	**SEND-A**	**RE-CEIVE**	**REC-A**	**FETCH**	**CON-TROL**	**RESET**	**SYN-CHRO NOUS**		
SSNR	x	x	x	x	x	x	x	x	SSNR	Section 1
A-NR	x	x	x	x	x	x	x	x	BLGR	
ANZW	x	x	x	x	x	x			ANZW	
QTYP	x		x		x				ZTYP	Section 2
DBNR	x		x		x				DBNR	
QANF	x		x		x				ZANF	
ALAE	x		x		x				ZLAE	
PAFE	x	x	x	x	x	x	x	x	PAFE	Section 3

The parameters of section 1 can either be specified directly or indirectly (the procedure, once selected, has to apply to all the parameters of the section).

Independent of section 1, the parameters of section 2 can also be specified directly or indirectly (same restriction as above) or are passed to the handling block by the CP.

Only the PAFE byte (chapter 3) is always directly specified.

With direct parameter assignment, the data handling block immediately processes the parameters specified in the block call. With indirect parameter assignment, a pointer to a parameter field is passed with the block parameters to the handling block. The ”actual” parameters are located here in an unbroken sequence, and the order is the same as with direct parameter assignment.

Assigning Parameters to the SSNR, A-NR, ANZW and BLGR

The high-order byte of the SSNR parameter is used as the changeover criterion for direct/indirect parameter assignment (see example).

- **SSNR high-order byte = 0: direct parameter assignment**

  SSNR, A-NR and ANZW or BLGR (if the data handling block knows both these parameters) are actual parameters of the function block.

- **SSNR high-order byte ≠ 0: indirect parameter assignment**

  SSNR, A-NR and ANZW or BLGR (if the data handling block knows both these parameters) are stored in the selected data block (DB or DX) starting at the data word specified by the low-order byte of the actual parameter of SSNR.

SSNR and A-NR have the same data format (KY) in both types of parameter assignment. With the ANZW condition codeword, the formats differ. Whereas with direct parameter assignment, the address of the condition codeword is specified in STEP 5 notation (for example, FW 100, DW 17), with indirect parameter assignment, a doubleword is available. In the first data word, the area is in the KS data format (ASCII characters):

- FW stands for condition codeword in the flag area
- DB stands for condition codeword in the DB data block
- DX stands for condition codeword in the DX data block

In the second data word, the ANZW address is in the KY data format, and in the case of DB or DX, the block number is also included in the high-order byte.

Examples of Assigning Parameters to the SSNR, A-NR and ANZW

a) Direct assigning of parameters to the SSNR, A-NR and ANZW

```
STL                                Explanation
     .
     .
          :  JU FB 120
     NAME :  SEND
     SSNR :  KY 0,21               SSNR parameter = 21
     A-NR :  KY 0,33               A-NR parameter = 33
     ANZW :  FW 100                ANZW = FW 100
```

b) Indirect assigning of parameters to the SSNR, A-NR and ANZW

```
STL                                Explanation
     .
+ ←       :  C DB 13               Calling a DB or DX data block
|         :
|         :
|         :  JU FB 120
|    NAME :  SEND                  Interpreted as pointer
+ ←  SSNR :  KY 255,10             Irrelevant
|    A-NR :  KY 0,0                Irrelevant
|    ANZW :  FW 0
|    .
+ →  DB 13                         SSNR parameter = 21
+ →  DW 10 :  KY 0,21              A-NR parameter = 33
     DW 11 :  KY 0,33              1st parameter for ANZW (area)
     DW 12 :  KS FW                2nd parameter for ANZW (address)
     DW 13 :  KY 0,100             ANZW = FW 100
```

Same example but with a condition codeword in the data block:

```
|    .
+ →  DB 13
+ →  DW 10 :  KY 0,21              SSNR parameter = 21
     DW 11 :  KY 0,33              A-NR parameter = 33
     DW 12 :  KS DB                1st parameter for ANZW (area)
     DW 13 :  KY 47,100            2nd parameter for ANZW (address)
                                   ANZW = DW 100 in DB 47
```

c) Indirect assigning of parameters to the SSNR and BLGR

```
STL                              Explanation
     .
+ ←       :  CX DX 24      Calling a DB or DX data block
|         :  JU FB 125
|    NAME :  SYNCHRON
+ ← SSNR :  KY 255,10     Pointer to parameter list
|    BLGR :  KY 0,0        Irrelevant
|    .
+ → DX 24
+ → DW 10 :  KY 0,10       SSNR parameter = 10
    DW 11 :  KY 0,5        BLGR parameter =  5
```

Assigning Parameters to Q/ZTYP, DBNR, Q/ZANF and Q/ZLAE

With **direct** parameter assignment, the data handling block directly processes the source parameters or destination parameters (consisting of QTYP/ZTYP, DBNR, QANF/ZANF and QLAE/ZLAE) specified in the block call.

With **indirect** parameter assignment, the block parameters form a reference to a parameter field in a data block which contains the ”actual” source or destination parameters.

The indirect assignment of the source or destination parameters is carried out with the QTYP/ZTYP ”XX” (KS data format). In the case of DBNR, the DB or DX block number must be specified in the low-order byte. If the high-order byte contains the value 0, the data handling block expects the parameter list in a DB data block, otherwise in a DX data block. QANF/ZANF contains the word number at which the parameter list begins.

QLAE/ZLAE is irrelevant.

In the case of operations with QTYP ”AS” (absolute addressed memory locations), the required 64K memory area is selected via the DBNR parameter using the four highest-value address bits.

In this case, the QANF/ZANF parameter designates the low value (16-bit) part of the 20-bit address. (See Example c) and Section 3.4 ”Memory Organization”).

DB Structure in the Case of Indirect Parameter Assignment (TYPE = XX)

QANF + 0 KS:	QTYP/ZTYP
1 KS:	DBNR
2 KF:	QANF/ZANF
3 KF:	QLAE/ZLAE

Figure 2-1 Data Block Structure in the Case of Indirect Parameter Assignment

Examples of DB Structure in the Case of Indirect Parameter Assignment

a) Direct assignment of parameters to QTYP, DBNR, QANF, QLAE

STL	Explanation
.	
: JU FB 120	
NAME : SEND	
SSNR : KY 0,21	
A-NR : KY 0,33	
ANZW : FW 100	
QTYP : KS DB	QTYP parameter = DB
DBNR : KY 0,17	DBNR parameter = 17
QANF : KF 3	QANF parameter = from DW 3
QLAE : KF 5	QLAE parameter = 5 words
PAFE : QB 13	

b) Indirect assignment of parameters to QTYP, DBNR, QANF, QLAE

STL	Explanation
.	
.	
: JU FB 120	
NAME : SEND	
SSNR : KY 0,21	
A-NR : KY 0,33	
ANZW : FW 100	
+ ← QTYP : KS XX	**Indirect parameter assignment**
+ ← DBNR : KY 0,25	**Parameters are located in DB 25**
+ ← QANF : KF 11	**from DW 11**
| QLAE : KY 0	**Irrelevant**
| PAFE : QB 13	
| .	
|	
+ → DB 25	
+ → DW 11 : KC DB	**Parameter QTYP = DB**
DW 12 : KY 0,17	**Parameter DBNR = 17**
DW 13 : KF 3	**Parameter QANF = 3**
DW 13 : KF 5	**Parameter QLAE = 5**

c) Absolute addressing AS

STL	Explanation
Absolute address (hexadecimal)	1 AB00
– comprises address of 64 K area	1
– low-value part of the address	AB00
(hexadecimal) or fixed-point	43776

: JU FB 120	
NAME : SEND	
SSNR : KY 0,21	
A-NR : KY 0,33	
ANZW : FW 100	
QTYP : KS AS	AS operation
DBNR : KY 0.1	64 K area: 1
QANF : KF 43776	Low-value address 43776 = AB00H
QLAE : KF 200	
PAFE : QB 13	

2.3 Parameter Description

SSNR: Interface Number

The number of the interface at which the job to be addressed is located (see Section 1.1 Configuration).

- Parameter type/data type: Data/constant byte (D/KY; KY = 2 bytes)
- Permissible range: 0,0 ... 0,255 (direct parameter assignment)
  1,0 ... 255,255 –N (indirect parameter assignment)
  N = Number of words required for indirect parameter assignment
- High byte = 0: Direct parameter assignment; low-order byte = SSNR
- High byte $\neq$ 0: Indirect parameter assignment; low-order byte = pointerr

A-NR: Job Number

The job number addressed at the interface. Under the same number, a program or a parameter set, through which the function of the CP is defined, is located at the interface.

- Parameter type/data type: Data/constant byte (D/KY)
- Permissible range: 0,0 (”ALL” function)
  0,1 ... 0,223 (”DIRECT” function)

For the running of the blocks, there is an essential difference between the job number = 0 (an ALL function) and the job number $\neq$ 0. This operating mode is called DIRECT function (not to be confused with direct parameter assignment).

ANZW: Condition Codeword

Address of the condition codeword in which either the processing of the job specified under A-NR will be indicated to the user (DIRECT functions) or a job number (ALL functions).

- Parameter type/data type: Input/word (I/W)
- Permissible range: FW 0 ... 252
  DW 0 ... 254

With direct parameter assignment, DW refers to the DB/DX data block specified before the data handling block call. For indirect parameter assignment, see above.

The data blocks must be of sufficient length. If, for example, the ANZW address is DW 7, then the DB/DX block must be at least 14 words long (5 words for block header, DW 0 to DW 8), so that a possible subsequent ANZW (see below) can be processed.

The blocks which write to the condition codeword and the method of evaluating the latter are described in detail in Section 2.5 ”Evaluating the Output Parameters”.

BLGR:
Frame Size

The maximum number of bytes which can be transferred by one SEND or RECEIVE block is called the frame size. If the quantity of data to be exchanged is greater than the frame size, as many blocks must be called as are necessary to complete the transfer.

On startup of the programmable controller, the frame size between the processor and the interface is decided by SYNCHRON. The frame size can be influenced by the BLGR parameter (see SYNCHRON block description).

– Parameter type/data type: Data/byte (D/KY)

– Permissible range : 0,0 ... 0,255

The following frame sizes can be set:

0	Frame with max. 256 bytes [1)]
1	Frame with max. 16 bytes
2	Frame with max. 32 bytes
3	Frame with max. 64 bytes
4	Frame with max. 128 bytes
5	Frame with max. 256 bytes
6	Frame with max. 512 bytes
7..	
254	Frame with max. 256 bytes [2)]
255	Frame fixed at 512 bytes

Increasing block execution time

Increasing number of block calls

1) Default for CPU 948; the block execution time is thus less than 10 ms (acknowledgement time not taken into account)

2) Corresponds to parameter assignment with frame size ”0”.

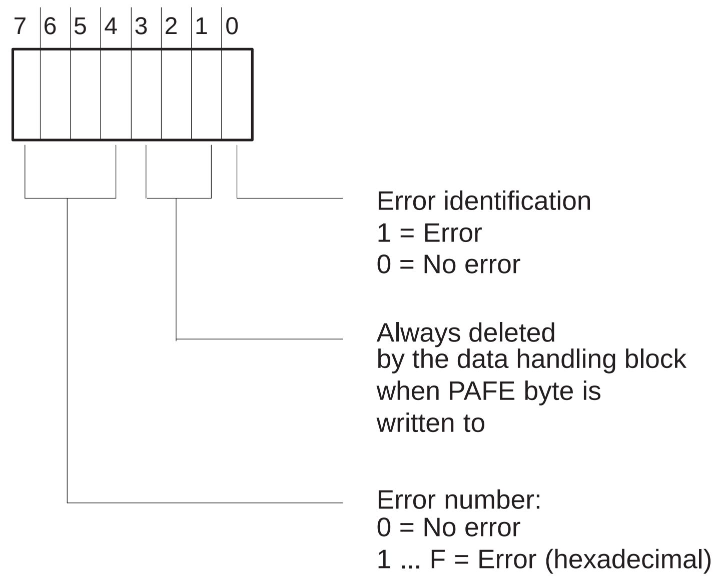
PAFE:
Error Indication in the Event of Parameter Assignment Errors

The PAFE byte (flag byte, output byte or input byte) indicates when problems occur in processing a data handling block. When evaluating this parameter, indication of the (transitory or permanent) interface status (e.g. interface overloaded, not ready) must be distinguished from indication of ”parameter assignment errors”, for example, assignment of illegal parameters to A-NR, QTYP/ZTYP etc. In this case, the parameters assigned of the data handling block and/or the CP (interface) must be changed.

– Parameter type/data type: Output/byte (Q/BY)

– Permissible range: FY 0 ... FY 255
QB 0 ... QB 127 (if present)
IB 0 ... IB 127 (if present)

PAFE Byte Structure



The error numbers are described in detail in Section 2.5 ”Evaluating the Output Parameters”.

2.4 Source and Destination Parameters (Q/ZTYP, DBNR, Q/ZANF and Q/ZLAE)

Source Parameters: QTYP, QANF, QLAE

The term ”source parameter” covers the following parameters:

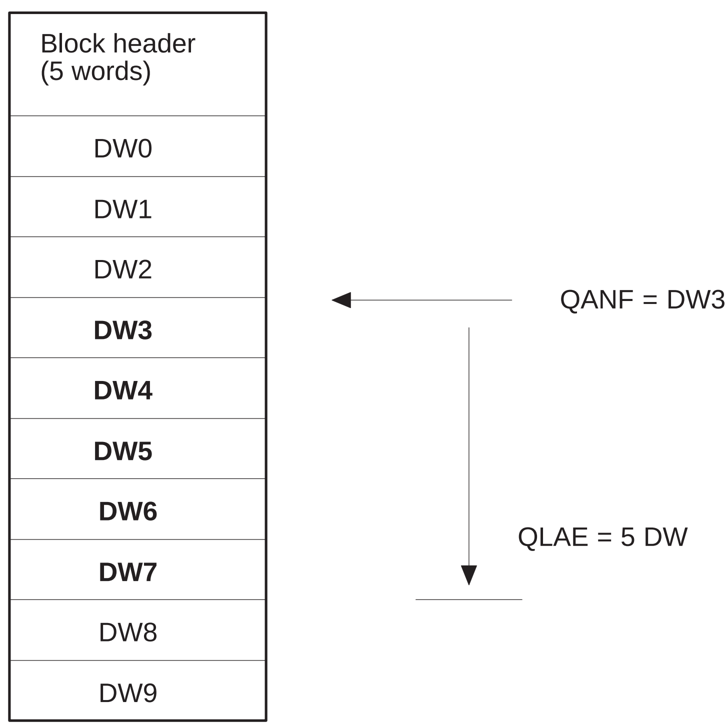
Table 2-1 Structure of the Source Parameter

Parameter	Meaning	Example
QTYP	Source type	DB
DBNR	Data block number or: 64K memory area in AS mode	(DB) 17
QANF	Source start	(DW) 3
QLAE	Source length	5 (DW)

These parameters identify an area. This area forms a data source; that is, the data of this area are transferred (copied) to the interface.

Example

QTYP/DBNR = DB17



Destination Parameters: ZTYP, ZANF, ZLAE

The term ”destination parameter” covers the following parameters:

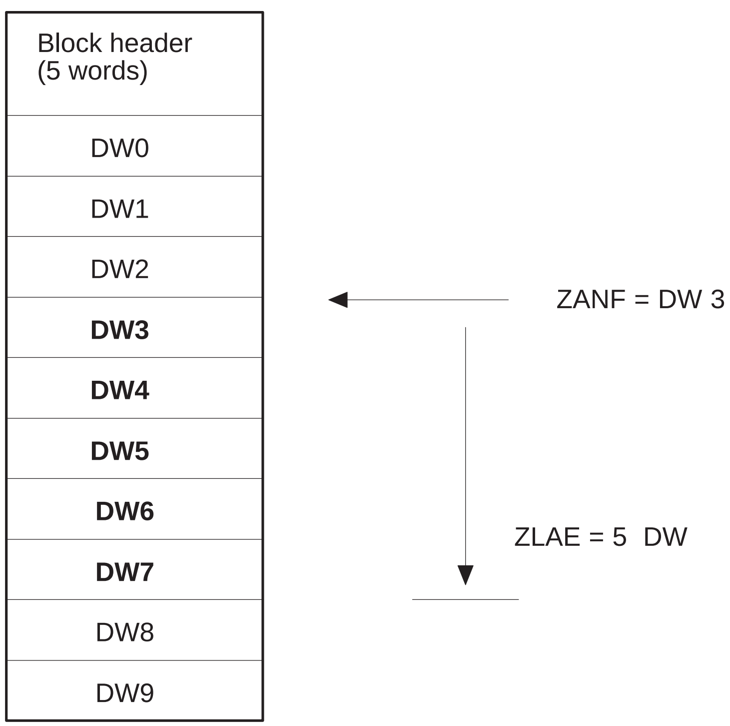
Table 2-2 Structure of the Destination Parameter

Parameter	Meaning	Example
ZTYP	Destination type	DX
DBNR	Data block number or: 64K memory area in AS mode	(DX) 18
ZANF	Destination start	(DW) 3
ZLAE	Destination length	5 (DW)

These four parameters identify an area. This area forms a data sink; that is, it receives data supplied from the interface. Do not forget that in this process the ”old” data are overwritten.

Example

ZTYP/DBNR = DX 18



See Section 3.4 ”Memory Organization, Area Limits” for further information.

QTYP/ZTYP: Type of Data Source/Data Destination

With this parameter, the type of data source (with SEND block) or type of data destination (with RECEIVE and FETCH blocks) can be specified by means of ASCII characters.

– Parameter type/data type: Data/constant character (D/KY; KS = 2 ASCII characters)

– Permissible area: DB, DX, ZB, TB, BS, AS (direct parameter assignment, word areas)
MB, AB, EB, PB (direct parameter assignment, byte areas)
XX (indirect parameter assignment)
RW (READ/WRITE),
NN (source/destination parameters of CP)

DBNR: DB Number with DB, DX, XX, RW Type Identifiers

If an XX, RW, DB or DX identifier is specified for QTYP/ZTYP, the data handling block must be informed of the data block required in the low-order byte of this parameter.

– Parameter type/data type: Data/constant byte (D/KY; KS = 2 bytes)

– Permissible area: 0,3 ... 0,255 (with direct parameter assignment, high-order byte must be 0)
0,3... 255,255 (with indirect parameter assignment and READ/WRITE)
if high-order byte = 0: DB data block
if high-order byte $\neq$ 0: DX data block)

If, with QTYP, AS is assigned as the type of data source or data destination, the number of the 64K memory area should then be specified as a parameter for DBNR (see Section 3.4).

QANF/ZANF: Start Address of the Source/Destination Data Frame

Start address (relative to area start) of the source/destination frame with direct parameter assignment.

Using the XX (indirect parameter assignment) and RW (READ/WRITE) type identifiers, the DW numbers from which the parameters start can be specified here.

– Parameter type/data type: Data/constant fixed point (D/KF)

– Permissible area for CPU 948: 0 ... 65535

Note:
With the KF data format, the programmer accepts any value between –32768 and +32767. QANF/ZANF is considered by the handling block as an unsigned (positive) number between 0 and 65535 (corresponds to 0000H...FFFFH).

QLAE/ZLAE: Length of the Source/Destination Frame

Depending on the source/destination type, the information is understood to be in bytes or in words.

– Parameter type/data type: Data/constant fixed point (D/KF)

– Permissible area: 1 ... 32767, –1

The ”joker length” (QLAE, ZLAE = –1) means:

- In the case of RECEIVE, that as much data is accepted as the interface provides
- In the case of SEND, that as much data is transferred to the interface as the area permits (transmission up to the limit of the area).

The meaning and relationships between the source/destination parameters are listed in the table below:

Table 2-3 Meaning and Relationships of the Source/Destination Parameters; Word Areas (1)

QTYP/ZTYP Description	**DB** Source/destination data from/to data block	**DX** Source/destination data from/to DX data block	**ZB** Source/destination data from/to counters
DBNR Meaning Permissible area CPU 948	DB from which the source data are taken or into which the destination data are transferred 3 ... 255	DX from which the source data are taken or to which the destination data are transferred 3 ... 255	Irrelevant
QANF/ZANF Meaning Permissible area CPU 948	DW number starting from which data are read or written 0 ... 4090	DW number starting from which data are read or written 0 ... 4090	Number of counter starting from which data are read or written 0 ... 255
QLAE/ZLAE Meaning Permissible area CPU 948	Length of the source/destination frame in words 1 ... 4091	Length of the source/destination frame in words 1 ... 4091	Length of the source/ destination frame in words (1 counter = 1 word) 1 ... 256

Table 2-4 Meaning and Relationships of the Source/Destination Parameters; Word Areas (2)

QTYP/ZTYP Description	**TB** Source/destination data from/to timers	**BS** Source/destination data from/to system data area	**AS** Source/destination data from/to absolute addressed memory locations
DBNR Meaning Permissible area CPU 948	Irrelevant –	Irrelevant –	64 K area address 0.0 ... 0.13
QANF/ZANF Meaning Permissible area CPU 948	Number of timer starting from which the data are read or written 0 ... 255	Number of RS word starting from which the data are read or written 0 ... 255	Absolute start address starting from which data are read or written 0 ... FFFF (hex.) or 0 ... 65535 (fixed-point dec.)
QLAE/ZLAE Meaning Permissible area CPU 948	Length of the source/ destination frame in words (1 timer = 1 word) 1 ... 256	Length of the source/ destination frame in words (1 system data item = 1 word) 1 ... 256	Length of the source/ destination frame in words (1 counter = 1 word) 1 ... 32767

See Section 3.4 ”Area Limits” for further information.

Table 2-5 Meaning and Relationships of the Source/Destination Parameters; Word Area

QTYP/ZTYP Description	**MB** Source/destination data from/to flag area	**AB** Source/destination data from/to process image of the outputs (PIQ)	**EB** Source/destination data from/to process image of the inputs (PII)	**PB** Source/destination data from/to I/O modules, if source data: input modules, if destination data: output modules
DBNR	Irrelevant	Irrelevant	Irrelevant	Irrelevant
QANF/ZANF Meaning Permissible area CPU 948	Flag byte number starting from which data are read or written 0 ... 255	Output byte number starting from which data are read or written 0 ... 127	Input byte number starting from which data are read or written 0 ... 127	I/O byte number starting from which data are read or written. 0 ... 127 dig. I/O, 128 ... 255 dig. or analog I/O
QLAE/ZLAE Meaning Permissible area CPU 948	Length of the source/destination frame in bytes 1 ... 256	Length of the source/destination frame in bytes 1 ... 128	Length of the source/destination frame in bytes 1 ... 128	Length of the source/destination frame in bytes 1 ... 256

Table 2-6 Meaning and Relationships of the Source/Destination Parameters; Special Cases

QTYP/ZTYP Meaning	XX Indirect parameter assignment; **Source or destination parameters are stored in the DB or DX data block (specified by DBNR and QANF)**	RW READ/WRITE; Source or destination parameters are stored in the DB or DX data block (specified by DBNR and QANF)	NN **No source/destination parameters in block; parameters can be supplied by interface**
DBNR Meaning Permissible area CPU 948	DB/DX in which the source/destinationparameters are stored; DB if high-order byte = 0 otherwise DX 1 ... 255	DB/DX in which the source/destinationparameters are stored; DB if high-order byte = 0 otherwise DX 1 ... 255	Irrelevant
QANF/ZANF Meaning Permissible area CPU 948	DW number starting from which the parameters are stored 0 ... 32767	DW number starting from which the parameters are stored 0 ... 32767	Irrelevant
QLAE/ZLAE	Irrelevant	Irrelevant	Irrelevant

See Section 3.4 Area Limits for further information.

Data Block: Structure in the Case of Indirect Parameter Assignment

Type = XX

QANF + 0 KS	QTYP/ZTYP but not XX, RW, NN
1 KY:	DBNR in the case of type DB, DX
2 KF:	QANF/ZANF start address
3 KF:	QLAE/ZLAE length

Figure 2-2 Data Block Structure in the Case of Indirect Parameter Assignment

Data Block: Structure in the Case of READ/WRITE

Type = RW

QANF + 0 KS	QTYP but not XX, RW, NN	”Data source” description
1 KY:	DBNR in the case of QTYP DB, DX	
2 KF:	QANF source start address	
3 KF:	QLAE source length	
4 KS:	ZTYP but not XX, RW, NN	”Data destination” description
5 KY:	DBNR in the case of ZTYP DB, DX	
6 KF:	ZANF destination start address	
7 KF:	ZLAE destination length	

Figure 2-3 Data Block Structure in the Case of READ/WRITE

2.5 Evaluating the Output Parameters

Output Parameters: RLO, PAFE, ANZW

PAFE is purely an output parameter, whereas RLO and ANZW are both input and output parameters. The following graphical representation shows in what way and in what context the data handling blocks influence the output parameters.

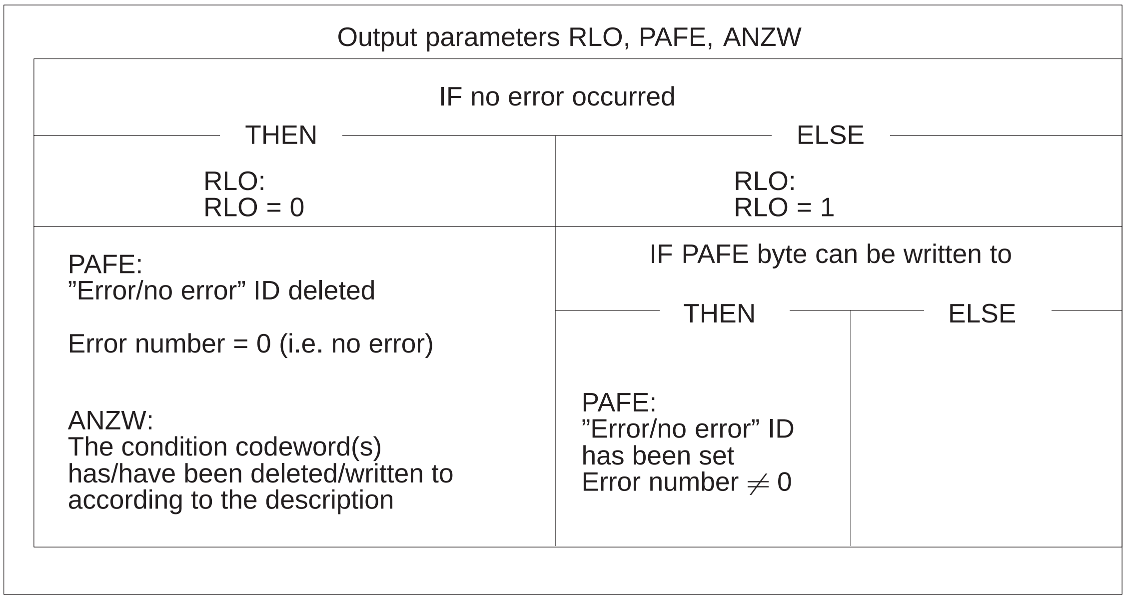


Figure 2-4 Influence of the Data Handling Blocks on the Output Parameters

If the condition accompanying ”IF” is fulfilled, then the column under ”THEN” is valid. If it is not fulfilled, the ”ELSE” column is valid, etc.

If an error has occurred, the condition codeword is irrelevant.

Parameters: PAFE and RLO

If an error occurs during the data handling block routine (this can be an ”actual” parameter assignment error, or other type of error [1]), the RLO is set. If no error occurs, RLO is reset (deleted). A quick error analysis can therefore be carried out following the function block [2)].

Error indication by means of RLO always takes place. The PAFE byte can only then be written to if the PAFE (actual) parameter is permissible.

1) **Note:** A typical parameter assignment error is, for example, a job number greater than the permissible maximum. If the CP is not ready to communicate (”interface overloaded”, ”interface reserved by other processor”), this, as well as other errors connected with the CP, will be recognized as an error and indicated with an error number in the PAFE byte.

[2] **Note:** No error has occurred if handshake signals are not exchanged (1-4) or if a handshake is broken off (5, 6) for any of the following reasons:

1. RLO (RLO ”input parameter” not to be confused with RLO ”output parameter” (= error indicator)) = 0
2. Job is already/still running (SEND/FETCH direct)
3. RECEIVE job is not (yet) ready (RECEIVE direct)
4. This function does not include a handshake (CONTROL)
5. Data transfer/reception is disabled
6. Only parameters are to be passed, etc.

It follows, therefore, that, in these cases too, no error numbers are defined in the PAFE byte. The individual block descriptions provide information as to which of these six situations may be applicable.

Structure: PAFE Byte

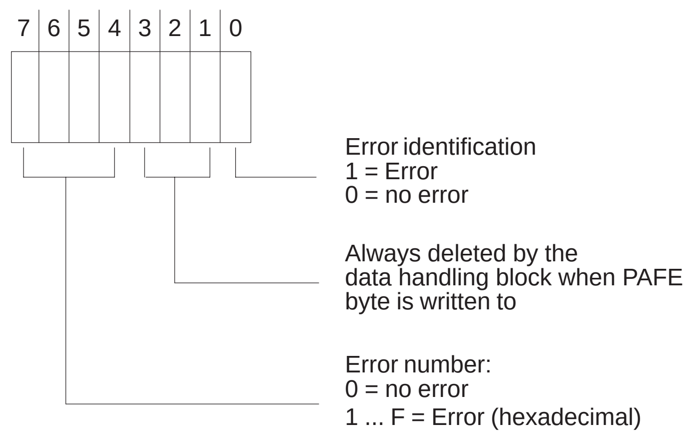


Table 2-7 Meaning of the Error Numbers in the PAFE Byte

Error No. (hex.)	Meaning
0	No error
1–F	Error
1–4	Error in source/destination parameter (QTYP/ZTYP, DBNR, QANF/ZANF or QLAE/ZLAE) or pointer to source/destination parameter incorrect with QTYP/ZTYP XX and RW, (XX = indirect parameter assignment, RW = READ/WRITE) or error in source/destination parameter from CP
1	Source/destination formally incorrect – QTYP/ZTYP illegal – DBNR data block number greater than 255; that is, high byte $\neq 0$ – QLAE/ZLAE length illegal, permissible length: 1...32767 and –1.
2	DB or DX data block does not exist or is not permissible; (for example: DB0, DX0; in the case of QTYP/ZTYP DB, DX, XX, RW).

Error No. (hex.)	Meaning
3	Area too small or sum of start address (QANF/ZANF) and length (QLAE/ZLAE) too great (with all QTYP/ZTYP).
4	Area does not exist or is not permissible (with QTYP/ZTYP, AS, AB, EB, PB).
5	(Address of) condition codeword incorrect
6	No. not reserved
7	Interface does not exist
8	Interface not ready
9	Interface overloaded
A	Interface reserved by other processor (multiprocessor operation)
B	Job number illegal or frame size (SYNCHRON) illegal
C	Interface does not respond or interface does not respond in time or interface rejects job (negative handshaking acknowledgement).
D	Other interface errors, including – Error (or illegal acknowledgement) in handshaking acknowledgement – Frame size of interface not permissible – Synchronization running (no error)
E	Other data handling block, errors including – No data block selected with indirect assignment of parameters to the SSNR, A-NR, ANZW, BLGR – If PAFE is assigned EB or AB and does not exist
F	FB call not permissible, including – Double call when interrupts can occur between statements.

Note:
If the ”Status” bit is set in the condition codeword ANZW and the identifier ”Job completed with error” (bit $2^3 = 1$) is set, an error number has been written in the bits 2^8 to 2^{11}. This error number corresponds to that of the PAFE byte as follows:

1 ... 5	These error numbers and their meanings are identical in the PAFE byte and ANZW: The interface stores the number received from the data handling block in the job status without carrying out any change. After the corresponding parameters have been assigned, the job status is copied into the condition codeword by the next data handling block called.
6 ... F	The meaning of these numbers in the PAFE byte, as it is described here, is not identical to the numbering in the job statuses. The CP descriptions contain specific error lists.

Parameter: ANZW

The jobs identified by a job number constitute the management unit of an interface (or of the CPs).

The corresponding assignment on the handling block

- is indicated by the A-NR parameter (SEND/RECEIVE/FETCH/CONTROL/RESET direct)
- is produced by the flagging of a job number in the ANZW (SEND/RECEIVE/CONTROL ALL)

In the interface, there is a job status for every job. The status is managed by the interface and it indicates whether a job is (still) running in the CP or whether it has been completed by the CP without any errors or with a particular error. Occupation of the condition codeword with "status" (see below) means, among other things, that this job is copied into the ANZW.

The STEP 5 program in the CPU should be structured so that a particular condition codeword is allocated to each defined job.

In this way, an image of the activities in the interface or in the CP can be obtained in the CPU. This can only take place if the condition codewords are regularly updated by calling suitable data handling blocks (see block description, for example, CONTROL, SEND direct when idling).

You must distinguish between the ANZW 1 and ANZW 2 parameters.

Furthermore, do not forget that when ANZW 1 is occupied with "status", it will be used both as an input parameter (bit 2^7 = 1: data transfer/reception disabled!) and as an output parameter.

Rules for Writing to ANZW by the DHB

1. The condition codeword(s) will basically only be written to (changed) if no error has occurred while the data handling block was being processed. In this case, the condition codewords will be written to according to the following table:

Table 2-8 Assignments of the Condition Codewords

Function	ANZW 1	ANZW 2
SEND/REC. DIRECT	Status	Quantity
SEND/REC. ALL	Job no.	–
FETCH (DIRECT)	Status	–
CONTROL DIRECT	Status	–
CONTROL ALL	Job no.	–

2. ANZW 1 and ANZW 2 (with SEND/REC DIRECT) is always written to (if no error has occurred).

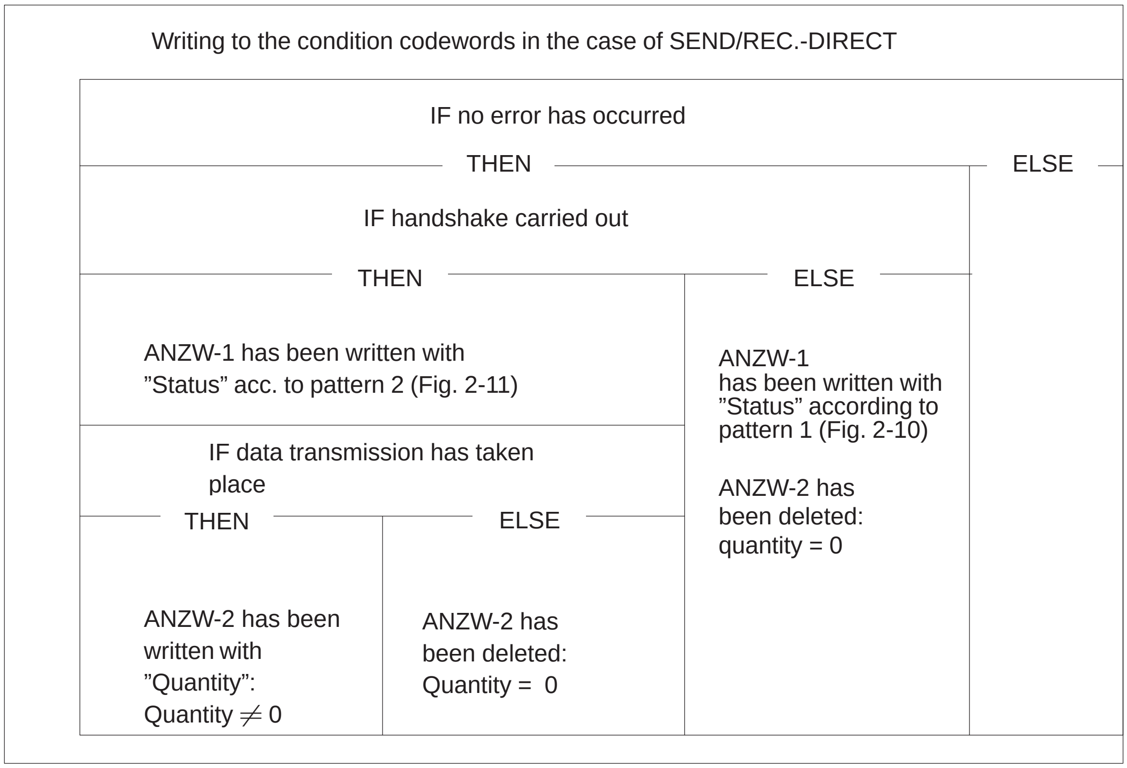


Figure 2-5 Influence of the Data Handling Blocks on the Output Parameters

Writing to Condition Codewords in the Case of SEND/ RECEIVE ALL

In the case of SEND/RECEIVE ALL, the job number is written to ANZW 1.

Job Number

If no error has occurred, the job number is written into the low-order byte and the high-order byte is deleted (ANZW 1).

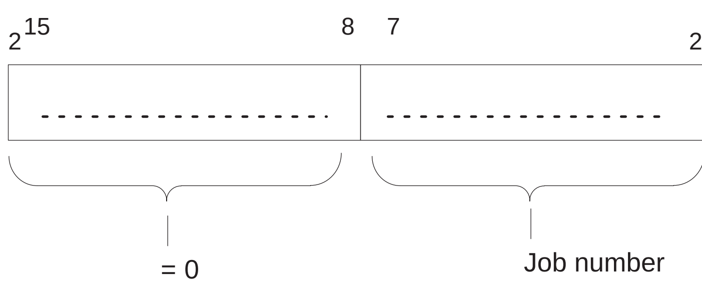


Figure 2-6 Job Number

	CONTROL ALL
= 0:	No job is being processed (by the interface/CP).
≠ 0:	This job is being processed.

	SEND/RECEIVE ALL
= 0 :	Idling; that is, no handshake carried out.
1...223:	A handshake has been carried out for this job.
= 255:	A handshake has been carried out. The CP supplied an alternative number instead of the actual job number.

Quantity of Transmitted Data

If no data is transmitted and no error has occurred, the ”Quantity” words (ANZW 2) are deleted. If data is transmitted, the quantity word contains the quantity of all the data already transmitted in this job which may be considerably more than the quantity of data transmitted by the last data handling block.

If the ”Data transfer/data reception completed” bit (bits 5 and 6) in ANZW 1 is set, ANZW 2 contains the source length or destination length of the job (job number). This is always indicated in bytes.

ANZW 2:

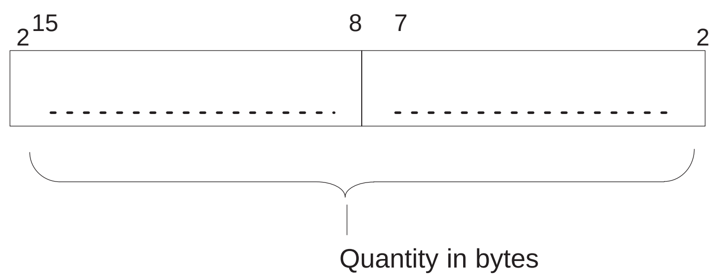


Figure 2-7 Quantity of Data to be Transferred

Job Status

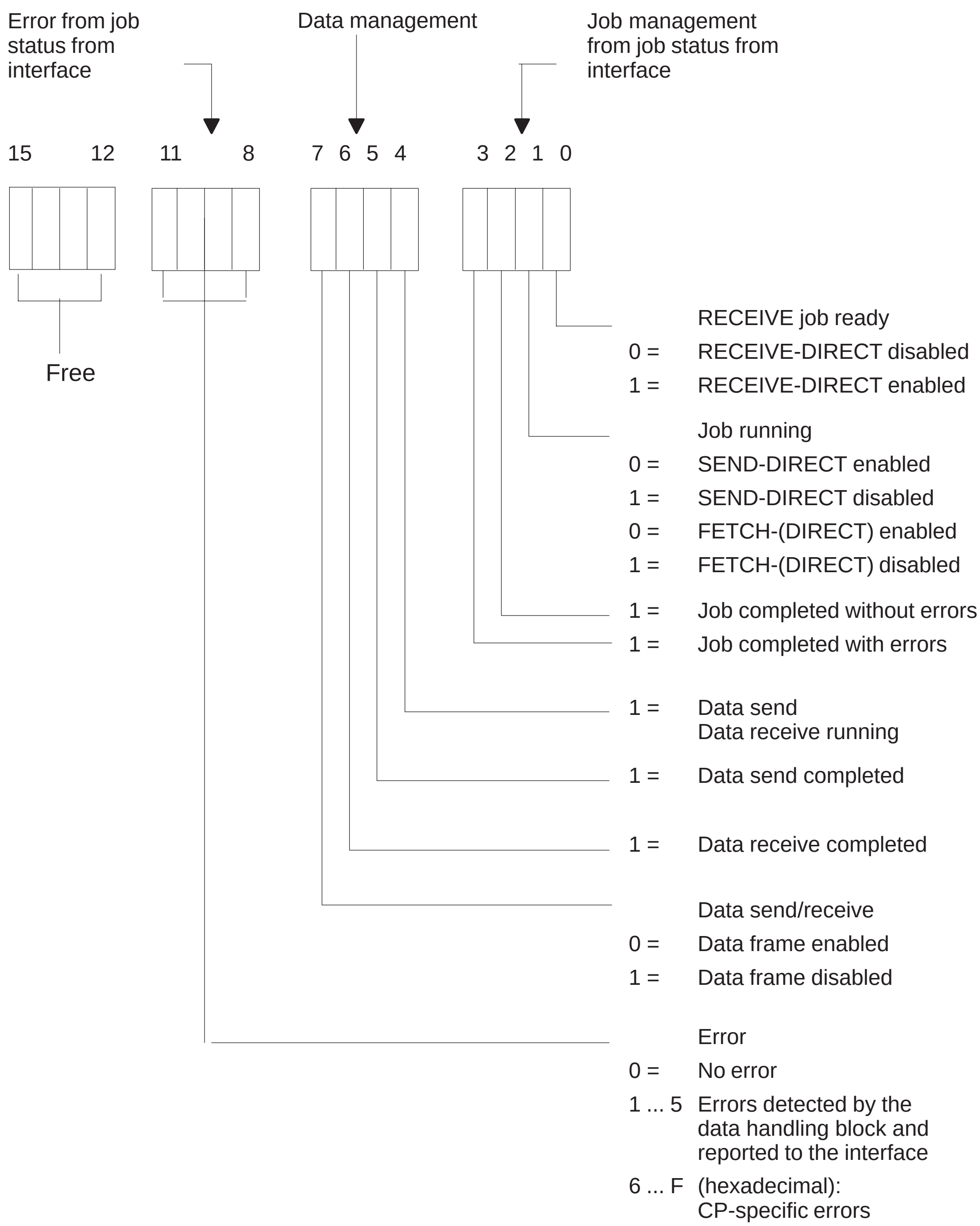


Figure 2-8 Condition Codeword

- Without handshake:

With SEND/REC./FETCH/CONTROL DIRECT, the job status must be read/evaluated by the data handling block before a handshake is carried out. This job status is written into ANZW 1 according to pattern 1 (Figure 2-9) if no handshake takes place (and no errors occur).

- <u>With</u> handshake:

In the case of all functions where a handshake was initiated (and executed without error), the job status will be

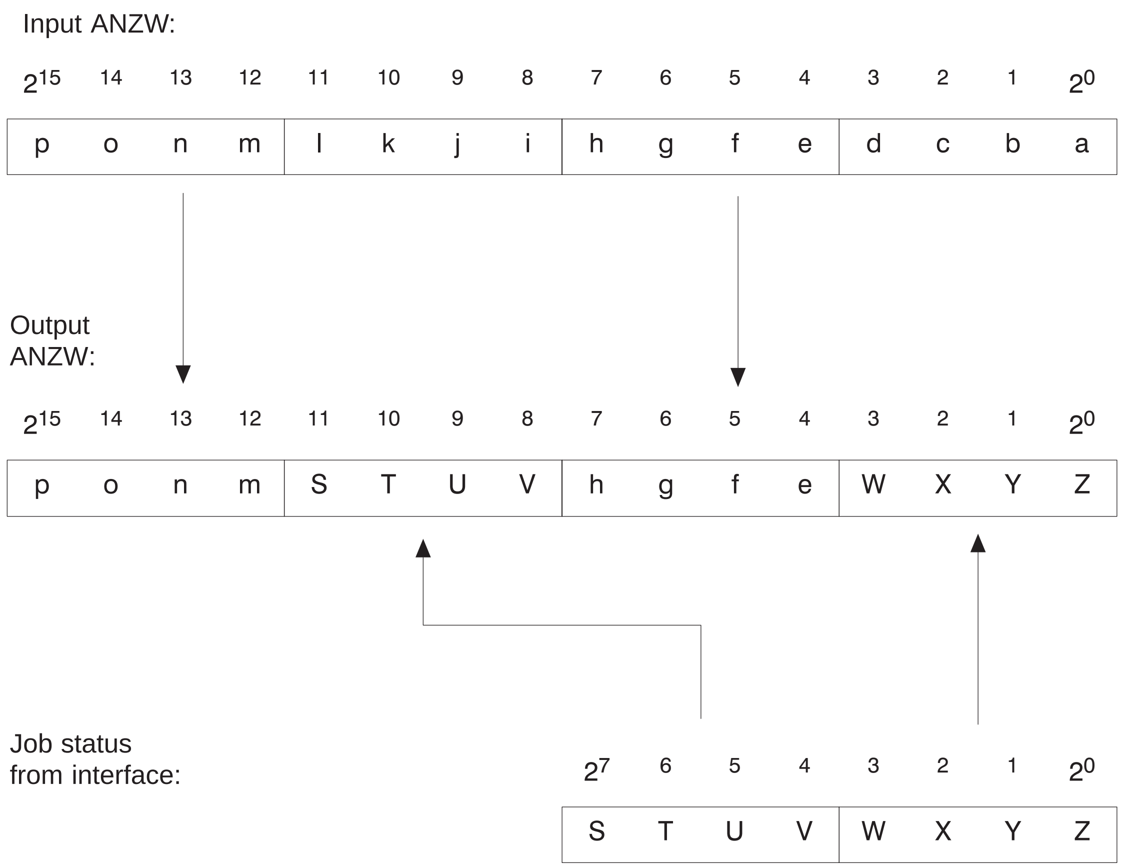
– re-read (in the case of DIRECT functions) or

– read for the first time (in the case of ALL functions)

by the data handling block at the end of the handshake.

This updated job status does not have to be evaluated by the data handling block. It will be inserted in ANZW 1 according to pattern 2 (Figure 2-10).

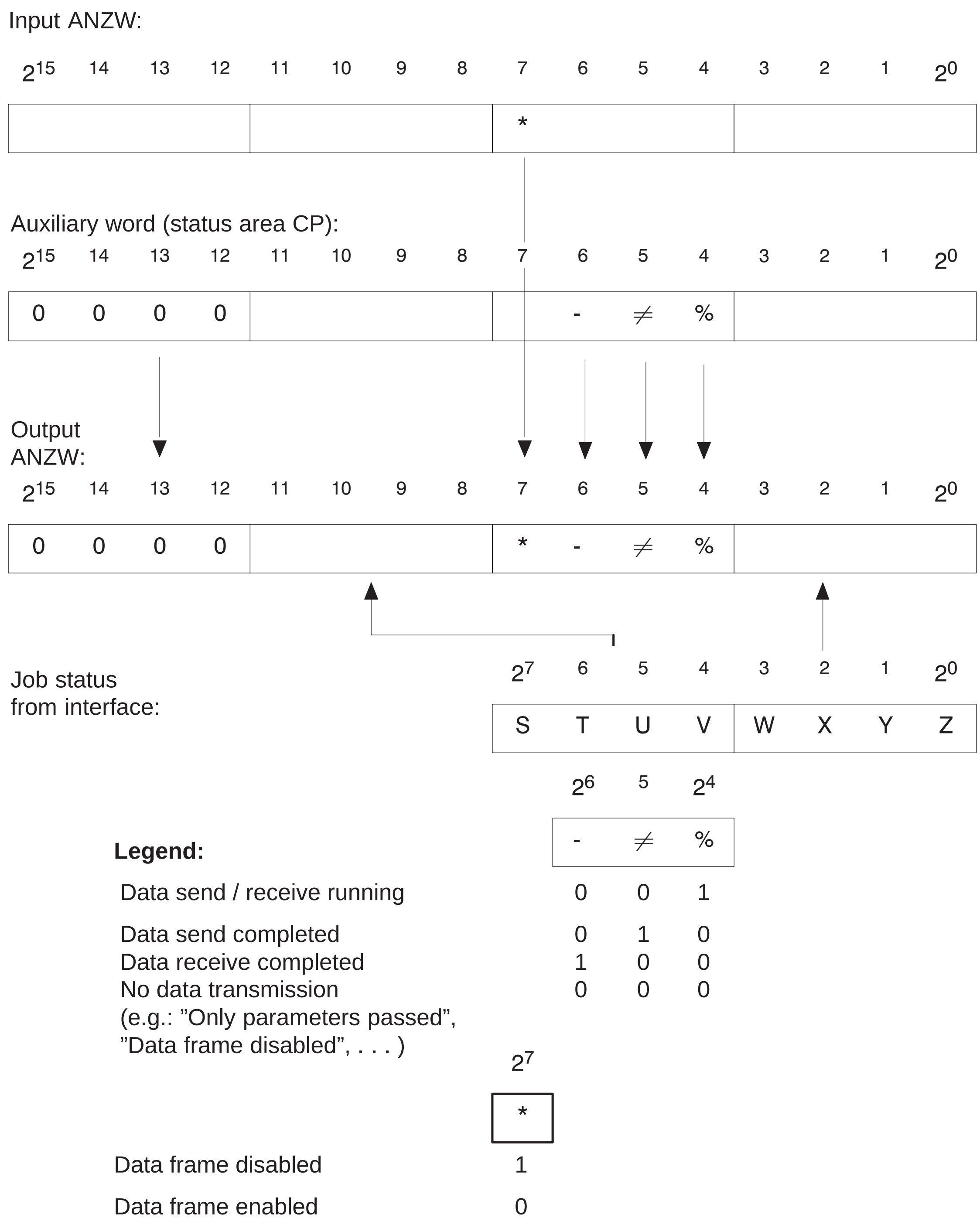
Structure of the Condition Codeword



Input ANZW: Condition codeword <u>before</u> data handling block is called

Output ANZW: Condition codeword <u>after</u> data handling block is called

Figure 2-9 Pattern 1



Input ANZW: Condition codeword before data handling block is called
Output ANZW: Condition codeword after data handling block is called

Figure 2-10 Pattern 2

Note:
If bit positions 2^{12} to 2^{15} have been deleted following the running of a data handling block, and if they were set (at least some of them) beforehand, then this is an obvious indication that:

1. The handling block was run without any errors (otherwise the condition codewords are not written to)
2. A handshake was carried out (otherwise the condition codeword would not be written to according to pattern 2).

Bit positions 2^4 to 2^6 now give information about whether data has been transmitted.

Division of the Condition Codeword

- **Nibble 1, bits 0 to 3, job management:**

The following is encoded here: whether a job has already been started or whether errors have occurred or whether the job has been disabled.

Important: Each of the bits has a significance of its own. In the case of several CPs, additional significance is assigned to the bit combinations. For example, if ”Job running” (bit 2) and ”Job completed” (bit 2 or 2) are set simultaneously (contradiction!) in the case of the CP 143, this has the supplementary meaning of ”CP not ready for this job/job disabled”.

- **Nibble 2, bits 4 to 7, data management:**

The following is encoded here: whether the data transfer for the job is still running or whether the transfer or reception of data has already been completed. With bit 7, the data block for the job can be disabled (bit 7 = 1: data block disabled; bit 7 = 0: data block enabled).

- **Nibble 3, bits 8 to 11, error number:**

These are the error indicators of the job. The error indicators are only valid if the bit ”Job completed with error” in the first nibble is set at the same time.

- **Nibble 4, bits 12 to 15, free**

Operation of the ”Status” Condition Codeword

a. **Bit 0** : RECEIVE job ready (handshake meaningful)

Setting/resetting: By the data handling blocks corresponding to the deletion condition code in the job status. The bit ”RECEIVE job ready” is used with the RECEIVE DIRECT function (received data available).

Evaluation: By the RECEIVE block; the RECEIVE block carries out the handshake with the interface only if bit 0 is set to 1.

– By the user to query whether or not received data is available.

b. **Bit 1** : Job running (SEND/FETCH disabled)

Setting/resetting: By the data handling blocks corresponding to the deletion condition code in the job status. The ”Job running” bit (= 0) is used with the SEND DIRECT and FETCH DIRECT functions.

Evaluation: By the SEND block and FETCH block. The block will only carry out the handshake with the interface if bit 1 = 0; that is, a job will only be assigned if the ”old” job has been processed.

– By the user in order to find out whether a ”new” job can be initiated.

c. **Bit 2** : Job completed without errors

Setting/resetting: By the handling blocks corresponding to the deletion condition code in the job status.

Evaluation: By the user to check whether the job was completed by the interface without errors.

d. **Bit 3** : Job completed with error

Setting/resetting: By the handling blocks corresponding to the deletion condition code in the job status.

Evaluation: By the user to check whether the job was completed by the interface with an error. If the ”Job completed with error” identifier is set, the reason for the error is to be found in bits 8 to 11 of the condition codeword.

e. **Bit 4** : Data transfer/reception running

Setting/resetting: By the SEND and RECEIVE handling blocks. If the transfer/reception for a job was started (1st subframe transferred) and not yet completed; for example, if data is still to be exchanged via the ALL functions. For this purpose, the initiation and transmission of the first subframe must have been carried out with a DIRECT function.

Deleting: By the handling blocks if the condition for setting has not been fulfilled.

Evaluation: By the user.
During CP-CPU data transmission, you may no longer change (SEND) or use (RECEIVE) the data frame of a job.

With ”small” data frames, this is not critical since data transmission here requires only one block call and leads immediately to the condition code ”Data transfer completed” or ”Data reception completed”. Larger data frames can, however, only be transmitted in subframes, and this requires several data handling block calls. In order to maintain the integrity of the data, you must first check whether the data frame has been transmitted completely before you change/use the data of a job. Otherwise, ”old” and ”new” data would be mixed.

f. **Bit 5** : Data transfer completed

Setting:	By the SEND handling block if the data of a job has been transferred complete to the interface (last subframe transmitted).
Resetting:	By the handling blocks if the setting condition has not been fulfilled. By the user if evaluation has taken place (edge generation).
Evaluation:	By the user
	With this bit, you can ascertain whether the data for a job has already been transferred complete to the interface.

g. **Bit 6** : Data reception completed

Setting:	By the RECEIVE handling block if the data for a job has been received complete by the interface (last subframe transmitted).
Resetting:	By the handling blocks if the condition for setting has not been fulfilled. By the user if evaluation has taken place (edge generation).
Evaluation:	By the user.
	With this bit, you can ascertain whether the data of a job has already been transmitted to the CPU.

h. **Bit 7** : Data transfer/reception disabled

Setting:	By the user in order to prevent a data frame being written to by the RECEIVE block or being read out by the SEND block.
Resetting:	By the user in order to enable the relevant data frame.
Evaluation:	By the SEND and RECEIVE handling blocks once only before the first subframe. If bit 2^7 is set, the blocks do not transfer any data. Instead, they report the ”error” to the interface.

i. **Bit 8 to 11** : Error number

Setting/resetting:	By the handling blocks according to the indicator in the job status.

Evaluation:	By the user.

The following indicators can appear:

0:	No error
1 to 5:	CPU or handling block error The meanings of the error numbers one to five are identical to the numbers in the PAFE byte (parameter assignment error).
6 to F :	CP or interface error The error numbers 6 to F (hex.) are CP-specific.

Data Handling Blocks in the User Program 3

This chapter contains important information for working with data handling blocks in the user program and for using data blocks in different functions. It also offers information on determining the area length remaining for data transfer, the runtime of the data handling blocks, possibilities of reducing runtime and a host of additional information of importance to your programming staff.

3.1 Calling Data Handling Blocks

Calling DHBs in the Program

At which points in the program can you call handling blocks? The following is the simplest course of action:

1. Calling the SYNCHRON block only at initial start and in the cycle.
2. Calling the remaining blocks SEND/SEND-ALL/RECEIVE/RECEIVE-ALL/CONTROL/FETCH/RESET only during cyclic program execution.
3. You can program events that you wish to be deleted during time-controlled or event-driven program processing and invoke a data handling block in such a way that only flags are set to begin with.

   During cyclic program execution, the respective data handling blocks will then be called.

Conditions for Calling DHBs

In principle, handling blocks can be called at any point within the user program, for example in the warm restart organization block or within time-controlled execution (OB 13, timed interrupt). However, the following limitations must be observed.

- The SYNCHRON DHB can only be called conditionally.
- The CPU 948R has the following three or four modes of program execution (among others)
  - Cyclic program execution (OB 1, lowest priority)
  - Time-controlled program execution (OB 6, OB 9, OB 10 to OB 18, priority is selectable)
  - Interrupt-driven program execution (OB 2 to OB 5 or OB 2 to OB 9, priority is selectable) and
  - ”Soft STOP” with cyclic execution of communication jobs (OB 39).
- The data handling blocks cannot be interrupted. This must be taken into account when calling handling blocks with long runtimes (see Section 3.5).

In ”soft STOP” (OB 39), handling blocks can be called irrespective of the point where the interrupt has occurred in RUN mode. For these purposes only, the required interfaces must have been initialized with a SYNCHRON at CPU restart for the ”soft STOP” (OB 38) status.

3.2 Calling SEND-ALL and RECEIVE-ALL

For the SEND and RECEIVE blocks, the operating mode SEND-ALL or RECEIVE-ALL can be selected using job number ”0” (see block description in Chapter 4). These blocks permit data transmission to be initiated and controlled by the interface.

The SEND-ALL and RECEIVE-ALL functions must be called ”regularly” so that a request for communication from the interface is detected in time. For example, the following options and combinations are available:

- Call once (n times) per cycle and per interface (short response times)

  Call with a call distributor: in the first cycle for interface 1, in the second for interface 2, etc. (low cycle load)
- Call within time-controlled execution (OB 13 every 100 ms, independent of cycle time fluctuations)
- Call whenever other blocks do not have to be called owing to the process (evenly distributed cycle load and/or assignment of priority to control activities over communication)
- Call one ALL function after another until the first, second, nth etc. run is not an idling run. In the next cycle, continue with the following ALL function (evenly distributed cycle load).

3.3 Using Data Blocks

The data handling blocks work with up to five DB or DX data blocks in total:

1. A data block which has been assigned the SSNR, A-NR, ANZW and BLGR parameters indirectly. Here, the corresponding data block must be selected before calling the handling block (see Section 2.2 ”Direct and Indirect Parameter Assignment”).
2. a) A data block which has been assigned its source parameters or destination parameters indirectly (see Section 2.2 ”Direct and Indirect Parameter Assignment”).

   b) A data block which, with READ/WRITE, contains the source parameters and destination parameters.
3. A data word of a data block can be used as a PLC condition codeword.
4. The data to be transmitted/received may have to be taken from/stored in a DB.

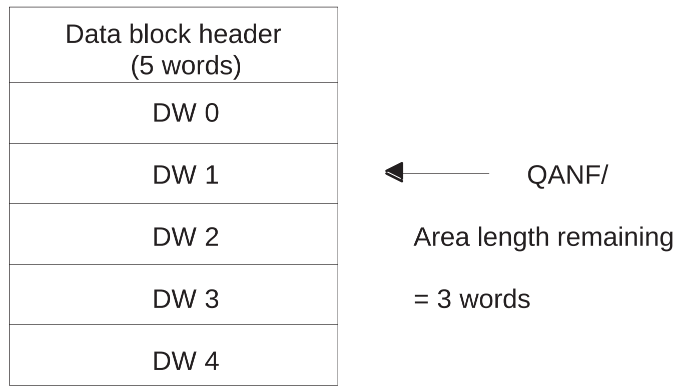
Here, care must be taken to ensure that all data blocks used exist and that they are long enough; the use of data blocks comprising more than 256 words is possible.

The use of DB 0, DB 1 and DX 0, DX 1 and DX 2 is permitted. If they are used, the handling block rejects them with an error indication.

3.4 Memory Organization, Area Limits

Area Length Remaining

The "area length remaining" is ascertained when executing the source/destination parameters in the handling block. Here, this means the difference between the length of an area (DB length, number of flag bytes, for example) and the preset QANF/ZANF start address.



The maximum quantity of data to be transmitted must not be greater than the area length remaining (legality check) or must be oriented to this area length remaining (area limit): joker length (joker length: see QLAE/ZLAE parameter); transmission of the length remaining is used by several CPs.

Naturally, the QANF/ZANF start address must exist. In the example (DB 17), the values from 0 to 4 would be permissible.

With all types of area, the rules for procedure set out above apply. The information blocks below contain additional information.

QTYP/ZTYP Counter Locations ZB, Timer Locations TB

The CPU 948R has 256 counter locations and 256 timer locations:

256 counter locations : C 0 to C 255

256 timer locations : T 0 to T 255

QTYP System Data Area BS

The CPU 948R has 256 system data values in the BS area:

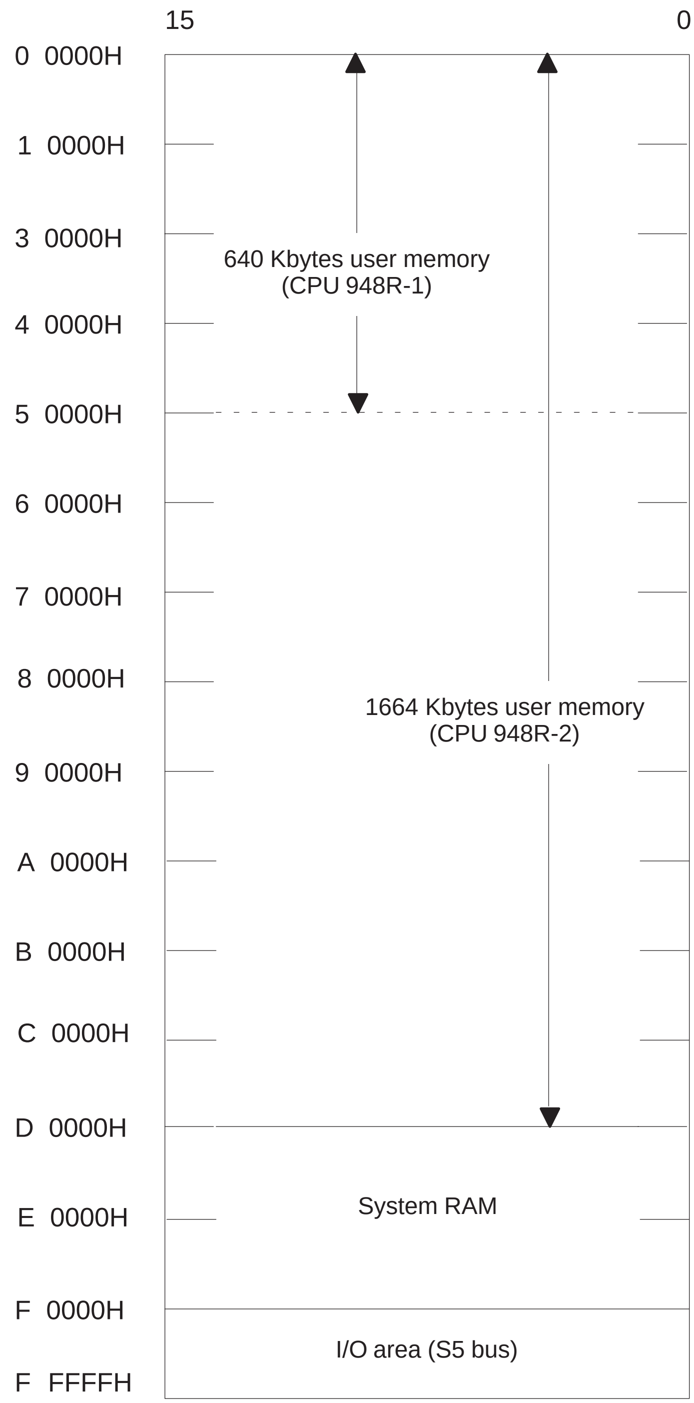
256 system data values : BS 0 to BS 255

With the exception of BS 60 to BS 63, BS data may only be read by the user. BS data should therefore only be assigned the as QTYP parameter. Please see the Programming Guide for the CPU 948R for more detailed information on the BS (= system data area RS) data.

QTYP/ZTYP Absolute Addresses AS

With the CPU 948R, all the addresses that have been released for the user program area in the Programming Guide for this CPU are permissible AS addresses.

Overview of the address area of the CPU 948R:



The position of blocks in the RAM can be changed by means of the ”Compress memory” function.

Special care must be taken when using the ”absolute addresses” type. When accessing data blocks, for example, please note that these blocks will disappear from memory or change their position within memory when

- being generated (G DB and GX DX operations)
- the memory is compressed (by programmer input or automatically) or
- input/updates are carried out on the programmer.

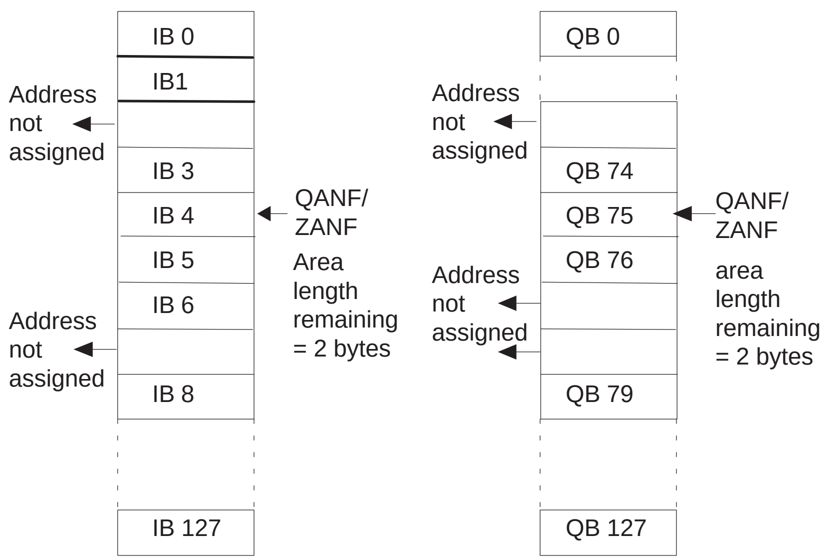
These changes are taken into account ”automatically” by the data handling blocks when using the ”DB” or ”DX” types. Any errors do **not** result in illegal areas being accessed, but an error bit is set in the PAFE byte.

QTYP/ZTYP Flags MB

The CPU 948R has 256 flag bytes: FY 0 to FY 255

QTYP/ZTYP PIQ/PII (AB/EB)

The I/O area (PY) can be an incomplete area (with gaps) since normally not all input and output addresses are assigned or enabled. Example:



The area length remaining is the number of assigned addresses up to the next gap.

Note: RI and RJ areas cannot be specified. If these areas are to be transferred by means of data handling blocks, they must be copied into a DB.

3.5 Runtime

Runtime without Handshake

Runtime without Handshake	SEND	RE-CEIVE	FETCH	RESET	CON-TROL
	idling				
CP in one-sided I/O	0.6 ms	0.7 ms	0.5 ms	0.5 ms	0.5 ms
CP in switched I/O	0.2 ms	0.2 ms	0.2 ms	0.2 ms	0.2 ms

Runtime with Handshake

As shown in the table below, the runtime of the data handling blocks comprises up to four components:

1. Basic runtime:

   The handling block requires this time, for instance, to prepare data transmission, update the ANZW, send parameters to, or receive parameters from, the interface, etc.

   These waiting times are interface-dependent (see CP description). However, the handling block aborts the function if the interface does not respond within a maximum waiting time (PAFE, ”Interface not responding in time”).

2. Waiting time A
3. Waiting time B

$\left.\begin{array}{l}\\ \\ \end{array}\right\}$ Waiting times of the handshake

4. Data transmission time:

   This time increases proportionally with the quantity of (net) data to be transferred (see SYNCHRON, parameter BLGR).

Runtime with Handshake	SEND	RECEIVE	FETCH	RESET	SYN-CHRON
1. Basic runtime	2.3 ms	3.0 ms	1.6 ms	1.0 ms	5.1 ms
+	+	+	+	+	
2. Waiting time A					
+	0 ... 5 ms	0 ... 5 ms	0 ... 5 ms	0 ... 5 ms	0 ... 10 s startup only
3. Waiting time B					
+	+	+	+	+	
4. Max. quantity of data to be transferred	0 ... 5 ms 512 (bytes)	0 ... 5 ms 512 (bytes)	0 ... 5 ms	0 ... 5 ms	0 ... 10 ms cycle only
x	x	x			
Time per byte in the area:					
one-sided					
– MB	15 µs	35 µs			
– EB/AB	30 µs	65 µs			
– DB/DX/ZB/TB/AS	2 µs	8 µs			
switched					
– MB	20 µs	40 µs			
– EB/AB	40 µs	70 µs			
– DB/DX/ZB/TB/AS	4 µs	9 µs			

The table above illustrates that the data handling block user can influence the runtime of SEND and RECEIVE blocks by means of the number of bytes to be transmitted. The quantity of data required for a job (QLAE/ZLAE parameter) can be reduced when the send/receive data is

- checked critically
- subjected to reasonable limitations
- structured without gaps.

Whereas the QLAE/ZLAE parameters determine the quantity of data required for a **job**, the frame size specifies the **maximum** quantity of data per block call to be transmitted by the handshake (see SYNCHRON, BLGR parameter).

The ”efficiency” of a SEND/RECEIVE block; that is, the relation

$$\frac{\text{Data transmission time (4.)}}{\text{Basic runtime (1.)} + \text{Waiting time A (2.)} + \text{Waiting time B (3.)}}$$

increases with the frame size.

Notes on the Runtime

The times listed apply for a one-sided CP plugged into the CC; the times apply for a switched CP installed 2.5 m from the CC.

”Runtime” is the processing time of data handling blocks.

You can save runtime by observing the following rules:

- Direct assignment of the SSNR, A-NR, ANZW and BLGR parameters is faster than assigning them indirectly.
- Direct assignment of the source/destination parameters is faster than assigning them indirectly (type XX).
- The use of data words in DB/DX is considerably faster than using input, output and I/O bytes.

Description: Data Handling Blocks 4

This chapter contains a representation of every available data handling block with block diagram, parameter table and detailed functional description.

4.1 SEND Function Block (FB 120)

Function Block

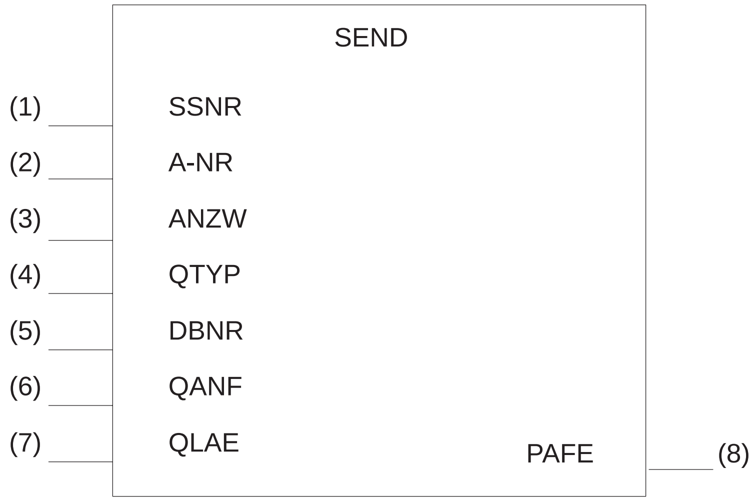


Figure 4-1 Block Diagram of the SEND FB

FB 120 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Number of the SEND/WRITE job
ANZW	I	W	Condition codeword, indicates the processing of the job
QTYP	D	KS	Type of data source (data block, flag, etc.) from which the data is transferred to the interface.
DBNR	D	KY	Number of the data block in the case of QTYP DB, DX, XX, RW; 64K area address with QTYP AS
QANF	D	KF	Relative start address of the data source
QLAE	D	KF	Quantity of source data (in bytes or words)
PAFE	Q	BY	Error bits

Function

The SEND block is used for sending of data and/or parameters from the CPU to the interface. The block has two operating modes:

- SEND-ALL
- SEND-DIRECT

The SEND-DIRECT function facilitates the ”direct” initiation of a particular SEND (or WRITE) job determined by the job number (A-NR parameter). 1 to 223 are possible job numbers. This function can, for example, be used in particular process statuses (which the user program detects and evaluates) to output a message on printer.

The SEND-ALL function is selected with job number ”0”. This function checks whether the interface has a (SEND) communication request. If it has, the interface allocates the source parameters; that is, the interface determines which data is to be transmitted from the handling block, and for which job or for which job number this data is intended. Here, ”all” job numbers can appear.

The SEND-ALL function is, for example, a simple means of having process images (process data) displayed on a monitor which can be updated regularly (CP 526). In this case, the CPU neither needs to know the image number (= job no.) which has just been selected, nor does it need to refresh the data, since the interface announces the communication request within the necessary time. The interface also fetches the data it needs for this display (and no others) from the next SEND-ALL called (see ”Additional notes”, ”Calling SEND-ALL and RECEIVE-ALL”).

SEND-DIRECT and SEND-ALL can/must also be combined if:

- the SEND-DIRECT is only being used to initiate a job – this is dependent on the parameters assigned to the data handling block and/or on the behavior of the interface during the handshake (see the CP description). The CPU transmits the data of this job to the interface via the SEND-ALL.
- the data length parameter (QLAE) assigned to the SEND-DIRECT is greater than the frame size. In this case, the interface independently calls for the subsequent blocks of this job from the SEND-ALL.

SEND-ALL

For the SEND-ALL function (job number = 0), the block requires the following parameters: ”SSNR” interface number, ”ANZW” (PLC) condition codeword, ”PAFE” error byte.

The block receives the source parameters from the interface.

It also receives the job number which is stored in the ANZW PLC and which indicates which job the ALL function was active for. A zero means ”idling”; that is, the interface has no SEND communication request.

SEND-DIRECT

A handshake with the interface to initiate a SEND job is only carried out if:

- ”RLO = 1” is transferred to the function block, and
- the interface has enabled the job (”job is running” bit in the job status = 0).

Otherwise (if no handshake takes place) it is a case of idling. When the block is idling, only the condition codeword is updated.

Typical Application

In the cyclic program, process statuses are evaluated, and influence the RLO. A SEND-DIRECT function is then called unconditionally (JU FB). Consequently, the result of the logic operation ”switches” the handshake on or off. Whatever the situation, a current copy of the job status exists in the ANZW.

For the SEND-DIRECT function, the block first requires the SSNR, A-NR ($\neq$ 0), ANZW and PAFE parameters. The block only requires the source parameters if a handshake is included. The SEND function is performed in different ways, depending on the parameters assigned to the block:

- If the interface can take the data, the SEND block transmits all the data to the interface.

  However, if the interface signals that it only requires the parameters of the job, only the source parameters will be transferred to the interface. If the quantity of data to be transferred is greater than the declared frame size, only the parameters will be transferred to the interface with the first data frame.

  The interface requests the data or the subsequent frames of this job from the processor via the SEND-ALL function.

- If the ”NN” identifier is entered in the QTYP parameter, the block accepts the source parameters from the interface, and transmits all the data or the first subframe. If the interface does not supply a set of parameters, it is a case of ”job initiation without data transfer”.

- Assigning parameters with QTYP = ”RW” is called ”WRITE”. SEND-DIRECT transmits the source and destination parameters as well as the address of the condition codeword to the interface. The interface fetches the source data via SEND-ALL.

  In the case of the CP 143, the destination parameters, together with the data, are transmitted to the communication partner, which stores them as destination data at the position specified by the destination parameters (see the CP description).

4.2 SEND-A Function Block (FB 126)

Function Block

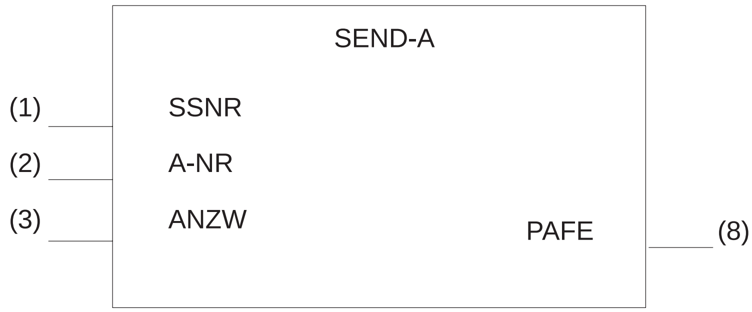


Figure 4-2 Block Diagram of the SEND-A FB

FB 126 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Job number: always 0
ANZW	I	W	Condition codeword: indicates processing of the job.
PAFE	Q	BY	Parameter assignment error: error indicators

Function

The SEND-A function block differs from the SEND function block by not having the QTYP, DBNR, QANF and QLAE parameters.

Whenever these parameters are irrelevant, the user of this block saves storage space as well as desk work and makes programs more transparent.

Further differences with reference to functionality or runtime do not exist.

4.3 RECEIVE Function Block (FB 121)

Function Block

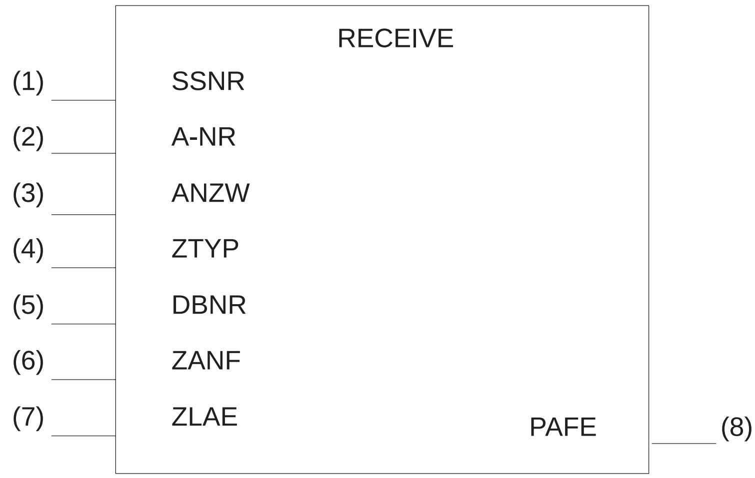


Figure 4-3 Block Diagram of the RECEIVE FB

FB 121 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Job number: number of the RECEIVE job
ANZW	I	W	Condition codeword: indicates processing of the job.
ZTYP	D	KS	Type of data source (data block, flag etc.), in which the data received from the interface is stored.
DBNR	D	KY	Number of the data block in the case of ZTYP DB, DX, XX, RW; 64K area address with ZTYP AS
ZANF	D	KF	Relative start address of the data destination
ZLAE	D	KF	Quantity of destination data (in bytes or words)
PAFE	Q	BY	Error byte

Function

The RECEIVE block is used for transferring data and/or parameters from the interface to the CPU. The block has two operating modes:

- RECEIVE-ALL
- RECEIVE-DIRECT

The RECEIVE-DIRECT function facilitates the ”direct” initiation of a particular RECEIVE job determined by the job number (A-NR). 1 to 223 are possible job numbers. This function can, for example, be used to transmit data from an intelligent I/O module to the CPU (cf. IP 252 closed-loop control module).

The RECEIVE-ALL function is selected with job number ”0”. This function checks whether the interface has a (RECEIVE) communication request. If it has, the interface allocates the destination parameters; that is, the interface determines where data received from the handling block is to be stored and for which job or for which job number this data is intended. ”All” job numbers can appear here.

The RECEIVE-ALL function is, for example, a simple means of transmitting input values (from a monitor with a keyboard) to the CPU. In this case, the CPU neither needs to know the image mask (= job no.) which has just been selected, nor whether input values are available or when they will be available, since the interface announces the communication request only when needed and the next RECEIVE-ALL called transmits the values to the CPU.

RECEIVE-DIRECT and RECEIVE-ALL can/must be combined if:

- the RECEIVE-DIRECT is only being used to initiate a job. This depends on the handling block parameter assignment and/or on the behavior of the interface during the handshake (cf. CP description). The data of this job will be transmitted from the interface to the CPU by means of the RECEIVE-ALL.
- the data length parameter (ZLAE) assigned to the RECEIVE-DIRECT is greater than the frame size. In this case, the interface independently supplies the subsequent frames of this job via the RECEIVE-ALL.

Owing to the runtime, only the data which is already in the CP can be transmitted by the RECEIVE function to the CPU.

Data which first must be requested by the CP via a bus link or which must be generated in some other way, is transmitted to the CPU by the combined action of the FETCH (see block description) and the RECEIVE-ALL function.

RECEIVE-ALL

For the RECEIVE-ALL function (job number = 0), the block requires the following parameters: ”SSNR” interface number, ”ANZW” (PLC) condition codeword, ”PAFE” error byte.

The block receives the destination parameters from the interface. It also receives the job number, which is stored in the ANZW-PLC, and indicates which job the ALL function was active for. A zero means ”idling”; that is, the interface had no RECEIVE communication request.

RECEIVE-DIRECT

A handshake with the interface to initiate a RECEIVE job is only carried out if:

- ”RLO = 1” is transferred to the function block, and
- the interface has enabled the job (”RECEIVE job ready” bit in the job status = 1).

Otherwise (if no handshake takes place) it is a case of idling. When the block idling, only the condition codeword is updated.

If a RECEIVE-DIRECT function is called unconditionally (JU FB), the result of the logic operation ”switches” the handshake on or off. In any case, a current copy of the job status exists in the condition codeword.

For the RECEIVE-DIRECT function, the block first requires the SSNR, A-NR ($\neq$ 0), ANZW and PAFE parameters. Only if a handshake is started does block require the destination parameters. The RECEIVE function performs in different ways, depending on the parameters assigned to the block:

- If the interface can provide the data, the RECEIVE block transmits all the data to the CPU. However, if (1) the interface signals that it only requires the parameters of the job, or if (2) the quantity of data to be transferred is greater than the declared frame size, only the destination parameters will be transferred to the interface. In the second case, the first data frame will also be accepted.

  The data or the subsequent frames of this job are transferred by the interface to the processor by means of the RECEIVE-ALL function. The parameters remain the same in any case for the user of the blocks. Only the time of data transfer is delayed in the cases just mentioned.
- If the ”NN” identifier is written to the ZTYP parameter, the block receives the destination parameters from the interface, and transmits all the data or the first subframe. If the interface does not supply a set of parameters, it is a case of ”job initiation without data transfer”.
- The assignment of parameters with ZTYP = ”RW”, (READ/WRITE) is meaningless with the RECEIVE function and is not permissible.

4.4 REC-A Function Block (FB 127)

Function Block

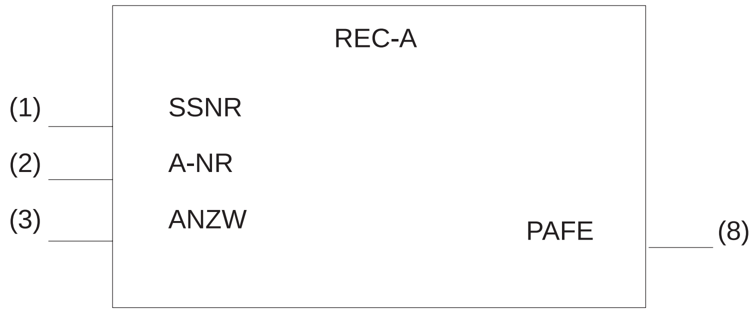


Figure 4-4 Block Diagram of the REC-A FB

FB 127 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Job number: always 0
ANZW	I	W	Condition codeword: indicates processing of job.
PAFE	Q	BY	Parameter assignment error: error byte

Function

The REC-A function block differs from the RECEIVE function block by not having the ZTYP, DBNR, ZANF and ZLAE parameters.

In cases where these parameters are irrelevant, the use of this block saves storage space as well as desk work and makes programs more transparent.

Further differences with reference to the functionality or runtime do not exist.

4.5 FETCH Function Block (FB 122)

Function Block

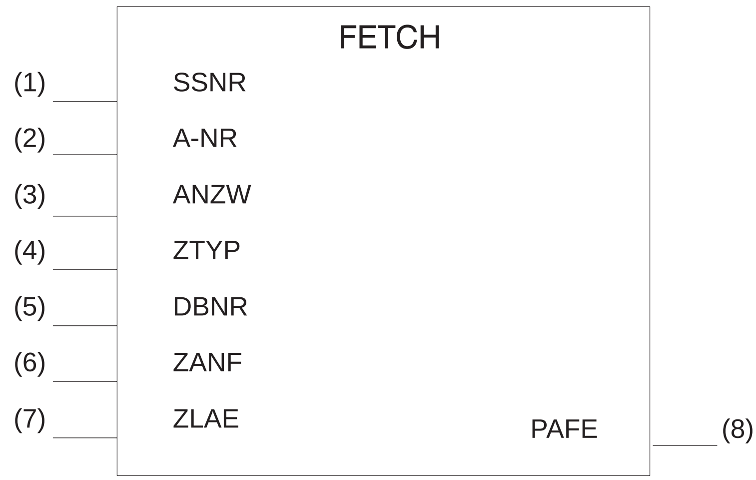


Figure 4-5 FETCH Function Block (FB 122)

FB 122 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Job number: always 0
ANZW	I	W	Condition codeword: indicates processing of job.
ZTYP	D	KS	Type of data destination (data block, flag, etc.) in which data transferred from the interface is stored.
DBNR	D	KY	Number of the data block in the case of ZTYP, DB, DX, XX, RW; 64K area address in the case of ZTYP AS
ZANF	D	KF	Relative start address of the data destination
ZLAE	D	KF	Quantity of destination data (in bytes or words)
PAFE	Q	BY	Parameter assignment error: error byte

Function

The FETCH block initiates a fetch job. This gives the CPU access to data which is not in the CP, but which must first be generated/acquired by the CP, for example, from another programmable controller by means of a bus link.

The FETCH block has only one operating mode:

- FETCH-DIRECT

1 to 223 are possible job numbers.

By transferring the job number, the destination parameters and the condition codeword address, the FETCH block informs the interface of the data required (job number), where this data is to be stored in the CPU (destination parameters) and which condition codeword this is to be indicated in. As soon as the data requested is in the CP, the interface provides the RECEIVE-ALL function with the parameters and the data. The FETCH block itself does not transmit/receive any data.

The handshake with the interface is only carried out if:

- ”RLO = 1” has been transferred to the function block, and
- the interface has enabled the job (”job running” bit in the job status = 0).

Otherwise (if no handshake takes place) it is a case of idling. When the block is idling, only the condition codeword is updated.

If a FETCH-DIRECT function is called unconditionally (JU FB), the result of the logic operation ”switches” the handshake on or off. In any case, a current copy of the job status exists in the condition codeword.

For the FETCH-DIRECT function, the block first requires the SSNR, A-NR ($\neq$ 0), ANZW and PAFE parameters. Only if a handshake is started does the block require the destination parameters. The FETCH function executes in different ways, depending on the parameters assigned to it:

- If the ”NN” identifier is written into the ZTYP parameter, this is a case of ”job initiation without parameter passing.”
- The assignment of parameters with ZTYP = ”RW” is referred to as ”READ”.

  In the case of the CP 143, this parameter assignment allows a READ job to be initiated (see the CP description).

The FETCH block transmits the source parameters and destination parameters as well as the address of the condition codeword to the interface. ”Later”, the interface transfers the data requested to the RECEIVE-ALL, which stores it at the position specified by the destination parameters.

4.6 CONTROL Function Block (FB 123)

Function Block

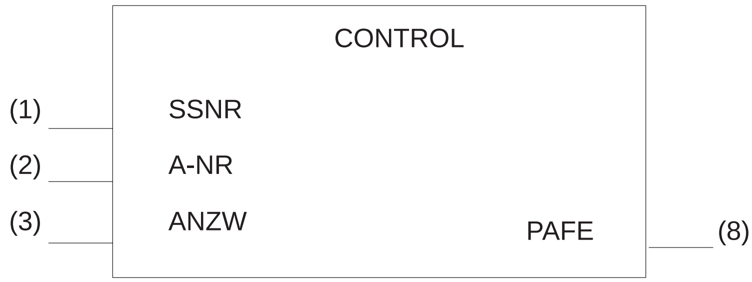


Figure 4-6 Block Diagram of the CONTROL FB

FB 123 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Job number of the job to be monitored
ANZW	I	W	Condition codeword: contains the result of the scan.
PAFE	Q	BY	Parameter assignment error: error byte

Function

The CONTROL block is used for scanning the status information of the interface. The block has two operating modes:

- CONTROL-ALL
- CONTROL-DIRECT

CONTROL-ALL

The CONTROL-ALL function (job number = 0) indicates in the low-order byte of the ANZW which job is currently being processed by the CP (or by the interface).

CONTROL-DIRECT

A job status exists in the interface for each job. It is managed by the interface and indicates, for example, whether a job is (still) running, or whether it has been completed without errors/with a particular error.

The CONTROL-DIRECT function transmits the job status selected with the A-NR parameter (job number 1 to 223) according to pattern 1 (see page II/2-24) to the condition codeword (see ANZW parameter).

4.7 RESET Function Block (FB 124)

Function Block

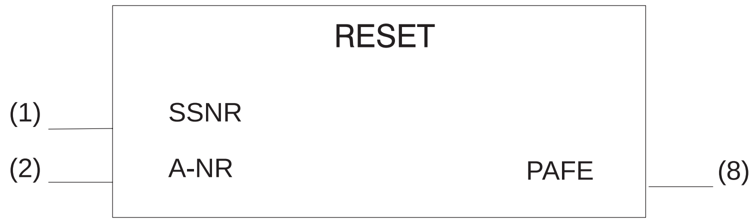


Figure 4-7 Block Diagram of the RESET FB

FB 124 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
A-NR	D	KY	Job number of the job to be reset
PAFE	Q	BY	Parameter assignment error: error byte

Function

The RESET block is RLO-dependent; the handshake with the interface is only carried out if ”RLO = 1” has been transferred to the function block.

- RESET-ALL
- RESET-DIRECT

The RESET-ALL function (job number = 0) resets all jobs of this interface. It deletes all user data or interrupts all currently running jobs.

With the ”direct” reset function (job $\neq$ 0), only the specified job of the interface is reset.

4.8 SYNCHRON Function Block (FB 125)

Function Block

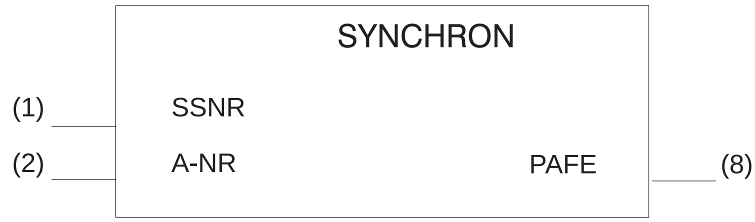


Figure 4-8 Block Diagram of the SYNCHRON FB

FB 125 Parameters

Parameter	Parameter Type	Data Type	Meaning
SSNR	D	KY	Interface number
BLGR	D	KY	Frame size
PAFE	Q	BY	Error byte

Function

The SYNCHRON block initializes the interface. The interface is deleted and preset, and the frame size is declared between the interface and the CPU. Every interface must be initialized on a ”cold restart” (OB 20), in the ”manual warm restart” (OB 21) and on a ”cold restart with memory” (OB 22). If the ”soft” STOP mode is also to be used, the SYNCHRON block must be called from the associated restart block (OB 38) for the required interfaces.

Examples of SYNCHRON DHB Calls on Restart

In the programming examples below, FB 125 is called depending on the evaluation of the H flag word.

CP switched:

```
STL                              Explanation
        :A      F0.2             Am master
        :JC     FB 125
NAME    :SYNCHRON
```

SYNCHRON DHB (FB 125) call on restart (OB 20, 21, 22), CP one-sided, CP is in subunit A:

```
STL                              Explanation
        :A      F0.4             Am subunit A
        :JC     FB 125
NAME    :SYNCHRON
```

SYNCHRON DHB (FB 125) call on restart (OB 20, 21, 22), CP one-sided, CP is in subunit B:

STL			Explanation
	:A	F0.4	**Am subunit B**
	:JC	FB 125	
NAME	:SYNCHRON		

Calling the SYNCHRON DHB (FB 125) Cyclically

If the interface has been passivated by an error (NAU..., for instance), you must depassivate and synchronize after correcting the error.

The identifier D0H is set in the PAFE byte for the duration of synchronization. FB 125 must therefore be called as long as this identifier exists.

STL			Explanation
	:		**Program for CP 1**
	:O F 10.0		F 10.0 must be set when
	:L KT 150.2		CP 1 has been repaired
	:SE T	1	Duration of depassivation max. 15 sec.
	:O(		
	:L	FY 8	PAFE byte CP 1
	:L KH	0000	
	:><F		
	:)		
	:O F	10.0	F 10.0 must be set when
	:R F	10.0	CP 1 has been repaired
	:= F	11.0	
	:JC	FB 125	
NAME	:SYNCHRON		
SSNR	:	KY0.0	Page no. for CP 1
BLGR	:	KY0.6	
PAFE	:	FY 8	
	:A F	11.0	Depassivation requested?
	:A T	1	15 sec. not yet elapsed?
	:BEC		Yes –>BE because only 1 CP can be inserted
	:		at any one time
	:A F	11.0	15 sec. not yet elapsed?
	:R F	11.0	
	:JC	FBxx	Error message: CP 1 cannot be depassivated
	:L KB	0	
	:T FY	8	

(Continued on next page)

```
STL                    Explanation
        :
        :              Program for CP 2
        :O F   10.1    F 10.1 must be set when
        :L KT  150.2   CP 2 has been repaired
        :SE T  1       Duration of depassivation max. 15 sec.
        :O(
        :L     FY 9    PAFE byte CP 2
        :L KH  0000
        :><F
        :)
        :O F   10.1    F 10.1 must be set when
        :R F   10.1    CP 2 has been repaired
        := F   11.1
        :JC    FB 125
NAME    :SYNCHRON
SSNR    :      KY0.2   Page no. for CP 2
BLGR    :      KY0.6
PAFE    :      FY 9
        :A T   1       Only one CP can be inserted at any one
        :BEC           time
        :
        :A F   11.1
        :R F   11.1
        :JC    FBxx    Error message: CP 2 cannot be depassivated
        :L KB  0
        :T FY  9
        :              Program for CP 3
        :
```

The FB is called once only via flag 10.0. The block call remains autonomous thanks to the ”D0” identifier.

Only one interface may be synchronized at any one time. The interfaces are processed in sequence.

IMPORTANT:

Please note that only one SYNCHRON DHB call can be executed per cycle since, otherwise, errors would occur in the acknowledgement monitoring time between the CPU and the CP.

Frame Size

Declaration of the frame size takes place in such a way that the SYNCHRON block transfers a ”desired” frame size to the interface corresponding to the BLGR parameter. This request is checked and, if necessary, **changed** by the interface (see the CP description). The ”resulting” frame size forms the upper limit for the SEND and RECEIVE blocks and limits the maximum quantity of (net) data bytes to be transmitted/received per block call.

If the length of the area to be transmitted (QLAE/ZLAE) is larger, subsequent frames are transmitted by the SEND-ALL/RECEIVE-ALL functions. If, for example, a SEND-DIRECT is called with a QLAE = 70 bytes, and if the frame size is 32 bytes, the SEND-DIRECT transmits 32 bytes, the first SEND-ALL transmits 32 bytes and the second SEND-ALL transmits the remaining 6 bytes.

Table 4-1 Significance of the ”Frame Size” Parameter

BLGR parameter	Frame with	
0	max. 256 bytes (default value)	Frame size desired
1	max. 16 bytes	
2	max. 32 bytes	
3	max. 64 bytes	
4	max. 128 bytes	
5	max. 256 bytes	
6	max. 512 bytes	
7 . . . 254	max. 256 bytes (default value)	
255	0 512 bytes (fixed)	

Select large frames in order to maintain high data transmission rates; low short runtimes of the data handling blocks require a small frame size (see runtime).

SIEMENS

SIMATIC S5

COM 155 H
Programmer Software for Configuring the S5-155H Programmable Controller

User's Guide
(S5-155H, Part III)

C79000-B8576-C135-05

Safety Guidelines

This manual contains notices which you should observe to ensure your own personal safety, as well as to protect the product and connected equipment. These notices are highlighted in the manual by a warning triangle and are marked as follows according to the level of danger:

Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

Caution

indicates that minor personal injury or property damage can result if proper precautions are not taken.

Note

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

The device/system may only be set up and operated in conjunction with this manual.

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground, and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

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Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

Preface (How to Use This Manual)

This User's Guide describes the purpose and use of the functions of the COM 155H (CPU 948R) Configuring Package. This package not only enables user-friendly configuring of the S5-155H PLC, but also offers diagnostics and documentation functions. These are designed specifically with the requirements of the S5-155H in mind.

COM 155H comprises a screen form system for user prompting in the following situations:

- When configuring the S5-155H
- Fault diagnostics and error display in plaintext
- Documentation of the redundancy-specific part of the configuration.

The COM functions are grouped into screen forms according to task and can be activated in the relevant screen form on the programmer. The screen forms have a menu structure (see Chapter 1).

Target Group

This User's Guide is aimed at technicians, programming staff and maintenance personnel with general systems knowledge. If you have any questions which are not answered by this Guide, please consult your local Siemens representative.

Notes on the Contents

The information below concerning the contents of the individual chapters is designed to make it easier for you to use this User's Guide.

Chapter 1: Working with COM 155H

This chapter gives you information on the component parts, the scope of supply and all possible operator inputs (menu tree) of the COM 155H software package.

Chapter 2: Main Menu

Here, you are introduced to the main menu for your configuring work with all the relevant screen forms, including the input and output parameters.

In the main menu, you can define the data source (programmable controller or programmer) for the configuration. In addition, you have access to functions such as start/stop programmable controller, diagnostics, system handling with output of directories of contents and initiation of load and delete procedures.

Chapter 3: Configuring and Initializing

This chapter describes assignment of parameters to the operating system, the DB and DX data blocks and the I/O areas of the individual expansion units (EUs). There is also an explanation of how to define the address areas of one-sided and redundant I/O.

Chapter 4: Configuring the I/O

In this chapter, you will learn how to configure the I/O - digital input and output modules, analog input and output modules, CPs and IPs.

You will find out how to get from the main I/O basic screen to the individual I/O screen forms where you enter the configuring data for the digital and analog inputs/outputs and the CPs and IPs.

Chapter 5: Error Diagnostics and Documentation

This chapter gives you information on the possibilities and methods of searching for errors which can occur in the programmable controller after transfer of the configuration data. You can gain an overview of errors which have occurred and you can also obtain detailed information on each individual error.

The procedure for documenting your configuration is then described.

Index

The alphabetical index at the end of the manual will help you locate the most important terms in the manual.

Remarks Form

The remarks form at the very end of the manual is provided for your comments and recommendations.

Reference Literature

See the Preface to ”S5-155H Programmable Controller” (Part I) in this manual.

Contents

Working with COM 155 H

1

This chapter describes how to start the COM 155H software package, the different versions of the main menu depending on whether you are using ”STEP 5 Version 3.x”, ”STEP 5 Version 6.x” or ”STEP 5 Version 7.x”, and important terms used in the configuring and operator software.

1.1 Installing and Operating COM 155H

Scope of Supply and File Names

The scope of supply of COM 155H consists of

- One 3 1/2” diskette in MS-DOS format (for STEP 5 Version 3.x and STEP 5 Version 6.x) and
- One 3 1/2” diskette in MS-DOS format (for STEP 5 Version 7.x)

You will find information on the contents of the diskettes in the relevant readme.txt file.

Configuration

The COM 155H software package runs on the following:

- AT-compatible PCs
  with MS-DOS > 5.0 or Windows 95 and the STEP 5 Basic Package, Version 3.x, 6.x or 7.x).

Installation

The installation depends on the STEP 5 version used (see Sections 1.2 and 1.4).

Operator Prompting

All COM 155H functions are activated via menu-driven operator prompting from the programmer.

- Under STEP 5 Version 3.x, COM 155H can be operated using the function keys and the keyboard, like all other programmer packages.
- Under STEP 5 Version 6.x or STEP 5 Version 7.x, the COM 155H screens can be selected using drop-down menus instead of the function keys.

  However, only the screen forms are selected using the drop-down menus; within the screen forms themselves, the function keys are used.

  Selection of a softkey on the screen with the mouse has the same effect as pressing the corresponding function key on the keyboard.

If COM 155H has been installed under STEP 5 Version 3.x, you can call COM 155H from the S5 command interpreter to access the following:

- The ”Language Selection” screen form, if COM 155H has been installed in several languages. If not, skip this screen form.
- The ”Defaults” screen form (see Figure 1-1).

  After setting the defaults (F3 <SELECT>), press F6 <EXEC> to reach the ”Main Menu” from where you can branch to the individual submenus using the softkeys <F2> to <F7>.

If COM 155H has been installed under STEP 5 Version 6.x or STEP 5 Version 7.x, you reach the Main Menu by starting STEP 5 (see Figure 1-4).

- You can use the ”Change” function to change to ”COM 155H” which will bring you to the COM 155H Main Menu.

Exiting a Screen Form (V 3.x)

If you exit a screen form with <F8>, COM 155H responds in the following way:

- If there is no screen form in the higher-level hierarchy (that is, you have returned to a branch menu), the screen form contents remain on the screen but can no longer be changed.

  The branch menu is then displayed and processed. Press the key again to clear the screen.
- If the higher-level hierarchy also contains a screen form to be processed, this new higher-level screen form is displayed and processed.

Alternatives in COM 155H

In the configuring screen forms of COM 155H, there are fields containing alternatives for your selection. You can make your selection using F3 <SELECT>. Press F3 and then press it repeatedly to display each available alternative in turn. The alternatives field is not exited.

The COM 155H V3.0 can be used with all CPU 946R/947R and 948Rs. To convert the DX1 of a CPU 946R/947R to a DX1 of a CPU 948R:

- Select presets for 948R (PG may not be online to a CPU 946R)
- Load DX1 of the 946R/947R from FD.

  Reply to the query whether the DX1 of the 946R/947R should be set with NO. The DX1 is then converted to 948R format and is located in the PG memory.
- Save DX1 to FD.

1.2 Installing and Starting COM 155H under ”STEP 5 to Version 3.x”

Installing on the Programmer with MS-DOS and STEP 5 to V3.x

- Insert the diskette for STEP 5 Version 3.x and STEP 5 Version 6.x in drive A:.
- Copy the files to the STEP5 system directory on the hard disk C: (for example, COPY A: *.* C:\STEP5\S5_SYS).

Starting COM 155H

Make sure all files are available on the hard disk. The COM 155H package can only be called up from the S5 command interpreter (KOMI). The Defaults screen form is displayed:

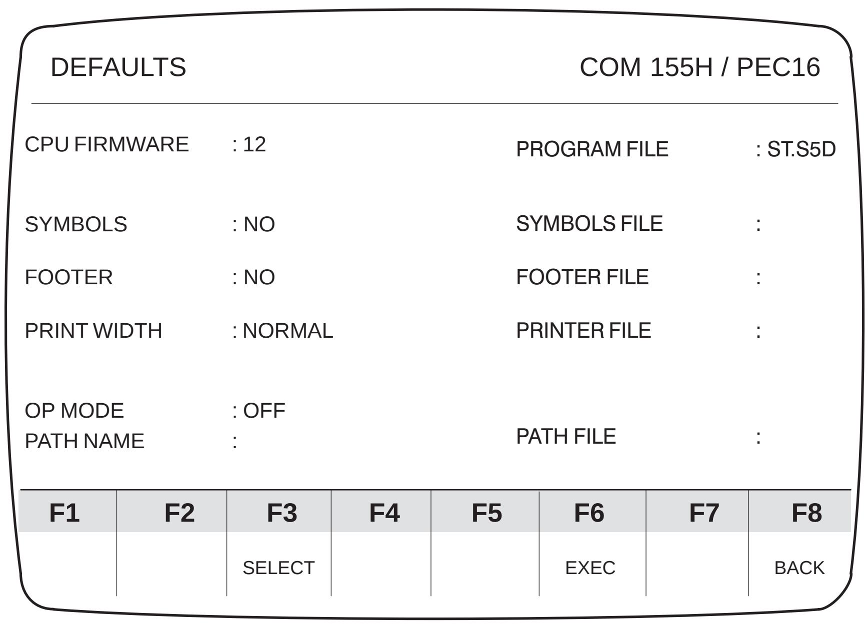


Figure 1-1 COM 155H Defaults Screen Form

- Press <SHIFT> + <Cursor to the right> or <Cursor to the left> to change from one half of the screen to the other. Press <Cursor up> and <Cursor down> to move the cursor up and down, respectively.
- If you position the cursor after the colon of the individual terms and then press F3 <SELECT>, you can enter or change the individual data easily.
- When you have entered all necessary data, press F6 <EXEC>. This enters the defaults and makes them immediately valid. The COM 155H Main Menu bar appears.
- If you want to exit the COM 155H package, press the <ESC> key.

1.3 COM 155H Functions under ”STEP 5 to Version 3.x”

Function Tree: COM 155H

The starting point for the COM 155H function tree is the ”Main Menu” (see Figure 2-1), which you reach after entering the defaults.

The individual operator screen forms are arranged in the form of the tree shown in Figures 1-2 and 1-3. In each case, the relevant menu bar is shown with the key numbers and the functions which can be called.

- The softkeys shown horizontally at the top of the figures below describe the COM 155H Main Menu.
- There are follow-on screen forms for each of the functions selectable in the main menu. The functions offered by the follow-on screen forms can be seen from the menu bars shown.

  The call paths and dependencies are symbolized by connecting lines.
- If the configuration branch (F1/F2/F3 in the Main Menu) is exited, you must store the configured data on the destination medium (diskette or programmable controller) by confirming the acknowledgement message before returning to the Main Menu.
- Function key F4 <PLC FCT> in the Main Menu contains mechanisms for starting and stopping the S5-155H programmable controller. Special error indicators and diagnostics functions can be activated using the <DIAGN.> key (F5).
- The Main Menu function <SYSHAN> (system handling = F7) enables the display of the configured external I/O available in system DB1. Following this, selective or complete documentation of the configured data from the programmable controller or from the program file can be generated. In addition, you can initiate deletions in the programmable controller or on diskette (see Figure 1-3).

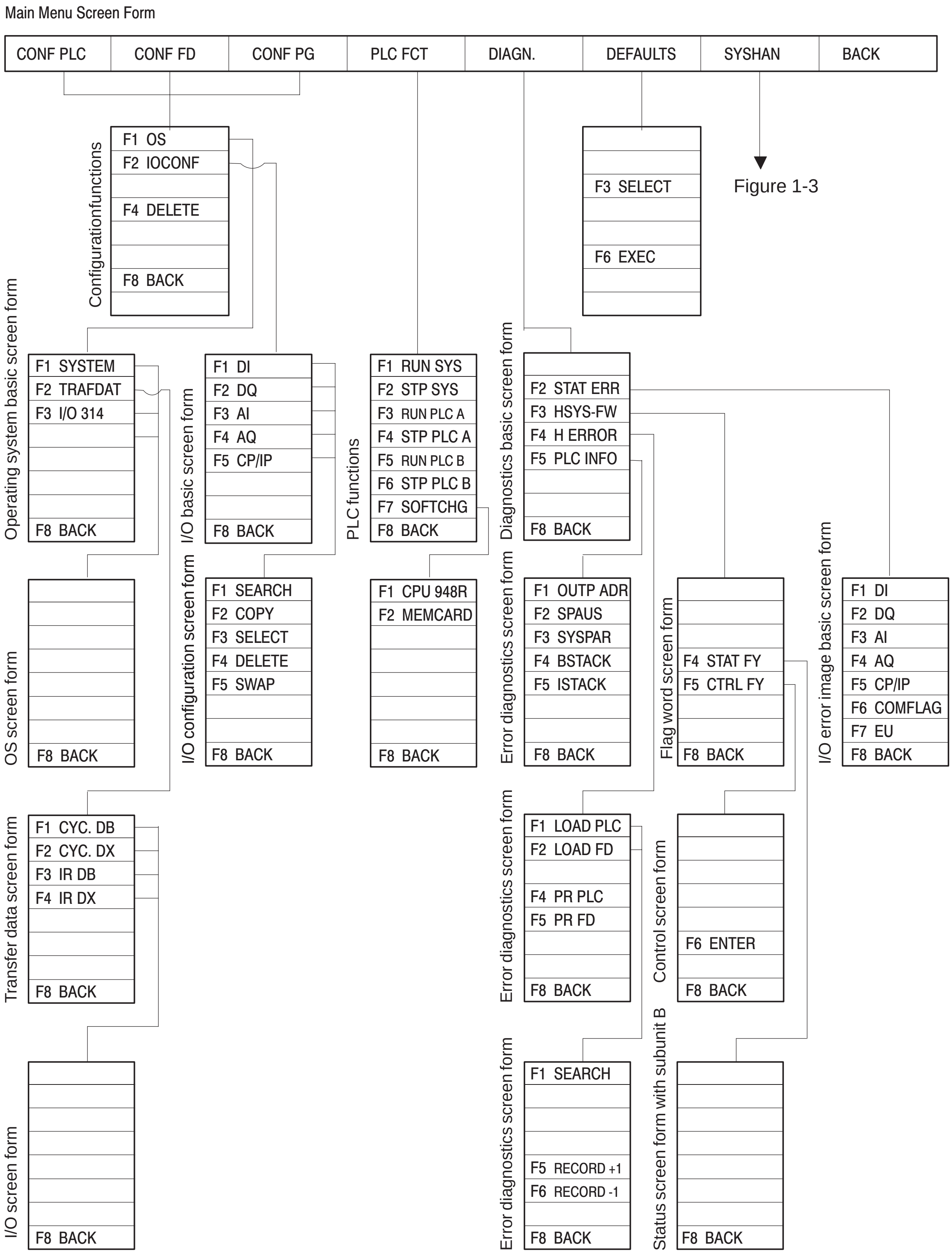


Figure 1-2 COM 155H Screen Form Tree for the S5-155H Programmable Controller (1)

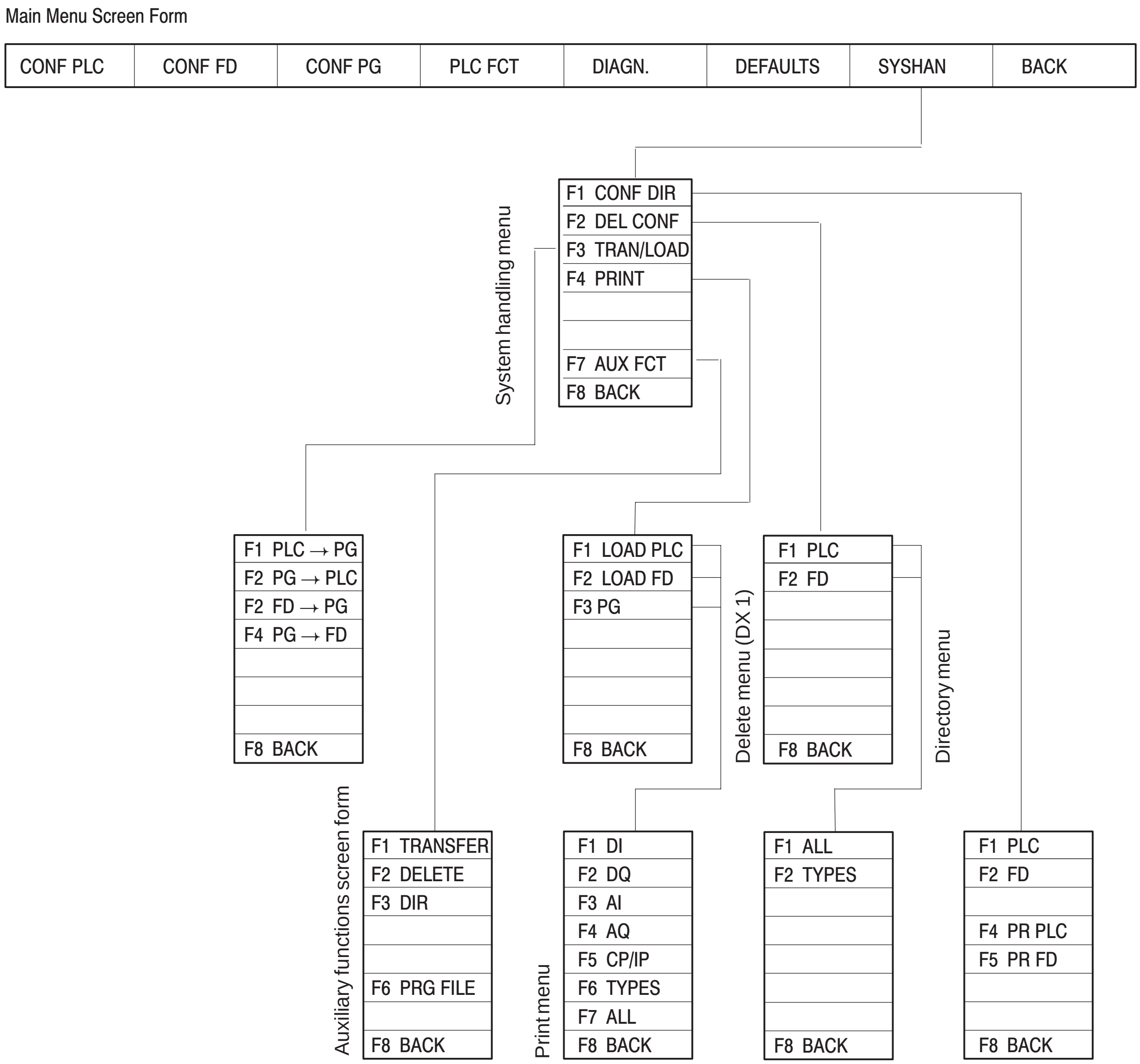


Figure 1-3 COM 155H Screen Form Tree for the S5-155H Programmable Controller (2)

1.4 Installing and Starting COM 155H under ”STEP 5 Version 6.x”

Installing on Programmer with MS-DOS and STEP 5 V6.x

1. Insert the diskette for STEP 5 Version 3.x and STEP 5 Version 6.x in drive A:.
2. Copy the files into the STEP 5 system directory on the hard disk (for example, COPY A: *.* C:\STEP5\S5_ST).
3. Change the logon file S5KES01X.OPT as described below:
   a) If there is not yet any software package loaded under STEP 5 V6.x, change the name of the S5PEC16X.OPT file supplied to S5KES01X.OPT, and copy this file also into the system directory.
   b) If there are software packages (GRAPH5, for example) already loaded, you must modify the S5KES01X.OPT file in your system directory:

      Load the S5KES01X.OPT file into the Editor and extend the user information by incrementing the ”Number of subsequent element entries” by 1 and by entering the code for the COM 155H software package.

```
Relevant texts (ITEMS) are enclosed between inverted commas. Everything
else is a comment. An element consists of three ITEMs, which must be within
one line (max. 80 characters): Meaning of the element items:
-1:5 bytes BYTE [2-6] of the program name of the executable program
-2:1-3 program number analogous to the parameter assignment
        in s5kes01x.men
-3:0 or 8 bytes of text to appear in the Change menu

File structure:     ITEM 1      Number of elements
                    ITEMS 2-4   ITEMS belonging to element    1
                    ITEMS 5-7                                 2

Start of user information:

”1”   Number of subsequent element entries for Level 6 applications
Program name         Program number        Text in CHANGE menu
”PXC16”                  ”101”                       ”COM 155H”
```

Starting COM 155H

Starting COM 155H from the STEP 5 menu bar:

- Beginning with the ”Change” menu command, select the COM 155H software package entered there.

  The drop-down menus then contain a range of COM-specific supplementary functions, as well as the standard functions of STEP 5.

1.5 COM 155H Functions under ”STEP 5 Version 6.x”

Function Tree: COM 155H

Figure 1-4 shows what the STEP 5 menu bar with the Main Menu and the individual drop-down menus look like after changing to COM 155H.

- The object-oriented or project-oriented defaults entered under STEP 5 V6.x are accepted by COM 155H.
- If you select an S5 standard function, the COM 155H user interface is suppressed and the relevant function is started. After completing the function, the COM 155H Main Menu bar appears again.

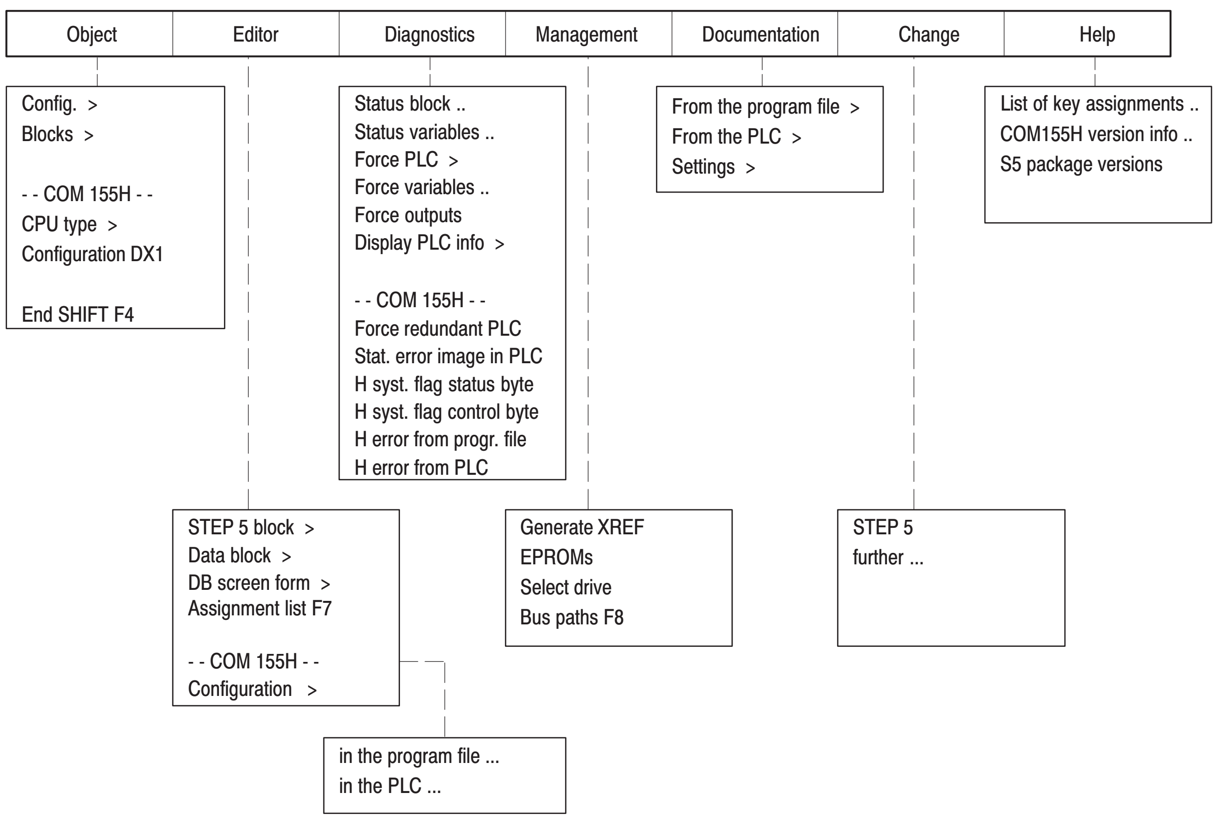


Figure 1-4 COM 155H Main Menu under STEP 5 Version 6.x

The Object Menu

Figure 1-5 shows the functions available in the Object menu for displaying directories or handling data blocks and files, and how you can activate these.

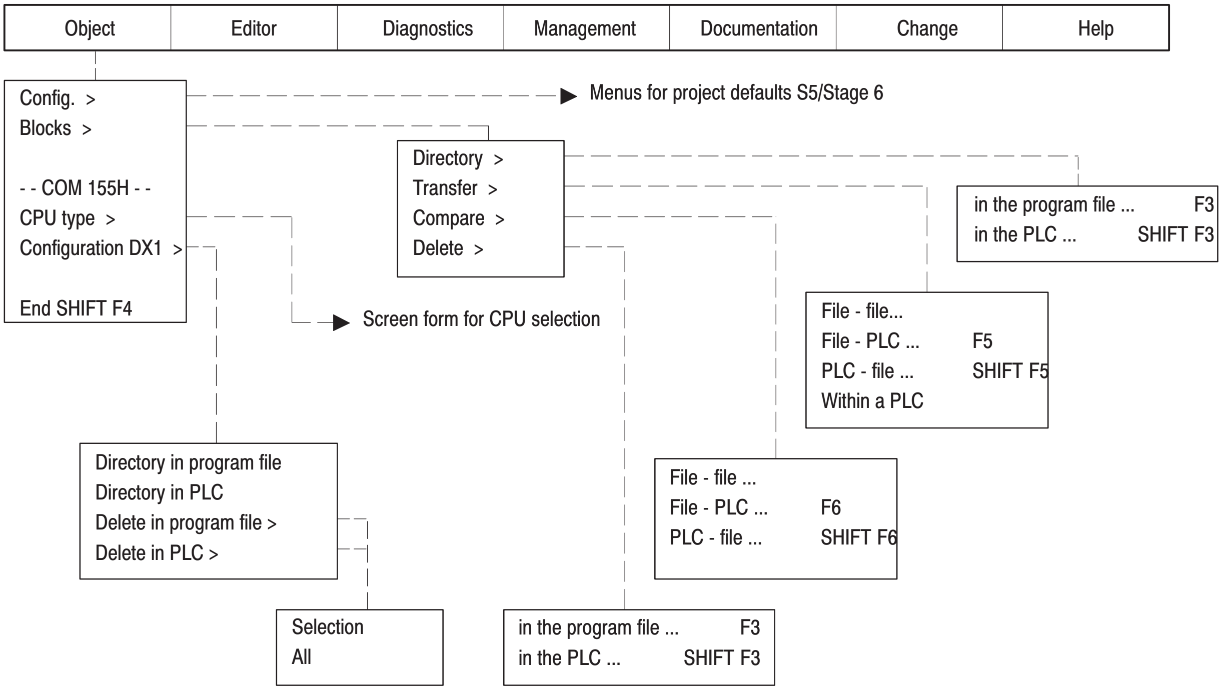


Figure 1-5 The COM 155H Object menu

CPU Type

You can choose between the following CPU types in the Selection screen form:

- CPU 946R up to firmware version 11
- CPU 948R from firmware version 12
- CPU 948R

Configuration DX1

Selection of this menu entry calls the COM 155H directory functions.

”Directory in program file” or ”Directory in PLC” gives you an overview of the configuration of DX1.

”Delete in program file” or ”Delete in PLC” takes you via a Selection menu to the ”Delete I/O” screen form, where you can select certain parts of the DX1 configuration for deletion.

The ”All” function deletes the complete DX1.

The Configuration Menu

Figure 1-6 shows the COM 155H functions available in the Configuration menu for initializing the operating system and for configuring the I/O, and how you activate these functions.

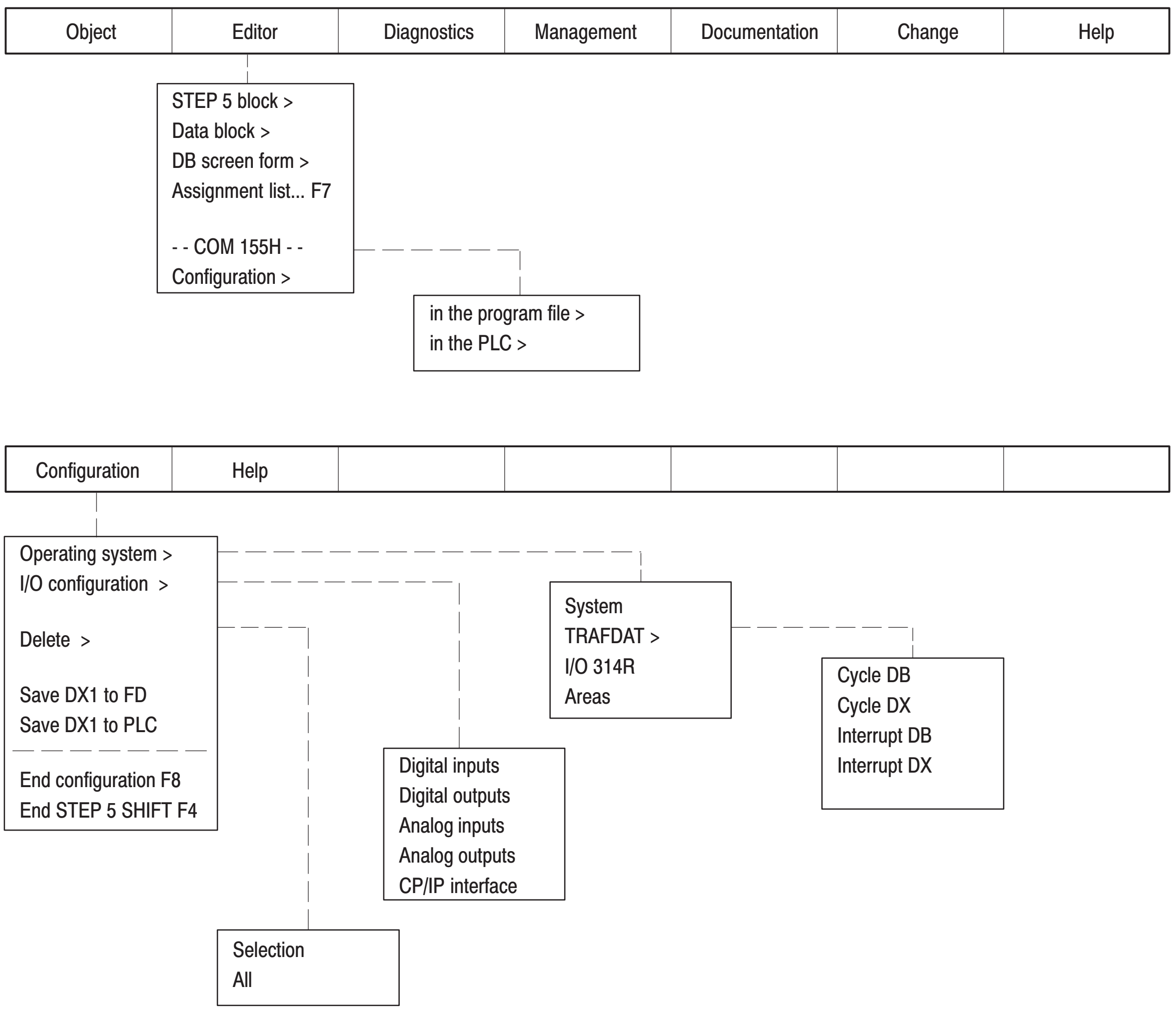


Figure 1-6 The COM 155H Configuration Menu

Initializing the Operating System

You reach the submenu for initializing the operating system via the ”Program file/PLC” Selection menu.

- Select ”System” to open the operating system basic screen form (see Figures 3-2 and 3-5).
- ”TRAFDAT” takes you to the next submenu (see Figure 3-6) for selecting the screen forms for activating the standby (see Section 3.3).
- After selecting ”I/O 314”, COM 155H opens the screen form for entering the I/O areas for the switched I/O (see Figure 3-7).

Configuring the I/O

You reach the submenu for configuring the I/O via the ”Program file/PLC” Selection menu.

- After selecting the relevant menu command, the associated I/O screen form is opened (see Figure 4-1).
- Pressing F3 <SELECT> in the softkey bar of the I/O screen form sets the relevant I/O type.

The Diagnostics Menu

Figure 1-7 shows which COM 155H functions you can activate for diagnostics purposes on the S5-155H in addition to the STEP 5 test functions.

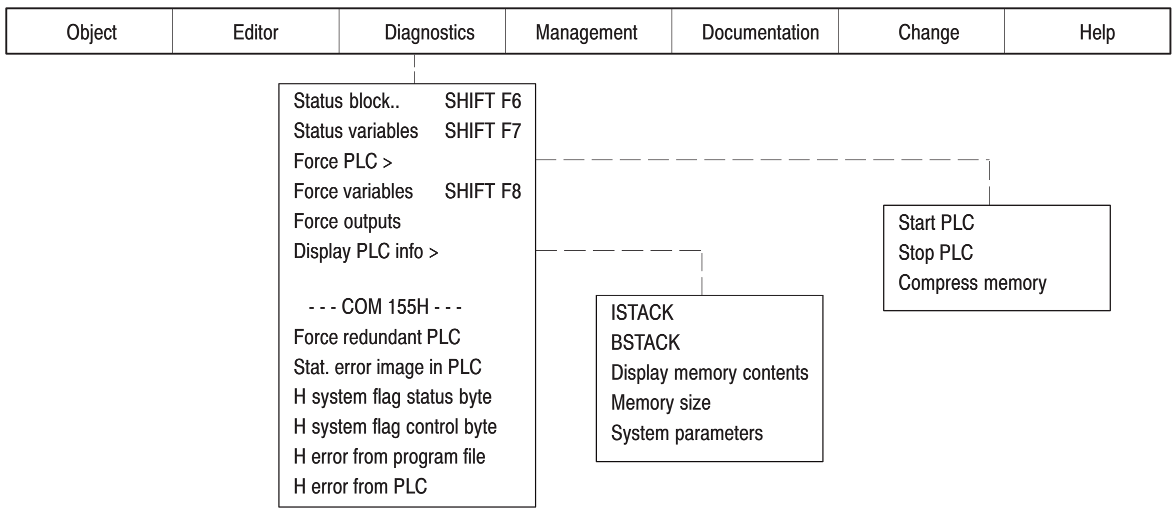


Figure 1-7 The COM 155H Diagnostics Menu

Activating Diagnostics Functions

After selecting one of the COM 155 functions in the Diagnostics menu, you reach the relevant processing screen form:

- **Force redundant PLC**

  Takes you to the ”PLC Functions” screen form (see Figure 2-2).
- **Static error image in PLC**

  Takes you to the ”Static Error Image of the I/Os” screen form (see Figure 5-1).
- **H system flag status byte**

  Takes you to the ”COM 155H Status Screen Form” (see Figure 2-6).
- **H system flag control byte**

  Takes you to the ”COM 155H Control Screen Form” (see Figure 2-7).
- **H error from program file**

  Takes you to the ”Error Diagnostics” screen form (see Figure 5-5). The error DB configured in DX1 is loaded from the diskette or the hard disk and displayed on the screen.
- **H error from PLC**

  Takes you to the ”Error Diagnostics” screen form (see Figure 5-4). The error DB configured in DX1 is loaded from the PLC and displayed.

The Documentation Menu

Figure 1-8 shows the print functions you can activate in COM 155H.

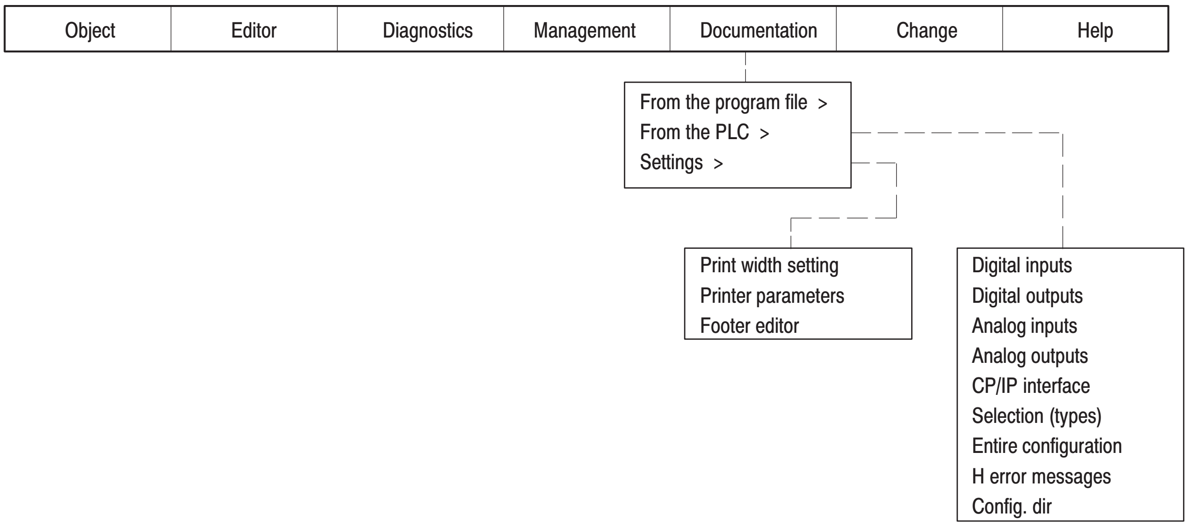


Figure 1-8 The COM 155H Documentation Menu

Activating Print Functions

You reach the submenu for print selection via the menu entries ”From the program file” or ”From the PLC”, depending on the source desired.

- Depending on the menu command selected, all types of the selected I/O category are output to the printer in each case.
- After activating **Selection (types)**, you reach the ”Print Menu” screen form in which you can select individual types for printing.
- If you activate the **H error messages** function, the reported errors located in the error DB of the selected file are printed out in compressed form.
- After selecting **Config. dir.**, an overview of the DX1 configuration is output.

1.6 Installing and Starting COM 155H under ”STEP 5 Version 7.x”

Installing on Programmer with MS-DOS and STEP 5 V7.x

1. Insert the diskette for STEP 5 Version 7.x in drive A:.
2. Start the program install.exe and follow the instructions given by the installation program.

Starting COM 155H

Starting COM 155H from the STEP 5 menu bar:

- Beginning with the ”Change” menu command, select the COM 155H software package entered there.

  The drop-down menus then contain a range of COM-specific supplementary functions, as well as the standard functions of STEP 5.

1.7 COM 155H Functions under ”STEP 5 Version 7.x”

Function Tree: COM 155H

Figure 1-9 shows what the STEP 5 menu bar with the Main Menu and the individual drop-down menus look like after changing to COM 155H.

- The object-oriented or project-oriented defaults entered under STEP 5 V 7.x are accepted by COM 155H.
- If you select an S5 standard function, the COM 155H user interface is suppressed and the relevant function is started. After completing the function, the COM 155H Main Menu bar appears again.

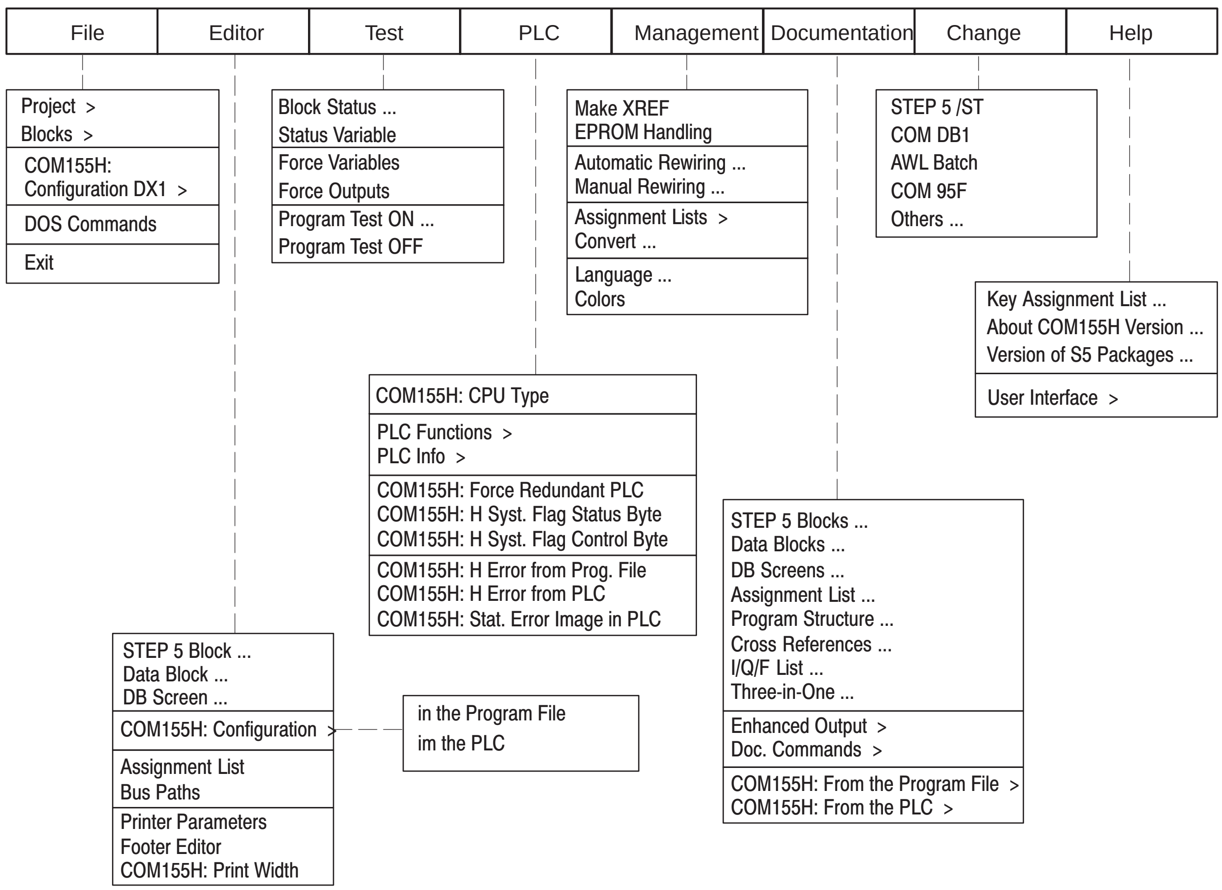


Figure 1-9 COM 155H Main Menu under STEP 5 Version 7.x

The File Menu

Figure 1-10 shows the functions available in the File menu for displaying directories or handling data blocks and files, and how you can activate these.

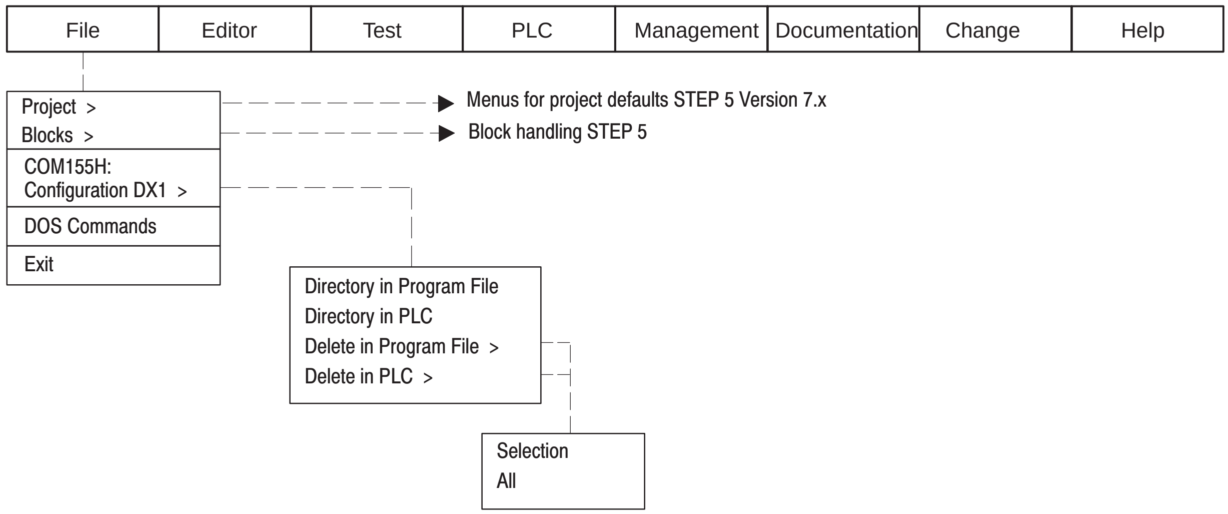


Figure 1-10 The COM 155H File menu

Configuration DX1

Selection of this menu entry calls the COM 155H directory functions.

”Directory in program file” or ”Directory in PLC” gives you an overview of the configuration of DX1.

”Delete in program file” or ”Delete in PLC” takes you via a Selection menu to the ”Delete I/O” screen form, where you can select certain parts of the DX1 configuration for deletion.

The ”All” function deletes the complete DX1.

The Configuration Menu

Figure 1-11 shows the COM 155H functions available in the Configuration menu for initializing the operating system and for configuring the I/O, and how you activate these functions.

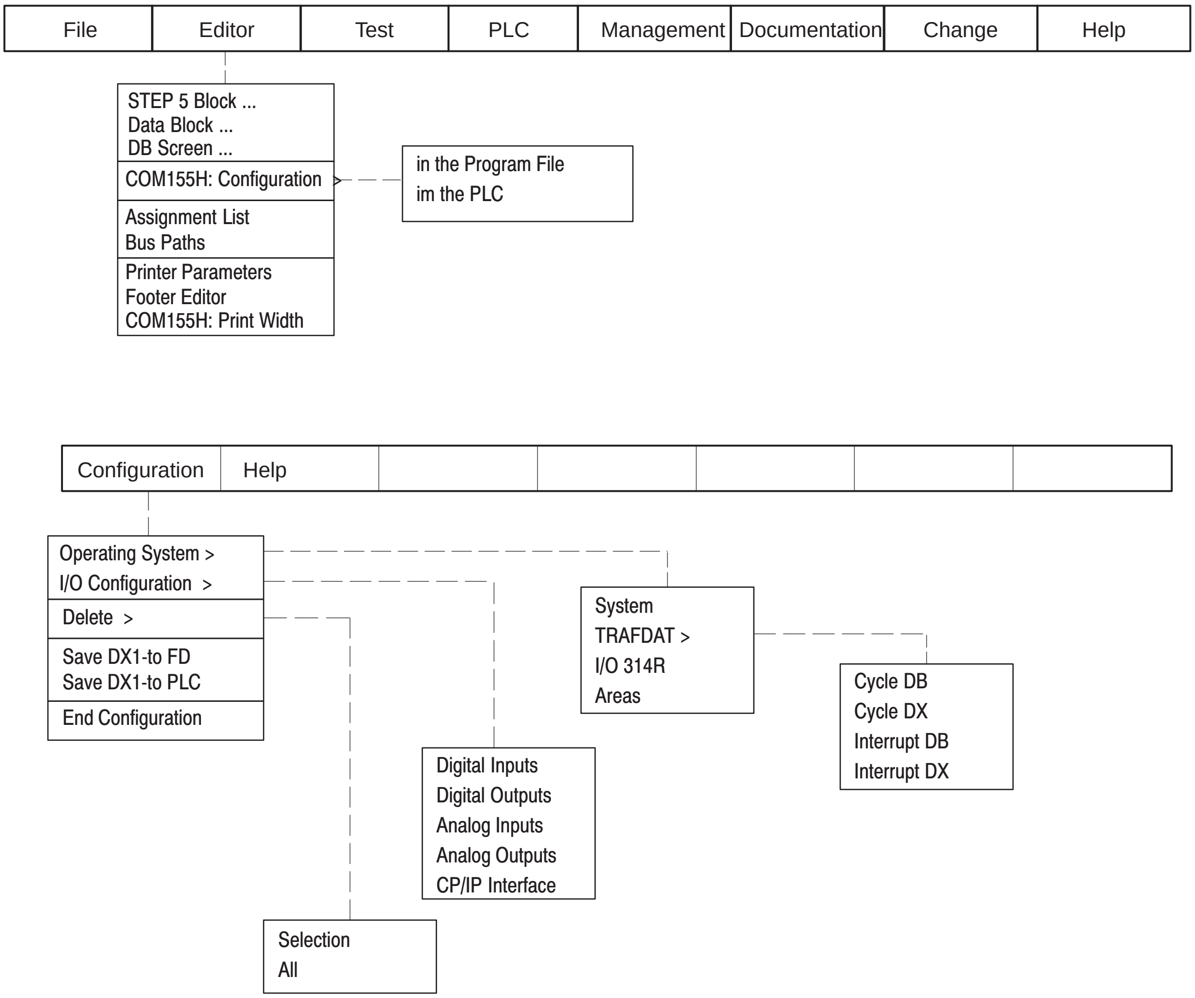


Figure 1-11 The COM 155H Configuration Menu

Initializing the Operating System

You reach the submenu for initializing the operating system via the ”Program file/PLC” Selection menu.

- Select ”System” to open the operating system basic screen form (see Figures 3-2 and 3-4).
- ”TRAFDAT” takes you to the next submenu (see Figure 3-5) for selecting the screen forms for activating the standby (see Section 3.3).
- After selecting ”I/O 314”, COM 155H opens the screen form for entering the I/O areas for the switched I/O (see Figure 3-6).

Configuring the I/O

You reach the submenu for configuring the I/O via the ”Program file/PLC” Selection menu.

- After selecting the relevant menu command, the associated I/O screen form is opened (see Figure 4-1).
- Pressing F3 <SELECT> in the softkey bar of the I/O screen form sets the relevant I/O type.

The PLC Menu

Figure 1-12 shows which COM 155H functions you can activate for diagnostics purposes on the S5-155H in addition to the STEP 5 test functions.

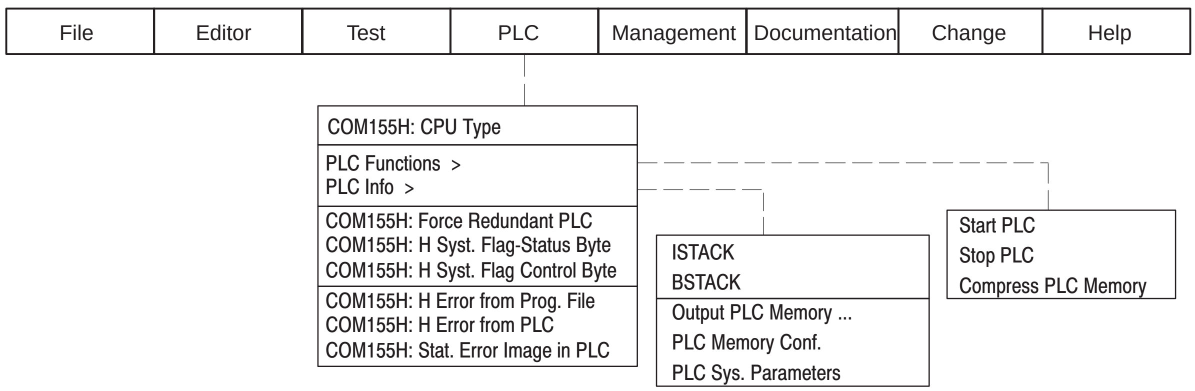


Figure 1-12 The COM 155H PLC Menu

CPU Type

You can choose between the following CPU types in the Selection screen form:

- CPU 946R up to firmware version 11
- CPU 946R from firmware version 12
- CPU 948R
- CPU 948RL

Activating Diagnostics Functions

After selecting one of the COM 155 functions in the PLC menu, you reach the relevant processing screen form:

- **Force redundant PLC**

  Takes you to the ”PLC Functions” screen form (see Figure 2-2).

- **Static error image in PLC**

  Takes you to the ”Static Error Image of the I/Os” screen form (see Figure 5-1).

- **H system flag status byte**

  Takes you to the ”COM 155H Status Screen Form” (see Figure 2-6).

- **H system flag control byte**

  Takes you to the ”COM 155H Control Screen Form” (see Figure 2-7).

- **H error from program file**

  Takes you to the ”Error Diagnostics” screen form (see Figure 5-5). The error DB configured in DX1 is loaded from the diskette or the hard disk and displayed on the screen.

- **H error from PLC**

  Takes you to the ”Error Diagnostics” screen form (see Figure 5-4). The error DB configured in DX1 is loaded from the PLC and displayed.

The Documentation Menu

Figure 1-13 shows the print functions you can activate in COM 155H.

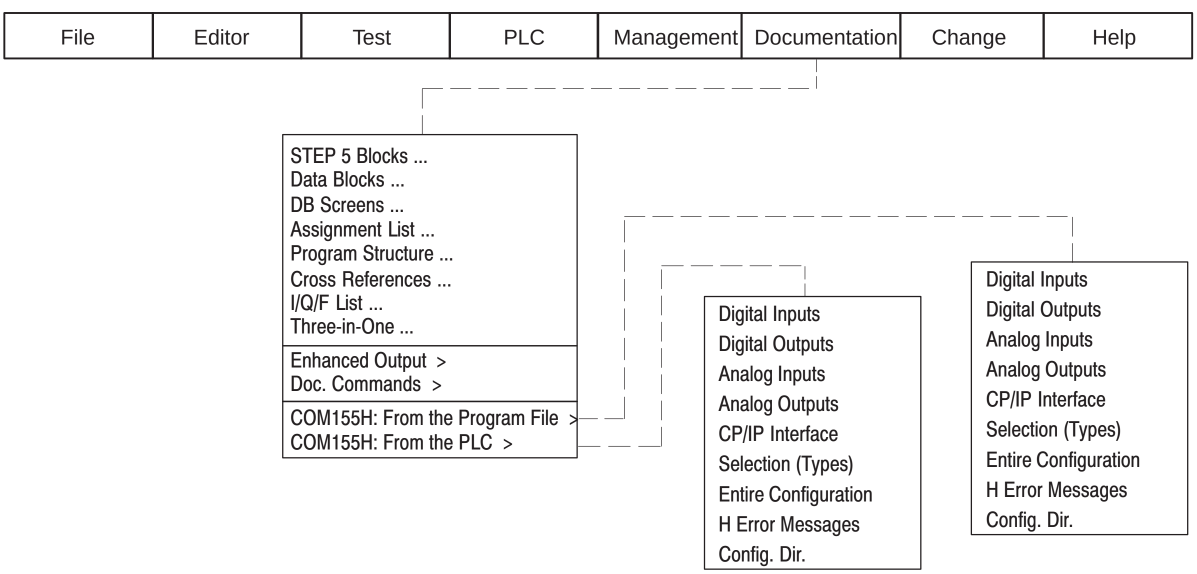


Figure 1-13 The COM 155H Documentation Menu

Activating Print Functions

You reach the submenu for print selection via the menu entries ”From the program file” or ”From the PLC”, depending on the source desired.

- Depending on the menu command selected, all types of the selected I/O category are output to the printer in each case.
- After activating **Selection (types)**, you reach the ”Print Menu” screen form in which you can select individual types for printing.
- If you activate the **H error messages** function, the reported errors located in the error DB of the selected file are printed out in compressed form.
- After selecting **Config. dir.**, an overview of the DX1 configuration is output.

1.8 Explanation of Terms Used

Firmware Version

In on-line mode, COM 155H determines the firmware version autonomously or signals if the wrong firmware version has been selected in on-line mode.

In off-line mode, the firmware version must be set to suit the version of the CPU 948R module.
Version xxx : Firmware version xx

Symbols

(see STEP 5 manual)

Footer

(see STEP 5 manual)

Print Width

You can specify three different print widths:

- Normal
- Narrow
- Extra narrow

Mode

(see STEP 5 manual)

Path Name

(see STEP 5 manual)

Program File

A program file must be set every time COM 155H accesses the hard disk or diskette (for example, load, transfer, delete).

Symbols File

(see STEP 5 manual)

Footer File

(see STEP 5 manual)

Printer File

(see STEP 5 manual)

Path File

(see STEP 5 manual)

Main Menu

2

This chapter explains the Main Menu with all associated screen forms including their input and output parameters.

2.1 The Main Menu

Main Menu Screen Form

The Main Menu appears after the defaults have been entered. The associated screen form looks like this:

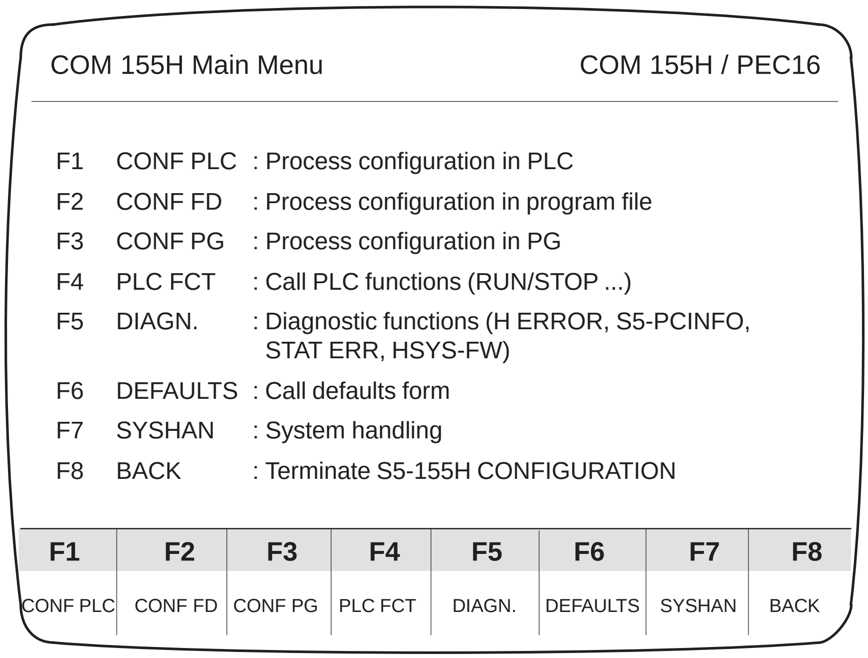


Figure 2-1 Main Menu Screen Form

You can exit COM 155H again at this point if you press F8 and answer the question ”EXIT COM 155H?” by pressing the <INSERT> key.

Before you can execute the configuration or make any changes, you must specify the data source:

Key:	**F1**	**F2**	**F3**
Source:	**<CONF PLC>**	**<CONF FD>**	**<CONF PG>**

You can then execute the configuration or make changes (see Chapter 4).

F1: <CONF PLC>

PLC is the data source for the configuration

After pressing F1, you reach the Configuration screen form (only possible on-line). This loads DX1, if it exists, from the PLC; if it does not exist, the message ”Data element does not exist” appears and an empty DX1 is generated in the programmer. This is then transferred to the PLC when you exit the configuration.

Changing the Configuration in RUN Mode

This function is required to permit defined selection of configuration changes even in the solo and redundant modes of the S5-155H.

The following configuration changes are permitted:

- Cycle DB/DX
- Interrupt DB/DX
- Switched EU numbers
- Switched I/O in the address area FF080H...FF1FFH (analog and O area)

Sequence of the Functions

1. Changing the configuration in the switched I/O: First, plug in the new I/Os.

1. Make the desired configuration change with the usual introductory function ”CONF PLC”.
2. When the function has been completed, COM 155H detects that the PLC is in RUN mode and also detects the CPU type/firmware version.
3. COM 155H now checks that the differences between the DX in the PLC and in the programmer are permissible. If they are not permissible, the message ”Change not possible - switch PLC to STOP” appears. If the changes are permissible, COM 155H transfers the DX1 to the programmable controller. All other changes can only be transferred to the programmable controller when it is in the STOP mode.
4. Start the depassivation function (control H flag word).
5. Update your user program only after you have done this.

F2: <CONF FD>

The FD is the data source for the configuration

After pressing F2, you reach the Configuration screen form. This loads DX1, if it exists, from the file; if it does not exist, the message ”File does not exist” or ”Data element does not exist” appears, and an empty DX1 is generated in the programmer. This is then stored on FD when you exit the configuration.

F3: <CONF PG>

The programmer is the data source for the configuration

After pressing F3, you reach the Configuration screen form. This loads DX1, if it exists, from the programmer memory; DX1 must then be stored with the help of the SYSHAN - TRAN PLC/FD function before you exit the configuration.

You need this selection if you have selected CONF PLC and if you have inadvertently ignored the message ”Set PLC to STOP” before exiting the configuration.

PLC Functions, F4

<PLC FCT>

By pressing F4 in the main menu, you can have COM 155H execute the following functions regardless of which subunit your programmer is connected to:

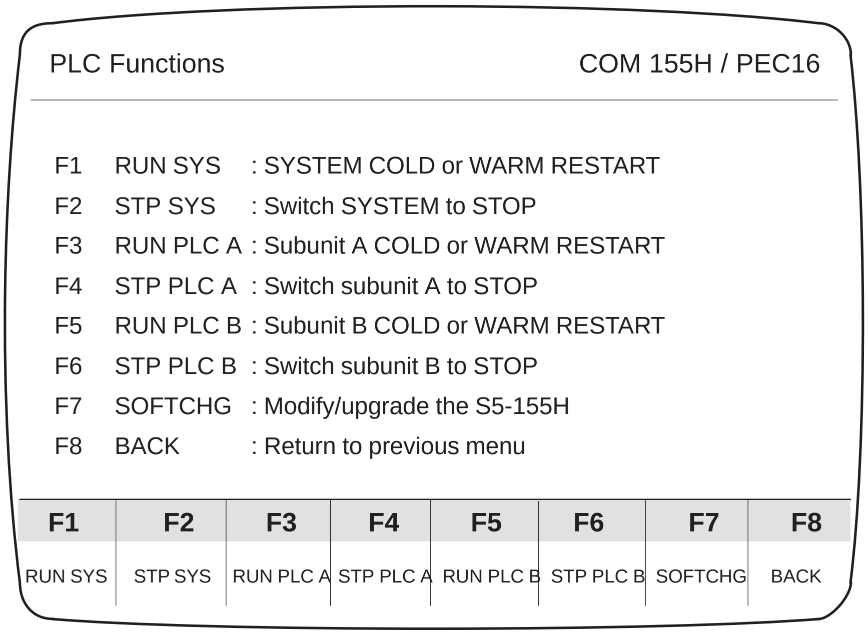


Figure 2-2 PLC Functions Menu

F1 <RUN SYS>:
The complete S5-155H PLC performs a restart routine (invocation of OB 20/OB 21).

After pressing F1, the following message appears:

”COLD (C)/WARM (W) RESTART/ABORT (BREAK):

WARM RESTART IS COLD RESTART WITH MEMORY RETENTION!”

Press the key for the desired restart mode or press <ESC>.

F2 <STP SYS>:
The complete S5-155H enters the STOP mode.

After pressing F2, the following message appears:

”SYSTEM STOP?”

Press <INSERT> for ”YES” or <ESC> for ”NO”.

F3 <RUN PLC A>:
Subunit A performs a restart routine.

After pressing F3, the following message appears:

”COLD (C)/WARM (W) RESTART/ABORT (BREAK):

WARM RESTART IS COLD RESTART WITH MEMORY RETENTION!”

Press the key for the desired restart mode or press <ESC>.

F4 <STP PLC A>:
Subunit A enters the STOP mode.

After pressing F4, the following message appears:

”PLC A STOP?”

Press <INSERT> for ”Yes” or <ESC> for ”No”.

F5 <RUN PLC B>:
Subunit B performs a restart routine.

After pressing F5, the following message appears:

”COLD (C)/WARM (W) RESTART/ABORT (BREAK):

WARM RESTART IS COLD RESTART WITH MEMORY RETENTION!”

Press the key for the desired restart mode (C or W) or press <ESC>.

F6 <STP PLC B>:
Subunit B enters the STOP mode.

After pressing F6, the following message appears:

”PLC B STOP?”

Press <INSERT> for ”Yes” or <ESC> for ”No”.

F7 <SOFTCHG>:
You can modify/upgrade the CPU or the memory card without interrupting program execution.

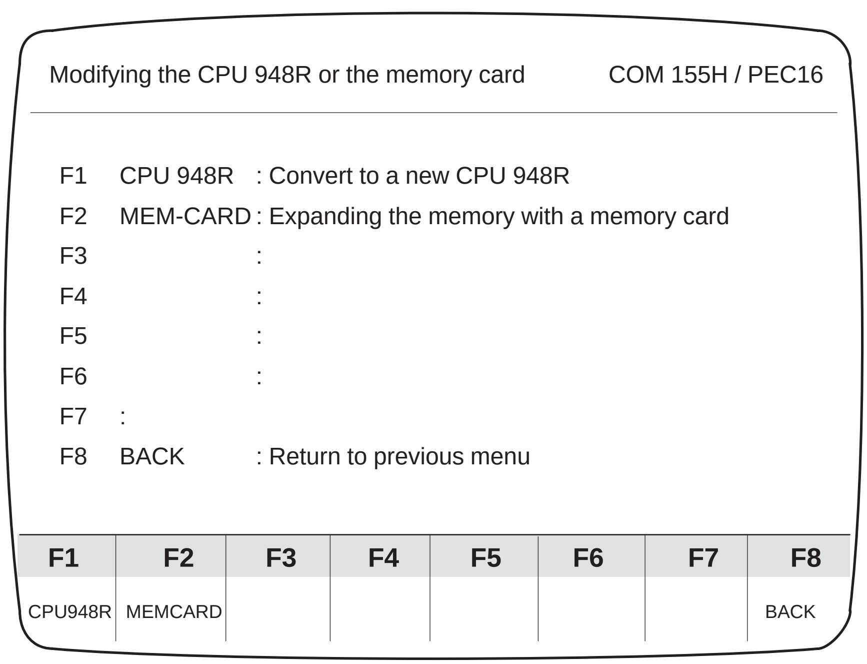


Figure 2-3 Modifying the CPU or the Memory Card

Diagnostics, F5

<DIAGN.>

Press F5 <DIAGN.> in the COM 155H Main Menu to reach the Diagnostics menu.

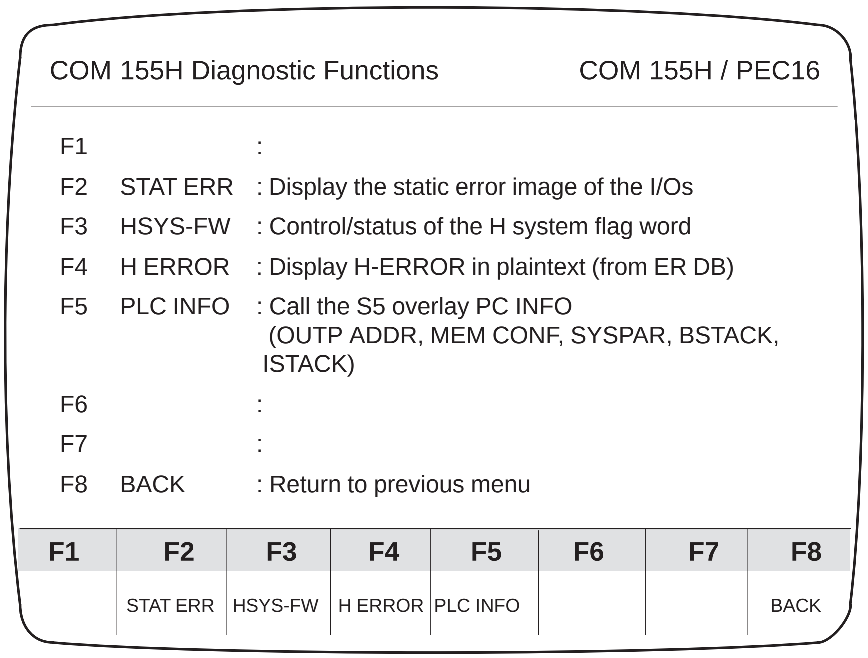


Figure 2-4 Basic Diagnostics Menu

F2 <STAT ERR>:
This key enables you to have a static error image of the I/O displayed and sorted according to the following criteria:

- Digital inputs
- Digital outputs
- Analog inputs
- Analog outputs
- CPs/IPs
- Interprocessor communications input flags
- Interprocessor communications output flags
- Expansion units.

Please refer to Chapter 5 ”Error Diagnostics and Documentation”.

F3 <HSYS-FW>:
Press this key to select either the status byte or the control byte of the H flag word. You can read out the current status information in plaintext and set the control information.

If you press F3 <HSYS-FW> in the Diagnostic Functions screen form, the following form appears on the screen:

Control/Status H System Flag Word COM 155H / PEC16

F1		:
F2		:
F3		:
F4	STAT FY	: Status display of the H system flag word
F5	CTRL FY	: Control of the H system flag word
F6		:
F7		:
F8	BACK	: Return to previous menu

F1	F2	F3	F4	F5	F6	F7	F8
			STAT FY	CTRL FY			BACK

Figure 2-5 Flag Word Menu

Press F4 to display the status byte (low-order byte of the H flag word;) FY 0, for instance.

Control/Status H System Flag Word COM 155H / PEC16

FY: 0 STATUS

PLC connected is subunit A and MASTER

0	0	
1	1	System in redundant mode
2	0	
3	0	
4	0	
5	0	Subunit B is master
6	0	
7	1	CAUTION: automatic master/standby switchover not possible

ACTIVE

F1	F2	F3	F4	F5	F6	F7	F8
							BACK

Figure 2-6 Status Form Showing Subunit B in STOP Mode and Programmer Connected to Subunit A

This form shows the following constellation:
Subunit B is in STOP mode and the programmer is connected to subunit A.

The bits concerned are set to ”1” and their meanings are explained in plaintext. This form is dynamic; that is, all changes to the status byte are shown immediately.

Select F5 <CTRL FY> in the COM 155H Flag Word Menu to display the control byte (high-order byte of the H flag word;), FY1, for instance.

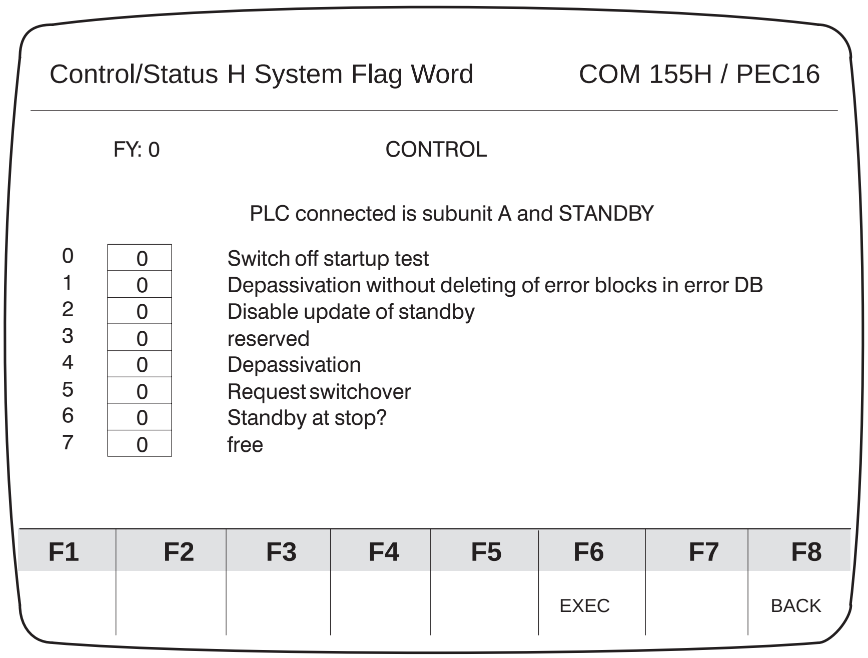


Figure 2-7 Control Form

Select the desired bit with the <Cursor up> and <Cursor down> keys. The associated texts appear in inverse video as long as the bit is ”0”. As soon as you overwrite the 0 with a 1, the text appears in normal representation. Make the change with F6 <EXEC>.

F4 <H ERROR>:
Please refer to Chapter 5 ”Error Diagnostics and Documentation”

F5 <PLC INFO>:
Press this key to call the S5 overlay ”PLC INFO” (see STEP 5 manual).

You can execute the following functions through the submenus:

- ”Output address”
- ”Memory size”
- ”System parameters”
- ”BSTACK”
- ”ISTACK”

Please also refer to the S5-155H Instructions (”H flag word”) for further information on the status and control bytes.

Defaults, F6

<DEFAULTS>

F6 <DEFAULTS> in the COM 155H Main Menu takes you to the Defaults screen form (see ”Starting COM 155H” in Section 1.4).

System Handling, F7

<SYSHAN>

Press F7 <SYSHAN> in the COM 155H Main Menu to reach the ”System Handling” menu.

The functions you can call from there refer to the configuration data block DX1. (Exception: ”Transfer to the PLC” function and ”AUX” function).

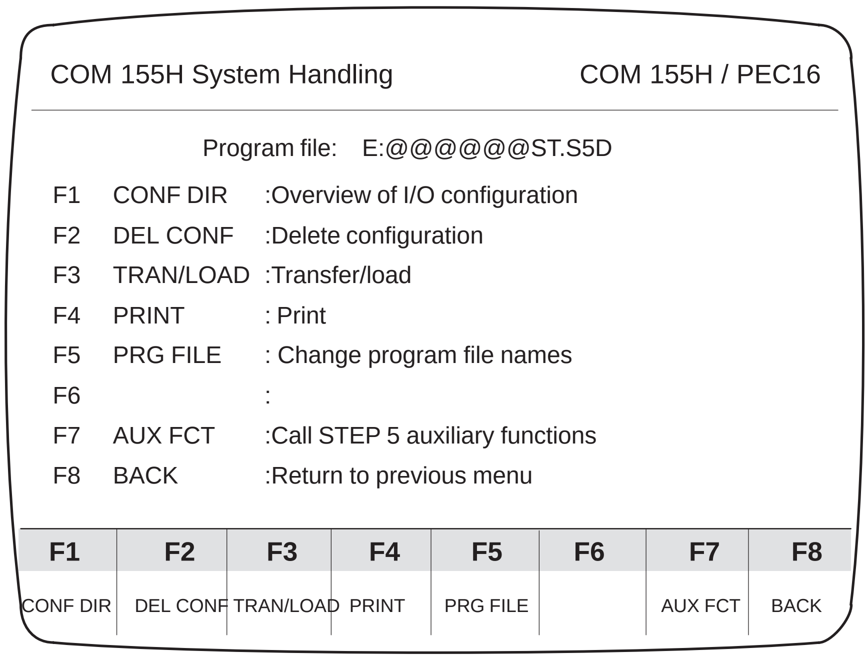


Figure 2-8 System Handling Menu

The individual functions are explained more closely below.

Make sure that a program file has been set before accessing (loading, transferring, deleting) the hard disk or the diskettes (see <F5> in the System Handling menu).

F1 <CONF DIR> (in the System Handling menu):

When this key is pressed, the Directory menu appears. This gives you an overview of your system configuration displayed on the screen. This overview can be read out from the **PLC** or from a **diskette (FD)** (see <F1> and <F2> in the directory).

If you require an overview of the configuration from the memory card, you must load DX 1 to diskette (via the S5 command interpreter EPROMs function) and then have the contents of DX 1 output from diskette (CONF DIR FD).

If access is not possible, an error message appears on the programmer screen.

If the function can be executed correctly, the overview of configured types is loaded and displayed on the programmer in the form of a list.

- <BACK> takes you back to the Directory menu.

You can also have this overview of your system configuration printed out from the programmable controller or diskette (<F4> or <F5>). Please refer to Section 5.3 ”Documenting with COM 155H”.

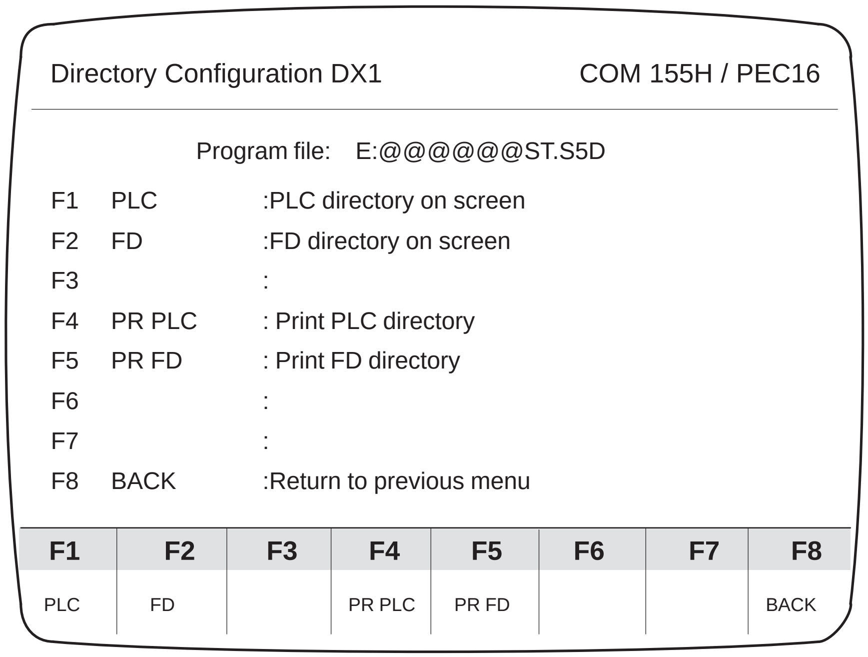


Figure 2-9 Directory Menu

F2 <DEL CONF> (in the System Handling Menu):

This key takes you to the I/O Delete menu. The Delete function refers to the DX 1 data block which has been loaded into the programmer. It deletes particular types (<F2>) of the configured digital or analog inputs and outputs, CPs/IPs or the entire system configuration (<F1>).

I/O Delete — COM 155H / PEC16

Program file: E:CPU948ST.S5D

F1	ALL	:Delete entire configuration in the PLC memory
F2	TYPES	:Delete individual types
F3		:
F4		:
F5		:
F6		:
F7		:
F8	BACK	:Return to previous menu

F1	F2	F3	F4	F5	F6	F7	F8
ALL	TYPES						BACK

Figure 2-10 Delete Menu (DX 1)

When F2 in the Delete menu is pressed, a type matrix appears on the screen:

I/O Delete — COM 155H / PEC16

Program file: B:@@@@@@ST.S5D

	DI	DQ	AI	AQ	CP/IP
Types one-sided subunit A	x				
Types one-sided subunit B					
Types switched					
Types redundant					
Types 3-channel		xxxx		xxxx	xxxx

Type has been deleted

F1	F2	F3	F4	F5	F6	F7	F8
							BACK

Figure 2-11 Delete Menu (Types)

- Move the cursor to the field of the type you wish to delete and press <INSERT>.

The message ”Type has been deleted” appears on the screen to confirm what you have done, provided the type you have selected has also been configured.

Otherwise, the message ”Type not configured” appears.

F3 <TRAN/LOAD> (in the System Handling menu):

When <F3> is pressed, the Transfer/Load menu appears on the screen.

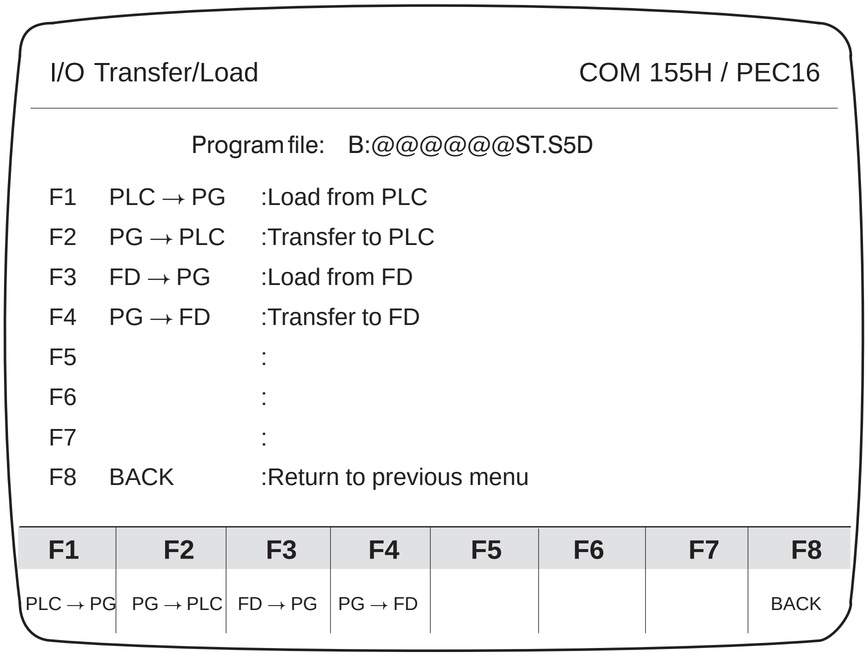


Figure 2-12 Transfer/Load Menu

<F1> <F3>: Loading in the Transfer/Load menu

The load functions enable you to read DX 1 from the programmable controller or diskette (FD) into the RAM of your programmer.

- When you press one of the load keys, the prompt ”Load configuration (DX 1)?” appears.
- Confirm by pressing <INSERT> or press <ESC> for ”No”.

During the load operation, the ”ACTIVE” message appears on the screen. On completion of the load operation, the message ”Configuration (DX 1) has been loaded” appears.

If DX 1 does not exist, an appropriate error message is displayed.

F2, F4 <LOAD FD> <TRAN FD> (loading in the Transfer/Load menu):

The transfer functions enable you to transfer data from the programmer RAM to the programmable controller or diskette.

Press <F2> to reach the ”Transfer to PLC” submenu. Here, you can decide whether you wish to transfer

- only DX 1 from the programmer memory using <F1>, or
- only the STEP 5 user program (all blocks except DX 1 and RAM DB) from the selected program file with <F3>

to the programmable controller.

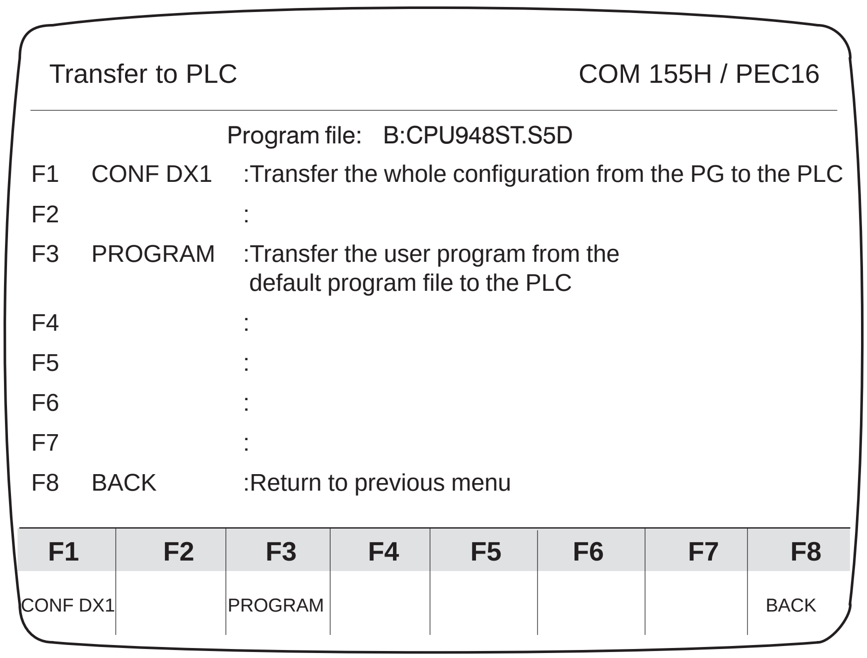


Figure 2-13 Transfer Menu

While DX 1 is being transferred, the ”ACTIVE” message appears on the screen and while the user program is being transferred, the following message appears:

”BLOCK xx yyy BEING TRANSFERRED”.

If DX 1 already exists, the following question appears:

”OVERWRITE CONFIGURATION (DX 1) IN PLC/FD?”

- Press <INSERT> for ”YES” and the existing DX 1 will be overwritten. If you press <ESC>, the DB transfer will not be executed.

If DX 1 is to be transferred to the programmable controller but the connected subunit is not in STOP mode, the following message appears in the event of an impermissible ”RUN change”:

”DX 1 change not possible – switch PLC to STOP”

F4 <PRINT> (in the System Handling menu):

First, load or determine via the screen form (Figure 2-14) the configuration data block to be used.

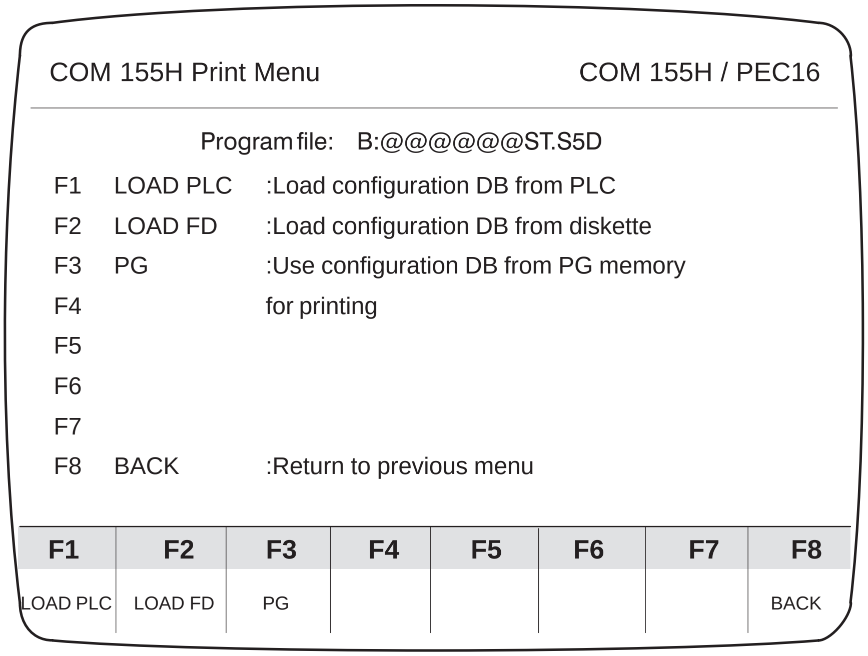


Figure 2-14 Print Menu

With the help of the Print functions (Figure 2-15), you can now

- Print all types of a particular category of configured I/O (DIs, DQs, AIs, AQs, CPs, IPs: using <F1> to <F5>)
- Print a particular type (for instance, ”switched I/O”) through all categories with <F6>
- Print the entire DX 1 with <F7>.

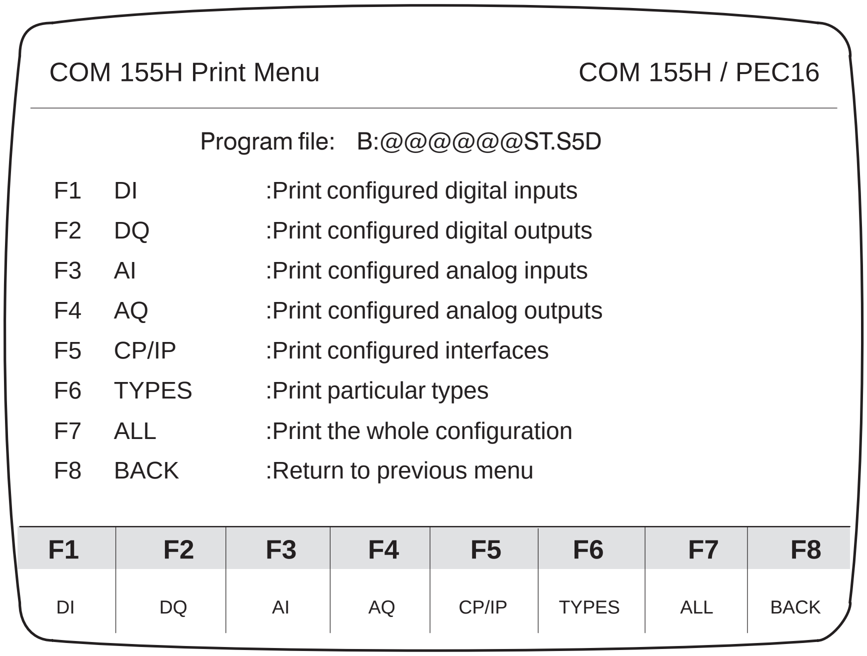


Figure 2-15 Print Menu

If the data is to be printed out from the programmable controller or diskette (FD), it must first be loaded into the programmer RAM. In the case of programmable controller and FD data, this is done via the System Handling menu, F3 <TRAN/LOAD>, and in the case of EPROM data it is done via the S5 command interpreter.

Please refer to Section 5.3 for more information on the Print menu.

F5 <PRG FILE> (in the System Handling menu):

This function enables you to create a specific program file. This setting is absolutely mandatory for all accesses (load, transfer, delete) to the hard disk or diskette. However, the function does not enable you to create a new program file. This is done with the AUX FCT (<F7>) function in the System Handling menu or in the Defaults form.

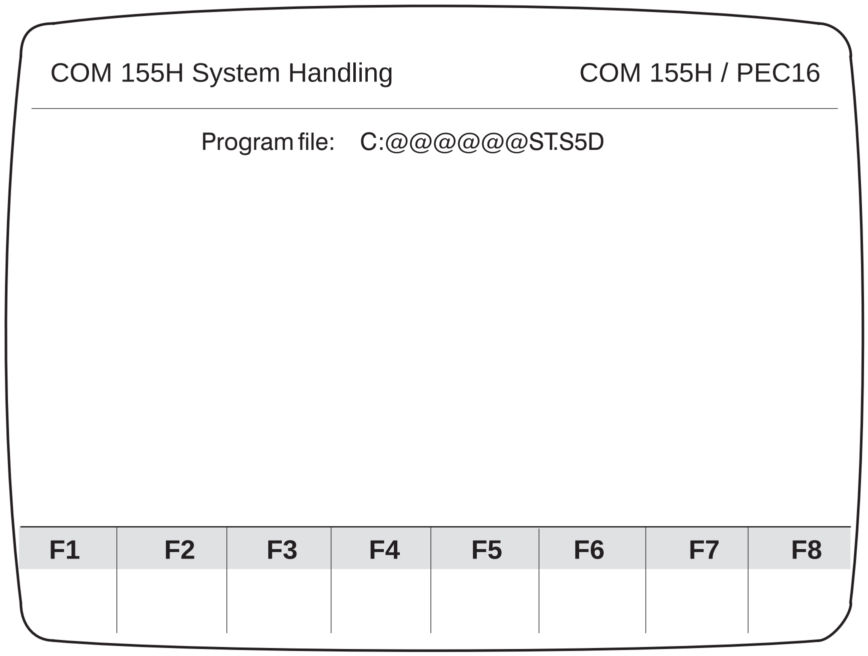


Figure 2-16 Select Program File Screen Form

Configuring and Initializing 3

From the COM 155H Basic Operating System Menu (see Section 3.1) you can reach the individual submenus via the function keys F1, F2, F3 and F4. In the submenus, you can

- Define the characteristics of the 155H operating system
- Define the DB and DX data blocks to be transferred when activating the standby
- Define the I/O areas of the individual expansion units of the switched I/O

3.1 Configuring the S5-155H PLC (S5-DOS/Stage 6)

Configuration Functions Screen Form

In this screen form, you can decide whether you want to initialize the operating system or configure the I/O.

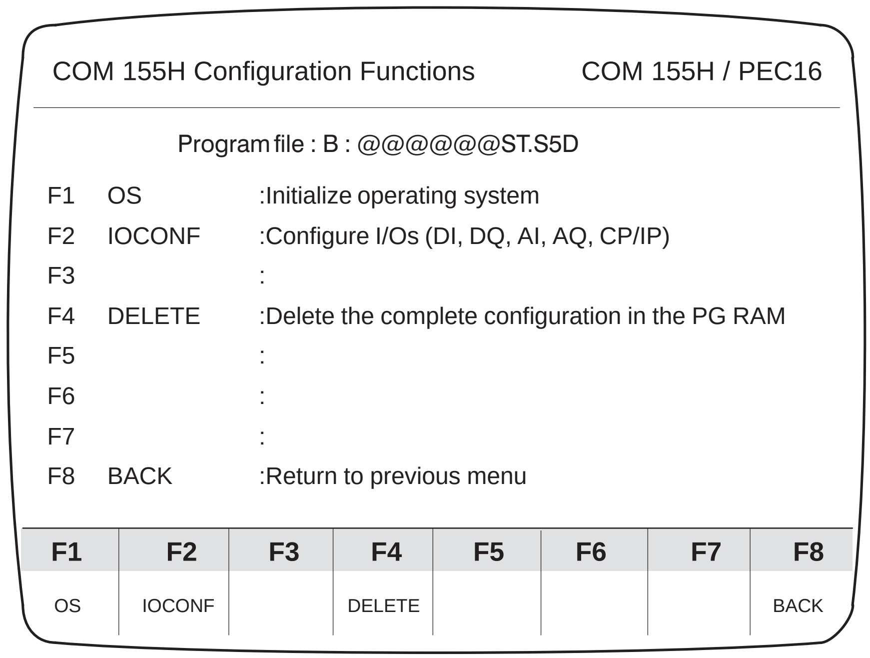


Figure 3-1 Configuration Functions Screen Form

Initializing the Operating System: <OS>

By pressing F1 in the Configuration screen form, you reach the ”Initialize Operating System” menu. Press <F1> to <F3> to select the various submenus and <F8> to exit these submenus again.

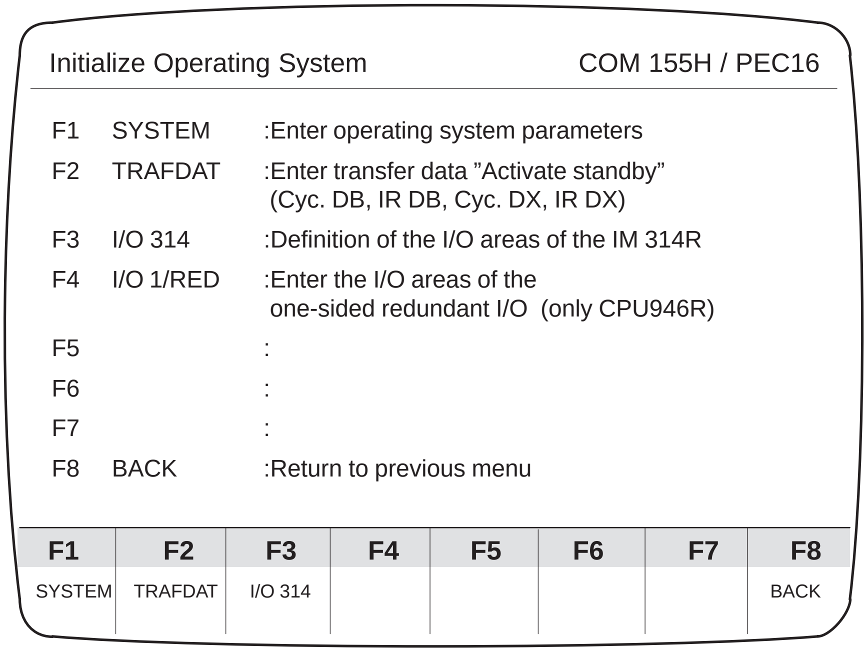


Figure 3-2 Initialize Operating System Screen Form

F1 <SYSTEM>: Initialize the redundant operating system

F2 <TRAFDAT>: Transfer data for once-only updating of the standby while activating the standby

F3 <I/O 314>: I/O areas of the expansion units of the switched I/O (IM 314R)

Initialization of the operating system is described in Section 3.2.

Configuring the I/Os: <IOCONF>

If you press F2 in the COM 155H Configuration Functions screen form, the basic screen form for configuring the I/Os appears on the programmer. Select one of the keys F1 to F5 to enter your configuration data for the digital and analog inputs and outputs and the CPs/IPs.

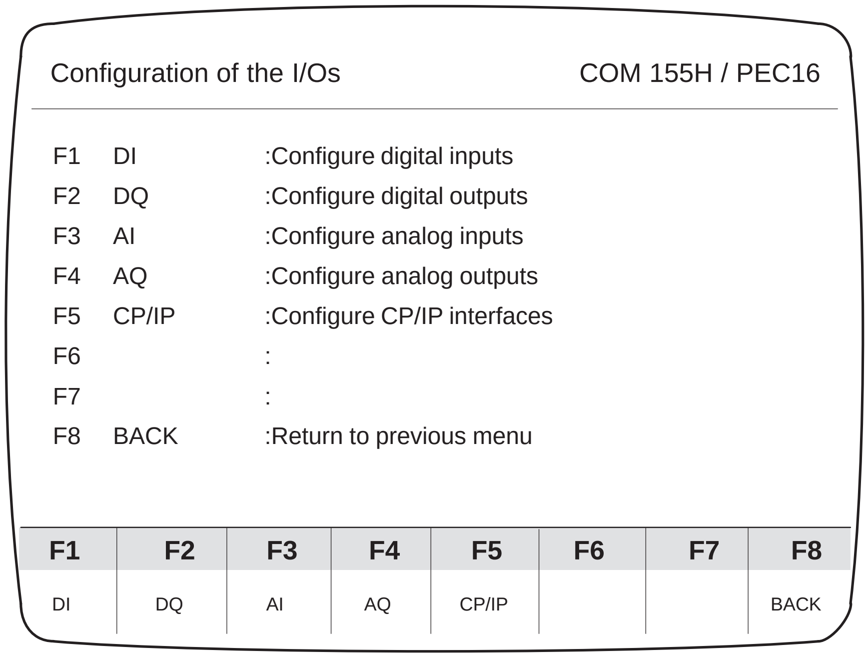


Figure 3-3 Configuration of the I/Os Screen Form

Initialization of the operating system is described in Section 3.2.

3.2 Initializing the Operating System

F1: <SYSTEM> (in the Initialize Operating System Basic Screen Form)

Operating System Parameters

You enter the relevant data for the H operating system in this screen form. If you have not loaded a DX 1 in the programmer memory (see F7 <AUX FCT> in the System Handling menu), the data input fields have default values that you can accept or modify as required.

If DX 1 has already been loaded into the programmer memory, the values initialized appear in the input fields. These can also be modified if necessary.

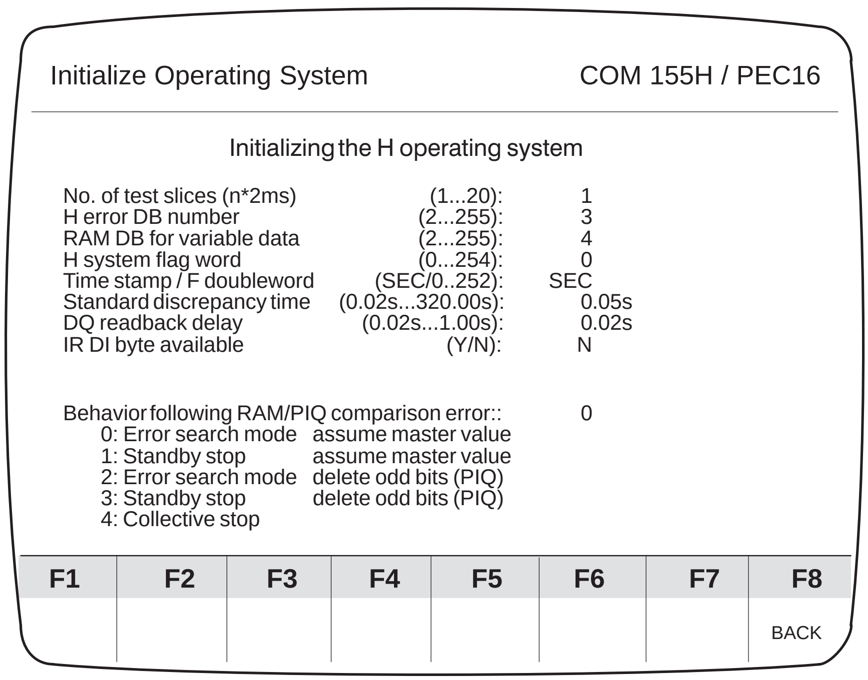


Figure 3-4 Initialize Operating System Screen Form

RAM/PIQ Comparison Error

In the case of ”RAM or PIQ comparison errors”, you can configure the following five operating system responses:

1. Master continues to operate unchanged and the standby enters the error search mode (default).
2. Master continues to operate unchanged, standby enters the STOP mode.
3. In the case of PIQ comparison error, the master sets the non-identical bit to 0, and the standby enters the error search mode;
   In the case of a RAM comparison error, the master leaves the non-identical bit unchanged, and the standby enters the error search mode.

4. In the case of a PIQ comparison error, the master sets the non-identical bit to 0, and the standby enters the STOP mode;
   In the case of a RAM comparison error, the master leaves the non-identical bit unchanged, and the standby enters the STOP mode.
5. Both subunits enter the STOP mode.

If a RAM or PIQ comparison error has been caused by a ”stuck at 0/1” error, the self-test locates the defective side immediately and sets it to STOP with an error message. Otherwise, the operating system reacts according to the configuration.

- Position the cursor at the input field whose value you wish to change, enter the new value there and confirm by pressing <INSERT> or <RETURN>.
- Use only permissible values; these are given in parentheses. If COM 155H detects a wrong input, the error message ”INVALID PARAMETER(S)” appears. Now enter a correct value or confirm the value suggested by COM 155H.

Operating System: Explanation of Parameters

Number of test slices:

Here you must enter the number of test slices that are to be used **within a PLC scan cycle** for processing the self-test routines. You can enter any number between 1 and 20.

Processing of a test slice takes 2 ms. The more test slices you process, the shorter the error detection time will be; however, the scan cycle time is increased accordingly.

H error DB number (number of error data block in the H system):

This field is for a DB number anywhere between 3 and 255. The H operating system needs this data block to manage H system errors. You can read out the data block with COM 155H support (see Section 5.2).

If you enter a number that has already been used for the RAM data block, the message

”DB NUMBER ASSIGNED”

will appear.

RAM DB for variable data

Here you can also enter any data block number between 3 and 255. The system program requires this data block to manage redundancy-specific values. It must be in the RAM.

The length of this data block depends on the scope of your system configuration and varies between one word and 32 Kwords.

If you enter a number already used for the H error data block, the message

”DB NUMBER ASSIGNED”

will appear.

H system flag word

Here you can enter a flag word between 2 and 254. One byte of this word is reserved for redundancy-specific status information entered by the H operating system. The second byte is reserved for control information that can be set by the user in his STEP 5 program.

Please refer to Section 8.5 of the S5-155H Programmable Controller Instructions for information on the structure of the H system flag word. If the value you have entered coincides with the value entered for the flag doubleword, the entry will be rejected with the message

”DOUBLE FLAG ASSIGNMENT”

Time stamp F doubleword

If you specify SEC (time stamp: year month day hour minute second) here as the parameter, the CPU real-time clock (with data and time of day) is automatically entered in the time stamp of the H error DB in the event of an error.

If you specify any flag doubleword between 0 and 255, the information in this doubleword is supplied to the time stamp in the H error DB automatically if an error message is entered there.

You can store the identifiers (for example, cycle counter, sequencer, etc.) in this flag doubleword.

Please refer to Section 8.3 of the S5-155H Programmable Controller Instructions for information on the H flag doubleword.

If the value you enter coincides with the value entered for the H system flag word, your entry will be rejected with the message

”DOUBLE FLAG ASSIGNMENT”

Standard discrepancy time

Redundant digital inputs and redundant analog inputs may have different signal states or input values over a relatively short time. By specifying a ”discrepancy time”, you can determine how long the H system is to tolerate such different signal states. A discrepancy time of between 0.01 and 320 s is permissible.

The standard discrepancy time specified in the Initialize Operating System screen form is displayed as default in the Configuration of the I/Os screen forms.

- Proceed as follows when entering the time:
  - Enter the time value before the decimal point
  - Press <RETURN>
  - Enter the time value after the decimal point
  - Press <RETURN>

IMPORTANT
This procedure applies to all time entries in COM 155H!

Readback delay

The various digital output modules have different signal propagation delays. For this reason, you must specify here the time by which the reading in of the readback DIs (digital inputs) is to be delayed.

This time then applies to **all** redundant digital outputs (see Readback delay times table in Section 11.3 of the S5-155H Instructions).

- When entering the time value, please proceed as described above.

IR DI byte available

Here you specify whether the input byte IB 0 (process-interrupt-driven program processing) is to be used as an interrupt DI byte or not.

Note:
IB 0 can only be operated as an interrupt DI in switched or redundant mode!

The maximum discrepancy time is 1.00 s. The discrepancy time specified for bit 0.0 applies to all eight inputs.

3.3 Initializing Activation of the Standby
F2: <TRAFDAT> (in the Initialize Operating System Basic Screen Form)

Transfer Data for Activating Standby

Use this form to enter all the data blocks that are to be transferred from the master to the standby when the latter is activated. These are the DB and DX data blocks.

Transfer Data ”Activate Standby” COM 155H / PEC16

F1	CYC. DB	:Configuration for transfer of DBs processed in the cyclic program part
F2	CYC. DX	:Configuration for transfer of DXs processed in the cyclic program part
F3	IR DB	:Configuration for transfer of DBs processed in the interrupt program part
F4	IR DX	:Configuration for transfer of DXs processed in the interrupt program part
F5		:
F6		:
F7		:
F8	BACK	:Return to previous menu

F1	F2	F3	F4	F5	F6	F7	F8
CYC. DB	CYC. DX	IR DB	IR DX				BACK

Figure 3-5 Transfer Data Screen Form

The contents of the DB and DX data blocks can be modified by the user program. A distinction is made between data blocks processed in the cyclic program (for example, DB or DX from OB 1 and the blocks called from there), and data blocks processed in timed interrupts and process interrupts (for example DB or DX from OB 13, timed interrupt).

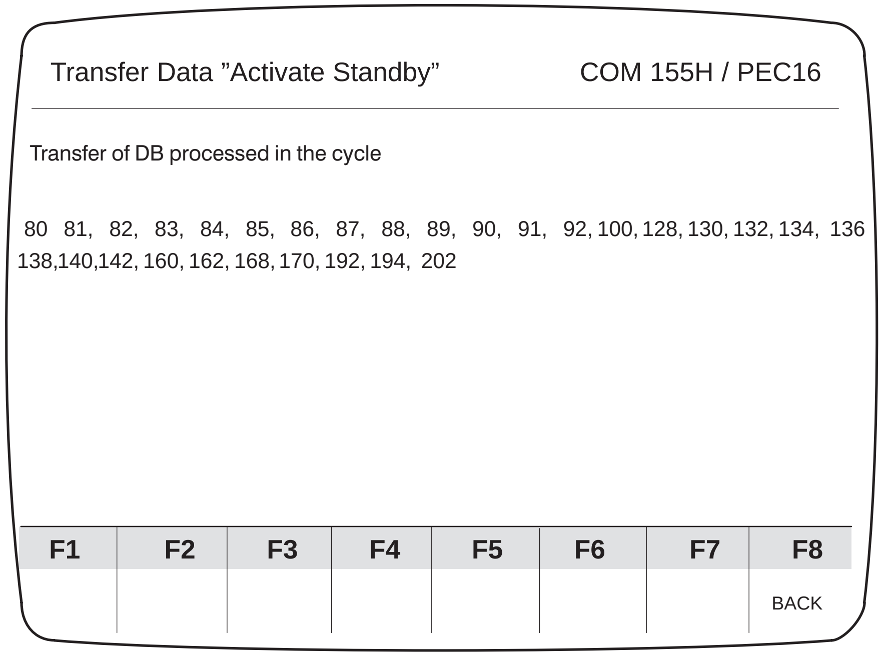
Data blocks that occur on both levels need only be entered in the interrupt DB/DX screen form.

The more data blocks you enter in these four screen forms, the longer the once-only update of the standby in the activation phase will take.

The more data blocks that have been entered in the interrupt DB/DX, the longer the interrupts are disabled by updating.

If the H error DB for the RAM DB is in one of the lists, it is automatically deleted from the list by COM 155H.

Example



Only DB/DX numbers between 3 and 255 are permissible. If a wrong number is specified, the message

”NUMERIC VALUE ILLEGAL”

appears.

- If you press <RETURN> repeatedly, COM 155H automatically increments the numerical value.

  Example:

  If you enter ”5” and press <RETURN> four times, the numerical sequence 5, 6, 7, 8, 9 appears on the screen.

- If you have to enter a longer numerical sequence, you can use the following convenient method:

  Key in ”30” ”–” ”75”, for example, and COM 155H automatically generates the complete numerical sequence from 30 to 75.

- If you wish to delete individual DB/DX numbers, overwrite these with the <space bar>.
- When you have entered all data blocks, press F8 <EXIT>. The message

  ”Data sorted and accepted”

  appears.

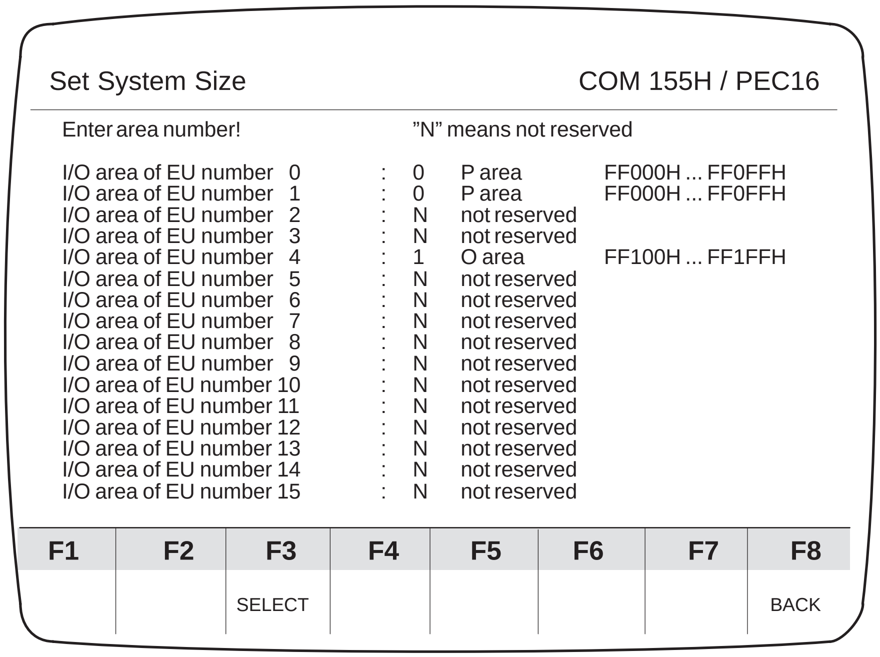
- Any entries made can be selected with the cursor.

3.4 Initializing the I/O Areas

F3: <I/O 314> (in the Initialize Operating System Basic Screen Form)

Area Parameters of the Switched I/O in the EU

This screen form is used to define the I/O areas of the IM 314R (switched I/O). The area numbers specified in the IM 314R I/O form automatically assign the relevant I/O area to the IM 314R and, consequently, to the associated expansion units.


Set System Size COM 155H / PEC16

Enter area number! ”N” means not reserved

I/O area of EU number 0	:	0	P area	FF000H ... FF0FFH
I/O area of EU number 1	:	0	P area	FF000H ... FF0FFH
I/O area of EU number 2	:	N	not reserved	
I/O area of EU number 3	:	N	not reserved	
I/O area of EU number 4	:	1	O area	FF100H ... FF1FFH
I/O area of EU number 5	:	N	not reserved	
I/O area of EU number 6	:	N	not reserved	
I/O area of EU number 7	:	N	not reserved	
I/O area of EU number 8	:	N	not reserved	
I/O area of EU number 9	:	N	not reserved	
I/O area of EU number 10	:	N	not reserved	
I/O area of EU number 11	:	N	not reserved	
I/O area of EU number 12	:	N	not reserved	
I/O area of EU number 13	:	N	not reserved	
I/O area of EU number 14	:	N	not reserved	
I/O area of EU number 15	:	N	not reserved	

F1	F2	F3	F4	F5	F6	F7	F8
		SELECT					BACK

Figure 3-6 IM 314R I/O Screen Form

Only block numbers 0, 1, 3, 12 and 13 are permissible. If you specify a wrong number, the message

”INVALID PARAMETER(S)”

appears.

When you press F8 <EXIT>, the message

”Data accepted”

appears to confirm this.

4 Configuring the I/O

The F1 to F5 keys in the I/O basic screen form take you into the individual I/O forms in which you can enter your configuration data for the digital and analog inputs/outputs, as well as the CPs and IPs (see Section 4.2).

4.1 General Structure of the I/O Configuration Screen Forms

I/O Basic Screen Form

The I/O Configuration screen form in COM 155H is structured according to the following pattern:

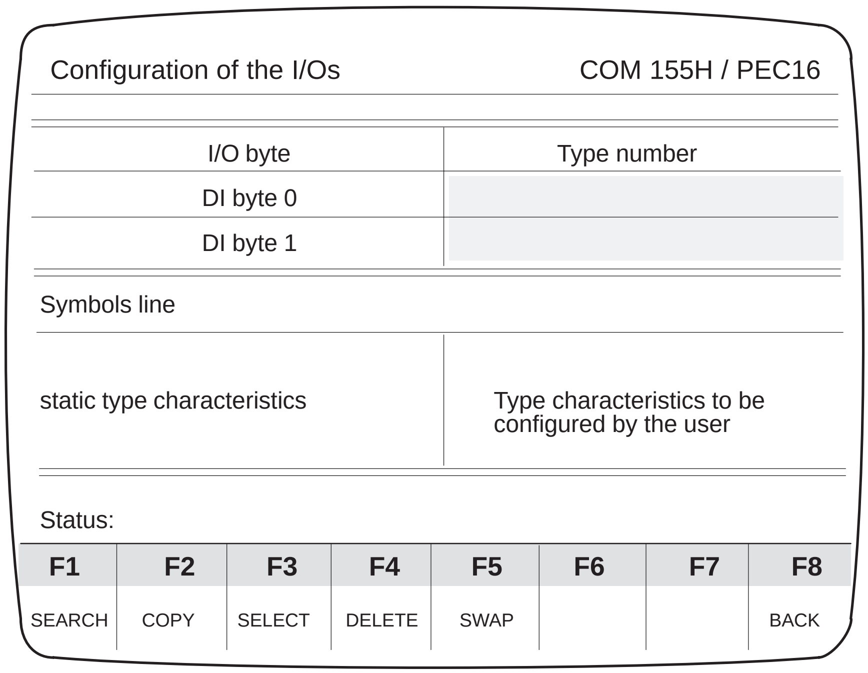


Figure 4-1 Structure of the COM 155H I/O Configuration Screen Form

To help you configure your I/O bytes/words, the S5-155H has a number of different I/O types. By specifying a **type number** for a specific I/O byte, you define the following:

a) the signal type: DI, DQ, AI, AQ, CP/IP

b) the mode: one-sided, switched, redundant, three-channel redundant

Address area:

DI	0 ... 255	P area
DI	256 ... 511	O area
DQ	0 ... 255	P area
DQ	256 ... 511	O area
AI/AQ	128 ... 254	P area
AI/AQ	256 ... 510	O area

The following table contains all configurable I/O types

Table 2-1 Configurable I/O Types

Type No.	Meaning	Fault Tolerance
1	DI byte 1-channel	Standard (as for S5-155U)
2	DI byte switched	Enhanced
3	DI byte 2-channel redundant	High
4	DI byte 3-channel redundant	Highest
8	DQ byte 1-channel	Standard
9	DQ byte switched	Enhanced
10	DQ byte 2-channel redundant	High
11	DQ byte 2-channel redundant	High, with 3 R-DIs
13	AI channel 1-channel	Standard
14	AI channel switched	Enhanced
15	AI channel 2-channel redundant	High
16	AI channel 3-channel redundant	Highest
18	AQ channel 1-channel	Standard
19	AQ channel switched	Enhanced
20	AQ channel redundant	High (without error location)
21	AQ channel redundant with error location	High
24	CP/IP 1-channel	Standard
25	CP/IP switched	Enhanced

Displays in the Configuration Screen Form

In the top left corner of the Configuration of the I/Os screen form (see Fig. 4-1), the I/O byte/word or the interface number is displayed and, to the right of this, the associated type. The next I/O bytes/words follow underneath.

When a specific configuration screen form (DI, DQ, AI etc.) is selected, the cursor is located in the Type number field.

- If you press F3, the lowest associated type number in each case is displayed (”1” for DI, ”8” for DQ, etc.)
- You can select another type by pressing F3 <SELECT> (e.g. for DI ring selection 1, 2, 3, 4, 1, 2, 3, 4, 1, etc.)

The **symbols** line indicates the I/O byte or word the cursor is currently positioned at (for example, digital input 2.3 or analog output 128). In addition, the associated abbreviated symbol (eight characters) and the non-abbreviated symbol (14 characters) are indicated here, provided you have created them (for the digital I/O area 0 to 127).

Example:

Symbols line: Valve 1 Valves for pumps 0 to 7

- Confirm the type by pressing <RETURN> or <INSERT>. The associated characteristics field appears. The cursor is located in the right-hand half of this field.

Processing the I/O Configuration Screen Form

The bottom half of the Configuration form contains the **characteristics field** in which the characteristics of the current type are displayed. The left-hand field contains the fixed or static characteristics assigned to a particular type. The right-hand field contains the characteristics to be configured by the user for the current type.

- Enter the necessary data and confirm each entry with <RETURN> or <INSERT>.

When you have made your last entry, the cursor will jump back up to the line of the next byte/word.

- The desired byte or word number can be selected with the <Cursor up> and <Cursor down> keys (scroll function).

When you have configured your system and stored it in the programmer memory, bytes/words that have already been configured will be automatically displayed when you make entries. This applies also to inputs or output already reserved as L-DI, L-DQ and R-DI. You can then no longer specify a type number.

The current processing status (”TYPE INPUT” or ”SWAP”, for instance) is displayed in the left-hand half of the **status and error line**; error messages appear in the right-hand half.

Keys in the Configuration Screen Form

F1: <SEARCH>

This function enables you to select a random byte, word or interface number quickly and without having to use the cursor.

- Press <F1> and enter the byte/word or interface number you are looking for. The cursor then appears in the line of the specified byte/word or the specified interface number.

F2: <COPY>

This function allows you to copy the configuration of a particular byte/word or interface number to another byte/word or another interface number.

After you have entered the desired byte number(s), the message

”DESTINATION END AT BYTE x COPY?”

appears on the screen.

Confirm with the <INSERT> key.

If you make an illegal specification, COM 155H aborts and an error message appears, for example:

”DESTIN. AREA IN SOURCE AREA” or

”READBACK I/O: ABORT”.

The following cannot be copied:

- L-DI
- L-DQ
- R-DI
- DI type 4
- DQ types 10 and 11

- AI type 16
- AQ type 21

F3: <SELECT>

When the cursor is in the top-right Type number field, you can use this specification to select all possible I/O types (for example, DI ring selection 1, 2, 3, 4, 1, 2, 3, 4, 1, etc.). Confirm the type number displayed with the <RETURN> key. Further, you can use the <SELECT> key for making selections in the characteristics field (for instance, AQ type 21).

F4: <DELETE>

This function deletes one or more bytes/words in your configuration. When you have entered the byte number(s), the question ”DELETE?” appears on the screen.

- Confirm with the <INSERT> key or press <ESC>.
- If you want to delete a number of successive bytes, you can specify, for example, ”10” ”-” ”15”. COM 155H then deletes bytes 10, 11, 12, 13, 14 and 15.

F5: <SWAP>

This function swaps configuration data between individual bytes words.

The following message appears on the screen:

”DESTINATION END IN BYTE x ABORT?”

- Confirm with <INSERT> or press <ESC>.

The following cannot be swapped:

- L-DI
- L-DQ
- R-DI

COM 155H generates the error message ”READBACK I/O: ABORT”

- DI types 1+2 in the analog area (AI and AQ screen forms, 128 to 254)
- DQ types 8+9 in the analog area (AI and AQ screen forms, 128 to 254)

4.2 Structure of the Individual I/O Configuration Screen Forms

When configuring your I/Os, please refer to the relevant chapter in the S5-155H Instructions.

Digital Inputs: F1

<DI> (in the I/O basic screen form)

The COM 155H Configuration of the I/Os Type 1 form appears on the screen.

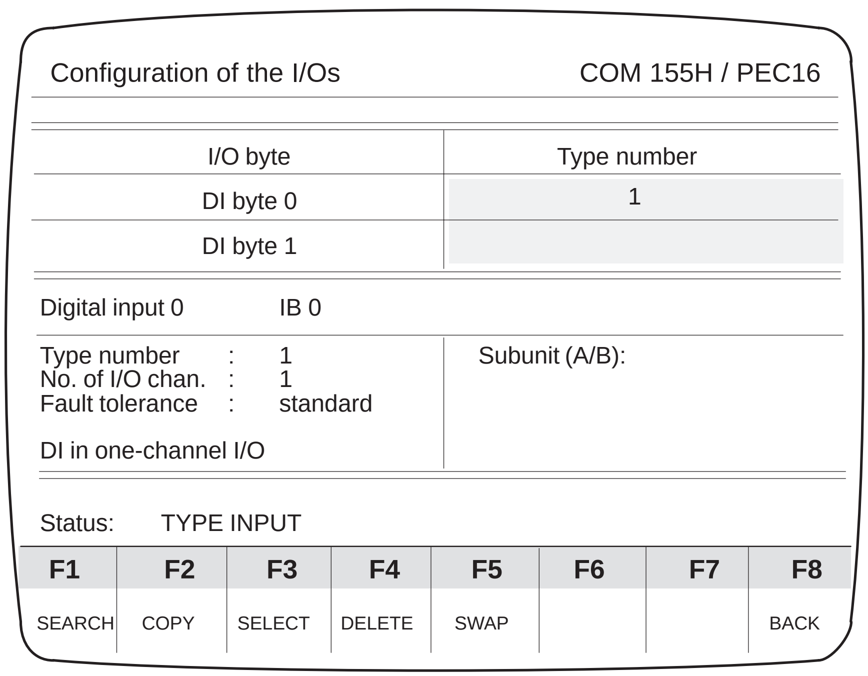


Figure 4-2 I/O Configuration Screen Form Type 1

All you have to do here is program the subunit in which the DI is operated.

Using <F3>, you can preselect the individual type numbers. These are shown on the screen in plaintext. This is valid for the entire configuration of the I/O.

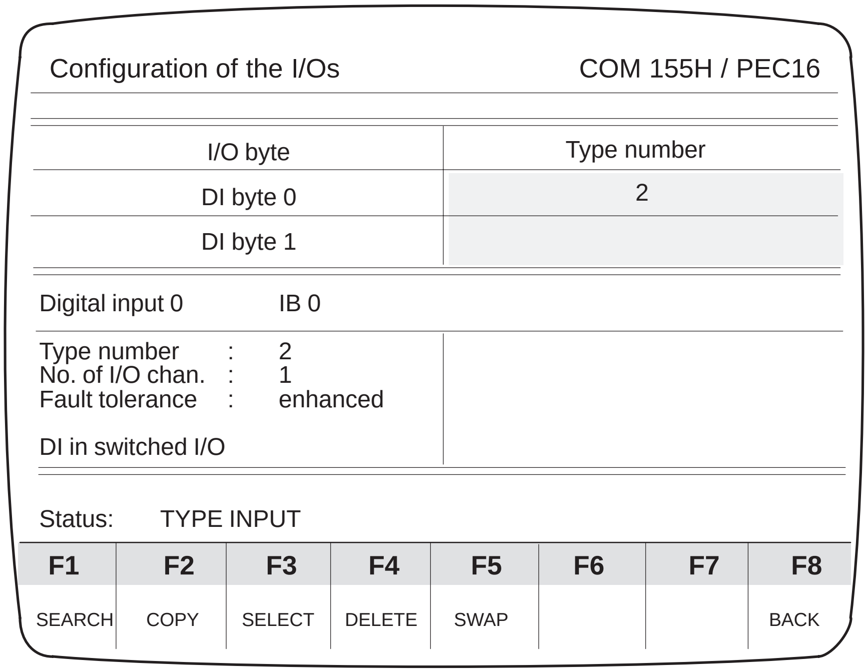


Figure 4-3 I/O Configuration Screen Form Type 2

No further initialization is necessary here.

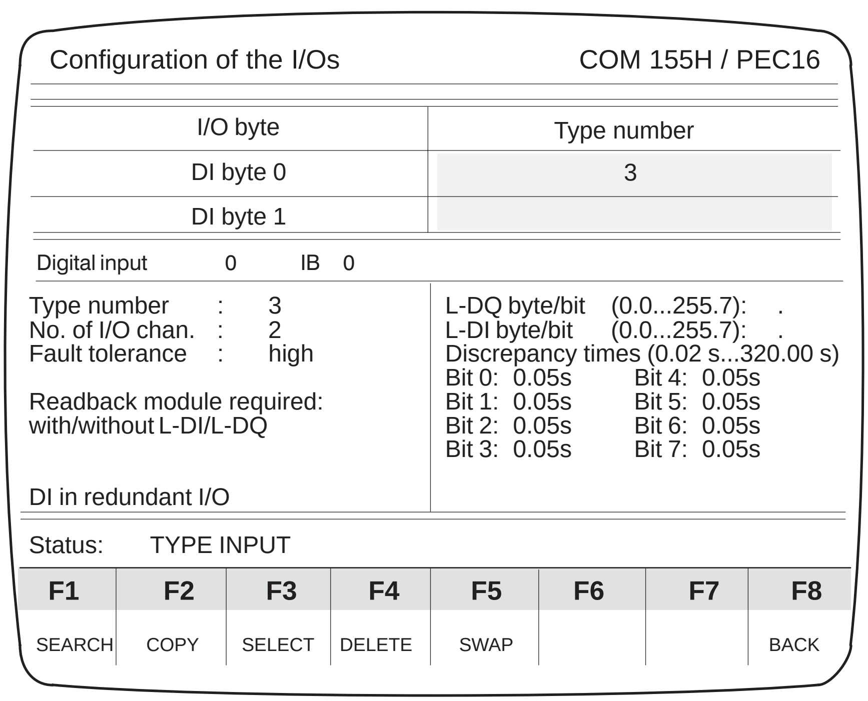


Figure 4-4 I/O Configuration Screen Form Type 3

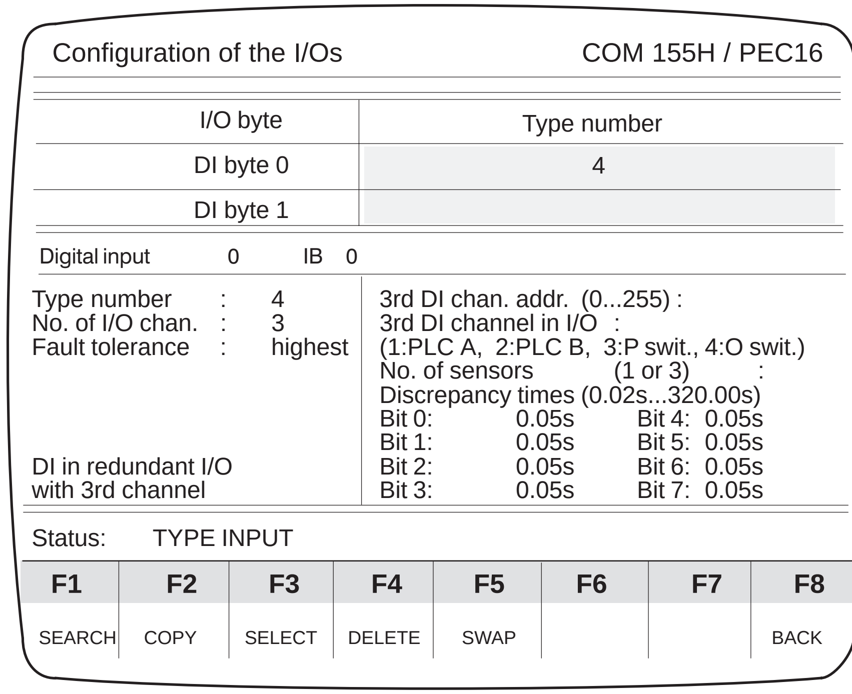


Figure 4-5 I/O Configuration Screen Form Type 4

Legend: DI

Locating DI, locating DQ:
You can use type 3 with or without error locating DI (L-DI) or L-DQ: If you use L-DI or L-DQ, the DI can be used as ”NON-STOP DI”.

Note:
Several redundant DIs can use the same locating facility (L-DI/L-DQ).

Discrepancy times
Since redundant digital inputs may have different signal states over a comparatively short period of time, you can use COM 155H to configure how long these different signal states can be tolerated.

If the configured discrepancy time is smaller than a PLC cycle time, the discrepancy time is set within the CPU to a PLC cycle time during cyclic processing (apart from with redundant process interrupts).

Various discrepancy times can be assigned to the individual bits of the DI. You can configure discrepancy times of between 10 ms and 320 ms in steps of 10 ms. The configured standard discrepancy time in the COM 155H ”Initialize Operating System” screen form is the default value.

Digital Outputs: F2 <**DQ**> (in the I/O basic screen form)

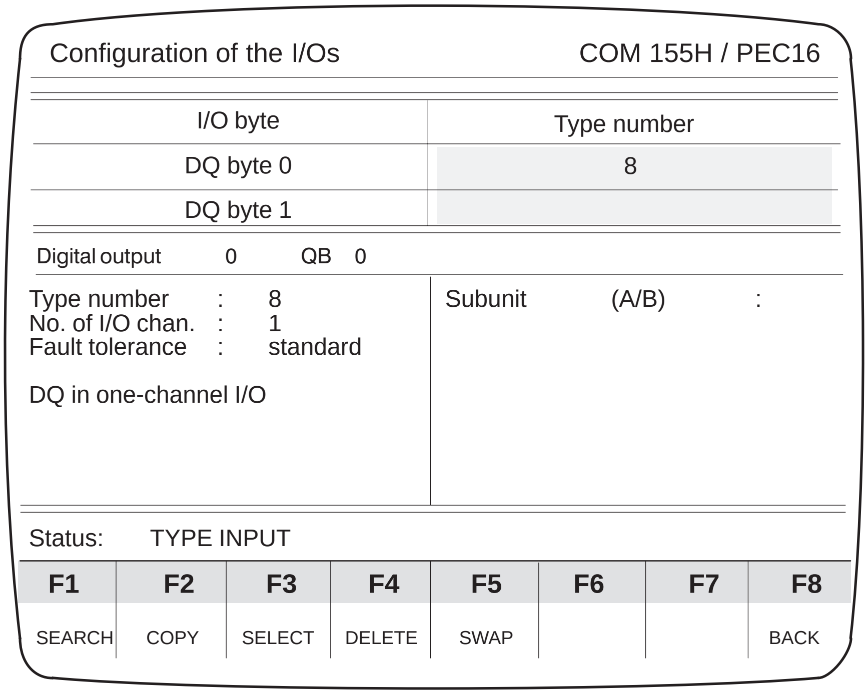


Figure 4-6 I/O Configuration Screen Form Type 8

Here you only have to program the subunit in which the DQ is operated.

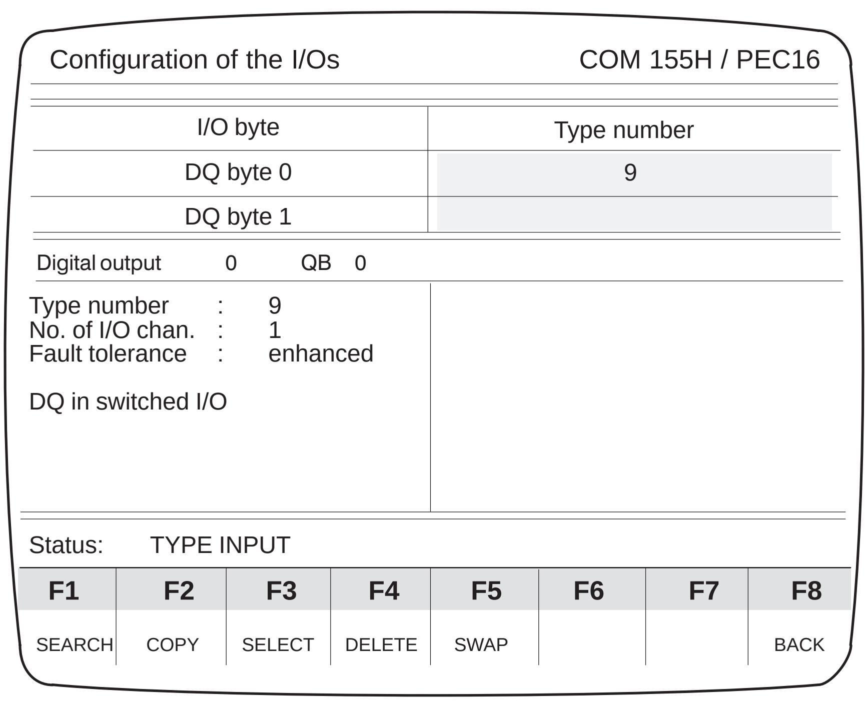


Figure 4-7 I/O Configuration Screen Form Type 9

No other parameters need be assigned here. However, remember to configure the I/O area of the relevant expansion unit using COM 155H.

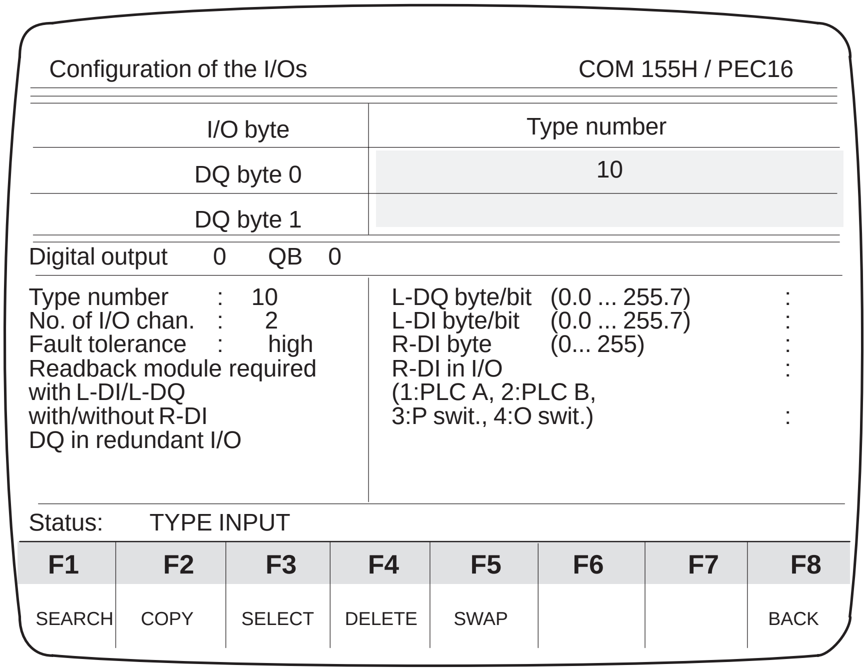


Figure 4-8 I/O Configuration Screen Form Type 10

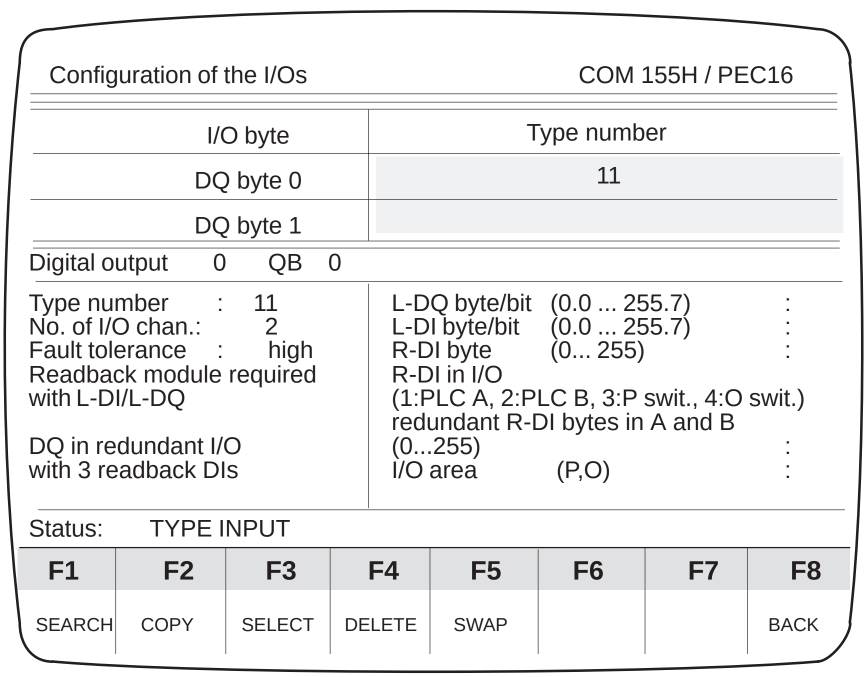


Figure 4-9 I/O Configuration Screen Form Type 11

Legend: DQ

Locating DI (L-DI), locating DQ (L-DQ):
see DI in I/O Configuration Screen Form Type 3

Readback DI (R-DI)
A readback DI must be specified for each redundant DQ, otherwise an error cannot be detected.

You must also specify a readback delay in the COM 155H ”Initialize Operating System” screen form for the readback DIs. This takes the different signal propagation delays of the various digital output modules into account.

Readback DI in the I/O
In this field, you specify the type of I/O in which the readback DI is to be operated.

1. The readback DI is one-sided: Subunit A.
2. The readback DI is one-sided: Subunit B.
3. The readback DI is switched: P area
4. The readback DI is switched: O area

Redundant readback DI
For the redundant DQ type 11, the redundant readback DI bytes must also be specified.

Analog Inputs: F3

<**AI**> (in the I/O basic screen form)

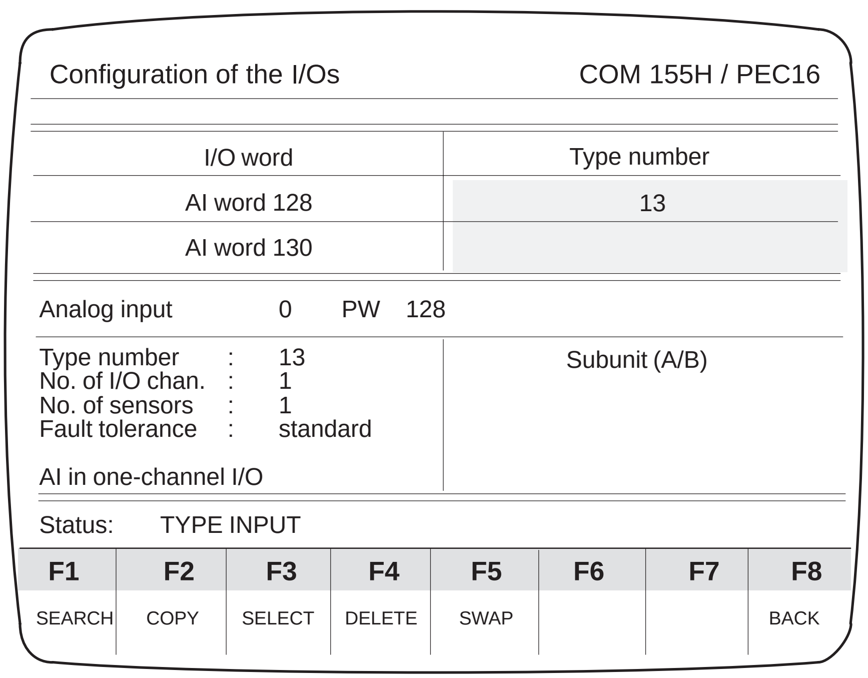


Figure 4-10 I/O Configuration Screen Form Type 13

Here you must program the subunit in which the AI is operated.

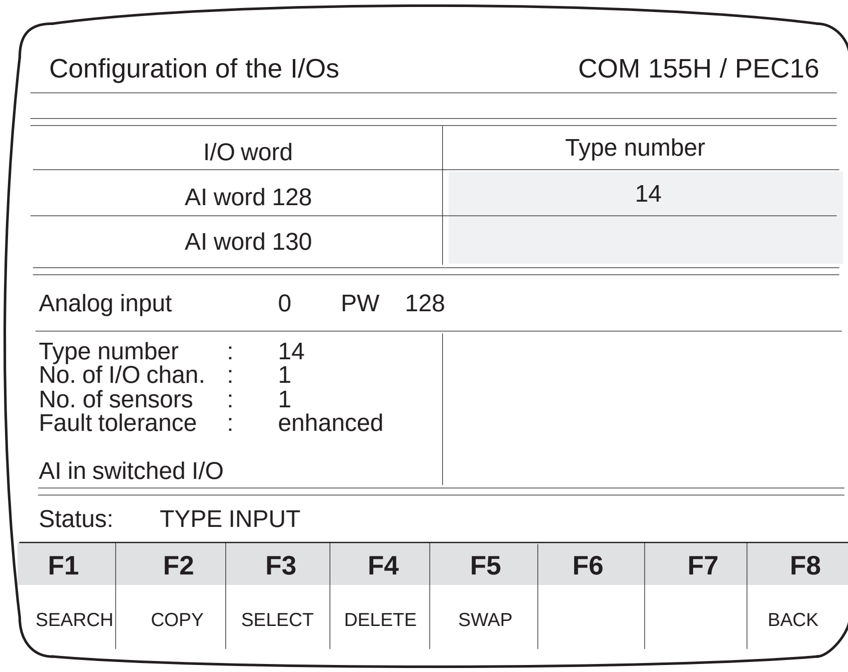


Figure 4-11 I/O Configuration Screen Form Type 14

No other parameters need be assigned.

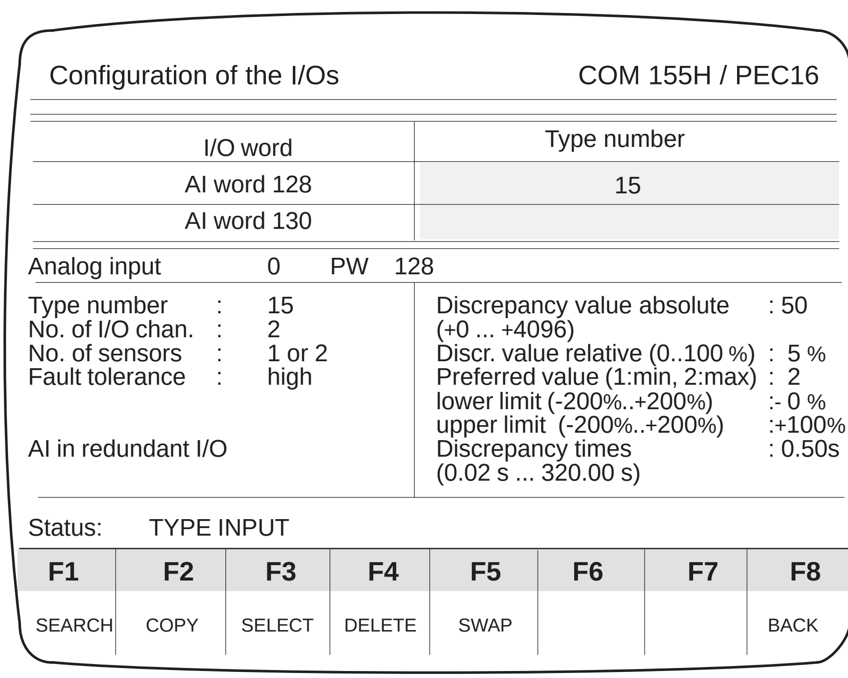


Figure 4-12 I/O Configuration Screen Form Type 15

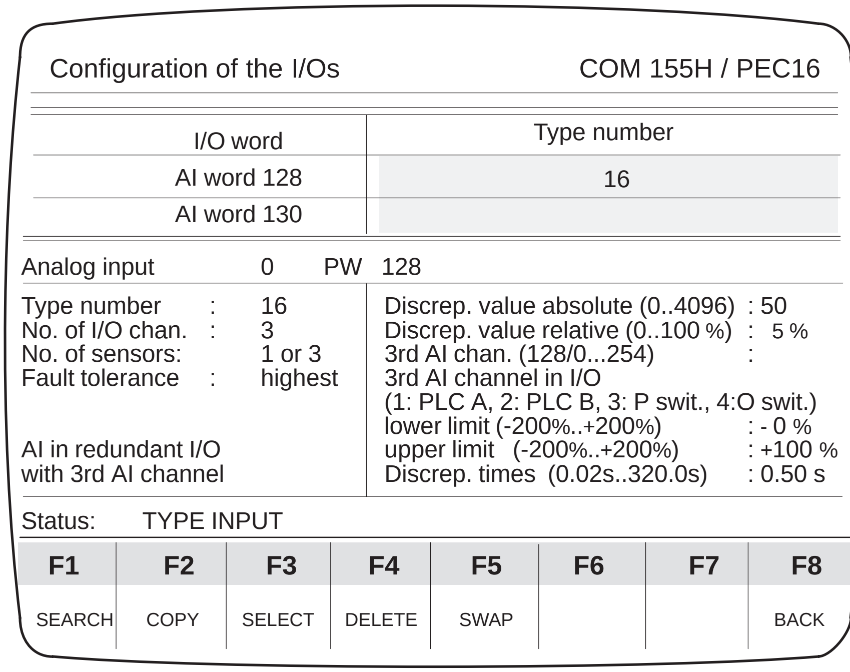


Figure 4-13 I/O Configuration Screen Form Type 16

Legend: AI (Types 15 and 16)

Absolute/relative discrepancy value:
Enter an absolute value ABS (decimal number) and a relative value REL (percentage).

The 155H operating system calculates the permissible analog value discrepancy DPERM according to the following formula:

$$D_{PERM} = ABS + \frac{REL * RAWV\ (max)}{100}$$

where for type 15 RAWV (max) is the greater of the two instantaneous analog values.

where for type 16 RAWV is the middle of the three instantaneous analog values.

Preferred value (type 15):
Specify here whether the 155H operating system is to give preference to the maximum or minimum value in the case of a discrepancy between the analog values.

Lower, upper limit (type 15/16):
The upper and lower limit values define a range for the analog value outside which the 155H operating system reports an error.

200% corresponds to 4096

100% corresponds to 2048

0% corresponds to 0

-100% corresponds to -2048

-200% corresponds to -4096

applies to voltage and current

Discrepancy time (type 15/16):
See Configuration screen form DI type 3

Analog Outputs: F4

<**AQ**> (in the I/O basic screen form)

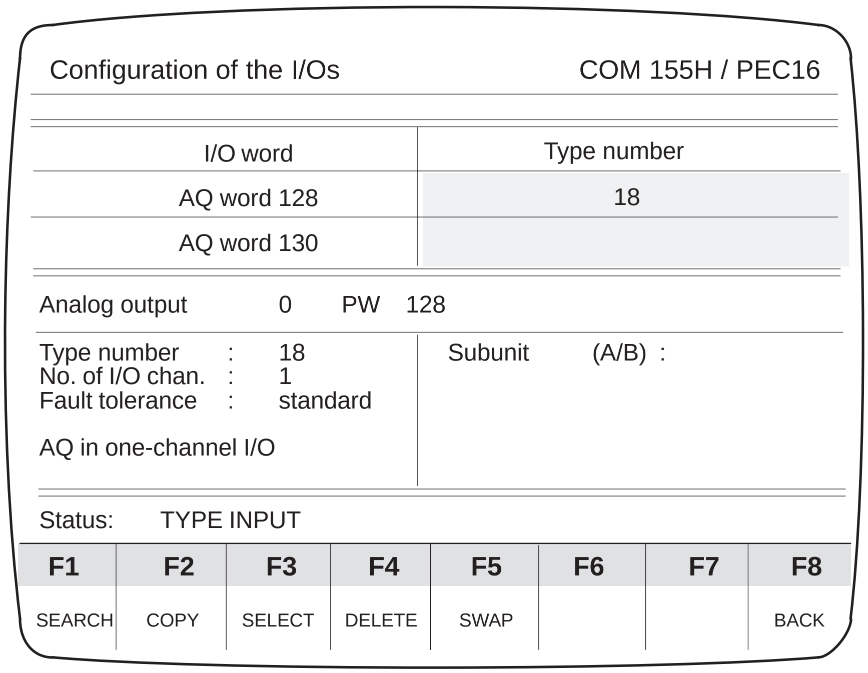


Figure 4-14 I/O Configuration Screen Form Type 18

Here you must specify the subunit in which the AQ is operated.

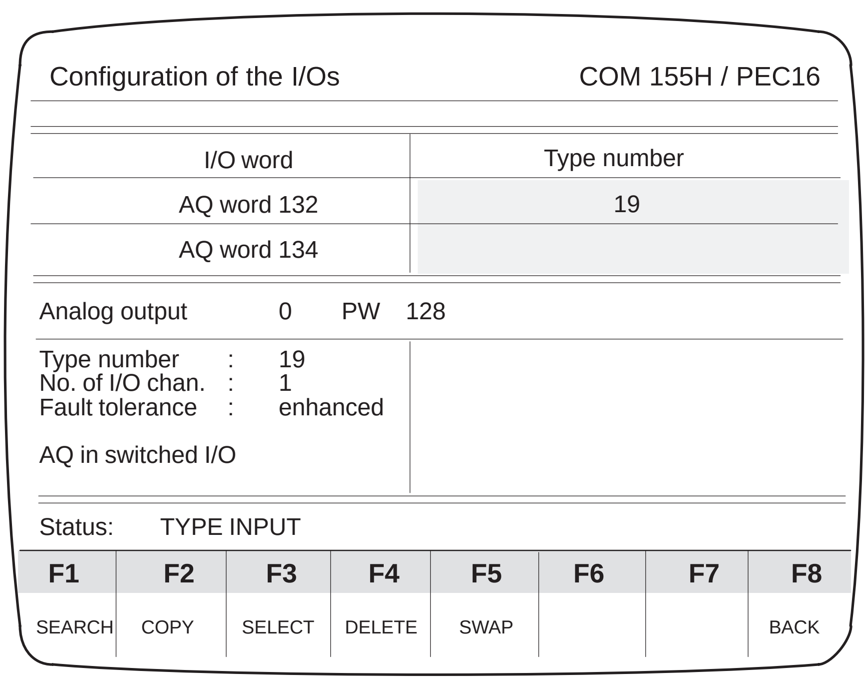


Figure 4-15 I/O Configuration Screen Form Type 19

No other parameter settings are required here.

Configuration of the I/Os COM 155H / PEC16

I/O word	Type number
AQ word 250	20
AQ word 252	

Analog output 0 PW 128

Type number : 20
No. of I/O chan. : 2
Fault tolerance : high

AQ in redundant I/O

Status: TYPE INPUT

F1	F2	F3	F4	F5	F6	F7	F8
SEARCH	COPY	SELECT	DELETE	SWAP			BACK

Figure 4-16 I/O Configuration Screen Form Type 20

The redundant analog output type 20 cannot locate errors.

Configuration of the I/Os COM 155H / PEC16

I/O word	Type number
AQ word 128	21
AQ word 130	

Analog output 0 PW 128

Type number : 21	L-DQ byte/bit (0.0...255.7) : 0.0
No. of I/O chan. : 2	L-DQ in area (P/O) : P
Fault tolerance : high	R-AI word (O:0..254; P:128..254) : 240
Error locating : yes	R-AI in I/O (F3: SELECT)
AQ in redundant I/O	Discrepancy value (abs.)(0..1023): 40
	Readback delay (0.02s..320.00s) : 0.05s
	Indic. update in disc time (1..10) : 2
	AQ output type (F3: SELECT) : 4-20 mA
	R-AI module (F3: SELECT):460-4UA..

Status: TYPE INPUT

F1	F2	F3	F4	F5	F6	F7	F8
SEARCH	COPY	SELECT	DELETE	SWAP			BACK

Figure 4-17 I/O Configuration Screen Form Type 21

The redundant analog output type 21 can locate errors and remedy them.

Channel 0 must always be configured before the other channels (1 - 7).

Legend: AQ Type 21

L-DQ byte/bit
Area: P or O (the L-DQ byte and bit lie in subunit A and B at the same address).

1. An L-DQ byte which is configured for a two-channel AQ may not also be used elsewhere (not even as the L-DQ for DI or DQ), because if a subunit fails, the byte on the intact side is written with 0FFh.
2. Assignment of channel number to L-DQ bit number is fixed:

   $$\frac{\text{Address AQ}}{\text{2 modulo 8}} = \text{L-DQ bit no.}$$

   Address AQ = base address + channel no. *2
   Example:
   Base address = 128 and channel no. = 5:
   → address AQ = 138, L-DQ bit no. = 5.
   Base address = 200 and channel no. = 3:
   → address AQ = 206, L-DQ bit no. = 7.

L-DQ Bit	Address of AQ Channel							
0	128	144	160	176	192	208	224	240
1	130	146	162	178	194	210	226	242
2	132	148	164	180	196	212	228	244
3	134	150	166	182	198	214	230	246
4	136	152	168	184	200	216	232	248
5	138	154	170	186	202	218	234	250
6	140	156	172	188	204	220	236	252
7	142	158	174	190	206	222	238	254

3. Free L-DQ bits may not be used elsewhere.

R-AI address
Area: P or O I/O area: one-sided in A or B or switched.

(Permissible) discrepancy value (absolute)
Suggestion for systems with minimal failure rate: 40

Readback delay
Default: 0.05 s
Readback delay time to be configured = R-AI encoding time or
R-AI cycle time + possibly ET 200 bus cycle time.

Indic. no. of updates (AQ) (FB calls and transfer direct access T PW/T OW) **per readback delay time (AQ)** (1...10)
Default: 10
The value for ”Indic. update in readback delay time” is:
N = readback delay time/AQ update interval.
Example 1 for ”Indic. update in readback delay time” = N

- AI 463: R-AI encoding time = 50 ms
- AQ updates every 10 ms (FB calls or T PW instructions on AQ)
  $\rightarrow$ N $\geq$ 50/10 = 5

Conditions

U Periphery:

The FB 41 : H-RLG : AA can be used for the following modules:

- AQ modules:

  6ES5 470-4UA..

  6ES5 470-4UB

  6ES5 470-4UC

- Readback AI modules:

  6ES5 466-3LA.. encoding time < 4 ms

  As this module has no interference suppression it can only be used as an R-AI if the high-frequency interferences arising on the user side are small enough.

  If the module is used as an R-AI for current outputs, only the 8 differential inputs may be used.

  6ES5 460-4UA.. encoding time < 480 (960) ms

  6ES5 463-4U... encoding time < 50 ms, only as R-AI for voltage output

  6ES5 465-4UA.. encoding time < 480 (960) ms,

- L-DQ modules:

  6ES5 458-4UA..

CP/IP: F5

<**CP/IP**> (in the I/O basic screen form)

Here you must specify the subunit to which communications processors/intelligent I/O modules have been assigned.

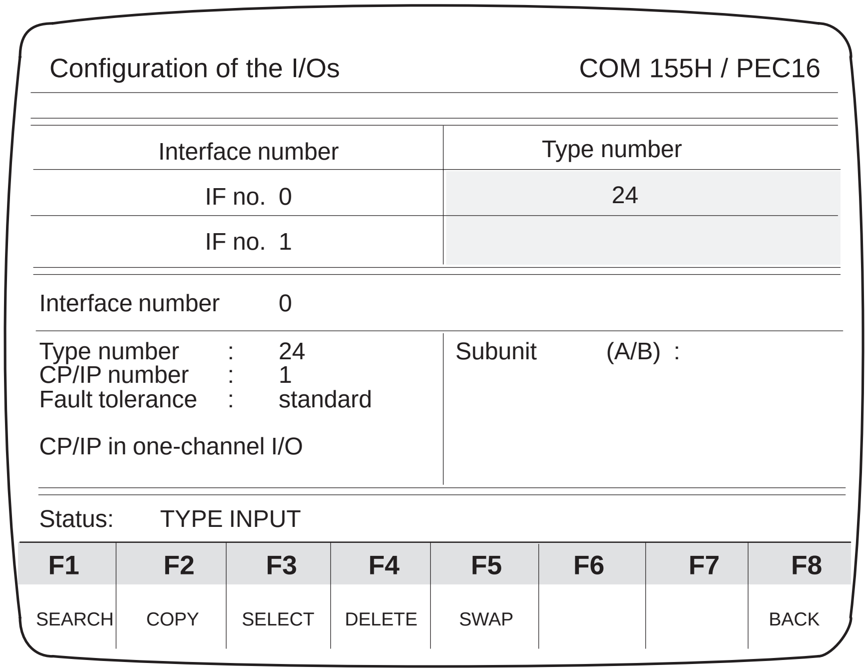


Figure 4-18 I/O Configuration Screen Form Type 24

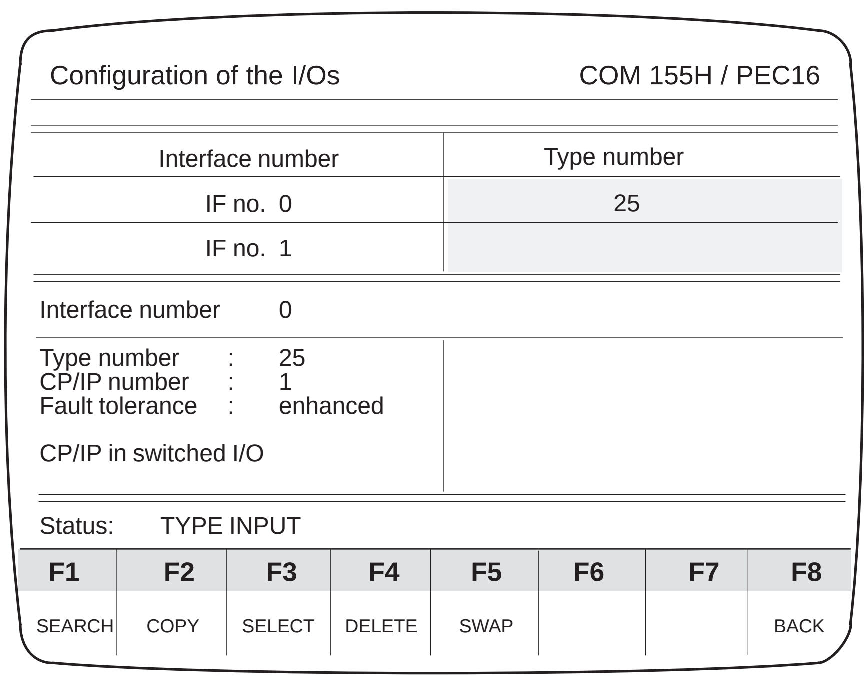


Figure 4-19 I/O Configuration Screen Form Type 25

No other parameter settings are required here.

Error Diagnostics and Documentation 5

The F2 and F4 function keys in the Diagnostics basic form support you when troubleshooting. You can obtain an overview of the errors that have occurred with F2 <STAT ERR>, as well as detailed information on each individual error with F4 <H ERROR>.

If you want to document your configuration, press <F7> in the Main Menu to reach the ”System Handling” menu and then press <F4> to reach the ”COM 155H Print Menu”.

5.1 Static Error Image of the I/Os

I/O Error Image Display

F2 <STAT ERR> in the Diagnostics menu takes you to the basic screen form for the I/O error image. All messages entered in the STATUS word (= DW 3 of the error DB) appear. If, for example, the ”CONFIGURATION ERROR” message appears, there is at least one and possibly several configuration errors (please refer to the S5-155H Instructions, Section 8.2 ”Structure of the Error DB”).

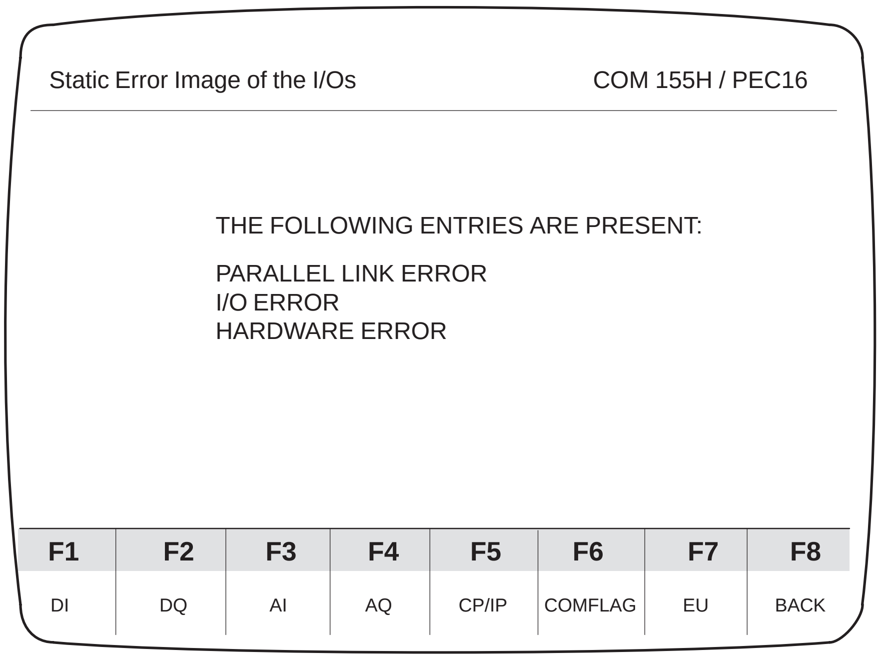


Figure 5-1 Basic Screen Form of the I/O Error Image

You can then have the static error image displayed as follows:

- Digital inputs <DI>
- Digital outputs <DQ>
- Analog inputs <AI>
- Analog outputs <AQ>
- CP and IP modules <CP/IP>
- Interprocessor communication input and output flags <COMFLAG>.

If you press F1 <DI>, for example, the following screen form will appear:

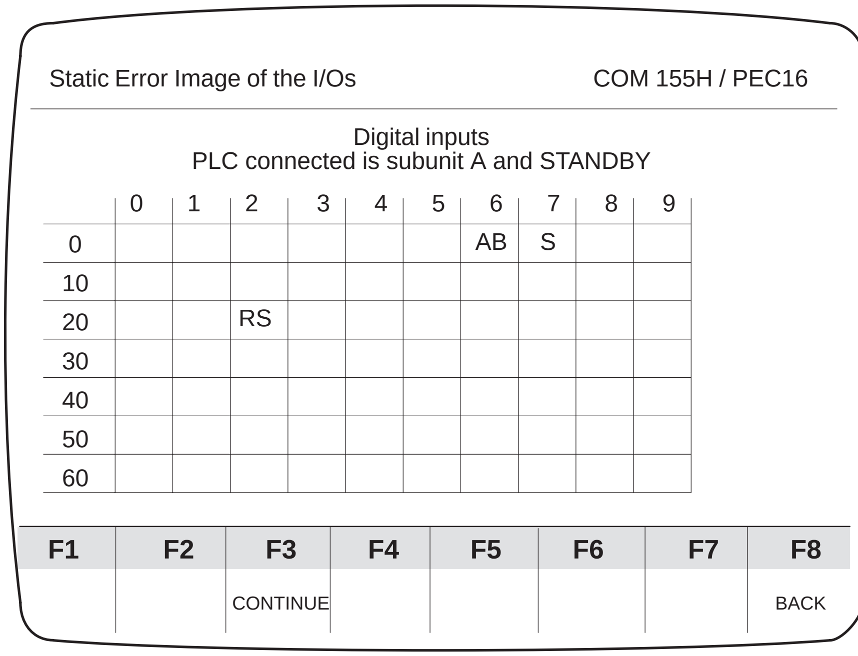


Figure 5-2 DI Error Image Basic Screen Form

F3 <CONTINUE> can be used, until DI 511 is reached. The following entries are possible:

- A Defect in subunit A
- B Defect in subunit B
- S Switched defective
- RA Configured redundant, defect in subunit A
- RB Configured redundant, defect in subunit B
- AB Configured redundant, A+B defective
- 3A 3-channel configured, defect in subunit A
- 3B 3-channel configured, defect in subunit B
- 3AB 3-channel configured, A+B defective
- R-A Readback DI/AI in subunit A defective
- R-B Readback DI/AI in subunit B defective
- RS Readback DI/AI in switched I/O defective
- 3-A 3rd channel in subunit A defective
- 3-B 3rd channel in subunit B defective
- 3-S 3rd channel in switched I/O defective
- L-A Locating DI in subunit A defective
- L-B Locating DI in subunit B defective
- L-AB Locating DI in subunit A and B defective

In the above example

- Input byte IB 6 in subunit A+B is defective
- Input byte IB 7 is switched defective
- Input byte IB 22 readback DI in switched I/O is defective

You can obtain the static error image of the expansion units by pressing F7 <EU> in the Basic Error Image form.

Static Error Image of the I/Os COM 155H / PEC16

ERROR: EU 0 05.04.94 01:46:52
P area I/O FF000H ... FF0FFH

ERROR: EU 1 05.04.94 01:46:52
P area I/O FF00H ... FF0FFH

ERROR: EU 4 05.04.94 01:46:52
O area I/O FF100H ... FF1FFH

F1	F2	F3	F4	F5	F6	F7	F8
		CONTINUE					BACK

Figure 5-3 EU Error Image Basic Form

The numbers of the defective expansion units and their associated address spaces have been entered. The time of day only appears if the error is still entered in the error block. You can return to the basic form by pressing F8 <BACK>.

5.2 Error Data Block

Calling the Error DB

After pressing F4 <H ERROR> in the Diagnostics Menu, you must specify whether you wish to read the error data block from the PLC (with F1: on-line diagnostics) or from diskette (with F2: off-line diagnostics):

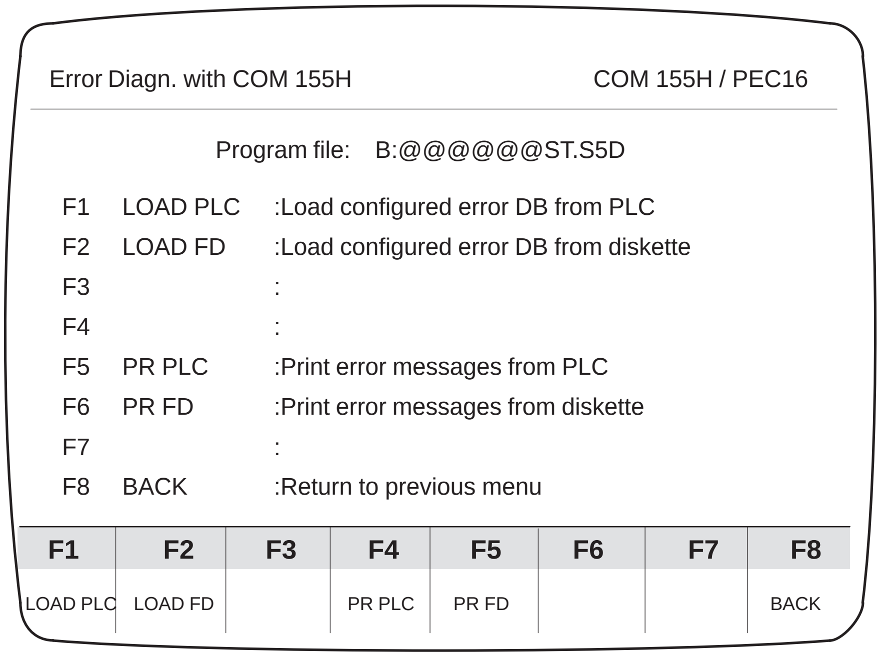


Figure 5-4 Error Diagnostics Screen Form

When you have selected the desired function, the contents of the error DB will appear on the screen. This applies to both subunits.

F1 <LOAD PLC>:
The error DB configured in DX1 is loaded.

If DX1 does not exist (after an overall reset, for example), the standard default error DB 3 is loaded. If there is no error DB 3, the programmer prompts you for a DB number. If this DB is also not in the programmable controller, the error DB is loaded from the absolute programmable controller address.

F2 <LOAD FD>:
The error DB configured in DX1 is loaded from the hard disk or from the diskette drive in the programmer.

F4 <PR PLC>:
All errors signalled in the programmable controller are printed in compressed form.

F5 <PR FD>:
All reported errors which are in the error DB of the file selected are printed in compressed form. The respective DX1 must also be available in the file.

Example of an Error Record Printout (Programmable Controller)

Error Diagnostics with COM 155H
COM 155H/PEC16

SUBUNIT B

ERROR RECORD NO. :2
CURRENT ERROR RECORD NO.: 3

Error class	: Message
Error : 95	: DI MODULE NOT CONFIGURED
Time stamp	: 25.04.94 17:16:28
DI ADDRESS	: F00B DI BYTE NO. :11

SUBUNIT B

ERROR RECORD NO. : 3
CURRENT ERROR RECORD NO.: 3

Error class	: Passivation
Error:51	: TIMEOUT ON OUTPUT MODULES
Time stamp	: 25.04.94 17:16:32
DI ADDRESS	: F007 INSTR. CODE: 0000

Structure of the Error Diagnostics Screen Form

If several errors occur, the error last entered is displayed first. Each screen form corresponds to an error record in the error DB.

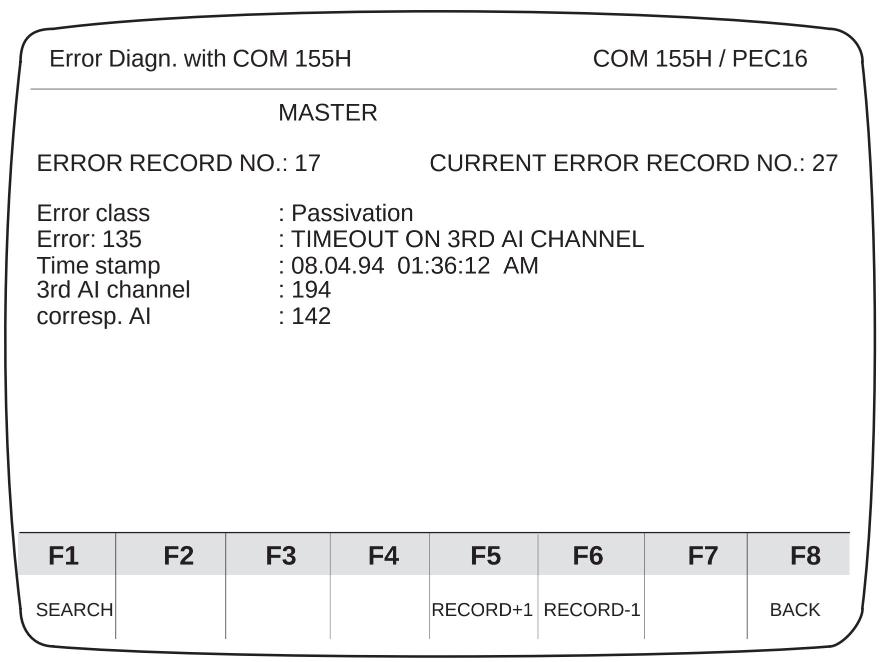


Figure 5-5 Error Diagnostics Screen Form (Example)

F1 <SEARCH>:

- If you wish to read out a particular error record quickly, press this key and enter the number of the desired record.

- If you want to find a particular error record quickly, press the <Cursor down> key and type in the error number.

F5 <RECORD+1> (or Cursor down ↓):
F6 <RECORD-1> (or Cursor up ↑):

These functions enable you to page through the error DB (forward and backward) record by record; all errors of both subunits stored up until that particular instant can be read out.

When the last error entered is read out, the message

”NO MORE ENTRIES”

appears.

Legend: Error DB

Each screen form tells you whether the error occurred in the MASTER or in the STANDBY.

ERROR RECORD NO. x:
Number of the error record you are presently reading out.

CURRENT ERROR RECORD NO. x:
The last stored error is located in error record number x.

Error class:
This indicates the standard error response (for example, hard STOP on a CPU fault, passivation in the case of a timeout, etc.).

Error:
The error number entered in the error DB is displayed in plaintext here (for example, I/O bus fault, timeout on output module, etc.).

Time stamp
Provided the CPU clock is set, the current date and time of day (from the system data area in the master CPU) appears here when a fault or error occurs.

All other specifications are supplementary information dependent on the errors or faults that have occurred (for example, instruction code, step address counter, EU number, etc.).

Please also refer to the structure of the error data block in Section 8.2 of the S5-155H Instructions.

5.3 Documenting with COM 155H

Printing the Configuration Overview

Press <F7> in the Main Menu to get into the "System Handling" menu. The <F1> key takes you into the Directory menu. From this menu, you can print out an overview of your configuration in the form of a list. With <F4> you get the configuration from the programmable controller, with <F5> from the diskette.

Example:

I/O group	! I/O type	! Subunit	! Number
Digital inputs	! one-sided I/O	! A	! 2
Digital inputs	! one-sided I/O	! B	! 2
Digital inputs	! switched I/O	!	! 36
Digital inputs	! redundant I/O	!	! 6
Digital inputs	! 3-channel I/O	!	! 3
Digital outputs	! one-sided I/O	! A	! 4
Digital outputs	! one-sided I/O	! B	! 0
Digital outputs	! switched I/O	!	! 40
Digital outputs	! redundant I/O	!	! 13
Analog inputs	! one-sided I/O	! A	! 2
Analog inputs	! one-sided I/O	! B	! 0
Analog inputs	! switched I/O	!	! 14
Analog inputs	! redundant I/O	!	! 8
Analog inputs	! 3-channel I/O	!	! 6
Analog outputs	! one-sided I/O	! A	! 0
Analog outputs	! one-sided I/O	! B	! 8
Analog outputs	! switched I/O	!	! 8
Analog outputs	! redundant I/O	!	! 8
CP/IP interfaces	! one-sided I/O	! A	! 1
CP/IP interfaces	! one-sided I/O	! B	! 1
CP/IP interfaces	! switched I/O	!	! 9

Printing the Configuration DB/DX

Press <F4> in the ”System Handling” menu to get into the COM 155H Print Menu. You can have your configuration printed out in tabular form from this menu.

If the data is to be printed out from the programmable controller, diskette or EPROM flash memory card, it must first be loaded into the programmer’s memory. This is done from the System Handling menu, F3 <TRAN LOAD>.

A footer is printed out on each page.

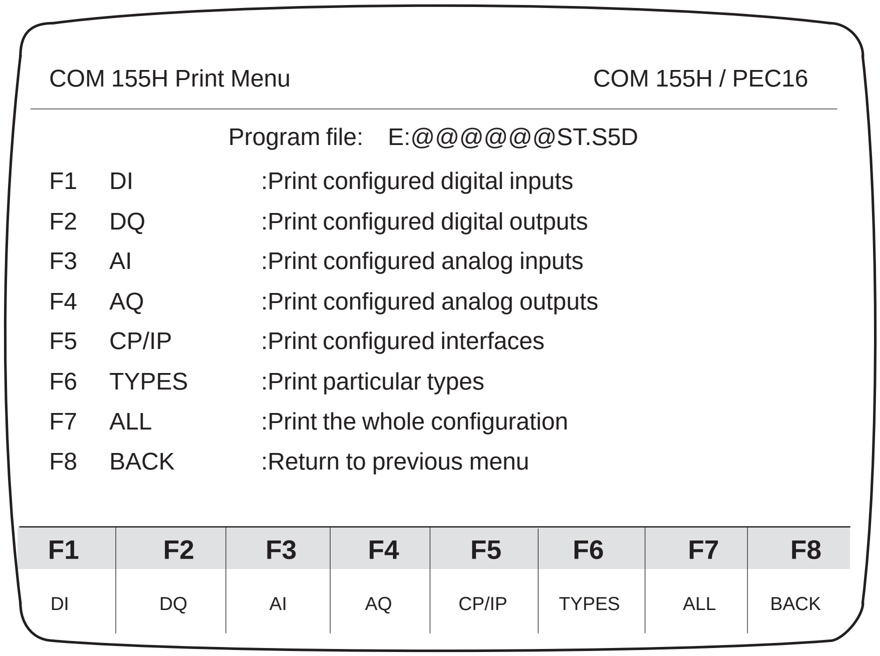


Figure 5-6 Print Menu

Functions in the Print Menu

You can execute the following functions using <F1> to <F7>:

F1 <DI>: Print out all DI types (digital inputs)

F2 <DQ>: Print out all DQ types (digital outputs)

F3 <AI>: Print out all AI types (analog inputs)

F4 <AQ>: Print out all AQ types (analog outputs)

Example: Table of DI Types (F1)

I/O byte	! Short symbol	! Type !	! Subunit !	I/O byte	! Short symbol	! Type !	! Subunit !
IB 0	!	! 2	!	IB 1	!	! 2	!
IB 126	!	! L-DI	!	IB 127	!	! L-DI	!

F5 <CP/IP>: Print all CP and IP types (interface no.)

Example: Table of CP/IP Types (F5)

Interface number	! Type	! Subunit	Interface number	! Type	! Subunit
0	! 24	! A	10	! 24	! B

F6: <SELECT> Printout of individual types, printout of the configured L-DIs, L-DQs and R-DIs (bit assignment) or printout of your operating system parameter settings.

COM 155H Print Menu COM 155H / PEC16

Program file: B:@@@@@@ST.S5D

	DI	DQ	AI	AQ	CP/IP
Types one-sided subunit A	x				
Types one-sided subunit B					
Types switched					
Types redundant					xxxx
Types 3-channel		xxxx		xxxx	xxxx
L-DI, L-DQ, R-DI					
OS configuration					

Figure 5-7 Print Menu (TYPES, F6)

- Position the cursor to the desired field and press <RETURN> or <ESC>. What you have selected will be output to the printer.

Example: Types; redundant DI

DI type 3: Two-channel digital inputs ”redundant I/O”

DI byte	! Short symbol	! Discrep. time (sec)	! L-DQ byte/bit	! L-DI byte/bit
I 5.0	!	! 0.05	! 130.5	! 6.2
I 5.1	!	! 0.05	! 130.5	! 6.2
I 5.2	!	! 0.05	! 130.5	! 6.2

Example: L-DI, L-DQ, R-DI

Bit assignment digital outputs:

Bits ->	! 0	! 1	! 2	! 3	! 3	! 5	! 6	! 7
DQ byte 130	!	!	!	!	!	!DI-LDQ	!	!

Bit 5 of digital output byte 130 has been configured as a locating digital output for a redundant digital input. The other bits are still unassigned.

If you mark the OS configuration field in the Print Menu with a cross ("check" it), you get a printout of the following:

1. The operating system parameters
2. The transfer data for standby activation and
3. The I/O areas of the expansion units.

F7 <ALL>: The entire configuration is printed out.

This function enables you to print out out all the data of your configuration:

1. The operating system parameters (see above) and
2. The entire I/O configuration.

SIEMENS

SIMATIC S5

CC 155H

Instructions
(CC 155H, Part IV)

C79000-B8576-C139-06

Safety Guidelines

This manual contains notices which you should observe to ensure your own personal safety, as well as to protect the product and connected equipment. These notices are highlighted in the manual by a warning triangle and are marked as follows according to the level of danger:

Danger

indicates that death, severe personal injury or substantial property damage **lm**result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage **dao** result if proper precautions are not taken.

Caution

indicates that minor personal injury or property damage can result if proper precautions are not taken.

Note

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

Only **r anlilf e pf ssooof n**should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground, and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

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Geschaeftsgebiet Industrie Automatisierungssysteme
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Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

Preface

Purpose of the Manual

This manual describes the hardware of the 155H central controller and the differences between the CC 155H and the S5-155H programmable controller.

The CC 155H differs from the S5-155H programmable controller mainly by the fact that smaller redundant systems with only one rack and therefore very compact can be constructed.

This manual describes all the steps necessary to install and operate the CC 155H. It supports you in learning the functions of the CC 155H quickly and effectively.

Audience

The manual is intended for the following audience:

- Installers
- Startup specialists
- Service and maintenance personnel

Validity of this Manual

This manual contains the description of the 155H central controller which was valid at the time the manual went to print. We reserve the right to describe any changes to the functionality of the CC 155H in a Product Information.

Approvals

The following approvals exist for the CC 155H:

UL Recognition Mark
Underwriters Laboratories (UL) in accordance with
Standard UL 508

CSA Certification Mark
Canadian Standard Association (CSA) in accordance with
Standard C 22.2 No. 142

The approvals apply if the appropriate labels are visible on all components.

CE Mark

Our products meet the requirements of EC Directive 89/336/EEC 'Electromagnetic Compatibility'.

In accordance with the Article 10 of the above-mentioned EC Directive, the EU declarations of conformity are held at the disposal of the competent authorities at the address below:

Siemens AG
Automation Group
AUT E 148
Postfach 1963
D-92209 Amberg

Other Relevant Documentation

This manual describes the hardware of the 155H central controller. You will require the following additional manuals for programming and commissioning a CC 155H:

Manual	Content	Order Number
SIMATIC S5 S5-135U/155U System Manual	• Centralized and distributed configuration of a programmable controller • Installation guidelines • Central controllers and expansion units • CPUs, memory cards, memory submodules, interface submodules • Interface modules • Digital input/output modules • Analog input/output modules • Monitoring modules • Connector assignments	6ES5 998-0SH21
SIMATIC S5 S5-155H Programmable Controller Programming Guide	• Components of STEP 5 user programs • Basics of STEP 5 programming with examples • Operating statuses and program execution levels of the CPU 948R • Interrupt and error diagnosis • Special functions of the system program • Memory assignment and memory organization of the CPU 948R • PG interfaces and PG functions	6ES5 998-4SR21

Structure of this Manual

To facilitate rapid access to special information, the manual contains the following aids:

- Given at the beginning of the manual is a full table of contents.
- In the chapters, each page contains information in the left column which summarizes the contents of the section.

Additional Assistance

If you have any questions regarding the products described in this manual and cannot find an answer, please contact the Siemens representative in your area. You will find a list of addresses in catalogs, and in Compuserve (`go autforum`).

If you have any questions or comments on this manual, please fill out the remarks form at the end of the manual and return it to the address shown on the form. We would be grateful if you could also take the time to answer the questions giving your personal opinion of the manual.

Siemens also offers a number of training courses to introduce you to the SIMATIC S5 automation system. Please contact your regional training center or the central training center in Nuremberg, Germany for details:

Tel. (+49) (911) 895 3154.

The Latest Information

You will find the latest updated information on SIMATIC products:

- On the Internet under http://www.aut.siemens.de/
- Via fax polling no. 08765-93 02 77 95 00

SIMATIC Customer Support offers help by means of up-to-date information and downloads which may be useful to you when using SIMATIC products:

- On the Internet under http://www.aut.siemens.de/simatic-cs
- Via the SIMATIC Customer Support Mailbox under the number +49 (911) 895-7100

  Use a V.34 (28.8 Kbps) modem to access the mailbox and set its parameters as follows: 8, N, 1, ANSI, or dial in using ISDN (x.75, 64 Kbits).

You can reach SIMATIC Customer Support by phone using the number +49 (911) 895-7000 and by fax using the number +49 (911) 895-7002. You can also send your queries by E-Mail on the Internet or by mail to the above mailbox.

Contents - Part IV

155H Central Controller 1

Chapter Overview

Order Numbers

Name	Order Number
CC 155H	6ES5 188-3UH31

1.1 Overview of the CC 155H

Introduction

This manual shows the special features of the CC 155H and is intended for users who are familiar with the S5-155U and S5-155H programmable controllers.

The CC 155H is a fault-tolerant programmable controller for machine and plant control. It is similar in function to the S5-155H programmable controller.

The CC 155H is an event-synchronized master-standby system like the S5-155H with a 1-out-of-1 structure. In contrast to the S5-155H, both subunits (master and standby) in the CC 155H can be mounted in one single subrack. This allows you to structure a redundant programmable control system with a minimum of space.

Warning

The CC 155H programmable controller (H system) is, despite its high fault-tolerance and its isolated structure, not a fail-safe system.

It must never be used in plants or installations in which a programmable controller fault (e.g. an improbable total failure of both subunits) could cause dangerous operating statuses and therefore result in danger to persons, machines or the environment.

Safety-related automation tasks of this nature require either the use of a safety-oriented programmable controller (e.g. an S5-115F system which was prototype-tested by the TÜV (German Technical Inspectorate)) or the CC 155H must be equipped with suitable interlocks or protective systems which prohibit the occurrence of dangerous operating statuses.

Components of the CC 155H

The CC 155H (see Figure 1-1) comprises the following components:

- Subrack
- Power supply units
- Fan subassembly

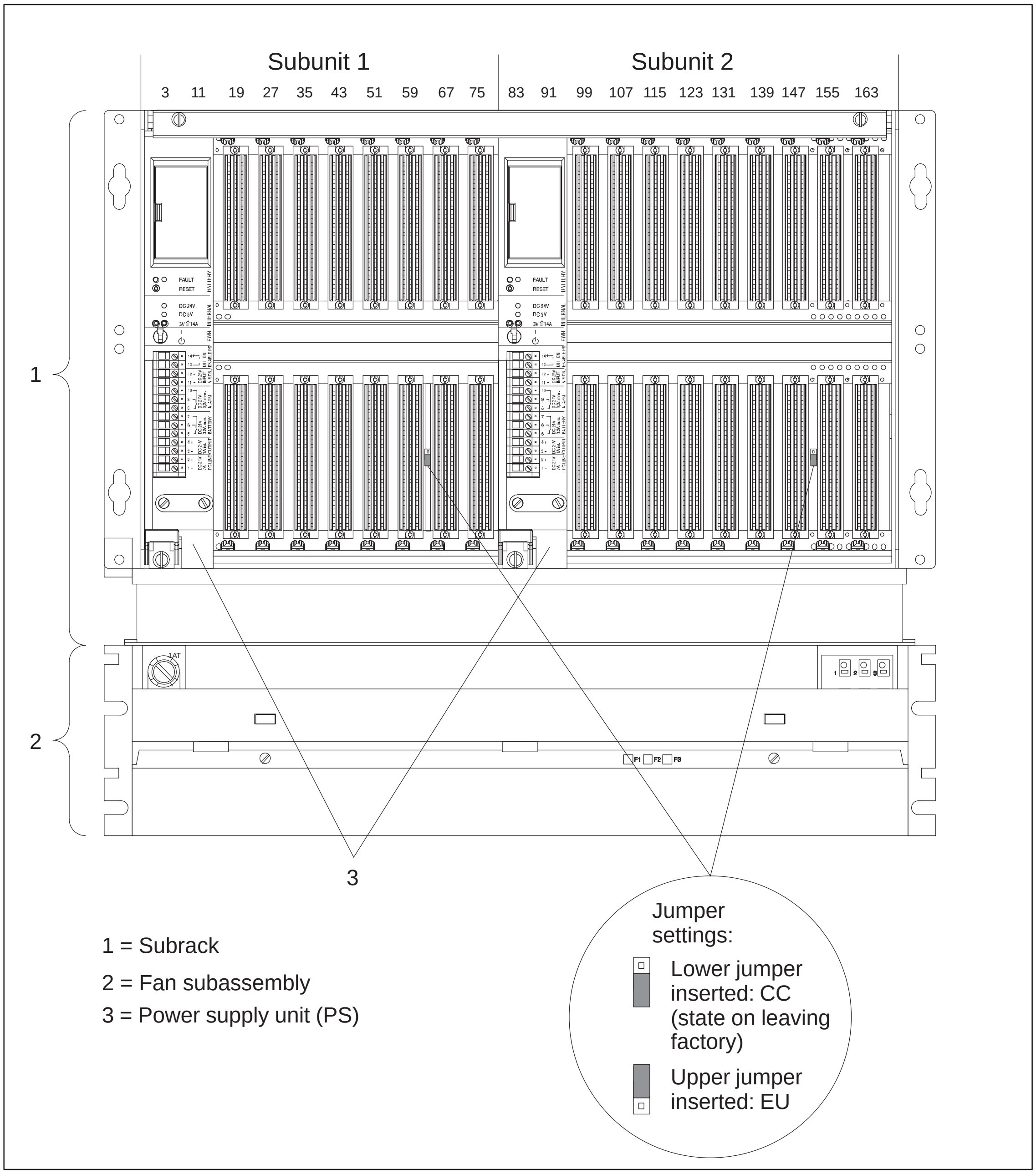

Figure 1-1 CC 155H, Front View

You can insert the following modules in the free slots in each subunit:

- CPU 948R
- Interface modules (IMs)
- Communications processors (CPs)
- I/O modules (DI, DO, AI, AO)

Subrack

The CC 155H contains two independent subunits in one subrack and combines the functions of two independent central controllers in one subrack. Each subunit requires its own power supply unit.

You will find more details about the rack in Chapter 2.

Power Supply Unit

The power supply unit supplies the other modules in each subunit with their operating voltages via the backplane bus of the subrack.

You will find more details about the power supply module in Chapter 3.

Fan Subassembly

The fan subassembly is used to ventilate the CC 155H. It is an obligatory part of the system and must always be installed immediately below the subrack of the CC 155H.

You will find more details about the fan subassembly in Chapter 4.

Jumper Settings

The following operating modes can be set for each subunit of the CC 155H independently:

- Central controller mode (CC)
- Expansion unit mode (EU)

The modes are set using jumpers. These jumpers are accessible from the front in the subrack (see Figure 1-1).

The state on shipping from the factory is central controller mode (lower jumpers inserted).

1.2 Device Configurations with the CC 155H

Overview

This section shows how you can configure various different programmable controller structures with the CC 155H.

Connecting Expansion Units

You can connect expansion units to the central controller CC 155H. You use the interface modules IM 304 and IM 314R to link them up.

CC 155H with EU 185U

Figure 1-2 shows an example of how you can expand the CC 155H with an EU 185U.

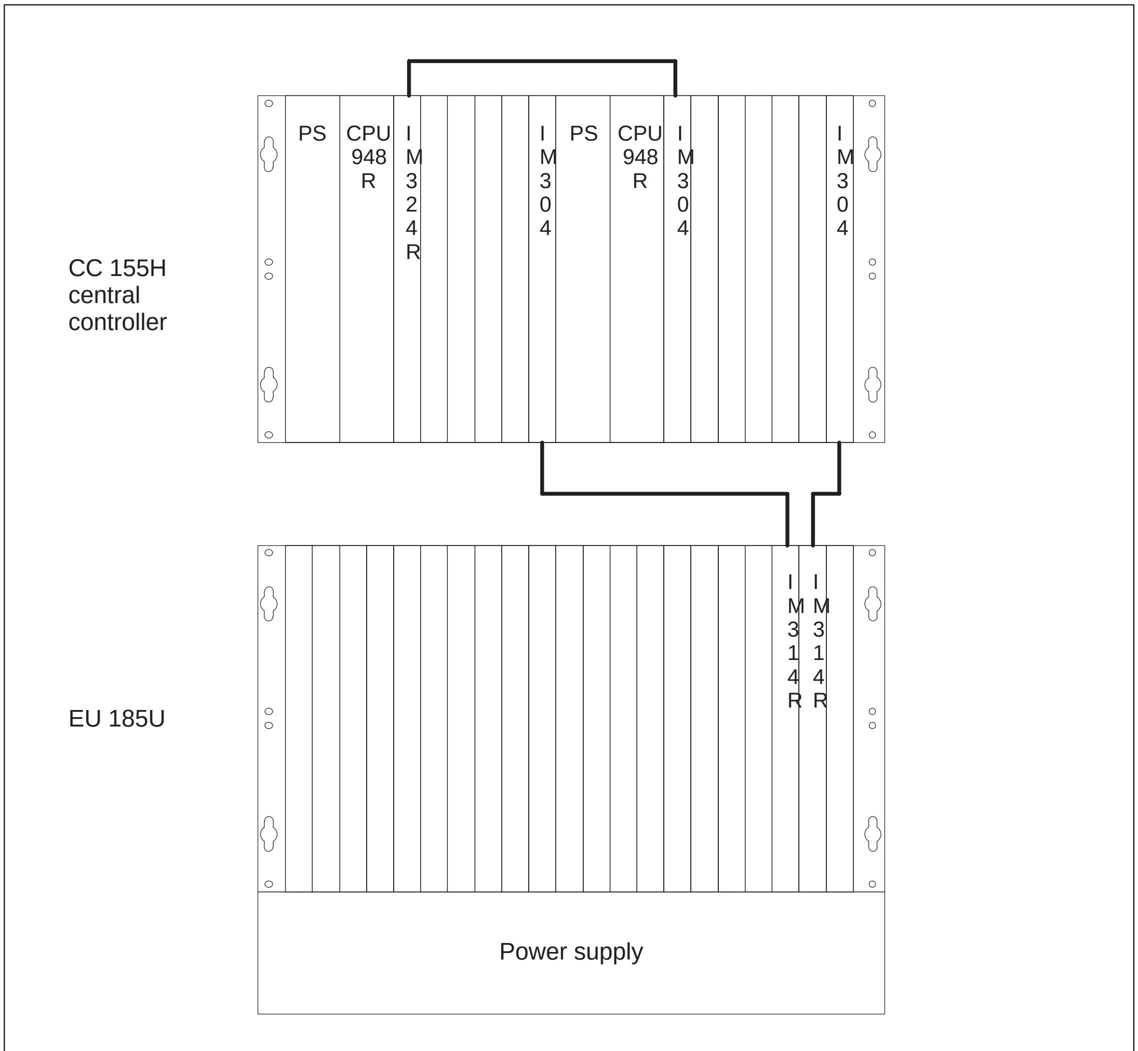

Figure 1-2 CC 155H with EU 185U

CC 155H as a "Shared" Expansion Unit

You can also use the CC 155H as a "shared expansion unit". This means you can connect up to six or seven I/O modules in the "switched I/O" mode to a CC 155H (see Figure 1-3).

This has the advantage that two central controllers with a switched I/O can be completely contained in one cabinet.

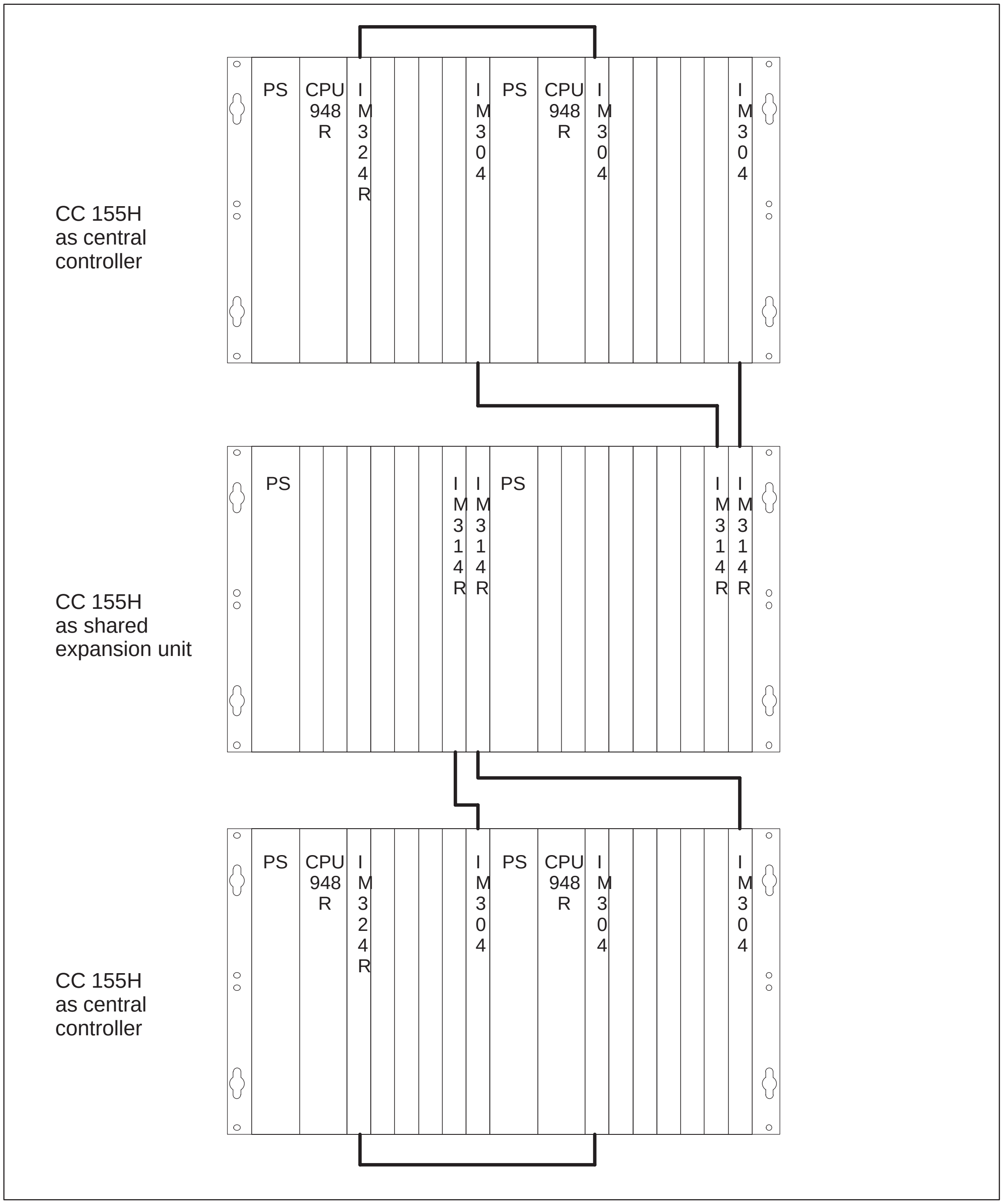

Figure 1-3 CC 155H as a "Shared" Expansion Unit

1.3 Installing the CC 155H

Mounting a CC 155H

The CC 155H is suitable for the following types of installation:

- Cabinet installation
- Mounting on racks

Figures 1-4, 1-5 and 1-6 show the most important dimensions for the installation of the CC 155H and its installation position in a 19-inch cabinet.

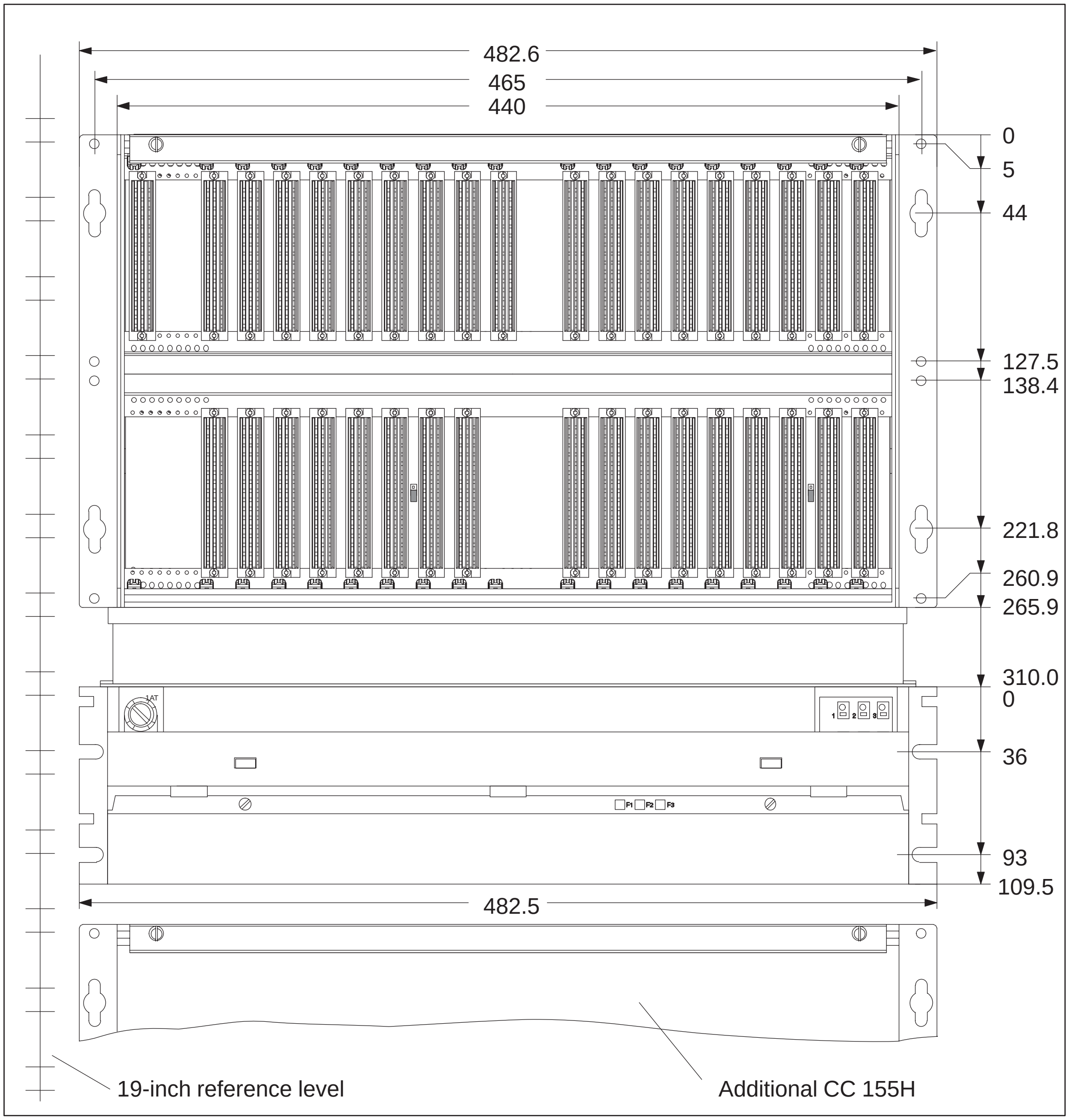

Figure 1-4 Mounting Dimensions of a CC 155H

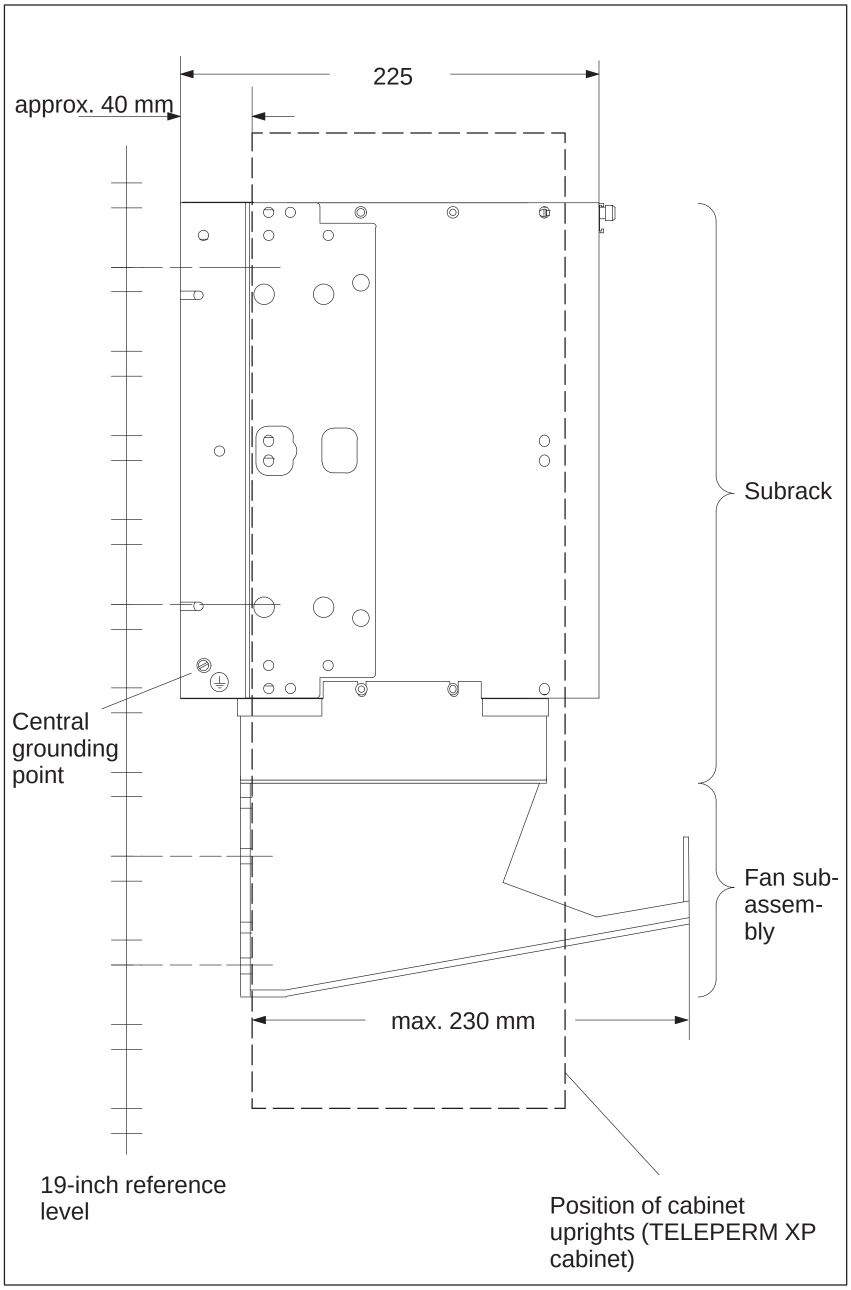

Figure 1-5 Installation Position of the CC 155H (Side View)

The CC 155H is suitable for “one-man installation”.

For connection and maintenance purposes, the CC 155H only needs to be accessible from the front.

Use M6 screws to fix the CC 155H.

Use self-tapping M6 screws to fix the CC 155H in a TELEPERM XP cabinet.

Proceed as follows to install the CC 155H:

1. First fix the fan subassembly. It is screwed directly to the cabinet or rack uprights by its fixing surfaces from behind.

   You can only mount the fan subassembly in certain intervals within the 19-inch reference level owing to the arrangement of the cutouts. If you fix the rack first, the fan subassembly may not be able to be arranged immediately below it.

2. Fix the CC 155H subrack immediately above the fan subassembly. It should be screwed from behind directly to the cabinet or rack uprights using its mounting brackets.

   To make installation easier, you can rest the subrack on the fan subassembly which is already fixed.

3. Connect the central grounding point of the CC 155H to chassis ground. An M5 screw is provided for this purpose at the bottom rear left of the subrack (see Figure 1-5).

   The minimum cross section of the chassis ground cable should be: 16 mm^2.

Note

Ensure that there is always a low-impedance connection to chassis ground. You achieve this by using a short a cable as possible, with low resistance and a large-area good quality contact.

Note

If you do not mount the subrack immediately above the fan subassembly as shown in Figures 1-4 and 1-5, there is no guarantee that the CC 155H will be adequately ventilated.

Figure 1-6 shows an example of the mounting position of the CC 155H in a TELEPERM XP cabinet.

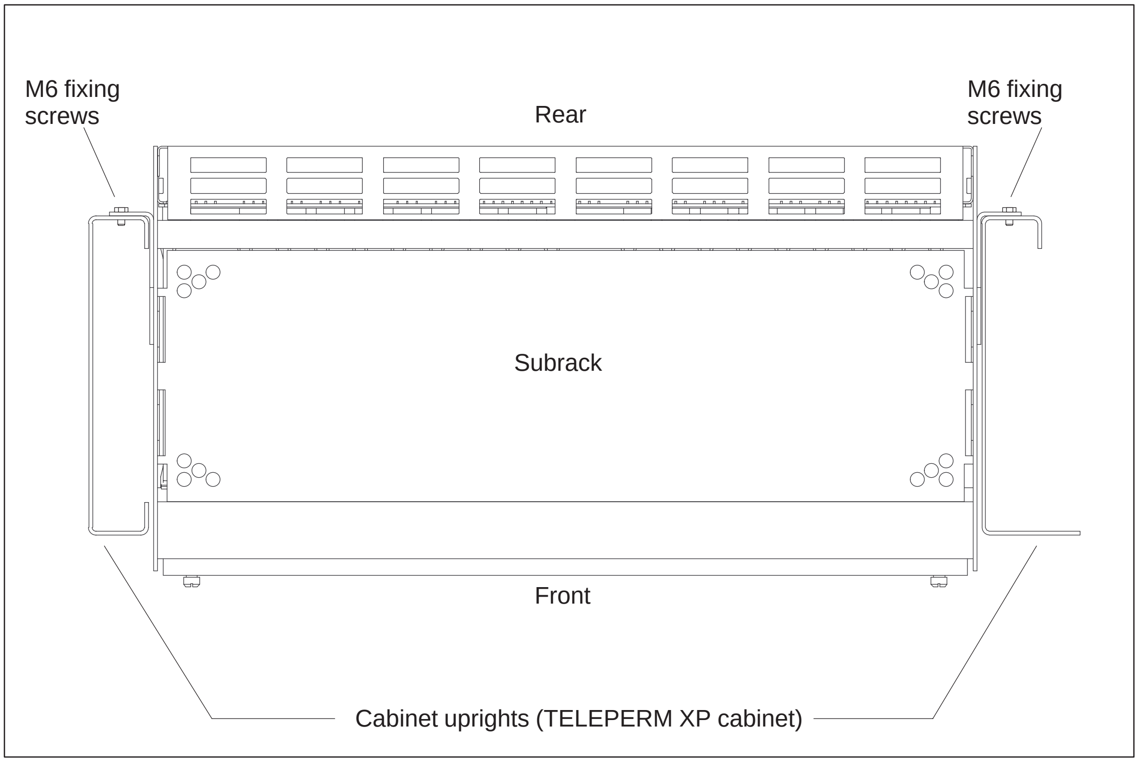

Figure 1-6 Mounting Position of the CC 155H (Top View)

Subrack

2

Chapter Overview

Order Numbers

Name	Order Number
CC 155H subrack	6ES5 188-3UH51

2.1 Subrack

Characteristics of the Subrack

The subrack for the CC 155H is divided into two electrically separated areas. The first ten slots (BEP 3 to 75) are assigned to subunit 1, the remaining eleven slots (BEP 83 to 163) are assigned to subunit 2.

The extreme left slot in each subunit is intended for the power supply unit.

The CPU is always inserted immediately next to the power supply unit. Multiprocessor operation is not possible in the CC 155H.

In addition to the CPU, there is a slot for connecting up via the interface module pair IM 304/324R.

Unused slots should be covered with dummy front plates. This directs the cooling air in the subrack and prevents the inside of the slot being touched.

The dummy front plates should be ordered separately. Their order numbers are as follows:

- Dummy front plate width 1 slot: 6XF2008-6KB00
- Dummy front plate width 2 slots: 6XF2016-6KB00

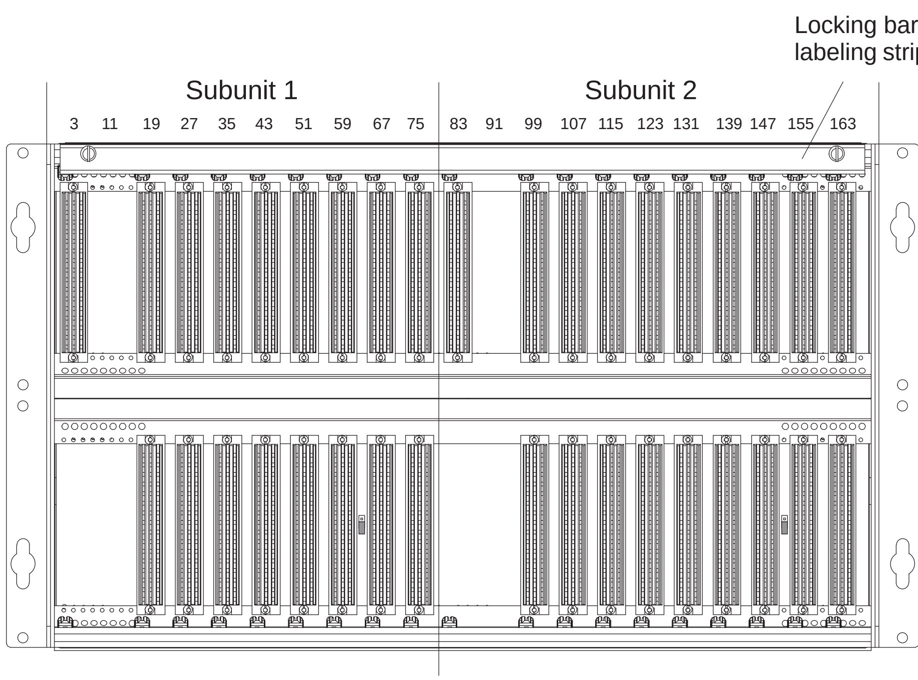

Figure 2-1 CC 155H Subrack

2.2 Configuration with SIMATIC S5 Modules

Overview

The CC 155H can be used in the following ways:

- CC 155H as a central controller
- CC 155H as a shared, switched expansion unit
- CC 155H split as both CC and EU

This means the configuration possibilities are different.

Configuration as a Central Controller

Table 2-1 shows the valid slot assignments for the CC 155H using SIMATIC S5 modules when the CC 155H is operating as a central controller (CC). The following rules apply to slot assignments:

- The power supply unit (PS) always occupies both the extreme left slots in each subunit.
- The CPU is always inserted immediately to the right of the power supply unit.
- The IM 304 or IM 324R module for linking the two subunits is inserted immediately to the right of the CPU.
- The remaining slots are “standard slots” for operating I/O, FM and CP modules.
- Only modules which have an 8-bit wide data bus connection can be operated in the two extreme right slots of each subunit.

Table 2-1 Slot Assignments as a Central Controller

Slot No.: / Module Type	3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139	147	155	163
PS																					
CPU 948 R																					
IM 304/IM 324 R																					
IM 304								1)	2)	2)									1)	2)	2)
IM 308																					
CP 1430																					
CP 5430																					
CP 581																					
DI, DO, AI, AO																					
IP 2xx																					

1) 16-bit access is also permitted to these slots; there are no restrictions to the use of the IM 304.
2) Only 8-bit access is permitted to these slots. If you connect the switched I/O via the IM 304 here, the CPU 948R recognizes in its self-tests that the upper eight data bits cannot be read back and enters this as message no. 40 in the error data block. This message can be ignored. If the message disturbs you, you can switch off the respective test step by entering the following instruction sequence in the startup OBs (OB20, OB21, OB22):

```
Segment 1
Name: seq-absc

    :SU RS 137.8
    :L DH 000E CFF3
    :LIR 1
    :L KH 0100
    :OW
    :L DH 000E CFF3
    :TIR 3
    ...
    ...
    :BE
```

Jumper Settings for Central Controller Mode

For operation as a central controller, both “lower” jumpers in the subrack must be inserted (see Figure 1-1).

Configuration as a Shared Expansion Unit

Table 2-2 shows the valid slot assignments allowed for the CC 155H using SIMATIC S5 modules when the CC 155H is operating as a shared expansion unit. The following rules apply to slot assignments:

- The power supply unit (PS) always occupies the two extreme left slots in each subunit.
- An IM 314R module pair is inserted in the two extreme right slots in each subunit.
- The remaining slots are “standard slots” for operating I/O, FM and CP modules.

Table 2-2 Slot Assignments as a Shared Expansion Unit

Slot No.: / Module Type	3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139	147	155	163
PS																					
IM 314 R																					
IM 308/ IM 308B/ IM 308C																					
CP xxx																					
DI, DO, AI, AO																					
IP 2xx																					

Jumper Settings as a Shared Expansion Unit

For operation as a shared expansion unit, both “upper” jumpers in the subrack must be inserted (see Figure 1-1).

Configuration for Split CC/EU

You can operate one subunit in the subrack as a central controller and the other as an expansion unit. To do this, the “lower“ jumper in the subunit you want to run as a CC must be inserted, in the other subunit the “upper” jumper must be inserted (see Figure 1-1).

Refer to Tables 2-1 and 2-2 for the configuration possibilities for both subunits.

Labeling Strips

The CC 155H is provided with two labeling strips to mark the slots:

- Labeling strip for central controller configuration (when shipped, mounted on the locking bar of the subrack)
- Labeling strip for configuration as a shared expansion unit (supplied loose)

For configuration as one CC and one EU, you can divide the strips in half in the middle and use them for the respective half of the subrack.

Power Supply Unit 3

In this Chapter...

This chapter gives you an overview of the power supply unit, its functions, indicators and controls, and inputs and outputs.

Chapter Overview

Order Numbers

Name	Order Number
Power supply unit	6ES5 955-7NC11

3.1 Characteristics

Introduction

The power supply unit supplies the other modules in the subrack with their operating voltages via the backplane bus. It does not provide load voltages for the signal modules.

Characteristics

The most important characteristics of the power supply unit are:

- Nominal input voltage:
  - 24 V DC
- Output voltages:
  - 5 V DC / 14 A
  - 24 V DC / 1 A
- Short-circuit proof
- Ability to withstand overload currents
- Reverse voltage protection
- Protection against incorrect insertion
- Overvoltage protection for 5-V output
- Control and monitoring signals
- Display LEDs
- Redundant backup battery with monitoring (option)
- Both output voltages (5 V DC and 24 V DC) share a common ground
- Primary/secondary galvanic isolation
  (see following note)

Note

The power supply unit 6ES5 955-7NC11 has no safe isolation between input and output. The 24 V DC supply to this power supply unit must be generated with safe isolation.

Note

The power supply unit 6ES5 955-7NC11 is only intended for operation in the CC 155H.

3.2 Inputs and Outputs

Overview

The inputs and outputs of the power supply unit are arranged on the front plate. Figure 3-1 shows the position of the inputs and outputs on the front plate.

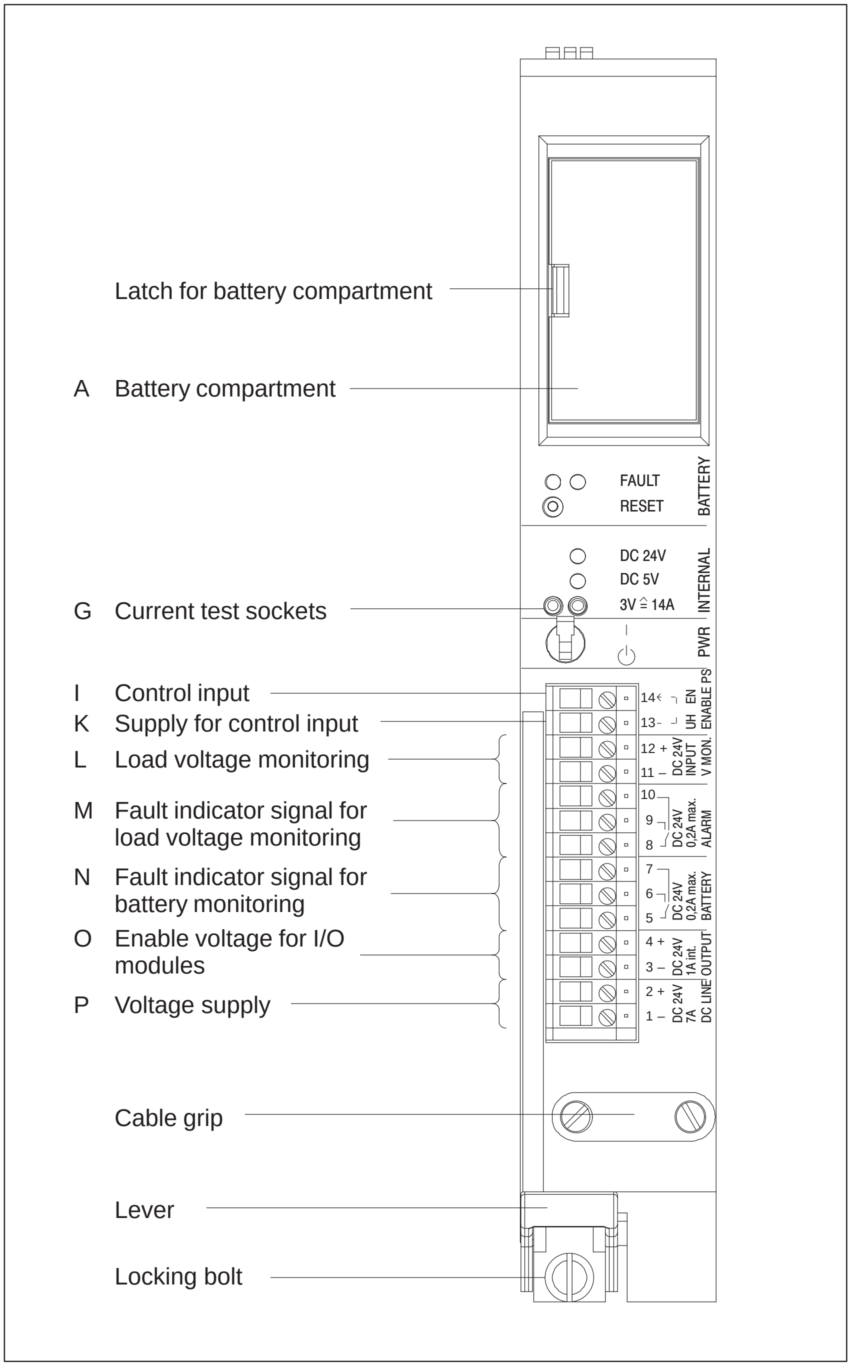

Figure 3-1 Front View of the Power Supply Unit

Table 3-1 gives an overview of the labeling and purpose of the inputs and outputs.

Table 3-1 Meaning of the Inputs and Outputs

ID	Label	Element	Purpose
G	3V ≙ 14A INTERNAL	2 test sockets	Current measurement sockets for test purposes only; no continuous operation, linearity range 0 V / 0 A to 3 V / 14 A
I	EN	Screw terminal 14	Control input for power supply unit (Enable Power Supply): V $<$ 2.72 V = OFF V $>$ 3.27 V = ON
K	UH	Screw terminal 13	5 V auxiliary voltage to supply control input EN
L	DC 24 V INPUT V MON.	Screw terminals 11 and 12	Load voltage input (Voltage Monitor), monitors 24 V load voltage for > 15.2 V
M	DC 24 V 0,2A max. ALARM	Screw terminals 8, 9, 10	Relay fault indicator signal for load voltage monitoring:
		8 – 10 closed	Rest position of relay: load voltage failed or BASPA signal from CPU active or power supply unit has no current
		8 – 9 closed	Work position of relay: load voltage in valid range
N	DC 24 V 0,2A max. BATTERY	Screw terminals 5, 6, 7	Relay fault indicator signal for battery monitoring:
		5 – 7 closed	Rest position of relay: at least one battery monitoring operating or the battery voltage on the bus is too low
		5 – 6 closed	Work position of relay: no battery monitoring operating
O	DC 24 V 1A int. OUTPUT	Screw terminals 3 and 4	24 V DC for supply enable voltage for I/O modules
P	DC 24 V 7A DC LINE	Screw terminals 1 and 2	Input for 24 V DC supply voltage

3.3 Indicators and Controls

Overview

The indicators and controls of the power supply unit are arranged on the front plate. Figure 3-2 shows the position of the indicators and controls on the front plate.

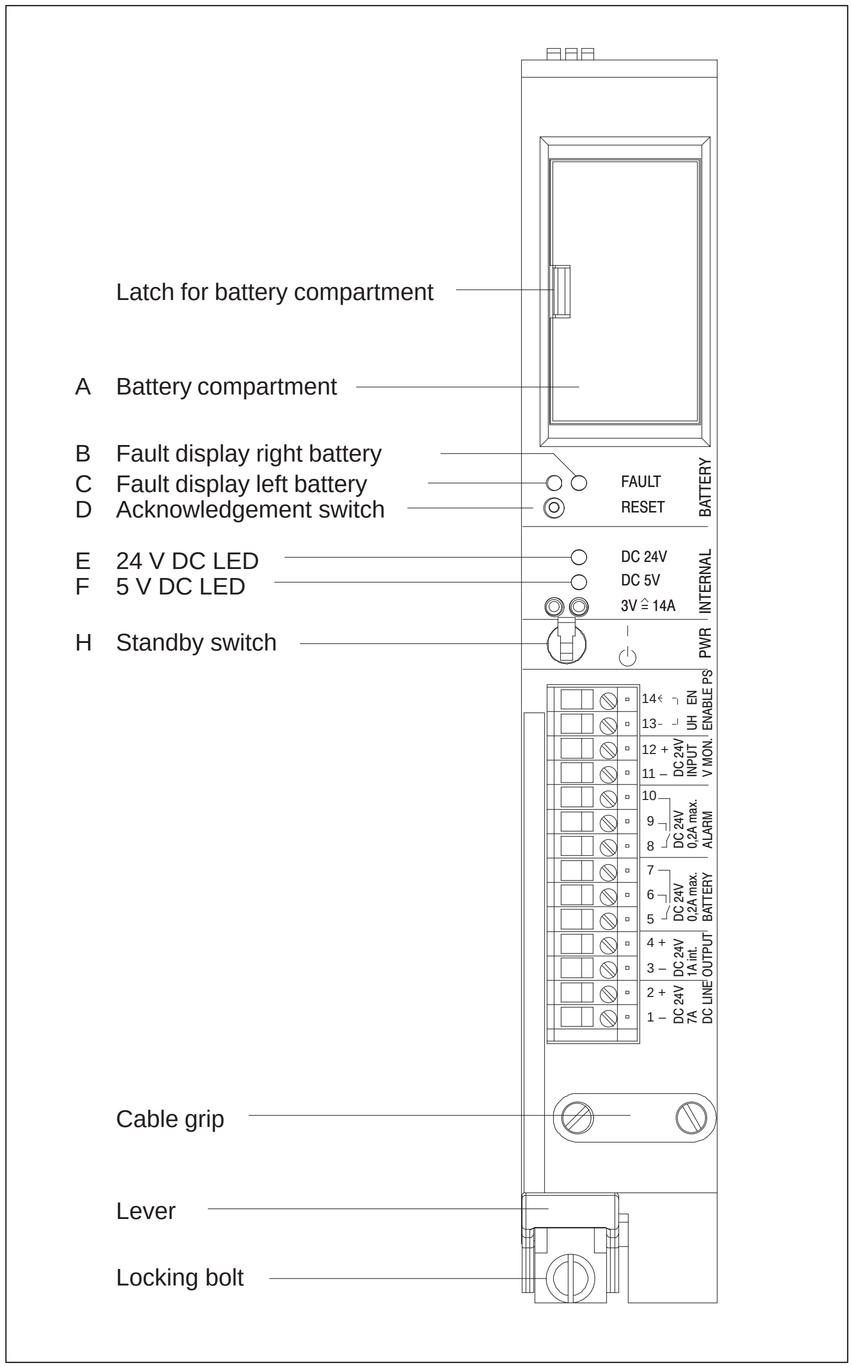

Figure 3-2 Front View of the Power Supply Unit

Table 3-2 gives an overview of the labeling and purpose of the indicators and controls.

Table 3-2 Meaning of the Indicators and Controls

ID	Label	Element	Purpose
A	–	Battery compartment	1 or 2 backup batteries behind a cover
B	FAULT BATTERY	Yellow LED right	Fault display for the right backup battery
C		Yellow LED left	Fault display for the left backup battery
D	RESET BATTERY	Pushbutton	Acknowledge a battery failure once the battery is replaced
E	DC 24V INTERNAL	Green LED	Lights up when the output voltage is in the valid range
F	DC 5V INTERNAL	Green LED	Lights up when the output voltage is in the vaid range
H	PWR	Switch	Standby on/off witch (no power on/off switch) Position ⏻: both output voltages and the enable voltage for I/O modules are 0. Position : both output voltages and the enable voltage for I/O modules exact.

3.4 Configuration Switches

Where?

The configuration switches are accessible from the right side of the power supply unit. They can only be switched when the power supply unit is disconnected from the mains supply and removed.

Function of the Configuration Switches

Using the configuration switches the behavior of some of the monitoring functions on the power supply unit can be set. The configuration switches are in the form of DIL switches.

Figure 3-3 shows the configuration switches.

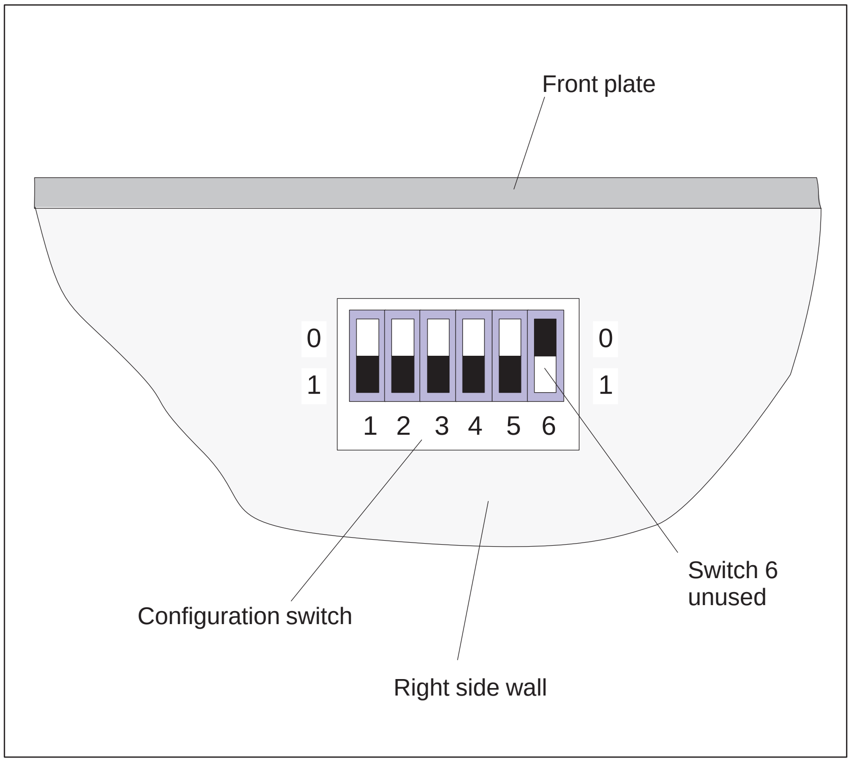

Figure 3-3 Configuration Switches

The meaning of the switch positions of the configuration switches is listed in Table 3-3. The factory default setting is shown in bold typeface in the table.

Table 3-3 Function of the Configuration Switches (Default in Bold Type)

Switch Position					Function
Switch 1	**Switch 2**	**Switch 3**	**Switch 4**	**Switch 5**	
0	0				No battery monitored
1	0				Left battery is monitored
0	1				
1	1				Both batteries are monitored
		0			Signal BAU only after power on
		1			Signal BAU also during operation
			0		Load voltage monitoring deactivated
			1		**Load voltage monitoring activated**
				0	Mains failure stored energy time 5 ms
				1	**Mains failure stored energy time 20 ms**

Switch 6 is unused.

3.5 Fault Display via LEDs

Where are Faults Indicated?

Faults in the power supply unit and the backup battery(ies) are indicated on the front plate of the power supply unit.

How are Faults Indicated?

If all monitoring functions are activated (see Section 3.4, Configuration Switches), the following fault indicators may appear:

LED	Cause	Remedy
Left LED BATTERY FAULT lights up	The left battery is missing or has failed	Insert new battery (see Section 3.10) Acknowledge by pressing RESET switch
Right LED BATTERY FAULT lights up	The right battery is missing or has failed	Insert new battery (see Section 3.10) Acknowledge by pressing RESET switch
Green LEDs DC 5V and DC 24V dark	The Enable jumper EN–UH has come loose	Check the EN–UH jumper
	P5V overloaded ($<$4.75 V)	Remove overload
	Retentive power off by overvoltage at output of P5V	Switch supply voltage off and on again (if this does not correct the fault, there is an internal fault)
	Fuse blown following reversal of supply voltage	Remove power supply unit and replace fuse (see Sections 3.6 and 3.7)
	Internal defect of the power supply unit	Replace the power supply unit
Green LED DC 24V dark	P24V overloaded ($<$19.56 V)	Remove overload
	External input of voltage $>$29.6 V at output of P24V	Remove faulty input
	Internal defect of the power supply unit	Replace the power supply unit

3.6 Installing and Removing a Power Supply Unit

Installing a Power Supply Unit

You install the power supply unit as follows:

1. Loosen the upper locking bar of the subrack and check whether the locking bolt of the power supply unit is in the correct position: the slit should be in a horizontal position.
2. Push the power supply unit into the guide rails of the subrack at slots 3 and 11, and 83 and 91.
3. Push the power supply unit into the subrack until the lever is in a horizontal position.

   Caution: Do not apply pressure to the standby switch!
4. Lock the power supply unit by turning the locking bolt with a suitable screwdriver by 90°: the slit should be in a vertical position (see Figure 3-4).
5. Fasten the upper locking bar of the subrack.

When Should You Remove the Power Supply Unit?

You must remove the power supply unit if you:

- Change the setting of the configuration switch
- Send the power supply unit to be repaired
- Replace the fuse in the power supply unit
  (e.g. after accidental reversal of the input voltage)

How You Remove the Power Supply Unit

You remove the power supply unit as follows:

1. Switch the standby switch to the position ⏻ .
2. Disconnect the power supply unit from the mains.
3. Ensure that the other connections on the front terminals of the power supply unit are de-energized.
4. Disconnect any cables from the front plate terminals and release the strain relief cable grip.
5. Loosen the upper locking bar of the subrack.
6. Undo the locking bolt of the power supply unit by turning it with a suitable screwdriver by 90°: the slit should be in a horizontal position (see Figure 3-4).
7. Press down the lever.
8. Pull the power supply unit out of the subrack.

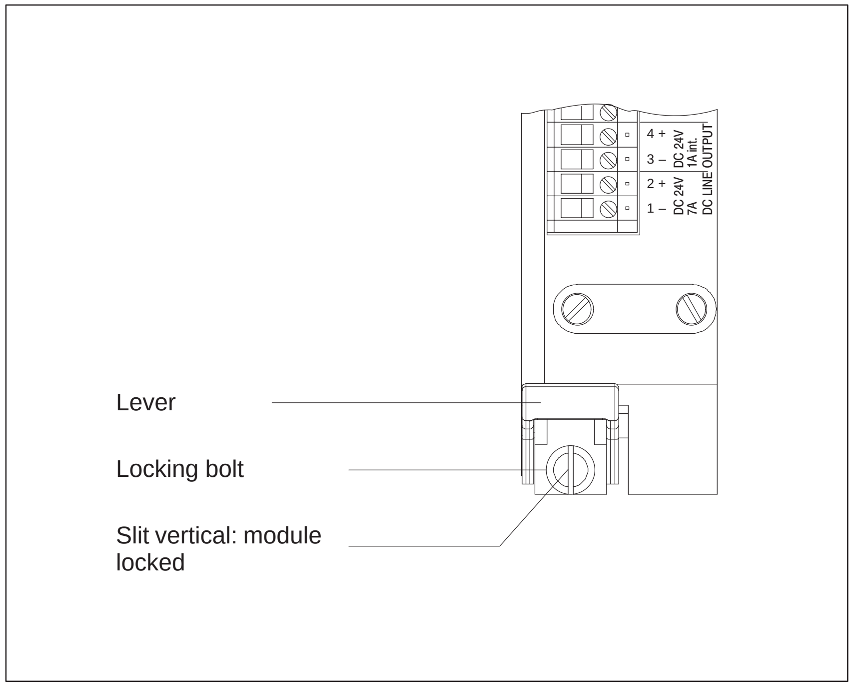

Figure 3-4 Front View of the Power Supply Unit, Locking Mechanism

3.7 Replacing a Fuse

When Should You Change the Fuse?

You must change the fuse in the power supply unit if you, for example, reverse the input voltage polarity.

How Do You Change the Fuse?

To change the fuse in the power supply unit, proceed as follows:

1. Remove the power supply unit (see Section 3.6).
2. The fuse is accessible from below. It is located on the power supply unit PCB near the lever (see Figure 3-5).

   Lever out the blown fuse from the fuse carrier using a pointed object (for example, screwdriver).
3. Press the new fuse into the fuse carrier.

Which Fuse Do You Use?

Use only the following widely available fuse for the power supply unit:

Fuse type: 19341, 10 A / 250 V medium time-lag, 6.3 × 32mm (UL/CSA)

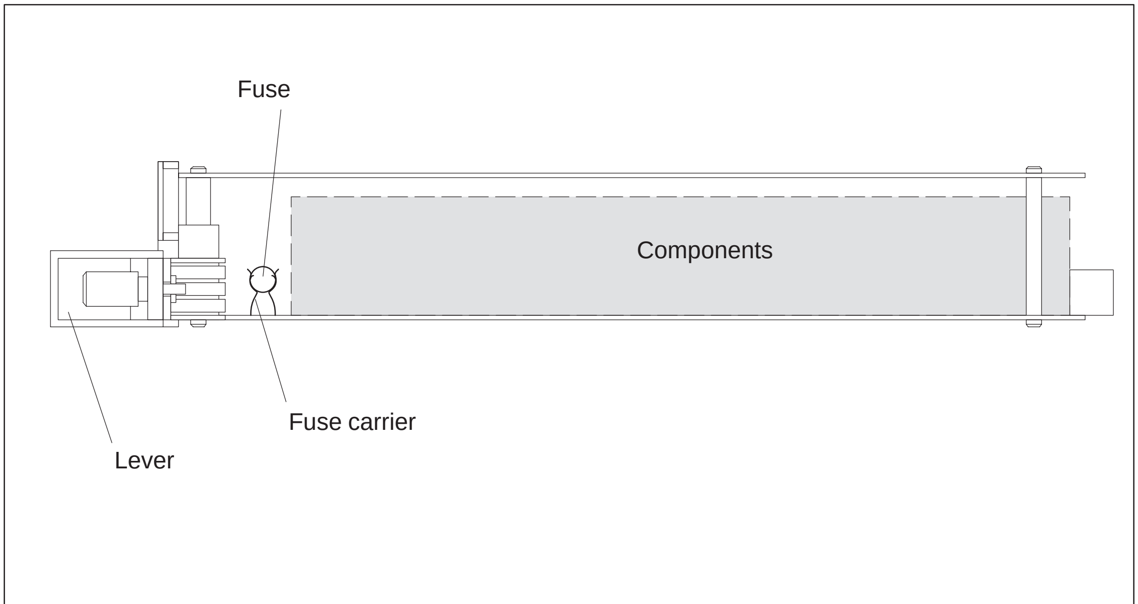

Figure 3-5 Power Supply Unit, View from Below

3.8 Wiring the Power Supply Unit

Rules for Wiring

Table 3-4 shows what you should note when wiring the power supply unit.

Table 3-4 Wiring Rules

Rules for...	Power Supply Unit
Connectable cable cross sections • without wire end ferrule • with wire end ferrule	 0.2 to 2.5 mm^2 0.2 to 2.5 mm^2 For supply lines, a minimum of 1.5 mm^2
Number of cables per connection	1 or combination of cables to 2.5 mm^2 (sum) in a shared wire end ferrule
Maximum diameter of cable insulation	∅ 3.8 mm
Stripped length of cables	11 mm
Wire end ferrules acc. to DIN 46228 • without insulating collar • with insulating collar	 Form A, 10 to 12 mm long Form E, to 12 mm long
Blade width of screwdriver	3.5 mm (cylindrical design)
Tightening torque for turning cables	0.5 to 0.8 Nm

Wiring

The following applies to the assignment of the cables to the power supply unit connections:

Table 3-5 Connection Assignments

Connection	Cable Routing
Mains connection DC LINE	Connect L+ to terminal 2
	Connect L– to terminal 1
Load voltage monitoring V MON.	Input 24-V DC load voltage. Note polarity
Control input ENABLE PS	Insert jumper from EN to UH or feed voltage ≥ 3.6 V with respect to the output chassis ground to EN
Relay terminals (suitable up to 24 V DC/0.2 A)	Connect signaling circuits for battery and load voltage monitoring
DC 24 V OUTPUT	Connect 24-V DC enable voltage for I/O modules

Use shielded cables for the connections EN, UH and V MON. and contact the cable shields to the fan subassembly with the aid of the shielding clamps supplied.

Cable Grip

Below the connection terminals is a strain relief cable grip. Feed the connecting cable for the power supply unit through this cable grip and tighten the screws of the cable grip when you have finished wiring up.

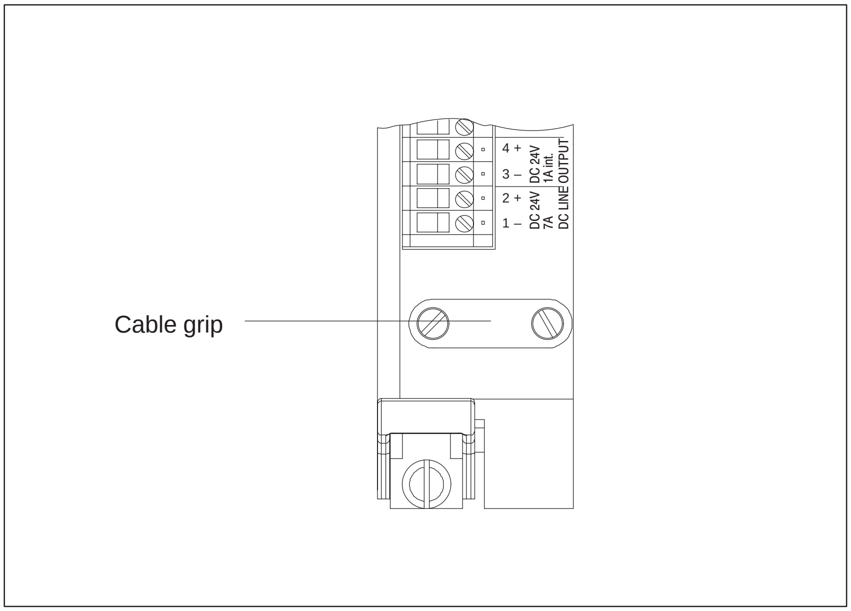

Figure 3-6 Front View of the Power Supply Unit, Cable Grip

3.9 Backup Battery (Option)

Introduction

The power supply unit has a battery compartment to hold one or two backup batteries.

Function of the Backup Battery/Batteries

If you use one or two backup batteries, the set parameters and the content of the RAM are backed up (stored) when the supply voltage fails via the backplane bus in the CPU and in programmable modules, as long as the battery voltage lies within the tolerance.

The backup battery also allows a warm restart of the CPU following POWER ON.

The battery voltage is monitored by the power supply unit.

Modes

The power supply unit can be operated as follows:

- without a backup battery
- with only one backup battery
  (if you operate the power supply unit with only one backup battery, this must be placed on the left in the battery compartment)
- with two backup batteries (redundant backup)

The monitoring of the backup batteries can be switched on and off for each battery individually via a configuration switch. When shipped, monitoring of both batteries is switched on. When a battery fails, the corresponding LED indicates the failure. The messages remain visible until the battery is replaced and the acknowledgement switch is pressed.

When operating with two batteries, the monitoring function ensures that one battery is fully discharged first before switching over to the reserve battery. The choice of backup and reserve battery following commissioning for the first time (or when both batteries are replaced at the same time) can be random. Once the assignment has been made, this is stored even following POWER OFF.

Battery Type

Lithium batteries of the type AA are used as the backup batteries. These have the following characteristics:

- Nominal voltage: 3.6 V
- Nominal capacity: 1.9 Ah

Only Siemens-approved batteries should be used.

Order number of the backup battery: 6ES7971-0BA00.

Inserting the Backup Battery(ies)

To insert the backup battery/batteries, proceed as follows:

1. First, discharge any static charge by touching a grounded metal part of the CC 155H.
2. Open the cover of the battery compartment.
3. Insert the backup battery/batteries in the battery compartment.

   Ensure correct polarity of the battery/batteries. If you are only using one backup battery, you must place it on the left in the compartment.
4. Switch on battery monitoring with the configuration switch (see page IV/3-8).

Reducing the Passivation Layer

Lithium batteries (lithium/thionyl chloride) are used as backup batteries for the CC 155H. In lithium batteries of this technology, a passivation layer can develop after storage for a very long time, and the immediate functional capability of the battery may not be certain. This may result in an error message when the power supply unit is switched on.

The power supply unit of the CC 155H is capable of reducing the passivation layer of the lithium battery with a defined load on the battery. This process may take some minutes. When the passivation layer has been reduced and the lithium battery has reached its rated voltage, the error message of the power supply unit can be acknowledged with the RESET switch.

Since the storage time of the lithium battery is not usually known, we recommend the following procedure:

- Insert the backup battery/batteries in the battery compartment.
- Acknowledge any battery error message of the power supply unit with the RESET switch.
- If the battery error cannot be cleared, try again after a few minutes.
- If the battery error still cannot be cleared, remove the battery/batteries and short-circuit it/them for one to three seconds maximum.
- Reinsert the battery/batteries and try to acknowledge with the RESET switch again.
- If the battery error message goes off, the battery/batteries is/are operational.
- If the battery error message does not go off, the battery/batteries is/are discharged.

Backup Times

The maximum backup time depends on the load on the backup battery. With a battery capacity of 63% of the nominal capacity, the following values result:

$I_{max} \leq 200\ \mu A$ backup time of approx. 250 days

$I_{max} \leq 4\ mA$ backup time of approx. 12.5 days

The maximum backup current is 4 mA.

Rules for Handling Backup Batteries

Backup batteries can be stored for 10 years. Long storage may result in a passivation layer being formed.

Store backup batteries in a cool, dry place.

Transport backup batteries in their original packaging if possible. No special measures are required for transporting the backup batteries used in the CC 155H. The lithium component in the liquid cathode of the backup battery is smaller than 0.5 g.

Observe the usual regulations/guidelines for disposing of lithium batteries in your country.

You must observe the following rules to avoid hazards in the handling of backup batteries:

Warning

Hazardous to persons and property, risk of pollutant emission.

A lithium battery can explode if treated incorrectly; improper disposal of old lithium batteries can result in pollutant emission. The following instructions should therefore be observed without fail:

- Do not throw new or discharged batteries into a fire and do not solder onto the cell body (max. temperature 100 °C).
- Do not recharge batteries.
- Do not damage batteries mechanically (drill them, crush them, etc.).
- Only replace batteries with one of the same type. Obtain the replacement via Siemens. This will ensure that you have a short-circuit protected type.
- Old batteries should be disposed of with battery manufacturers/recyclers if possible, or as hazardous waste.

3.10 Replacing the Backup Battery

Replacing the Backup Battery

Replacing a backup battery/batteries is described below.

You can replace the backup battery/batteries while the CC 155H is operating. Proceed as follows:

1. First, discharge any static charge by touching a grounded metal part of the CC 155H.
2. Open the cover of the battery compartment by unfastening the latch (see Figure 3-7).
3. Remove the discharged backup battery/batteries.
4. Insert the new backup battery/batteries in the battery compartment.

   Ensure correct polarity of the battery/batteries.
5. Close the cover of the battery compartment:

   Insert the lugs on the cover into the openings in the side of the battery compartment and swing the cover shut until it latches in place (see Figure 3-7).
6. Press the RESET switch on the front plate of the power supply unit.

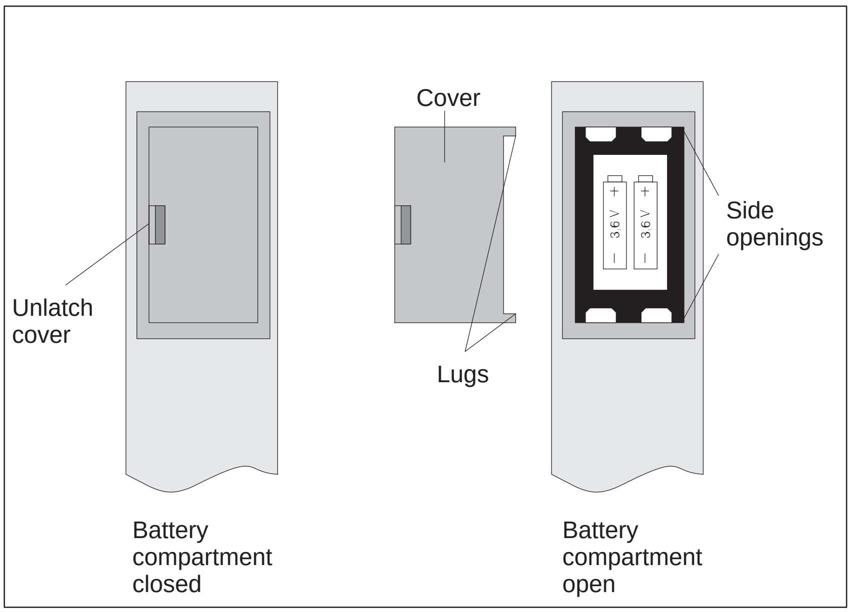

Figure 3-7 Battery Compartment of the Power Supply Unit

3.11 Technical Specifications

Dimensions, weight and cable cross sections	
Dimensions W × H × D (mm)	40 × 255 × 205
Weight	1.35 kg
Cable cross section	0.2 to 2.5 mm^2 (full wire or litz wire)
Input voltage	
Safety specifications	According to VDE 0805 / EN 60950 / IEC 950 / VDE 0160 and VDE 0106 part 101 VDE 0160
Protected against touch	Yes, when installed
Input fuse	10 A / 25 V medium time-lag, fuse, 6.3 × 32 mm (UL/CSA)
Galvanic isolation	Yes, test voltage 500 V
Nominal input voltage V_N	24 V DC (18 V to 33 V) generated with safe isolation acc. to the requirements of VDE 0100, part 410 ≙ IEC 364–4–41; VDE 0805 ≙ EN 60950 ≙ IEC 950; VDE 0106, part 101
Transient overvoltages	2 * V_N for 0.4 ms (single pulse)
Input current I_N at rated load and nominal voltage	≤ 7 A
Starting current inrush I_{max}	≤ 15* I_N, recovery time 40 s
Protection against reversing voltage polarity	Yes (replace fuse after reversing polarity)
Efficiency at rated load	≥ 0.7
Stored energy time for power failure at rated load and V_E = 18 V DC	> 20 ms or > 5 ms, can be set Recovery time at least 1 s, max. 10 events/h
5 V output voltage	
P5V output voltage	5.1 V DC
Isolation from ground	Ungrounded with respect to the casing Test acc. to VDE 0160, Test voltage 350 V AC / 500 V DC Not ungrounded once installed in the CC 155H subrack P5V ground connected to P24V ground
Nominal output current	14 A DC
Required base load	200 mA
Ripple	≤ 1% of P5V
Switching peaks	< 150 mV_S
Static voltage tolerance at variation in input voltage, load and temperature within the permitted limits	+2%/–0.5%
Dynamic voltage tolerances at load surge from 50% to 100% overshoot settling time	 ≤ 3% of P5V ≤ 5 ms
P5V startup	≤ 500 ms at 100 mF capacitive load
Voltage Monitor	Monitors voltage for < 14 V and > 15.2 V

Protection and monitoring overvoltage shutdown P5V undervoltage signal P5V Current limiting for overload	 6V ±5% 4.75V +3% 1.0 to 1.2 I_{AN}
Test sockets for P5V I5V	On front plate On front plate (3 V equals 14 A) Linearity range 0 V/0 A to 3 V/14 A
Protection and monitoring green LED 5V	LED lights up when P5V is in order
24 V output voltage	
P24V output voltage	24 V DC +25% / –12.5%
Isolation from ground	Ungrounded with respect to the casing Test acc. to VDE 0160, Test voltage 350 V AC / 500 V DC Not ungrounded once installed in the CC 155H subrack P24V ground connected to P5V ground
Nominal output current I_{AN}	1 A DC
Ripple	< 1% of P24V
Switching peaks	< 2% of P24V, pulse width < 100 ns
Dynamic voltage tolerances at load surge from 50% to 100% overshoot settling time	 ≤ 10% of P24V ≤ 5 ms
P24V startup	≤ 5 ms after P5V startup (max. capacitive load 200 μF)
Protection and monitoring overvoltage signal P24V undervoltage signal P24V Current limiting for overload	 30 V 19.2 V +3% 1.0 to 1.3 I_{AN} isolated from P5V
Monitoring green LED 24V	LED lights up when P24V is in order
Auxiliary voltage V_H	
Output voltage V_H	14.2 to 20.7 V
Internal resistance R_i	< 2.7kΩ
Short-circuit protection	Yes
Relay outputs	
Maximum voltage	24 V DC
Maximum current	0.2 A
Casing	No
Load voltage monitoring	
Ok signal level	16.7 to 18 V
Not ok signal level	14 to 15.2 V
Permitted range	0 to 36 V
Environmental data	See Chapter 5, Technical Data

Fan Subassembly

4

Chapter Overview

Order Numbers

Name	Order Number
Fan subassembly	6ES7 408-1TA01-0XA0

4.1 Characteristics

Order Number

6ES7 408-1TA01-0XA0

Characteristics

The fan subassembly has the following characteristics:

- The air inflow area is variable.
- Shield and cable clamping are possible.
- The fans can be replaced from the front during operation.
- The fan function is checked by means of speed monitoring.

Operator Controls and Indicators

Figure 4-1 shows you the front view of the fan subassembly.

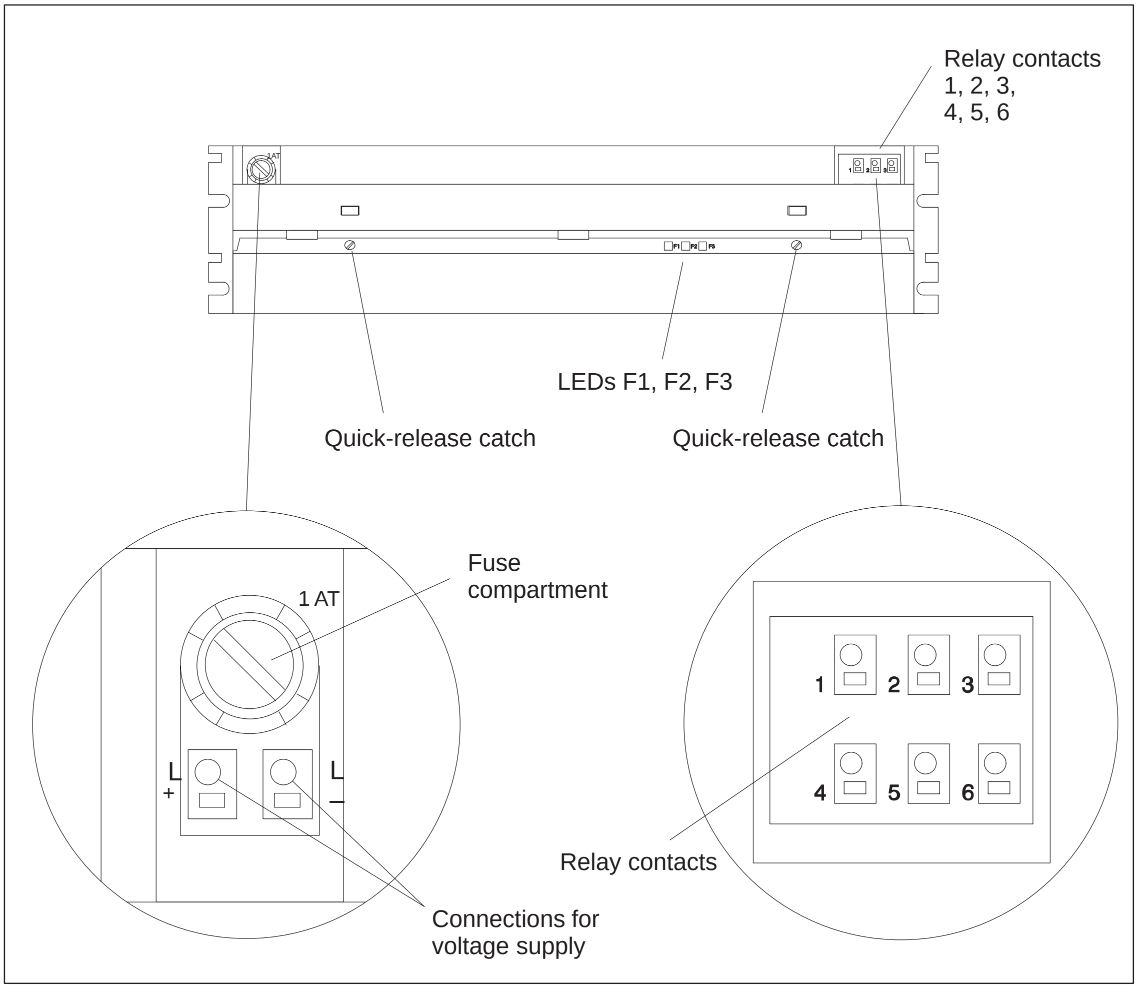

Figure 4-1 Operator Controls and Indicators on the Fan Subassembly

Components of the Fan Subassembly

Figure 4-2 shows you the component parts of the fan subassembly.

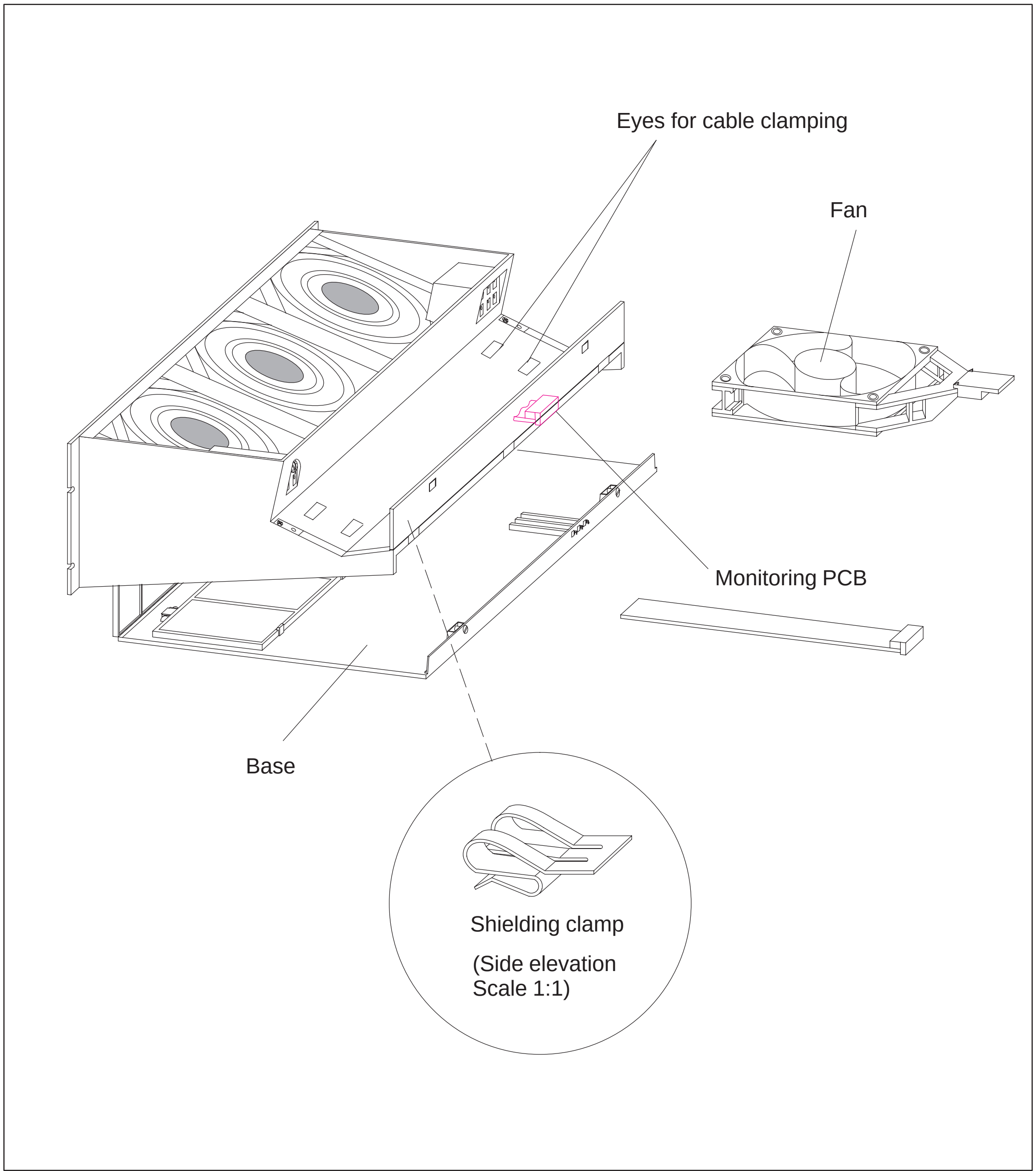

Figure 4-2 Component Parts of the Fan Subassembly

Fuse

Included in this fan subassembly are standard cartridge fuse links, 5 x 20 mm conforming to DIN

- 1.0 AT for 24 V

The fuse is already installed on shipping from the factory.

Shielding Clamps

If you do not require the shielding clamps supplied, do not install them in the fan subassembly.

Technical Specifications

Dimensions and weight	
Dimensions W × H × D (mm)	482.5 × 109.5 × 235
Weight	approx. 2.0 kg
Lifespan of the fans	
at 40 °C	70 000 h
at 75 °C	25 000 h
Maximum contact load of relay contacts 1 to 6	
• Switching voltage	24 V DC
• Switching current	200 mA
Input variables	
Input voltage	
• Nominal value	24 V DC
• Permitted range	Static: 19.2 to 30 V Dynamic: 18.5 to 30.2 V
Starting current	0.9 A at 24 V
Fuse	1.0 AT
Characteristics	
Power consumption	
• with fans	12 W
• without fans	1.4 W

Monitoring Function

In the case of a fault (defective fans) the fans are not switched off. Once you have replaced the defective fan(s), the fault is acknowledged automatically as soon as the fans have reached the required speed. Any faults that occur are not stored.

When you switch on the fan subassembly, the fans start running. After approximately 10 s the current status of the fans is indicated via LEDs and relays.

4.2 Fan Monitoring in the Fan Subassembly

Introduction

In this section, you will find out how to monitor the fans. There is a signaling concept example at the end of the section.

LEDs

The three red LEDs are assigned to the individual fans. From left to right, these are:

F1 – for fan 1

F2 – for fan 2

F3 – for fan 3

Fans

The fans have a redundant design. The fan subassembly continues to function even if one fan fails.

Fan Monitoring

The function of the fans is controlled by means of speed monitoring. If the speed of a fan drops below the limit speed of 1750 rpm, the LED assigned to it lights up. In addition, the relay K1 drops out.

If the speed of a second fan drops below the limit speed, the LED assigned to it lights up; in addition, the relay K2 drops out.

Table 4-1 is the function table for the fan monitoring.

Table 4-1 Function Table for the Fan Monitoring

Fan 1	Fan 2	Fan 3	LED F1	LED F2	LED F3	Relay K1	Relay K2
–	–	–	L	L	L	–	–
–	–	+	L	L	D	–	–
–	+	–	L	D	L	–	–
+	–	–	D	L	L	–	–
–	+	+	L	D	D	–	+
+	–	+	D	L	D	–	+
+	+	–	D	D	L	–	+
+	+	+	D	D	D	+	+
–*	–*	–*	D*	D*	D*	–*	–*

+ Fan in operation or relay picked up

– Fan failed or relay dropped out

D LEDs dark

L LEDs lit

* Power off

Signaling Concept Example

You can check the fault-free functioning of the fan subassembly using digital inputs.

You can cause the power supply to be cut off after the failure of at least two fans by using the relay K2. For example, you can use an intermediate contactor to interrupt the mains [solution a) in Figure 4-3] or interrupt the connection UH–UE of the power supply unit [solution b) in Figure 4-3].

The relay contacts are labeled as follows:

Relay K1: Nos. 1 to 3

Relay K2: Nos. 4 to 6

The diagram in Figure 4-3 explains the circuit in the fan subassembly when all fans are functioning.

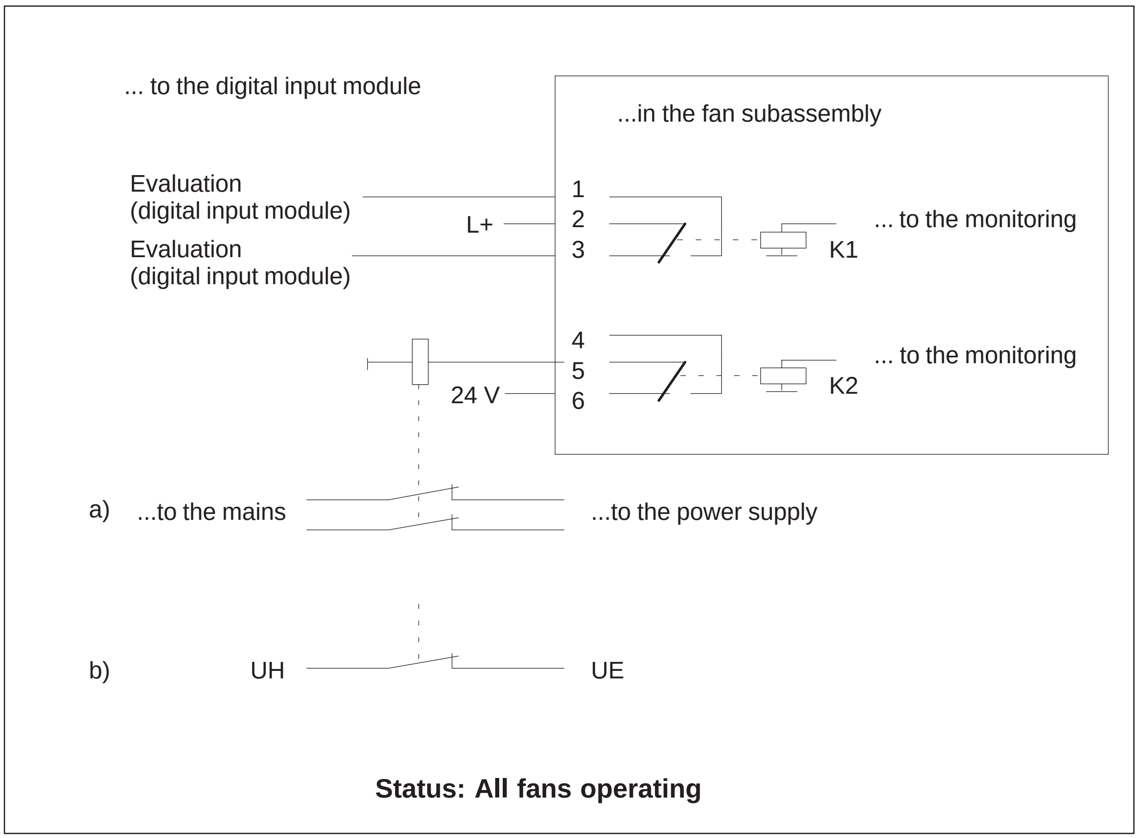

Figure 4-3 All Fans Functioning

4.3 Changing the Air Flow in the Fan Subassembly

Introduction

The fan subassembly offers two methods of ventilation: inlet air from behind or from below. For this purpose, there is a cover in the base of the fan subassembly which can be fitted according to the type of ventilation required.

When Shipped

The cover is fitted in the base of the fan subassembly. Inlet air flow is from behind.

Air Flow Possibilities

Figure 4-4 shows both air flow possibilities.

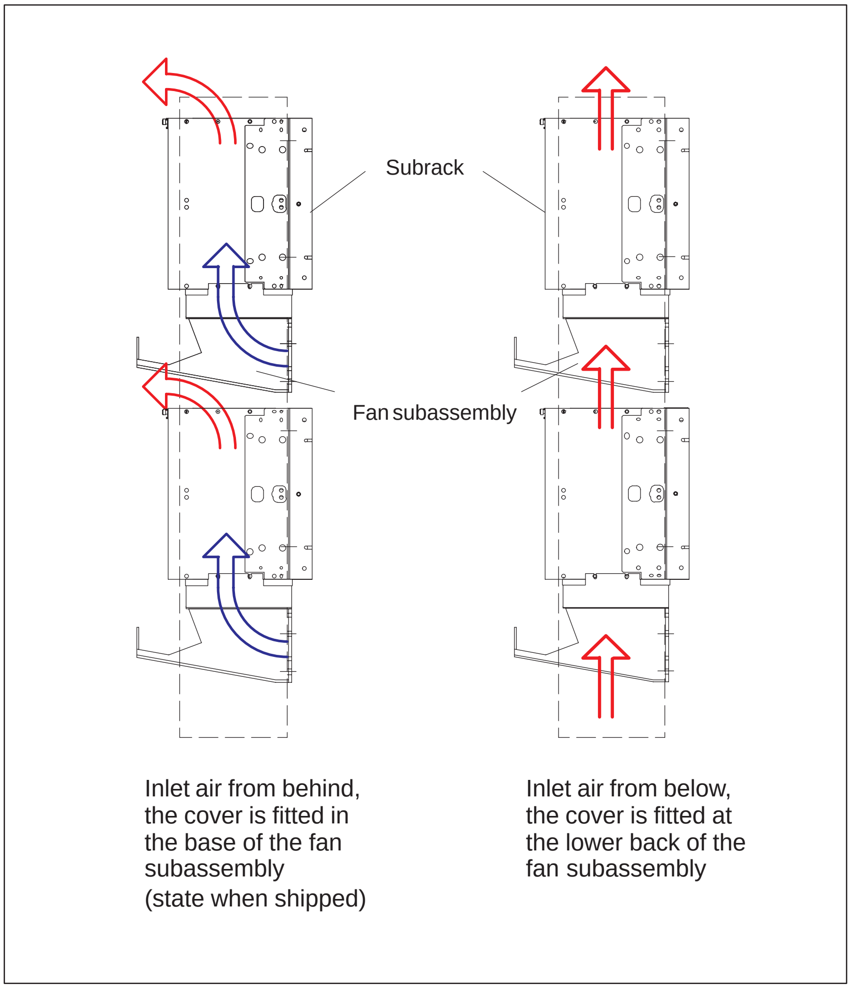

Figure 4-4 Air Flow in the Fan Subassembly

Changing the Air Flow

To change the air flow, you must refit the cover in the base of the fan subassembly following the steps described below:

1. Using a screwdriver, make a quarter turn counter-clockwise to open the two quick-release catches on the front of the fan subassembly.
2. Grasp the base with both hands; press it gently downwards and pull it fully out of the fan subassembly (see Figure 4-5).
3. The cover is secured to the base with snap catches. Press the cover from below, close to the snap catches, and remove the cover (see Figure 4-6).
4. At approximately a right angle to the base, insert the cover in the snap hinges at the rear edge of the base.
5. Push the base in again and press it upwards.
6. Using a screwdriver, make a quarter turn clockwise to close the two quick-release catches.

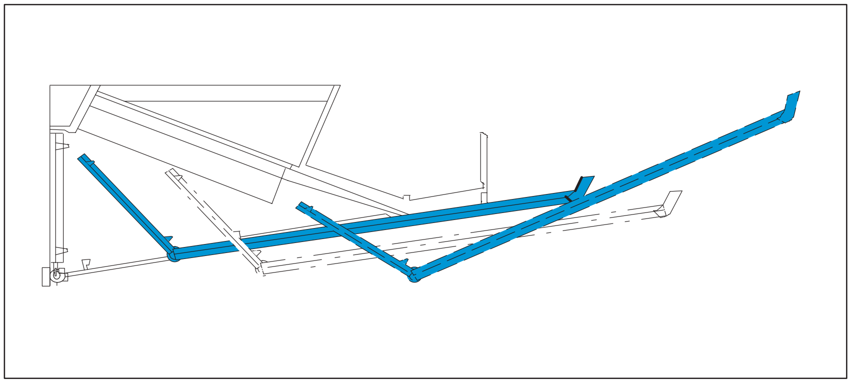

Figure 4-5 Removing the Base from the Fan Subassembly

Figure 4-6 shows you both methods of influencing the air flow by fitting the cover in the base of the fan subassembly.

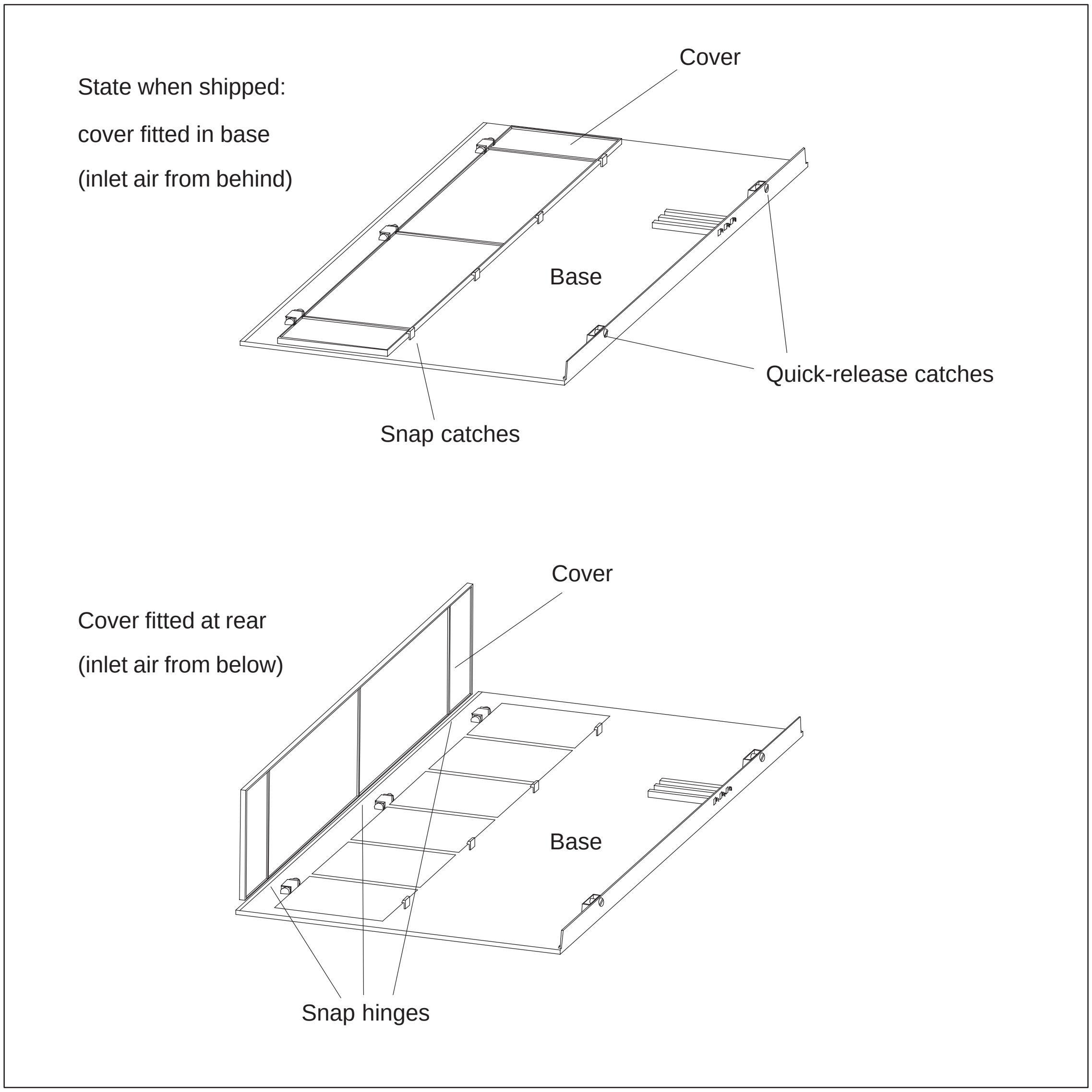

Figure 4-6 Methods of Ventilation

4.4 Installing the Fan Subassembly

Where Do You Install It?

The fan subassembly is mounted so that it is located immediately below the subrack.

How Do You Install It?

The fan subassembly is designed for installation on the rear upright, just like the subrack. Use M6 screws to fix it in place.

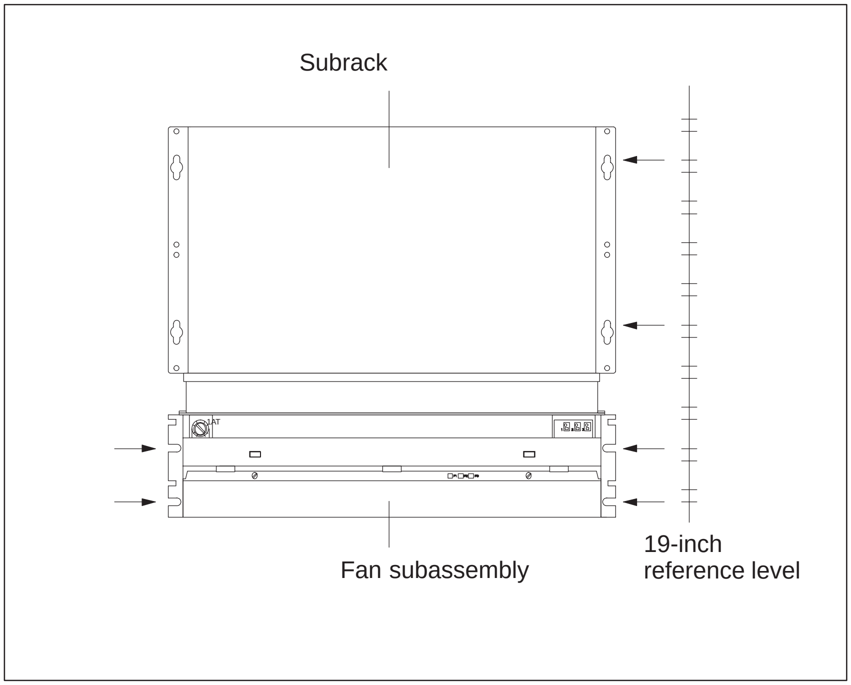

Figure 4-7 Installing the Fan Subassembly

Note

It is recommended that you install the fan subassembly first and then install the subrack immediately above it.

Monitoring the Fan Subassembly

If you want to monitor the function of the fan subassembly via your program, connect the outputs to a digital module.

You will find more details on the monitoring concept in Section 4.2 on page IV/4-5.

4.5 Wiring the Fan Subassembly

Initial Situation

You have mounted the fan subassembly directly below the subrack.

Wiring the Fan Subassembly

The following table shows what you should note when wiring up the fan subassembly:

Conductor	Conductor Cross Section	Pin-End Connectors	Stripped Length
Solid strands	0.5 to 2.5 mm^2	No	8 to 9 mm
Flexible conductors	0.5 to 0.75 mm^2	Yes,e.g.WAGO209-151	3.5 to 4.5 mm
	1.0 to 1.5 mm^2	Yes,e.g.WAGO209-164	
	1.5 to 2.5 mm^2	Yes,e.g.WAGO209-157	

Proceed as follows:

1. Strip the cores according to the above table. If you are using flexible conductors, press these with the pin-end connectors.
2. Undo the sprung terminal connections with a suitable screwdriver. Insert the cores into the terminals on the fan subassembly and pull the screwdriver out again. Ensure the correct polarity of the mains connections.
3. For relieving the strain on the cable you can fix the cable, using a cable binder, to one of the cable clamping eyes.

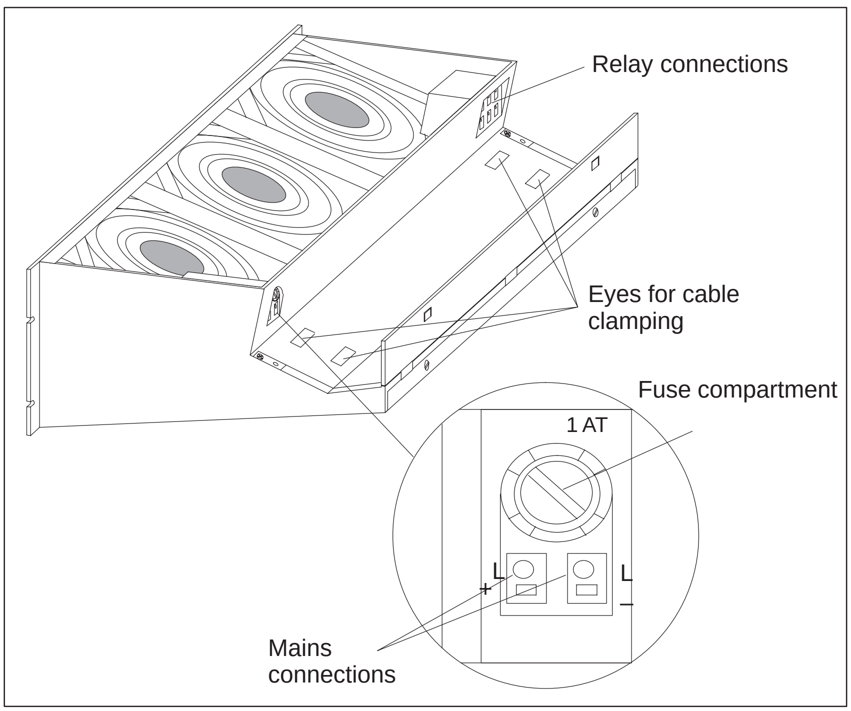

Figure 4-8 Wiring the Fan Subassembly

4.6 Cable Routing When Using the Fan Subassembly

Introduction

The fan subassembly is used to ventilate and also offers the following features:

- Cable routing
- Cable clamping
- Shield contact

Cable Routing

Depending on the number of cables and connecting lines leading to each subrack, the cross section of the fan subassembly may not be sufficient to hold all the cables.

In this case, you should route half the cables to each side via the fan subassembly.

Cable Clamping

There are eyes for cable clamping on both sides of the fan subassembly (see Figure 4-2 on page IV/4-3). You can secure the cables to these eyes with cable ties, for example.

Shield Contact

The fan subassembly offers the possibility of electrical contact for cable shields. You can use the shielding clamps supplied for this purpose (see Figure 4-2 on page IV/4-3).

To establish a contact for the cable shields, strip the outer insulation in the region of the respective shielding clamp and trap the cable shield under the clamp.

4.7 Replacing the Fuse in the Fan Subassembly

Initial Situation

The fan subassembly is mounted and wired up. The fuse is defective.

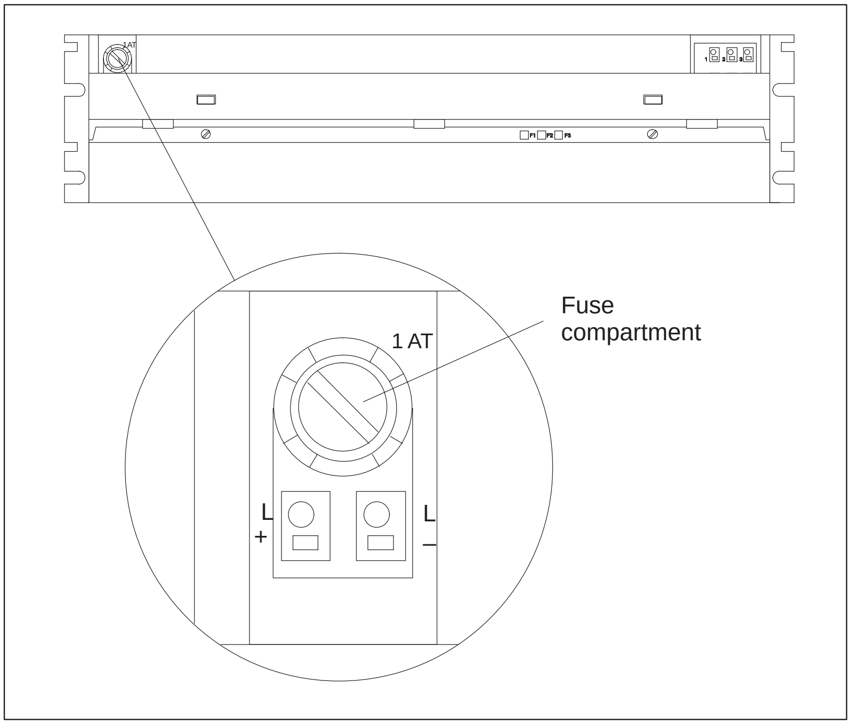

Figure 4-9 Front View of the Fan Subassembly

Which Fuse Do You Use?

Use only the following widely available cartridge fuse link for the fan subassembly:

Fuse type: 1.0 AT for 24 V, 5 x 20 mm conforming to DIN

How Do You Change the Fuse?

To change the fuse in the fan subassembly, proceed as follows:

1. Using a screwdriver, twist out the fuse cover (Figure 4-9).
2. Remove the blown fuse from the fuse cover.
3. Insert the new fuse in the fuse cover and twist this back into the fan subassembly.

4.8 Replacing Fans in the Fan Subassemblies during Operation

Initial Situation

The fan subassembly is mounted and wired up. A fan is defective. This is signaled by one of the three red LEDs (F1, F2, F3).

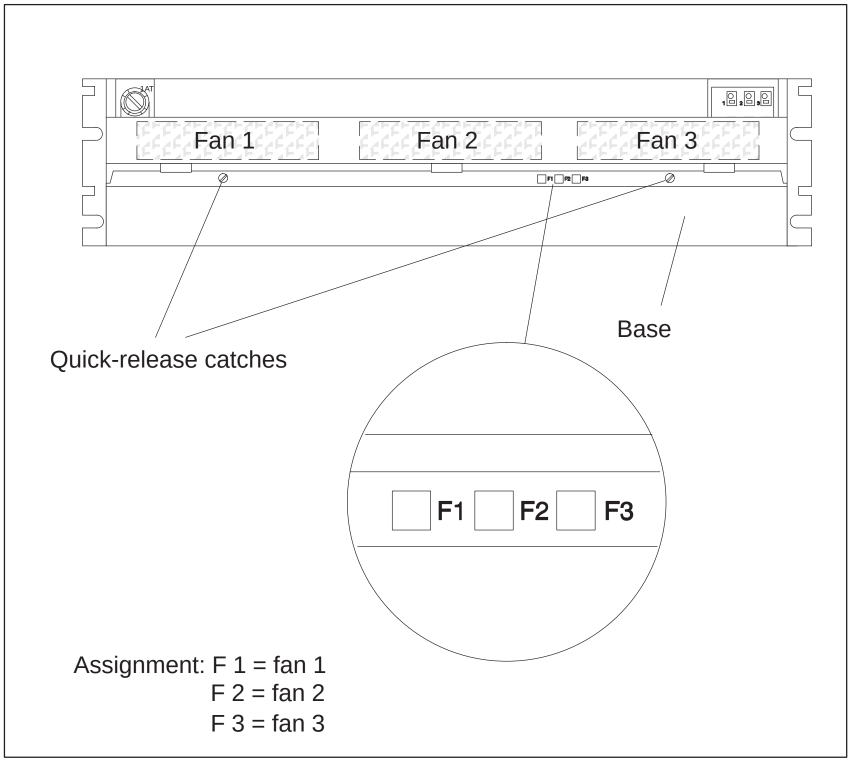

Figure 4-10 LEDs of the Fan Subassembly

Removing a Fan

Proceed as follows to replace one of the three fans:

1. Using a screwdriver, make a quarter turn counter-clockwise to open the two quick-release catches on the front of the fan subassembly (Figure 4-10).
2. Grasp the base with both hands; press it gently downwards and pull it fully out of the fan subassembly.
3. Release the fan you want to replace by pushing the fan lug (Figure 4-11) away from the casing with your thumb.

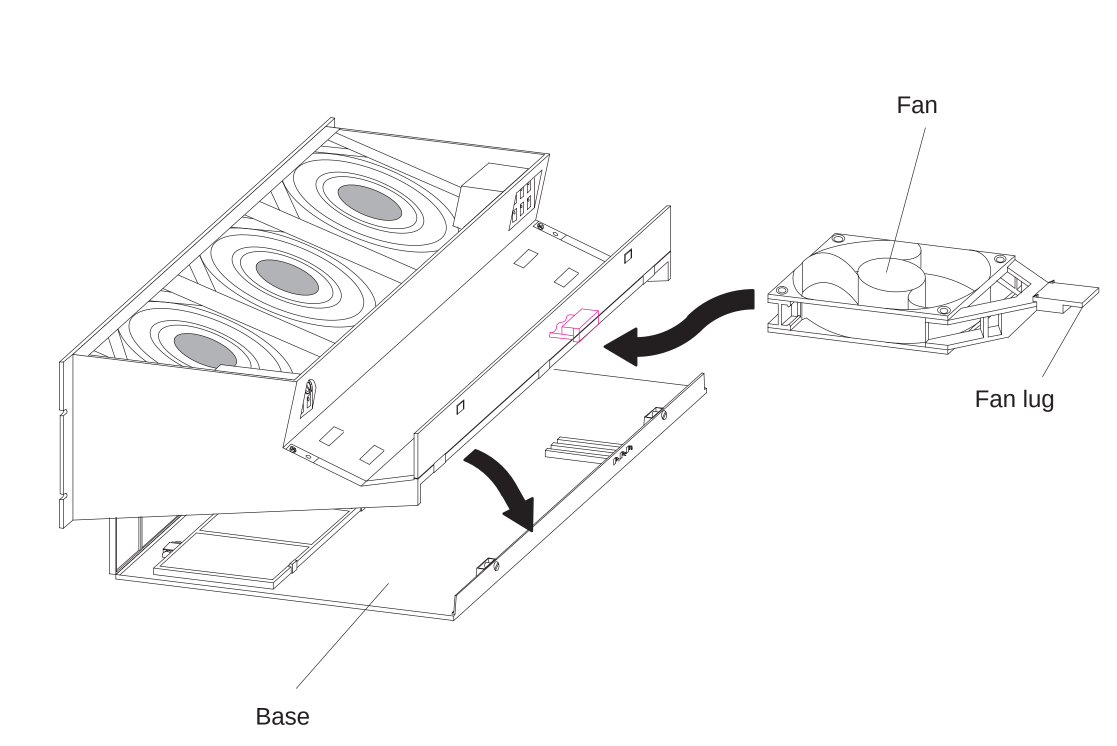

Figure 4-11 Releasing the Fan

4. Pull out the fan you want to replace.
5. Push in the new fan until it snaps into place. The fan starts to run and the fault LED goes out.
6. Push the base in again and press it upwards.
7. Using a screwdriver, make a quarter turn clockwise to close the two quick-release catches.

4.9 Replacing the Monitoring PCB of the Fan Subassembly

Initial Situation

The fan subassembly is mounted and wired up. The monitoring PCB is defective.

Replacing the PCB

Proceed as follows to replace the PCB:

1. Disconnect the mains cable of the fan subassembly from the mains voltage.
2. Using a screwdriver, make a quarter turn counter-clockwise to open the two quick-release catches on the front of the fan subassembly.
3. Remove the base of the fan subassembly (see Figures 4-5 and 4-11).

The figure below shows the front view of the fan subassembly. You can also see where the PCB is mounted.

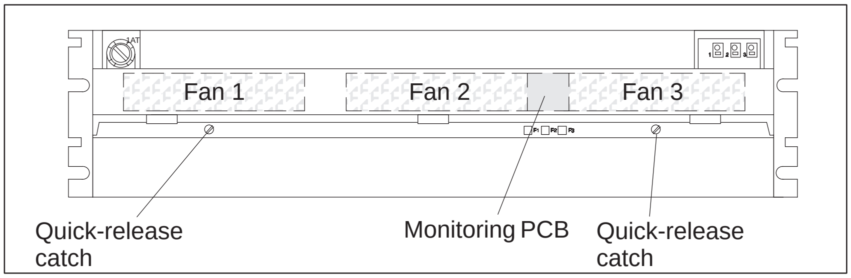

Figure 4-12 Monitoring PCB in the Fan Subassembly

4. Pull the defective PCB forwards out of the fan subassembly.
5. Push the new PCB in until it snaps into place.
6. Push the base in again and press it upwards.
7. Using a screwdriver, make a quarter turn clockwise to close the two quick-release catches.
8. Connect the mains cable of the fan subassembly to the mains voltage.

Caution

Electronic components can be destroyed.

If you do not observe the ESD guidelines when handling PCBs with electronic components, the electronic components may be damaged by static discharge.

Observe the ESD guidelines.

General Technical Data

5

Also listed in conjunction with the general technical specifications are the standards and test values that the modules of the CC 155H conform to and fulfill as well as the test criteria in accordance with which the CC 155H has been tested.

Approvals

The following approvals exist for the CC 155H:

UL Recognition Mark
Underwriters Laboratories (UL) in accordance with
Standard UL 508

CSA Certification Mark
Canadian Standard Association (CSA) in accordance with
Standard C 22.2 No. 142

The approvals apply if the appropriate labels are visible on all components.

5.1 Notes on the CE Mark

Introduction

All the components of the CC 155H meet the requirements of the standards in force in Europe provided they are installed in accordance with all the appropriate regulations.

CE Mark

The following applies to the SIMATIC products described in this manual:

CE

Products that carry the CE mark meet the requirements of EC Directive 89/336/EEC 'Electromagnetic Compatibility'.

In accordance with the Article 10 (2) of the above-mentioned EC Directive, the EU declarations of conformity and the relevant documentation are held at the disposal of the competent authorities at the address below:

Siemens AG
Automation Group
AUT 125
Postfach 1963
D-92209 Amberg

Products that do not carry the CE mark conform to the requirements and standards as specified in this manual in the sections entitled "Technical Specifications".

Areas of Application

For SIMATIC S5, the following area of application applies in accordance with the CE mark:

Area of Application	Requirements on	
	Noise emission	Noise immunity
Industry	EN 50081-2 : 1993	EN 50082-2 : 1995

Observe the Installation Guidelines

The installation guidelines for SIMATIC S5 and the safety-related guidelines which appear in this manual should be observed during commissioning and operation of the CC 155H. The following rules for the use of particular modules should also be observed.

Installing the Devices

Programmable controllers of the SIMATIC S5-135U/155U and S5-155H series and the CC 155H must be installed in metallic cabinets in accordance with these installation guidelines.

Working on Switchgear Cabinets

To protect modules from static discharge, the operator must discharge any static electricity from his/her body before opening cabinets.

5.2 Technical Specifications

Unit safety	
Device conforms to:	VDE 0805, EN 60950, IEC 950, VDE 0160 and VDE 0106 part 101
Protection class	I
Degree of protection (if empty slots are covered by dummy front plates)	IP 20 in accordance with IEC 529/DIN 40050
Climatic ambient conditions (tested to DIN IEC 68-2/-1/2/3)	
Ambient temperature in operation (air flow measured at the lower air inlet of the device)	0 to 55 °C
Transport and storage temperature	–40 to 70 °C
Temperature change:	
during operation	max. 10 K/h
during transport and while in storage (on delivery below 0 °C at least 3 h acclimatization time)	max. 20 K/h
Relative humidity:	
in operation, during transport and in storage	max. 95% at 25 °C, no condensation
Altitude:	
in operation	–1000 m to +1500 m above sea level (1080 hPa to 860 hPa)
during transport and while in storage	–1000 m to +3500 m above sea level (1080 hPa to 660 hPa)
Pollutant emissions:	
SO_2	0.5 cm^3 / m^3, 4 days
H_2S	0.1 cm^3 / m^3, 4 days
Mechanical ambient conditions (tested to DIN IEC 68-2-6)	
Vibration during operation	10 to 50 Hz (constant amplitude 0.075 mm) 58 to 500 Hz (constant acceleration 1 g)

Noise immunity, electromagnetic compatibility (EMC)	
RFI suppression	to EN 55011
limit value class	A [2]
Conducted interference on AC supply lines (230 V AC)	
to EN 61000-4-4/IEC 1000-4-4 (Burst)	2 kV
to IEC 1000-4-5	
between two lines (μs pulses)	1 kV
between line and ground (μs pulses)	2 kV
DC supply lines (24 V DC) to EN 61000-4-4/ IEC 1000-4-4 (Burst)	2 kV
Signal lines to EN 61000-4-4/IEC 1000-4-4 (Burst)	2 kV [1]
Immunity to static discharge to EN 61000-4-2/IEC 1000-4-2 (ESD) [2]	Proper installation ensures an interference immunity of 4 kV contact discharge (8 kV atmospheric discharge)
Immunity to electromagnetic high-frequency radiation [2], pulse-modulated to ENV 50140 / IEC 1004-4-3	80 MHz to 1000 MHz 10 V/m 80% AM (1 kHz)
Immunity to electromagnetic high-frequency radiation [2], amplitude-modulated to ENV 50204	900 MHz 10 V/m 50% ED
Immunity to high-frequency sine-form to ENV 50141	0.15 MHz to 80 MHz 10 V 80% AM
Mechanical data	
Mechanical requirements	Installation in stationary equipment, subject to vibration; installation on ships and in vehicles if special installation rules are observed, but not on the engine
Weight	
Subrack	approx. 7.5 kg
Fan subassembly	approx. 2.0 kg
Dimensions (W × H × D) (subrack plus fan subassembly)	483 mm × 420 mm × 270 mm

1) Signal lines that do not serve the process control, e.g. connections to the external I/O etc.: 1 kV
2) With cabinet door closed

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