SIEMENS

SIMATIC S5

IP 243 Analog Module with FB 160/ FB 161

Equipment Manual

Release: 02

Order No: 6ES5998–0KF21

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Warning

Risks involved in the use of so-called SIMATIC–compatible modules of non–Siemens ma-nufacture

"The manufacturer of a product (SIMATIC in this case) is under the general obligation to give warning of possible risks attached to his product. This obligation has been extended in recent court rulings to include parts supplied by other vendors. Accordingly, the manufacturer is obliged to observe and recognize such hazards as may arise when a product is combined with products of other manufacture.

For this reason, we feel obliged to warn our customers who use SIMATIC products not to install so-called SIMATIC–compatible modules of other manufacture in the form of replacement or add–on modules in SIMATIC systems.

Our products undergo a strict quality assurance procedure. We have no knowledge as to whether outside manufacturers of so–called SIMATIC–compatible modules have any quality assurance at all or one that is nearly equivalent to ours. These so–called SIMATIC– compatible modules are not marketed in agreement with Siemens; we have never recommended the use of so–called SIMATIC– compatible modules of other manufacture. The advertising of these other manufacturers for so–called SIMATIC–compatible modules wrongly creates the impression that the subject advertised in periodicals, catalogues or at exhibitions had been agreed to by us. Where so–called SIMATIC– compatible modules of non–Siemens manufacture are combined with our SIMATIC automation systems, we have a case of our product being used contrary to recommendations. Because of the variety of applications of our SIMATIC automation systems and the large number of these products marketed worldwide, we cannot give a concrete description specifically analyzing the hazards created by these so–called SIMATIC– compatible modules. It is beyond the manufacturer's capabilities to have all these so–called SIMATIC–compatible modules checked for their effect on our SIMATIC products. If the use of so–called SIMATIC– compatible modules leads to defects in a SIMATIC automation system, no warranty for such systems will be given by Siemens.

In the event of product liability damages due to the use of so–called SIMATIC–compatible modules, Siemens is not liable since we took timely action in warning users of the potential hazards involved in so–called SIMATIC– compatible modules. "

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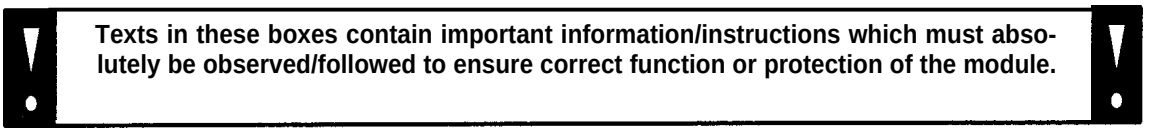
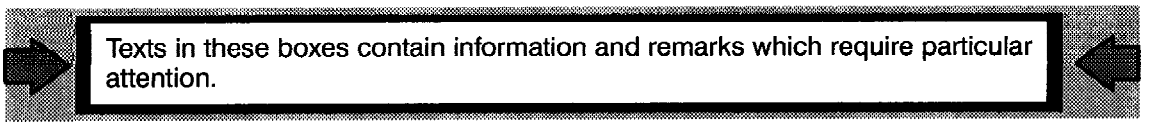




For clarity's sake, this equipment manual does not contain complete, detailed information and cannot cover every conceivable operating situation.

Contact your local Siemens office if you require additional information or if a special problem arises which is not covered in sufficient detail by this equipment manual.

In addition, be aware that the contents of this documentation do not constitute a part of a previous or existing agreement, promise, or a legal relationship, and are not intended to alter same.

All obligations on the part of Siemens are based on the respective purchase order which also contains the complete and solely valid warranty provisions. This IP 243 equipment manual neither widens nor restricts these contractual warranties.

1 Application and Application Area

The IP 243 is a module for input and output, for preliminary processing, and for jumpering of analog signals within short processing times. The submodule in its full configuration has eight quick analog input channels with max. 35 µsec. conversion time, four input channels with analog value conditioning and four analog output channels. Two comparators allow the comparison of analog values with each other and via two value difference amplifiers, the signals can be amplified up to 20 times their original strength. All analog signals can be freely jumpered via soldering bases on the circuit board. This means that as a user you can decide about the individual combinations of the available hardware components.

Furthermore, eight digital inputs and eight outputs with direct bus access are available. Customer–specific interrupt processing can be effected by means of the jumpering base.

The IP 243 submodule can be used for the following programmable controllers:

- S5–115U/H
- S5–135U
- S5–150S/U
- S5–155U/H

> **Attention:** Make sure that the module is only plugged into the insert slots provided for intelligent peripheral modules on the respective central or expansion units (see section 6.1).

For the programmable S5–115U, an adapter casing is required. No fan assembly is required.

2 Mechanical Construction

2.1 Dimensions and Mechanical Data

The IP 243 is a printed circuit board in double European format, with dimensions of 233.4 mm x 160 mm (DIN 41494). In accordance with the SIMATIC S5 compact peripheral system, the PCB takes up one slot in the rack. It has a width of 1–1/3 SPS[1] (20 mm). 42 Faston connector pins (2.4 mm x 0.8 mm) are located on the front plate. The bus connection is made via a second row, 48–way base connector. The base connector is located on the upper half. Ground (Mext) connection is provided via contact strips in the guide rails.

2.2 Overview of the Individual Variants

The IP 243 is available in one full–configuration version and two different part-configuration versions. The full–configuration module has the following independent functions:

- 1 Analog/digital converter, 8 channels, 12 bits, 35 µsec. conversion time, bipolar or unipolar
- 2 Digital/analog converters, 12 bits, bipolar
- 1 Digital/analog converter, 8 bits, unipolar
- 1 Analog output amplifier
- 4 Analog value conditioning circuits with operating point and amplifier setting
- 2 Difference amplifiers (P controllers) with adjustable gain
- 2 comparators with gating logic connected in series, can be read in statically and/or with interrupt generation (interrupt evaluation is only possible for the SIMATIC S5–150U/S and S5–155U with externally-wired digital input module for interrupt generation).
- 8 binary inputs can be read in statically and/or with interrupt generation (interrupt evaluation is only possible for the SIMATIC S5– 150U/S and S5–155U with externally–wired digital input module for interrupt generation).
- 8 binary outputs, 24 V, 200 mA, switching to P potential, not current–limited.

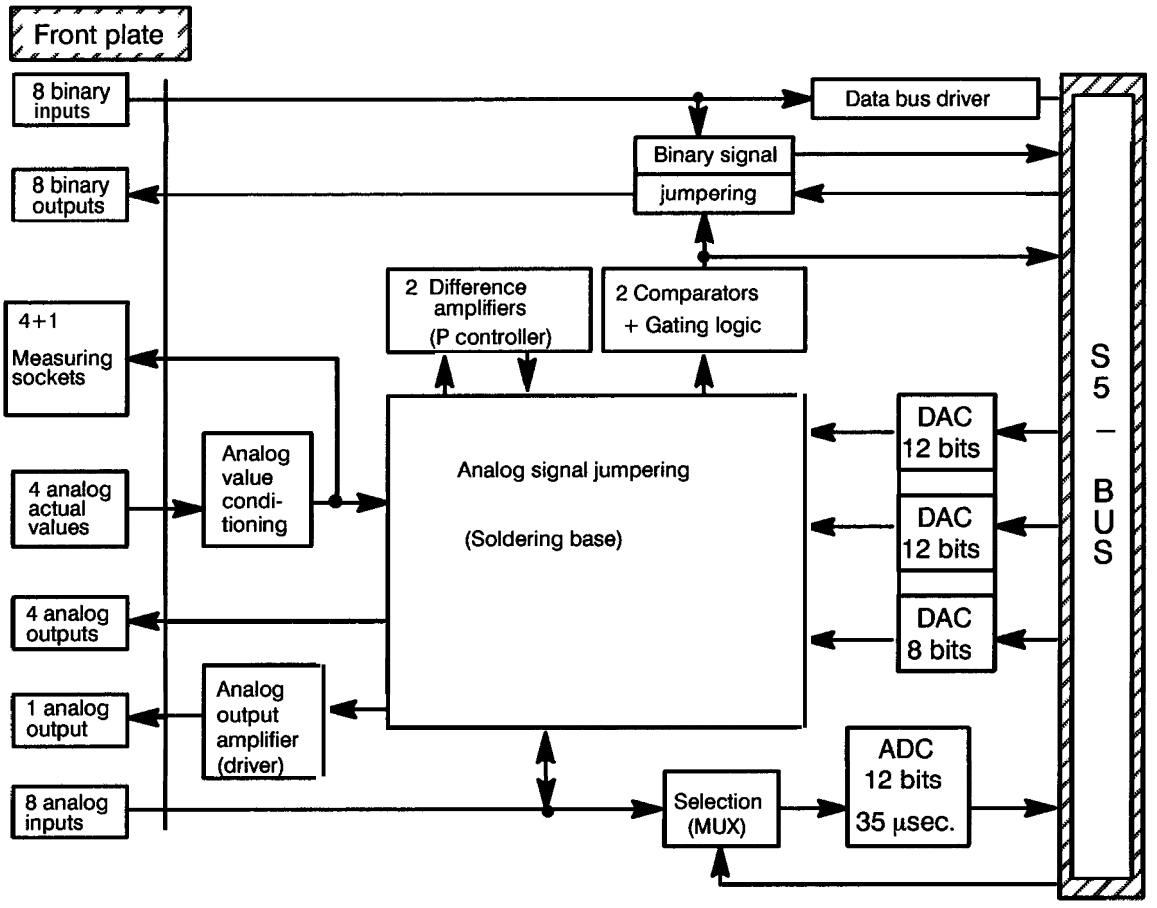
The inputs and outputs of the analog function groups are routed to the analog signal jumper block. This makes it possible to combine the individual functions to suit user requirements. All signals are nonfloating.

[1] standard plug–in station

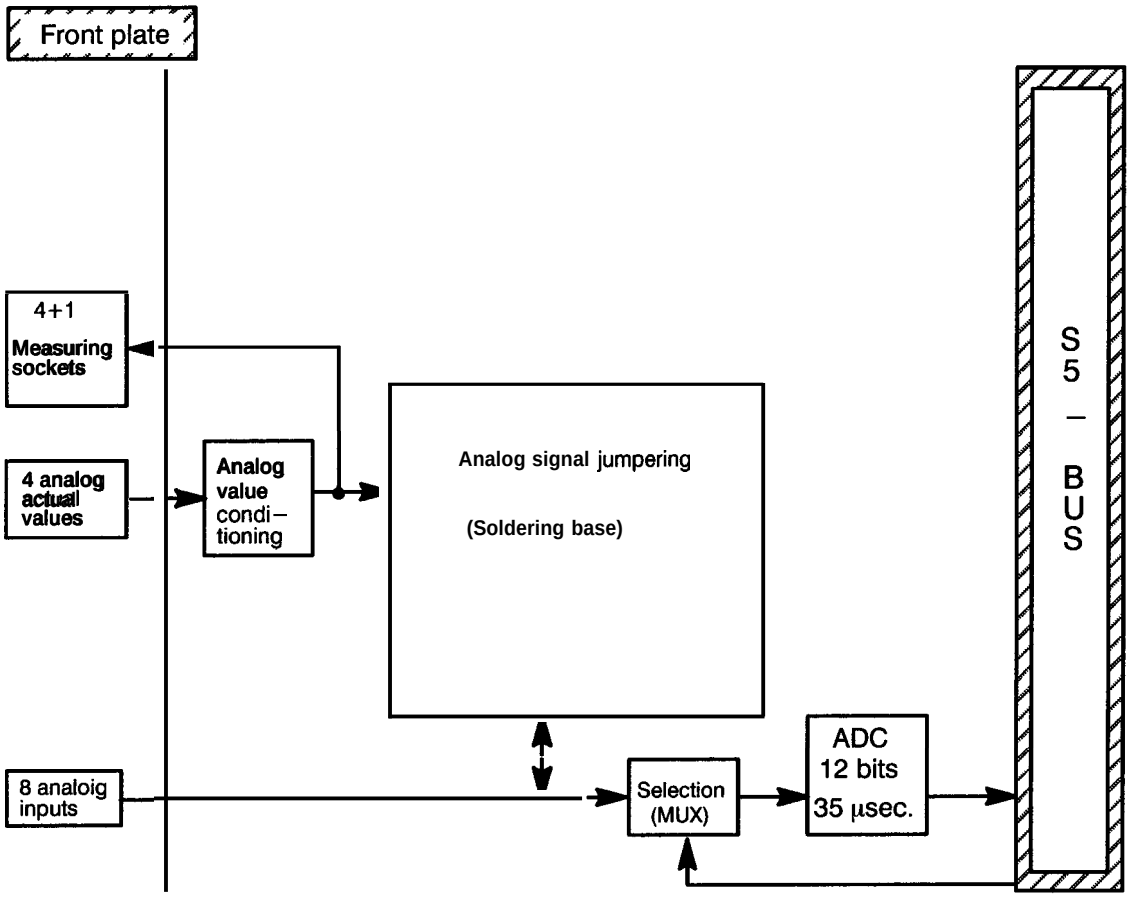
The following table shows which components are for the part-configuration versions:

Type	Full Con figuration Module 243- 1AA	Part Configuration Module 243–1AB	Part Configuration Module 243–1 AC
A/D converter, 12 bits	1	1	–
D/A converter, 12 bits	2	–	2
D/A converter, 8 bits (with driver)	1	–	1
Analog value conditioning circuit	4	4	2
Difference amplifier (P controller)	2	–	2
Comparators (alarm generation)	2	–	–
Binary inputs	8	–	–
Binary outputs	8	–	–
Interrupt/alarm	x	–	–

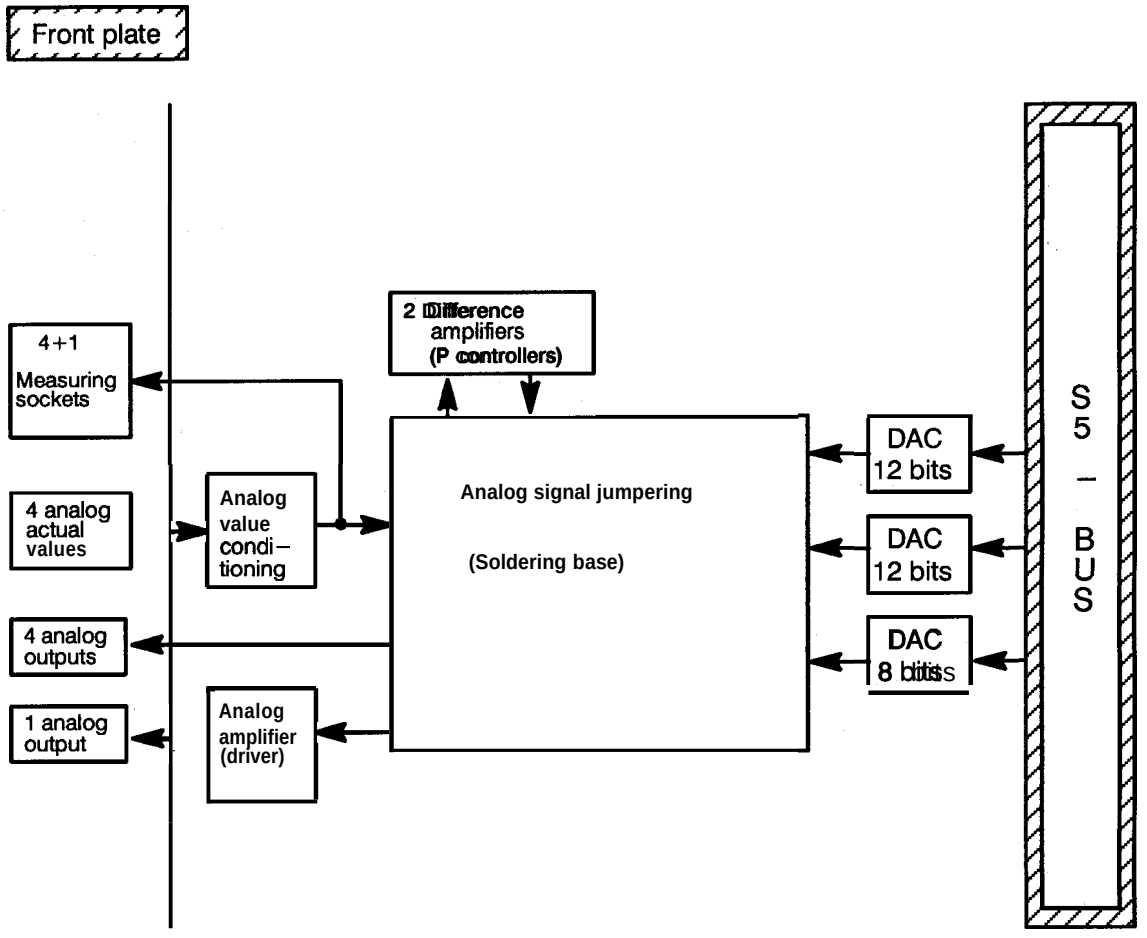
2.3 Block Diagram IP 243 – IAA, Full Configuration



2.4 Block Diagram IP 243- IAB, Partial Configuration



2.5 Block Diagram IP 243 – 1AC, Partial Configuration

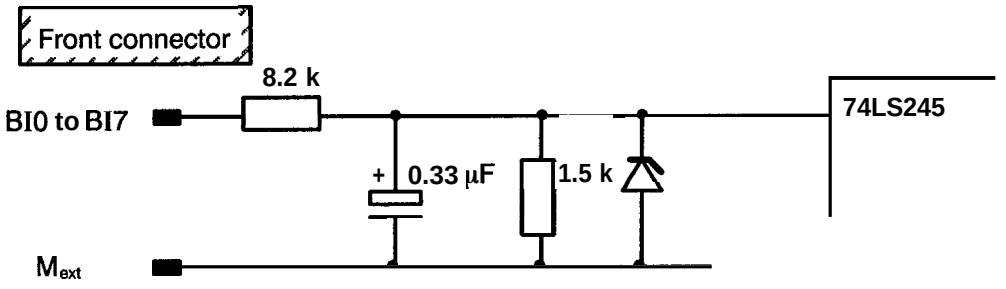


3 Function Description

3.1 Binary Input

The characteristics of the eight digital input channels BI0 to BI7 are:
- Rated input voltage : 24 V DC
- Input voltage for signal"1" : 12.7 Vto 30 V
- No potential isolation
- Pole protection available
- Input filtering: Typical delay time 2.7 msec.
- Inputs selectable for interrupt generation (therefore, input filtering time is relevant.)

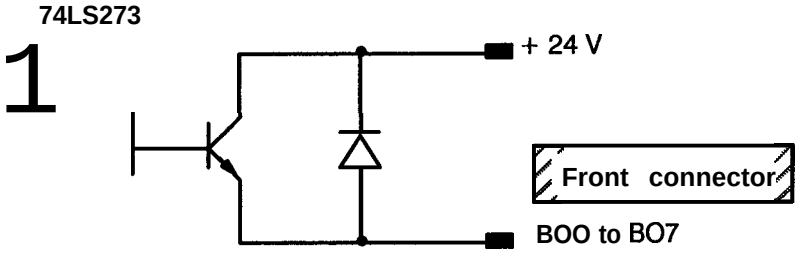
Input circuitry for one input



3.2 Binary Output

Eight digital output channels (BOO to BO7) are available which, however, are only used for triggering of indicator elements (e.g., lights). Contrary to the standard S5 set–up no BASP signal is generated. Other characteristics:
– P switching “open emitter”
– Not “short–circuit proof”
– After return of voltage all channels carry the signal “O”
– Output current per BO: maximum of 200 mA
– Output total current (for all 8 BOs): maximum of 600 mA

Output circuitry per output:



3.3 Analog Input

3.3.1 Rated Input Ranges

The analog input is applicable to the following voltage ranges:

–5 V to +5 V
–lo v to +10 v
o v to +10 v

The ranges can be set via jumpers on the module (seethe layout plan in section 5.4, Setting Elements and Jumpers). Upon delivery the jumpers are set for the voltage range O V to 10 V. The jumper settings for the respective rated input ranges must be made as follows:

Rated input range	Jumpers				
	Uni	Bi		10 V	20 V
–5 v to +5 v	⊙	⊙	⊙	⊙	⊙
–lo v to +10 v	⊙	⊙ |—| ⊙		⊙ |—| ⊙	⊙
o v to +10 v	⊙	⊙ |—| ⊙		⊙	⊙ |—| ⊙
	⊙ |—| ⊙	⊙		⊙ |—| ⊙	⊙

\|—\| → **Jumper installed**
Uni → Unipolar
Bi → **Bipolar**

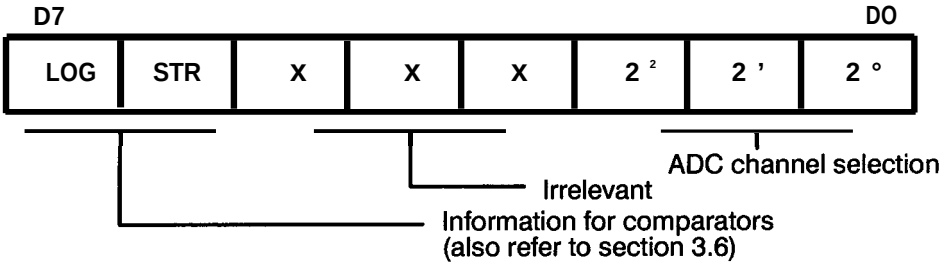
3.3.2 Conversion of the Analog Input Signals

The central circuit of the analog input is the analog/digital converter which converts an applied setpoint in a maximum of 35 µsec. with a resolution of 12 bits. An analog eight–channel multiplexer is connected on the input side of the converter. The conversion of the analog input values takes place in three stages:

1) Select the channel
2) Output the conversion command
3) Read the result

1) Select the channel:
The multiplexer is addressed under the module address +7. The channel to be converted (O to 7) is selected by writing the three data bits 2^0, 2^1, and 2^2.

Channel selection: (in the byte module address +7)



If the same channel is read in several times in sequence, it need not be selected each time. In such a case it suffices when the active values are converted and read out. The selected channel remains current until a different channel number is written.

The current channel selected by the program is indicated by the three yellow LEDs on the module front plate.

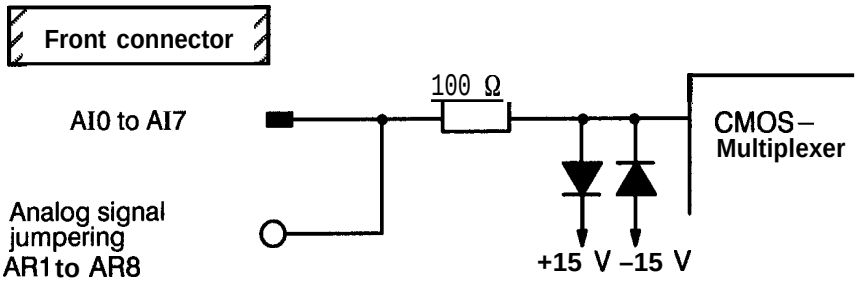
2) Output the conversion command:
The conversion command is given by writing the module address +6, whereby the written data is irrelevant.

3) Read the result:
The result can be read immediately in the peripheral word module address +6 as the "Ready" signal is only generated when the ADC has completed the conversion (i.e., after a maximum of 35 µsec.). No additional waiting time is required. It is also possible to process other parts of the user program within the 35 µsec. period.

3.3.3 Input Circuitry

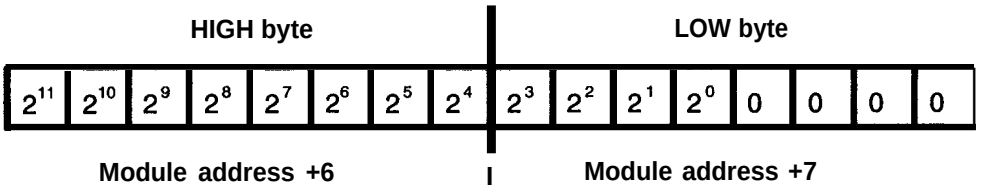
At the pins AR1 to AR8 of the analog signal jumping block, the analog input AIO to AI7 can be not only active, but they can also be switched to the inputs of the analog–value conditioning circuit or to the outputs of the difference amplifiers.

Input circuitry of the multiplexer input (per input)



3.3.4 Digital Representation of Measuring Values

For representation of the analog values in digital form, two bytes (per word) are required.



The coding of the analog input signals is accomplished by accepting only the positive values in the range O V to 20 V (rated input range &10 V) respectively O V tol O V (rated input range i-5 V). The digital values are then referred to the rated input range and are allocated in accordance with the following table.

Units	Input voltage [V]		HIGH Byte / LOW Byte	Conversion of bit pattern	Input voltage in reference to range	
	*1O v	±5 V	2^{11} 2^{10} 2^{9} 2^{8} 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} 0 0 0 0	0 Vto +20 v	o v to +1OV	
≥2048	≥10.0000	≥5.0000	1 1 1 1 1 1 1 1 1 1 1 1 0000	≥4096	220.000	≥10.000
+2047	+9.9951	+4.9976	1 1 1 1 1 1 1 1 1 1 1 1 0000	4095	19.9951	9.9976
+2000	+9.7656	i-4.8828	1 1 1 1 1 1 0 1 00 0 00000	4048	19.7656	9.8828
+1000	+4.8828	+2.4414	1 0 1 1 1 1 1 0 1 0000000	3048	14.8828	7.4414
+ 1	+0.0049	+0.0024	1 00 00 0 0 000 0 1 0000	2049	10.0049	5.0024
Switch pt.	+0.0024	+0.0012			10.0024	5.0012
0	0	0	1 000 0 0 000000 0000	2048	10.0000	5.0000
Switch pt.	– 0.0024	-0.0012			9.9976	4.9966
– 1	-0.0049	-0.0024	0 1 1 1 1 1 1 1 1 1 1 1 0000	2047	9.8951	4.9976
-1000	– 4.6628	-2.4414	0 1 00000 1 1 0000000	1048	5.1172	2.5566
–2000	– 9.7656	–4.8828	000000 1 1 00000000	48	0.2344	0.1172
–2048	–10.0000	-5.0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0.0000	0.0000
-2049	–10.0049	-5.0024	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	I	I	I

Attention: By adding 8000_H to the digital values, the values can be converted to a dual–complement format.

In the input voltage range O V to 10 V, the active analog value is represented directly as an amount (without sign).

Units	Input voltage [V]	HIGH Byte / LOW Byte
	o v to +1o v	2^{11} 2^{10} 2^{9} 2^{8} 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0}
≥+4096	≥+1 0.0000	1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
+4095	+9.9976	1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
+4000	+9.7656	1 1 1 1 1 0 1 0 0 0 0 0 0 0 0 0
+2000	+4.8828	0 1 1 1 1 1 0 1 0 0 0 0 0 0 0 0
+1	+0.0024	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0
0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
≤ –1	≤ –0.0024	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

3.4 Analog Output

3.4.1 Jumpering of Analog Output

Five channels are available (AO1 to AO5) which can be freely distributed via the soldering base. It is possible to output analog values (provided by the D/A converters) on a certain channel, and transfer this signal simultaneously to different outputs. In the same way, for instance, the outputs of the difference amplifiers (P controllers) or conditioned analog values can be directly output as analog values. Attention must be paid to the input side of the analog output AO5 to make sure that an analog amplifier is connected. It is not only able to amplify the value provided by DAC3, but also a value which, via an analog input, is present as an actual–value conditioning input on the P controller. Three digital/analog converters, which are described in more detail below, convert binary values into analog signals.

3.4.2 Digital/Analog Converters 1 and 2

3.4.2.1 Rated Output Range and Resolution

Digital/analog converters DAC1 and DAC2 are systems independent from each other. The resolution is 11 bits plus sign. Bipolar analog values in the range of ±1O V can be output.

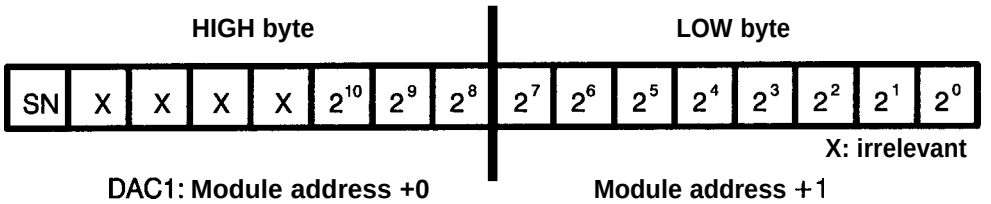
3.4.2.2 Writing the Analog Outputs

DAC1 is addressed under the module address +0 and DAC2 under the module address +2. The binary value should be transferred to DAC1/2 by a word statement to prevent possible peaks during byte-wise write procedures.

Example: S5 : TPW address

3.4.2.3 Digital Representation of Analog Values

Two bytes are required for representing the values, the output from DAC1 and DAC2, in digital form.



DAC1: Module address +0 Module address +1
DAC2: Module address +2 Module address +3

The representation of the digital values in the bit pattern is to be interpreted in a way that the output voltage range ±10 V is only considered as a positive range within O V to +20 V.

The 12th bit is cutoff and written separately as sign bit at position 2^{15}. The highest representable value FFF_H, at a resolution of 12 bits, corresponds to the maximum voltage +20 V, but it is adapted to the output voltage range and is converted to the negative voltage –10 V.

The digital representation of analog values over the entire rated output range appears as follows:

Units	output voltage [V]	HIGH Byte	LOW Byte	Amount of bit pattern (including sign)	Output voltage in reference to range o v to +20 v
		SN X X X X 2^{10} 2^9 2^8	2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0		
+2047	**+9.9951**	0 XXXX o 0 0 0 0 0 0 0 0 0 0		**0**	0.0049
+2000	**+9.7656**	0 XXXX o 0 0 0 0 1 0 1 1 1 1		47	0.2344
+1000	**+4.8828**	0 XXXX 1 0 0 0 0 0 1 0 1 1 1		1047	**5.1172**
+1	+0.0049	0 XXXX 1 1 1 1 1 1 1	1 1 1 0	2046	**9.9951**
0	**o**	**0 XXXX 1 1 1 1 1 1 1**	**1 1 1 1**	2047	**10.0000**
-1	**-0.0049**	**1 XXXX o 0 0 0 0 0 0 0 0 0 0**		2048	**10.0049**
–1000	**–4.8828**	**1 XXXX o 1 1 1 1 1 0 0 1 1 1**		3047	**14.8628**
–2000	**–9.7656**	**1 XXXX 1 1 1 1 1 0 0 1 1 1 1**		4047	**19.7656**
–2048	**–10.0000**	**1 XXXX 1 1 1 1 1 1 1**	**1 1 1 1**	4095	**20.0000**

Attention: If a value provided in the two's complement form by the programmable controller is output as an analog value, this value must first be converted to a format suitable for a DAC1 or DAC2. For this purpose the sign bit 2^{15} must at first be saved, then the bit pattern must be inverted (command CFW) and the sign bit must be written back.

Attention: When the power supply of the programmable controller is initially turned on, or when the voltage returns after power–off, DAC1 and DAC2 are preset with the value 000000000000 = +9.9951. This value remains until it is overwritten.

3.4.3. Digital/Analog Converter 3

3.4.3.1 Rated Output Range and Resolution

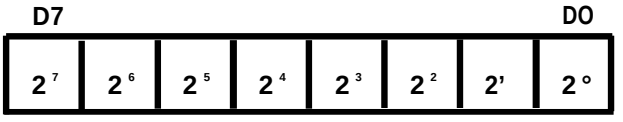
The digital/analog converter DAC3 has an 8–bit resolution. Unipolar analog values in the range O V to +10 V can be output. The analog output amplifier should be added on the output side of DAC3 to amplify the analog output signal, as output current from DAC3 is too low to carry a load.

3.4.3.2 Writing the Analog Output

DAC3 is addressed under the module address +4. The command TPY suffices, since only 8 bits need to be transferred to the output.

3.4.3.3 Digital Representation of Analog Values

The digital value to be converted to an analog voltage has a 1–byte format:



Module address +4

The value to be output is represented as an amount (without sign) in the following bit pattern:

Units	Output voltage	Byte
		272 6 2 5 2 4 232 2 1 0
255	9.961	1 1 1 1 1 1 1 1
200	7.812	1 1 0 0 1 0 0 0
100	3.906	0 1 1 0 0 1 0 0
1	0.039	0 0 0 0 0 0 0 1
0	0	0 0 0 0 0 0 0 0

Attention: When the power supply of the programmable controller is initially turned on, or when the voltage returns after power–off, DAC3 is not preset. It can assume any value which remains until it is overwritten.

3.4.4 Analog Output Amplifier

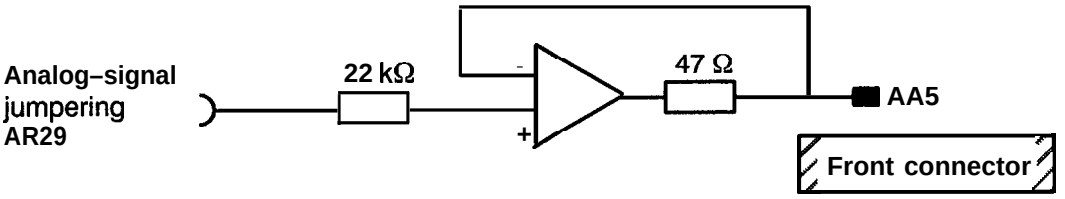
3.4.4.1 Description

Mainly in cases where DAC3 is used for analog output, the analog output amplifier is added on the output side of the digital/analog converter as a voltage booster. This is necessary because the converter is not permanently "short–circuit proof" and the short circuit current is not defined.

It is possible, however, to route signals other than those of DAC3 to the output amplifier, via analog–signal jumpering. The voltage booster has a 1:1 amplification.

3.4.4.2 Circuitry

The analog output amplifier has the following circuitry:



3.5 Analog Value Conditioning Circuit

3.5.1 Operating Elements

The four inputs of the analog value conditioning circuits are meant to standardize the voltages provided by encoders to the O V to +10 V range, and are conditioned in accordance with the setting of the trimming potentiometer on the module front plate. Conversion in the O to +10 V range is not possible unless input voltage > –4 V. Conditioning is always necessary when negative voltages are processed and routed via the comparators. The
comparators are designed for positive voltages so that the input voltages must be transformed to the positive range.
In addition to the 4 trimming potentiometers for setting the amplification and the offset, there are four measuring sockets on the front plate via which the conditioned analog values can be scanned. A socket (socket 6) is also available. This socket is connected to analog ground M_{ari}a. This socket can be used as the ground connection for a graphic recorder which records the conditioned analog signals.

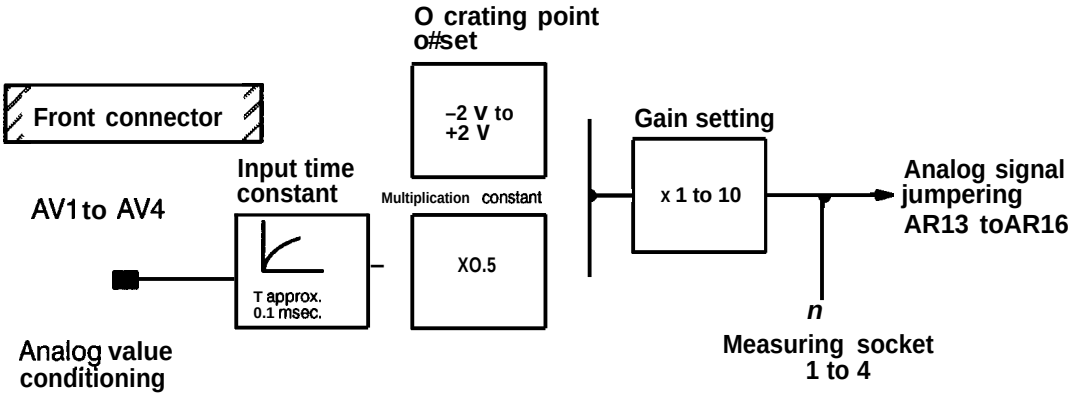
! Attention: Socket5 hasnofixed internal connection to a specific signal. Itis located on the analog–signal jumpering space AR32. This socket is free for switching, either for a signal from an IP 243. The conditional socket (i.e., the component routed to the soldering base) or for another external signal. !

3.5.2 Functioning

On the front plate of the IP 243 there is one trimming potentiometer per input (AV1 to AV4) for the offset of the operation point by a binary amount between –2 V and +2 V and for setting the amplification (gain) as a factor in the range from 1 to 10.

First, the active analog value is multiplied by the fixed factor 0.5 specified by the module. Then, the set offset is added, and finally this value is multiplied by the desired gain factor. The possible total gain is between 0.5 and 5.

The following block diagram shows the operating method of the analog value conditioning circuit:



Example:

An input voltage which can vary in the range from –1 V to –1.5 V is to be compared in terms of hardware with an input voltage from –0.5 V to –2 V.

Both signals are routed through the analog value conditioning circuit. The following settings are possible:

Offset = +2
Gain = 3

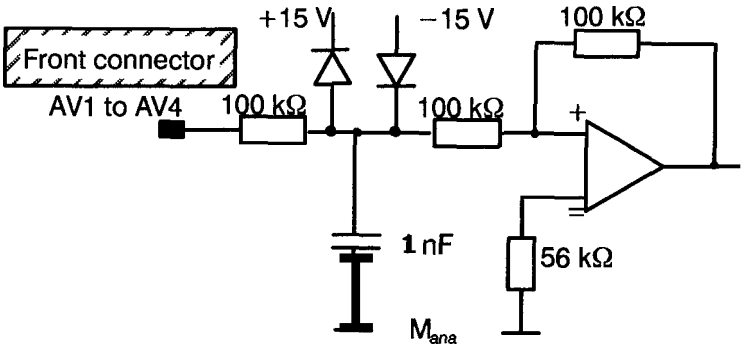
–1 .0 v x 0.5	= –0.50 v	
	+2.00 v	
	+1 .50 v x 3	= +4.50 v
–1.5 *v* x *0,5*	= –0.75 v	
	+2.00 v	
	+1.25 V x 3	= +3.75 v
–0.5 v x 0.5	**= –0.25 V**	
	+2.00 v	
	+1 .75 v **x 3**	= +5.25 **V**
–2.0 v **x** 0.5	= –1 .00 v	
	+2.00 v	
	+1 .00 v **x** 3	= +3.00 v

Accordingly, the voltages 3.75 V to 4.5 V on one side are compared with 3.0 V to 5.25 V on the other side.

There are many possibilities for setting the trimming potentiometers. The user decides which conversion is most suitable.

3.5.3 Input Circuitry

Input circuitry for value conditioning (per input)



Attention: The input constant of approximately 0.1 msec. was selected to filter out possible interferences. The delay is approximately proportional to the capacitor 1 nF.

3.6 Comparators and Gating Logic

3.6.1 Input Signal Range and Possible Circuitry

The two comparators are designed to compare positive voltages in the range of O V to +10 V. If negative input voltages need to be compared, they must be routed through the analog value conditioning circuit and converted to a positive value.

The inputs of the comparators are connected with analog–signal jumpering via a filter circuit (AR17 to AR20).

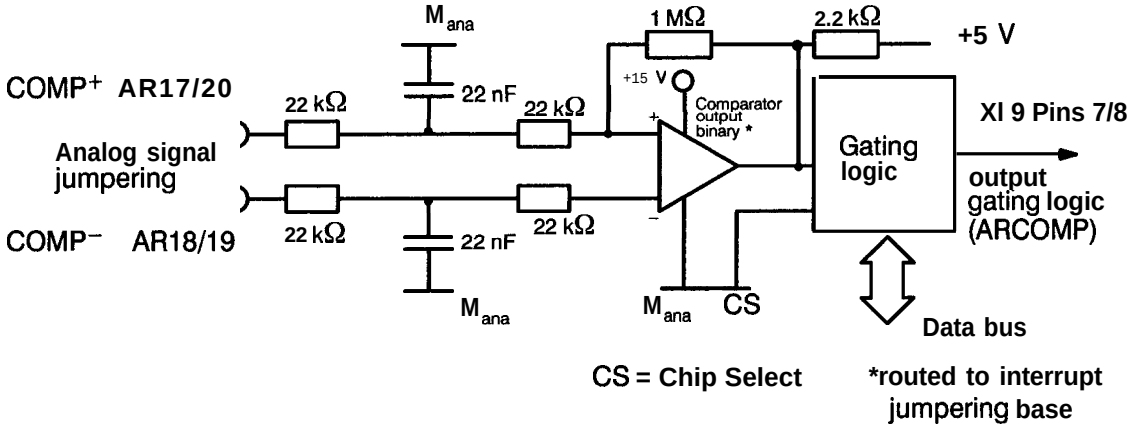
Depending on the application, the comparator inputs can be connected with two signals each that are routed through the soldering base.

Via gating logic, the current comparator status can be read in, and/or an interrupt can be generated.

! Attention: In case of interrupt processing, be aware that a hardware interrupt, fed directly from the module to the bus, can only be processed by the controllers S5–115U/H and S5–135U with CPU 922 or CPU 928A/B. (For interrupt processing with different programmable controllers, see section 4.) !

3.6.2. Input Circuitry

Input circuitry for each comparator

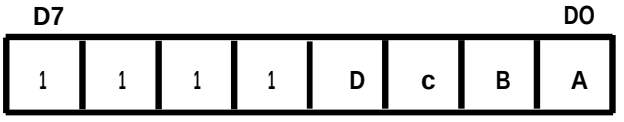


Attention: When comparators are used to compare voltages, the circuit specific, absolute hysteresis of approximately 4.4% of the voltage difference between comparator output (O V/5 V) and input COMP+ (O V to 10 V) must be considered.

3.6.3 Reading the Comparators and the Gating Logic

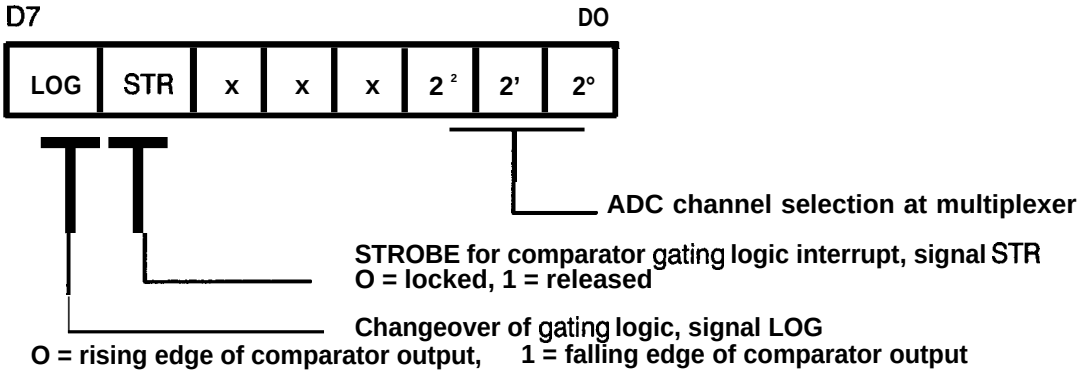
The two comparators are addressed under module address +5. The data bits O to 3 contain information about the current comparator status. The data bits are identified by the characters A, B, C, and D.

Read module address +5



Byte module address +7 not only specifies the analog input channel which is to be converted by the ADC, but also specifies the status of the signals LOG and STROBE. The bit LOG switches the gating logic from rising to falling edge, while STROBE locks or releases an interrupt.

Write to module address +7



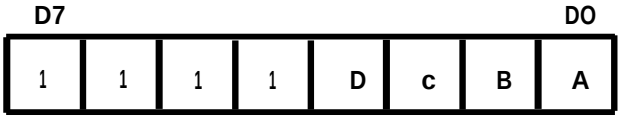
Attention: The default status of the STROBE signal is"1".

Attention: The signals LOG and STROBE must be allocated together for both comparators. Separate addressing is not possible.

3.6.4 Evaluation of the Comparator States

3.6.4.1 Representation of Comparator States

As already mentioned in section 3.6.3., information about current comparator status is read in byte module address +5. In this case, only the bits 2^0, 2^1, 2^2, and 2^3 (now represented by the characters A, B, C, and D) are relevant.



Module address +5

Data bits DO = A and
D1 = B are allocated to comparator 1

Data bits D2 = C and
D3 = D are allocated to comparator 2

The status of the evaluative bits A, B, C, and D of the respective comparator and the pertaining gating logic depends on the input voltage at the comparator (+comparator and –comparator) and the selection of the signal states for LOG and STROBE. The individual possibilities are shown in the table in section 3.6.4.2.

3.6.4.2 Value Table for Comparators 1 and 2

Signals		Input voltage at comparators 1 and 2		Bits		Status	
STROBE	LOG	+ Comp	– Comp	A/C	B/D	Comparator status 1 and 2	Gating logic 1 and 2
1	1	U_1	U*	1	0	0	1
1	1	U*	U_1	1	1	1	0
1	0	U_1	U_2	1	1	0	0
1	0	U_1	U_1	0	1	1	1
0	1	U_1	U_2	1	0	0	0
0	1	U*	U_1	1	1	1	0
0	0	U_1	U_2	1	1	0	0
0	0	U_2	U_1	0	1	1	0

Attention: The input voltages applied at the comparators are identified as U_1 and U_2 in the value table where U_2 is always greater than U_1.

Explanation of signal names:

STROBE: Enable/Inhibit a hardware interrupt in case of exceeding or dropping below the setpoint

O = Interrupt inhibited
1 = Interrupt enabled

LOG: Changeover of the gating logic as a reaction (interrupt) to rising or falling edge (i.e., exceeding or dropping below a setpoint).

O = Rising edge
1 = Falling edge

+ Comp: "+" input of the comparator with the rated input range O V to +1O V;

– Comp: "–" input of the comparator with the rated input range O V to +1O V;

3.6.4.3 Explanation of the Value Table and the Individual Values

Some important deductions can be drawn from the value table presented below. A clear definition of the status of the comparators and gating logic is dependent on the evaluation of "bits" A, B, C, and D. The easiest way to evaluate the "bits" is to apply the conditions necessary to make the status of one "bit" (i.e., either A or B, or C or D) equal to "O".

> **Attention: The text of section 3.6.4.3 applies when STROBE = 1. If STROBE = O, then gating logic 1/2 = O. The comparator outputs comp. 1/2, however, react the same way as when STROBE = 1.**

A becomes O only if:
LOG = O and + comp. > – comp.
– > comp. 1 becomes 1
– > gating logic 1 becomes 1
– > interrupt is possible

B becomes O only if:
LOG = 1 and + comp. < – comp.
– > comp. 1 becomes O
– > gating logic 1 becomes 1
– > interrupt is possible

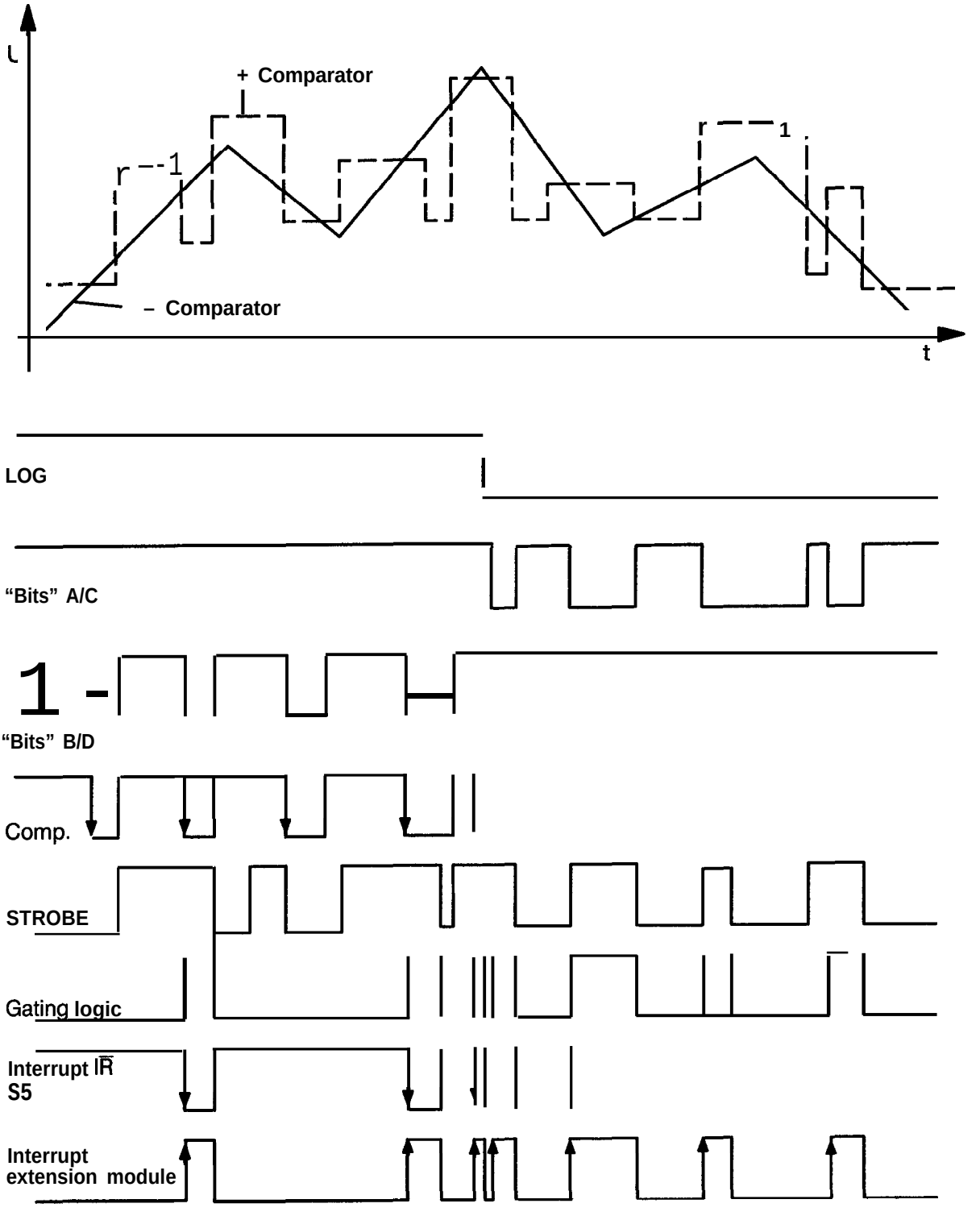
C becomes O only if:
LOG = O and + comp. > – comp.
– > comp. 2 becomes 1
– > gating logic 2 becomes 1
– > interrupt is possible

D becomes O only if:
LOG = 1 and + comp. < – comp.
– > comp. 2 becomes O
– > gating logic 2 becomes 1
– > interrupt is possible

Summarized statements:

– Gating logic 1/2 = 1 if LOG < > comp. 1/2
– Comp. 1/2 = 1 if + comp. > – comp.

3.6.4.4 Representation in the Time/Voltage Diagram



The signals LOG and STROBE were selected randomly for this example.

3.7 Difference Amplifier (P Controller)

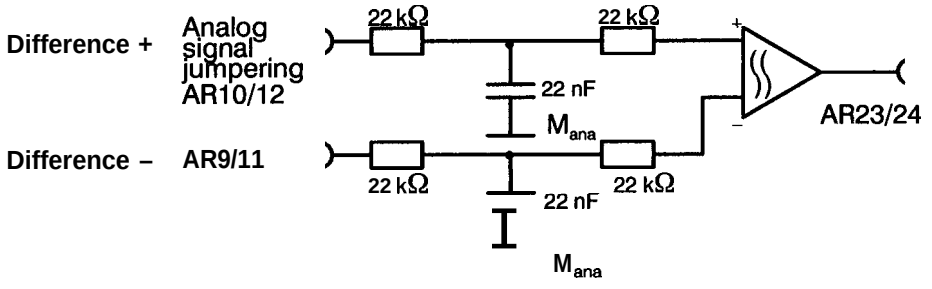
3.7.1 Input Signal Range and Amplification

Voltages in the range from – 10Vto + 10 V can be applied at the input of the two difference amplifiers. The desired amplification is set via the trimming potentiometer. For each of the two P controllers, one trimming potentiometer is available on the module front plate, and amplification factors from 1.1 to 20 can beset. The difference between the input voltages applied at P+ and P– is amplified.

3.7.2 Input Circuitry

Since the two P controllers are built as device amplifiers, both input values have the same polarity.

Input circuitry of the difference amplifiers (for each amplifier)



3.7.3 Circuitry Possibilities and Output Signal Range

The inputs and outputs of the difference amplifiers are routed to the analog jumpering block and can be connected to other analog signals also running to this same soldering base. Amplifier input values, for example, can be signals coming via the channels of the analog value conditioning circuits, or values provided by the digital/analog converters. Again, the respective output of the P controller can be either applied to the digital/analog converter or to the comparators, or it can immediately be used as an analog output. The output signal range of the difference amplifiers is within $\pm$10 V.

4 Interrupt Processing

4.1 General Conditions for Interrupt Processing

This section now covers specific characteristics of interrupt processing in relation to the individual programmable controllers. Interrupt jumpering on the IP 243 is described in section 5.7.

An interrupt can only be triggered by the comparators or the gating logic on the output side. The condition for generating an interrupt is its enable by the signal STROBE. The corresponding parameter assignment is described in section 3.6, as well as a description of the switching of gating logic between rising edge and falling edge (signal LOG).

This makes alarm processing only possible when the IP 243–IAA.. module is fully configured.

4.2 Possibilities for Interrupt Processing

In principle, interrupts can be evaluated in any programmable controller which allows operation with the IP 243. In practice, however, this evaluation depends on the type of controller. Only with the S5–115U/H and S5–135U with CPU 928A/B or with CPU 922, is direct access to the bus with interrupt lines possible. For all other programmable controllers, a separate digital input module with interrupt–generating capability must be used. This module must be externally wired with the binary outputs of the IP 243.

4.3 Direct Bus Access

Direct access to the interrupt lines is only possible for programmable controllers with edge–triggering. This means that the central unit reacts only to edge changes without regard to specific status levels. This applies to allCPUSoftheS5–115U/H series, CPU 922 and the 928A/B CPUS of the S5–135U series. If interrupts are triggered via direct bus access, the memory latch D9 may not be exchanged for the soldering base D9, included with delivery.

4.3.1 Interrupt Processing in the S5-115U/H

In the S5-115U with CPU 941A, interrupt lines $\overline{IRA}$ and $\overline{IRB}$ are available for CPU 941B, 942-7UH.... From CPU 942A/B on, the four interrupt lines $\overline{IRA}$, $\overline{IRB}$, $\overline{IRC}$, and $\overline{IRD}$ on, which interrupts can be initiated, are available. The two pins $\overline{IRF}$ and $\overline{IRG}$ on the interrupt-jumpering block X19 may not be used; they must always be grounded on M (pin 6). The same applies to $\overline{IRC}$ and $\overline{IRD}$ when CPU 941A is installed. Furthermore, all process interrupts which are not used must be connected to grounding M. An organization block is allocated to each interrupt in the S5-1 15U. The organization block must be programmed for interrupt evaluation. The following relations apply:

Interrupt $\overline{IRA}$ - OB 2
Interrupt $\overline{IRB}$ - OB 3
Interrupt $\overline{IRC}$ - OB 4
Interrupt $\overline{IRD}$ - OB 5

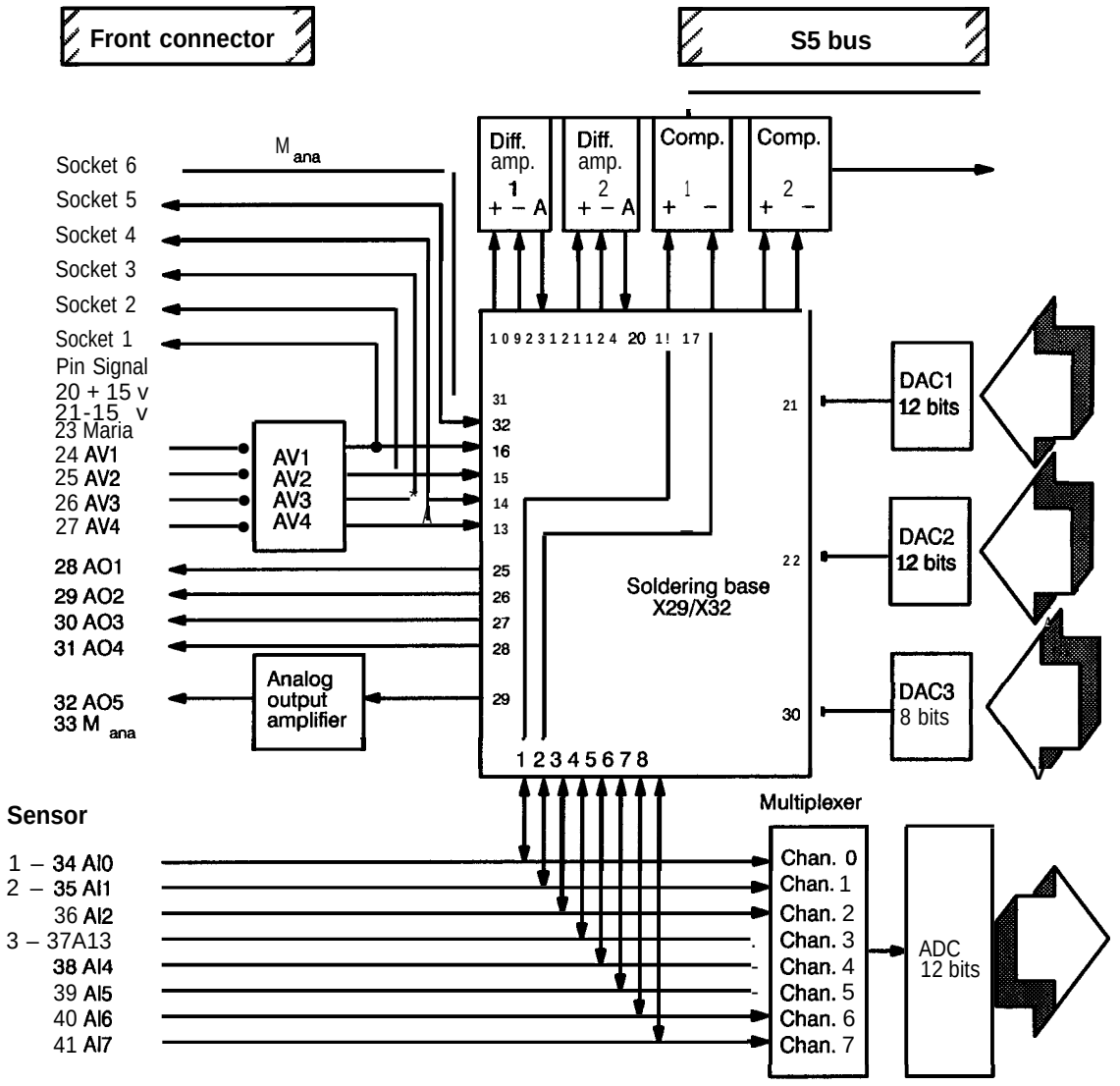
Each interrupt line should be allocated to only one interrupt-generating IP 243. In the case of several accessing modules, it would require considerable software effort to determine which IP 243 triggered an interrupt (no evaluation possible via peripheral byte 0!).

Attention: Interrupt requests can be processed only in the central unit. The interrup program structure and interrupt-OB handling are found in the S5-115U manual or the S5-115H manual.
Exception:
Alarm processing in the expansion device is possible with EG 701 -3 (from release 6ES5 701-31A13) or EG 186U, when ligth wave conductor interfaces 6ES5307-3UA1 1 and 6ES5 317-3UA11 are used.

Example:

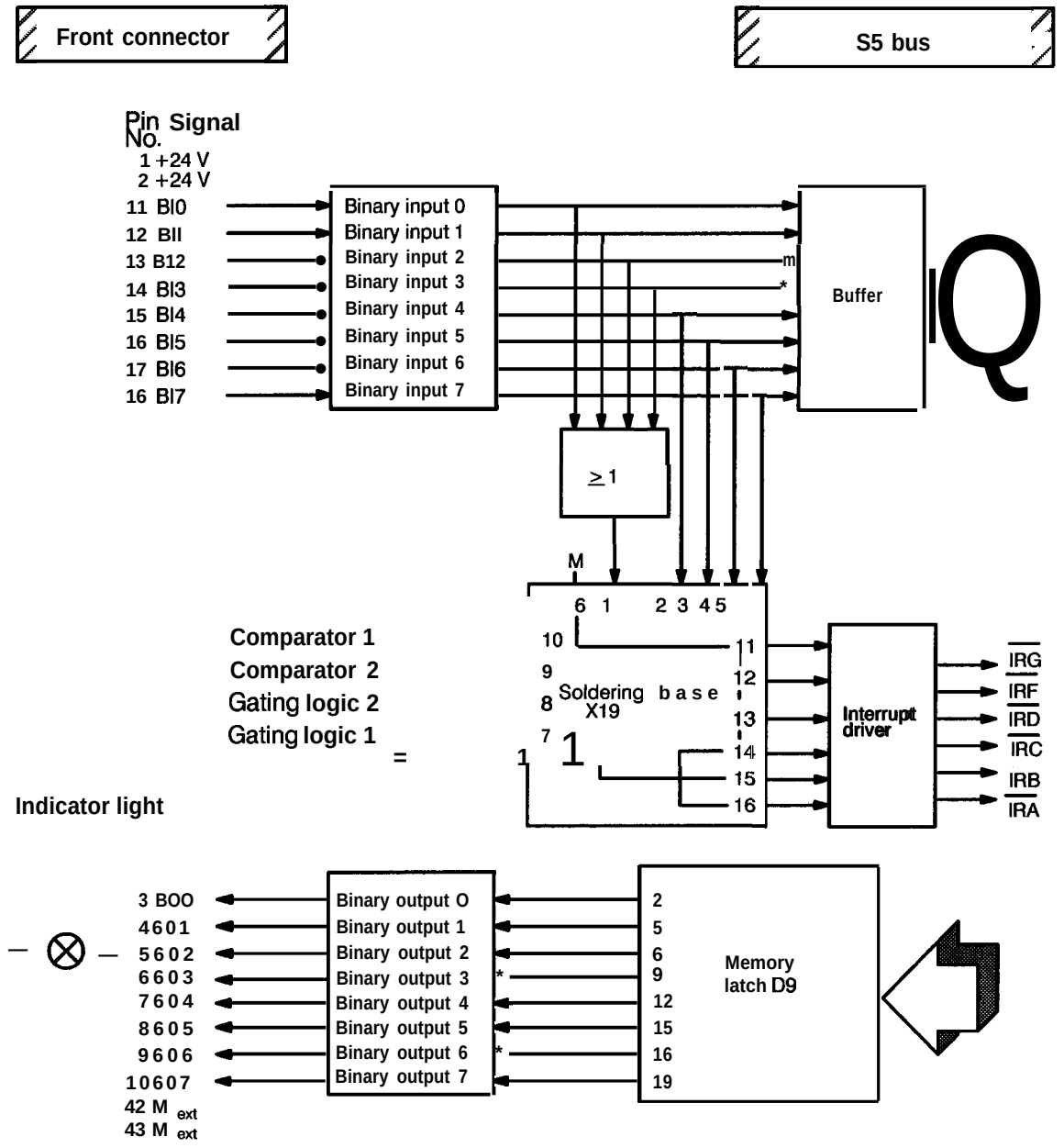
The two analog input channels AIO and All are compared with each other by comparator 1 (AI0 to +Comp. and All to -Comp.). As soon as All exceeds the value of AIO, this is indicated by a signal light connected to the binary output B02 of the IP 243. At the same time channel A13 is read in once in the interrupt program. The module starting address is given as 144, and interrupt line $\overline{IRB}$ is selected. Only in the case of parameterization for falling edge can a reasonable evaluation of the interrupt request be made.

The required solder connections on the jumpering block for analog signals are:



Diff. amp.	=	Difference amplifier
Comp.	=	Comparator
Chan.	=	Channel

The pins of the binary signal/interrupt jumpering are connected as follows:



The Step 5 program can have the following structure:

OB 1

```
NETWORK 1       0000          OB 1 for S5–115U
0000        :
0001        :L KM 1 1XXXXXX   Enable Interrupt ("STROBE"=1) and
0003        :T PY 151         Reaction to falling edge
0004        :                 ("LOG"=1)
0005        :
0006        :BE
```

OB 3

```
NETWORK 1       0000          Interrupt OB forS5–115U
0000        :JU FB X          Save scratchpad flag
0001 NAME   :SAVE
0002        :
0003        :L  PY 149        Load comparator states
0004        :T  FB 100
0005        :AN F 100.1       Evaluate parameter bit "B"
0006        :=  F 102.2       Set flag for output
0007        :A  F 102.2
0008        :JC FB Z          Interrupt reaction (S5–11 5U)
0009 NAME   :INTERRUPT
000A        :
000B        :JU FB Y          Load scratchpad flag
000C NAME   :LOAD
000D        :BE
```

FB Z

```
NETWORK 1       0000
NAME :INTERRUPT               Interrupt reaction (S5–1 15U)

0005        :L  FY 102
0006        :T  PY 149        Write binary outputs
0007        :L  KM 1 1XXX011  Read in A13
0009        :T  PY 151        Select ADC
000A        :T  PY 150        Convert ADC
000B        :L  Pw 150        Read ADC
000C        :T  FW 104        Store value
000D        :BE
```

> Attention: Save the scratchpad flag bytransferring itto a data block. Atthe **end, the scratchpad flag must be read into the interrupt processing. The flag bytes FY** 200 **to FY** 255 are **defined as scratchpad flags.**

4.3.2 Interrupt Processing in the S5–135U with CPU 922 or CPU 928A/B

In the multiprocessor system S5–135U, the four interrupt lines $\overline{IRA}$, $\overline{IRB}$, $\overline{IRC}$, and $\overline{IRD}$ are allocated to one CPU slot per tine:

CPU 1 – Interrupt $\overline{IRA}$
CPU 2 – Interrupt $\overline{IRB}$
CPU 3 – Interrupt $\overline{IRC}$
CPU 4 – Interrupt $\overline{IRD}$

An interrupt organization block OB 2 can be filed in each of the central modules.

Attention: The presetting of data block DX O for "edge-triggered interrupt processing" is mandatory to work with direct hardware interrupts. In the S5–135U, interrupt processing is also only possible in the central rack.

Exception:
Alarm processing in the expansion device is possible with EG 701–3 (from release 6ES5 701–3M13) or EG 186U, when ligth wave conductor interfaces 6ES5307–3UA1 1 and 6ES5317–3UA11 are used.

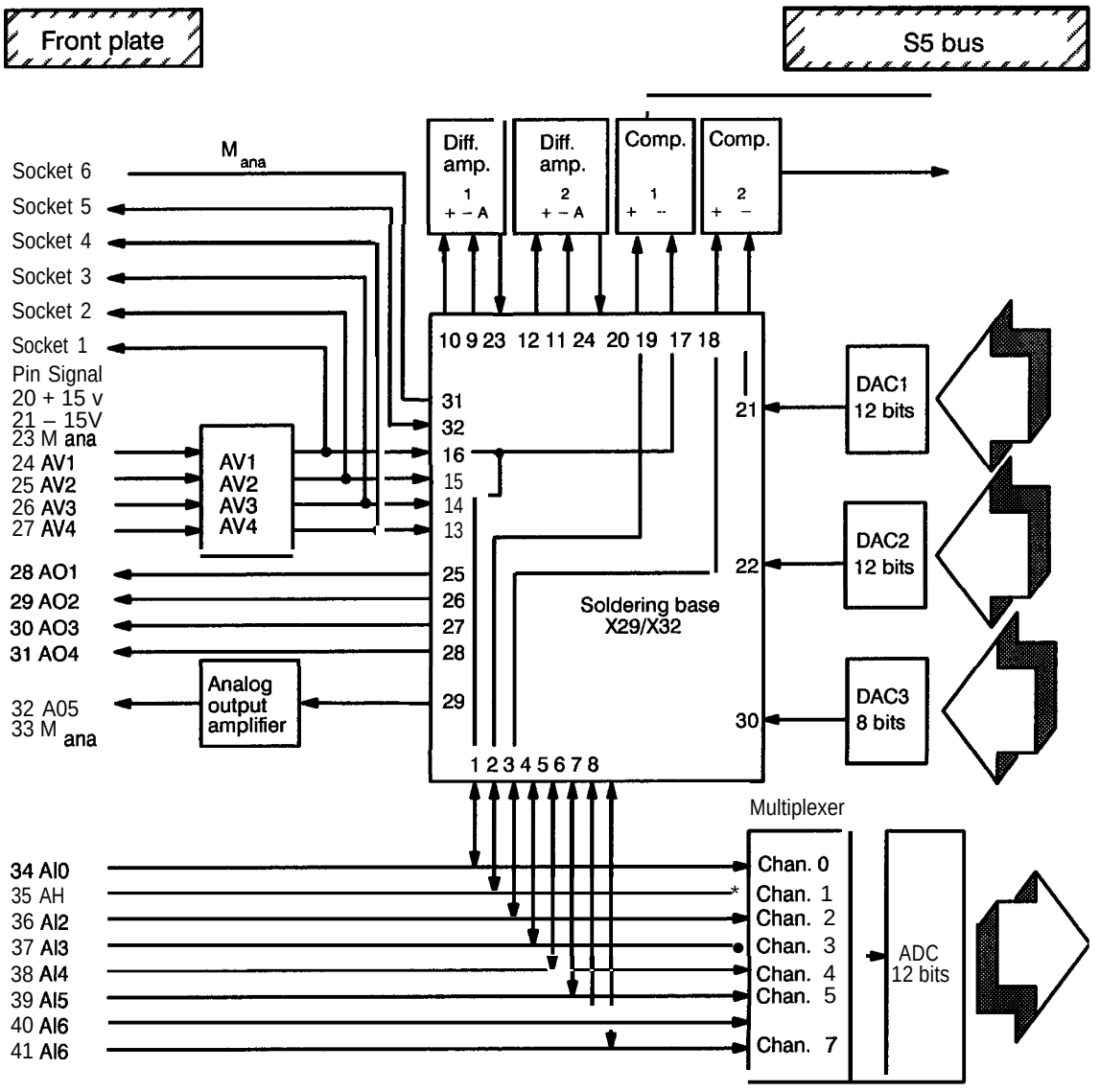
Only one IP 243 should access an interrupt line. Otherwise, no evaluation or only limited evaluation is possible (see also section 4.3.1).

See the appropriate equipment manual for a description of interrupt handling in the S5–135U with CPU 922 or CPU 928A/B.

Example :

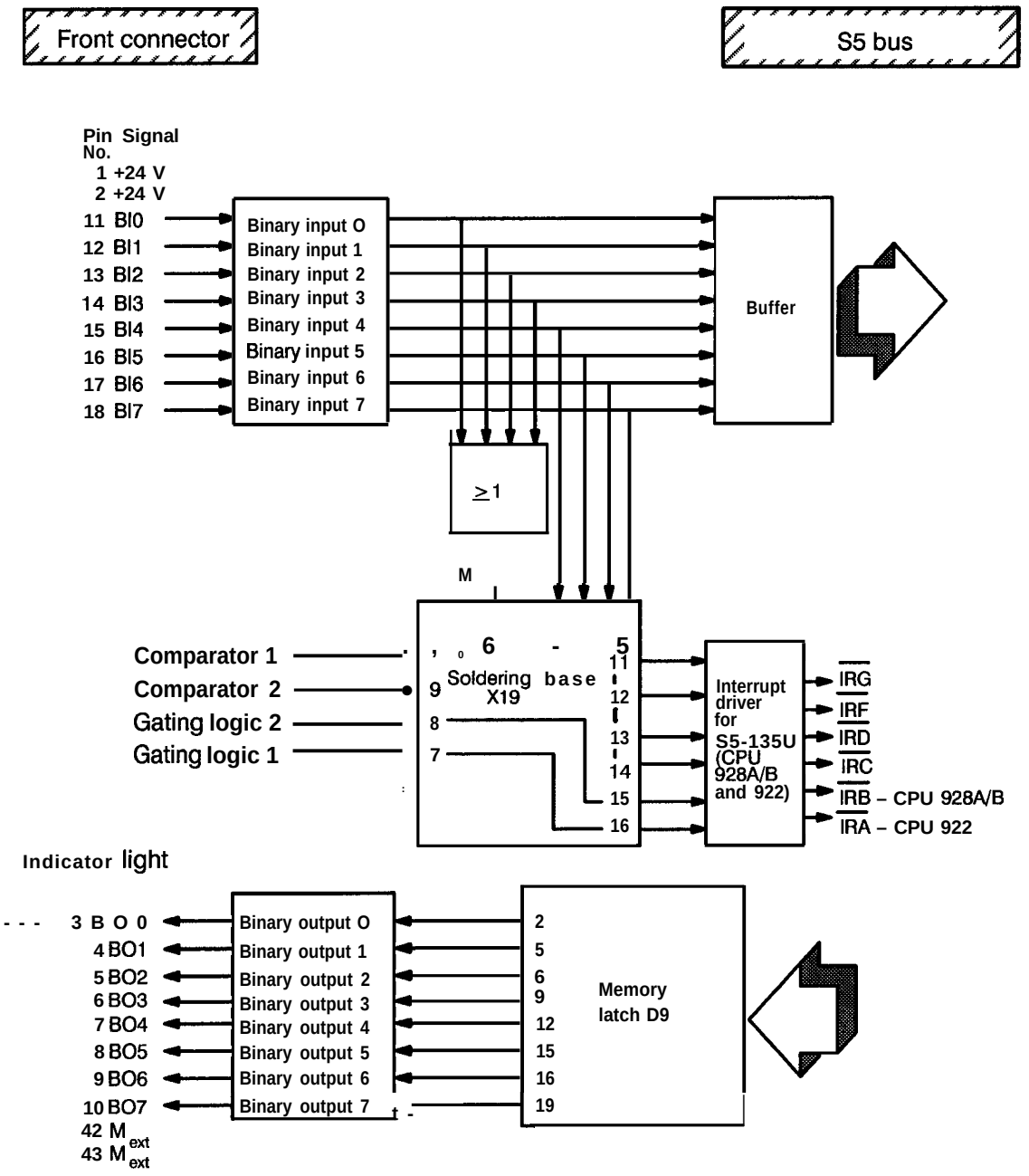
The S5–135U is operated with two central processors, (i.e., a CPU 922 and a CPU 928A/B). Comparator 1 of the IP 243 compares the two values AV1 and All (All to +comp., AV1 to −comp.). The +comp. of comparator 2 is connected with A12 which is compared with a user–specified value (KF = +5000). As soon as the two analog input channel values exceed the correlated "setpoints", an interrupt is generated. In case of an interrupt from gating logic 1, AV1 is read in at the ADC of CPU 922 and a check is made to see if the value exceeds KF = + 3000. If so, an output is set. If gating logic 2 reports an interrupt, the binary inputs BI3 to BI5 of the IP 243 are read into CPU 928A/B. As soon as one of the inputs has the signal"1", the output byte 4 is overwritten with $00FF_H$. The module starting address is given as 128, the parameter setting on rising edge.

Analog signal jumpering:



Diff. amp. = Difference amplifier
Comp. = Comparator
Chan. = Channel

Binary signal/interrupt jumpering:



At first, the DX O for the CPU 928A/B and the CPU 922 must be parameterized for edge–triggered interrupt processing. The DX O for the two central processors is as follows:

DX 0
```
O : KH = 4D41 >
1 : KH = 534B > Start identification
2 : KH = 5830 >
3 : KH = 0601 Block identification/length
4 : KH = 2001 Edge–triggered interrupt processing
5 : KH = EEEE End identification
```

The user programs for the CPU 922 and for the CPU 928A/B can look like this:

OB 1

```
NETWORK 1      0000                    OB 1 for CPU 922
0000      :
0001      :L   KM OIXXXXXX             Enable interrupt ("STROBE" = 1) and
0003      :T   PY 135                  Reaction to rising edge
0004      :                            ("LOG" = O)
0005      :
0006      :BE
```

OB 2

```
NETWORK 1      0000                    Interrupt OB for CPU 922
0000      :JU  FB  X                   Save scratchpad flag
0001 NAME :SAVE
0002      :
0003      :L   PY 133                  Load comparator states
0004      :T   FY 50
0005      :AN  F  50.0                 Evaluate parameter bit "A"
0006      :JC  FB  Z1                  Interrupt reaction (CPU 922)
0007 NAME :INTERRUPT 922
0008      :
0009      :JC  FB  Y                   Load scratchpad flag
000A NAME :LOAD
000B      :BE
```

FB Z1

```
NETWORK 1        0000                    Interrupt reaction (CPU 922)
NAME :INTERRUPT 922

0005        :L   KM OIXXXOO1             Read in All
0007        :T   PY 135                  Select ADC
0008        :T   PY 134                  Convert ADC
0009        :L   Pw 134                  Read ADC
000A        :L   KF +3000                Load KF = +3000
000C        :>F                          Compare for excess value
000D        :=   Q 12.0                  Set output
000E        :BE
```

OB 1

```
NETWORK 1        0000                    OB 1 for CPU 928A/B
0000        :
0001        :L   KM 01XXXXXX             Enable interrupt ("STROBE"=1) and
0003        :T   PY 135                  Reaction to rising edge
0004        :                            ("LOG"=1)
0005        :L   KF +4000                Load KF = +4000
0007        :T   PW 128                  Write DAC1
0008        :BE
```

OB 2

```
NETWORK 1        0000                    Interrupt OB for CPU 928A/B
0000        :JU  FB  X                   Save scratchpad flag
0001 NAME :SAVE
0002        :
0003        :L   PY 133                  Load comparator states
0004        :T   FY 60
0005        :AN  F 60,2                  Evaluate parameter bit "C"
0006        :JC  FB Z2                   Interrupt reaction (CPU 928A/B)
0007 NAME :INTERRUPT 928A/B
0008        :
0009        :JU  FB Y                    Load scratchpad flag
000A NAME :LOAD
000B        :BE
```

FB Z2

```
NETWORK 1        0000
NAME :INTERRUPT 928A/B          Interrupt reaction (CPU 928A/B)

0005    :L   PY 132             Read binary inputs
0006    :T   FY 65
0007    :O   F  65.3            Evaluate B13, B14, BI5
0008    :O   F  65.4
0009    :O   F  65.5
000A    :=   F  66.0
000B    :AN  F  66.0
000C    :BEB
000D    :L   KH OOFF            Load KH=OOFF
000F    :T   QB 12              Overwrite QB 12
0010    :BE
```

For the saving and loading of scratchpad flags, the system organization blocks OB 190 to OB 193 **in the CPU 922 and CPU 928A/B of the S5-135U can be used.**

4.4 Separate Interrupt Input Module

If a programmable controller is designed for fundamental mode operation (level–triggered mode), i.e., the CPU only reacts when a certain level is active on the interrupt lines, or if a control without interrupt lines on the S5 bus is involved, interrupts can only be evaluated by means of a separate binary input module with process interrupt generation. The CPUs of systems S5–135U (CPU 922 and CPU 928A/B when parameterized accordingly) and S5–155U/H oPerate in level–triggered mode. For devices without interrupt lines, the interrupt scan is made via the input byte O. This applies to the S5–150S and S5–150U controllers. If interrupt processing is desired for one of the aforementioned systems, replace the memory latch D9 on the IP 243 with the soldering base D9, included with delivery. In addition an interrupt module is required.

Attention: If the memory latch D9 is replaced with the soldering base D9, intermediate storage at the binary outputs BO0 to BO7 is no longer possible and their use no longer sensible.

4.4.1 Interrupt Processing in the S5–135U

In the S5–135U programmable controller, both CPU 922 and CPU 928A/B operate in level–triggered mode. The CPUs, however, can also be parameterized for edge–triggered processing.

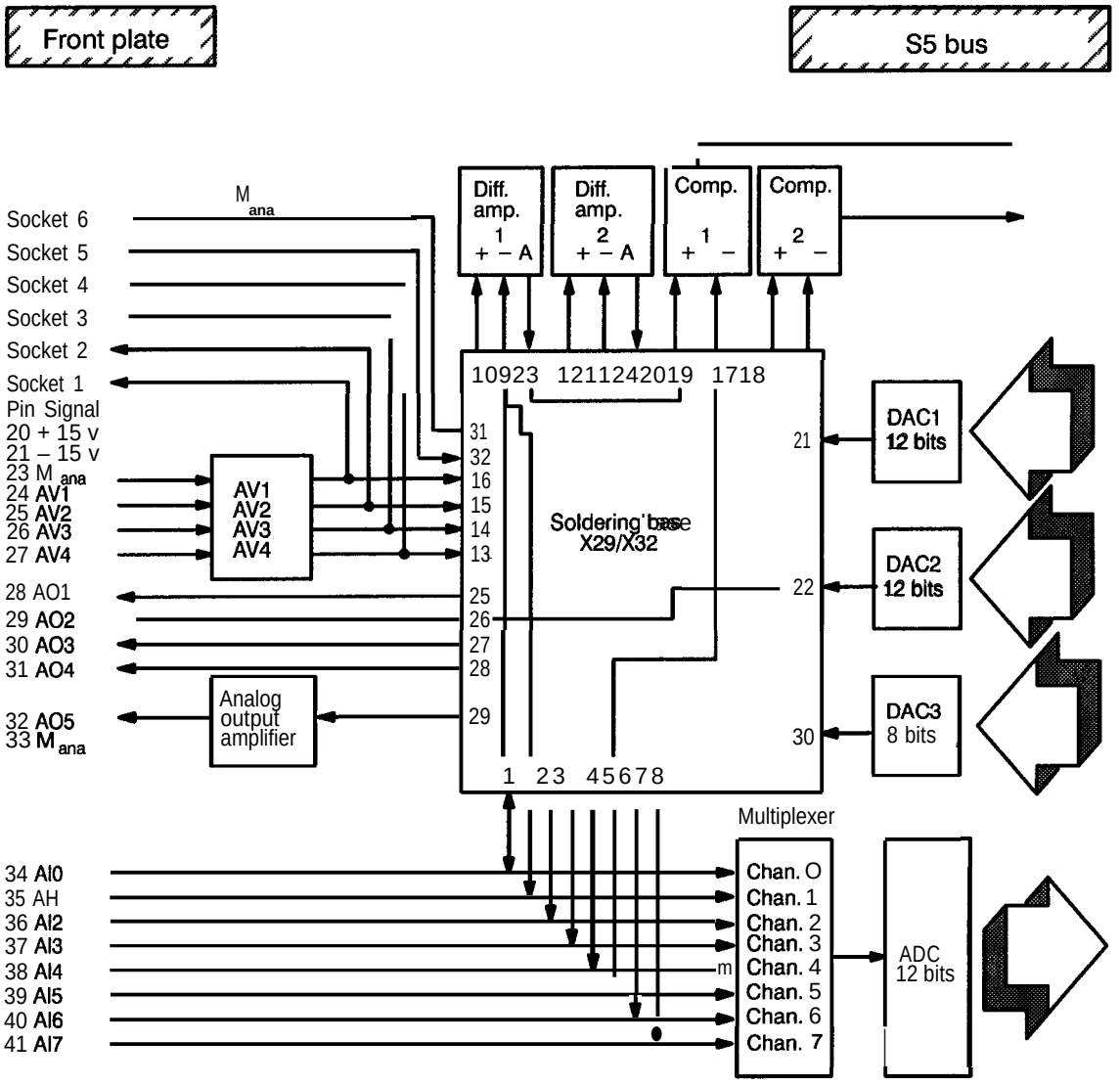
In case of level–triggered operation, the digital input module6ES5432–4UA11 must be additionally inserted. On the IP 243 module, the comparator outputs and the interrupt–generating outputs of the gating logic must be jumper–connected to the soldering base D9, which in turn is connected with the binary outputs of the IP 243. Furthermore, the jumper connections on the soldering base X19 (pins 11, 12, 13, 14, 15 and 16 connected to grounding M, pin 6) may not be changed from their original delivery condition. Then the binary outputs are externally connected to the inputs of the interrupt module. The interrupt triggering is handled exclusively by the module 6ES5432-4UA1 1. A description is found in the appropriate equipment manual.

Attention: When working with a separate interrupt input module, the IP 243 can operate from any IP slot, whether in the central unit or in anexpan– sion unit. The interrupt module 6ES5432–4UA1 1, however, must always be inserted in the central unit.

Several interrupts from one IP 243 or from different IPs 243 can be routed to a digital module with the capability of process interrupt generation.

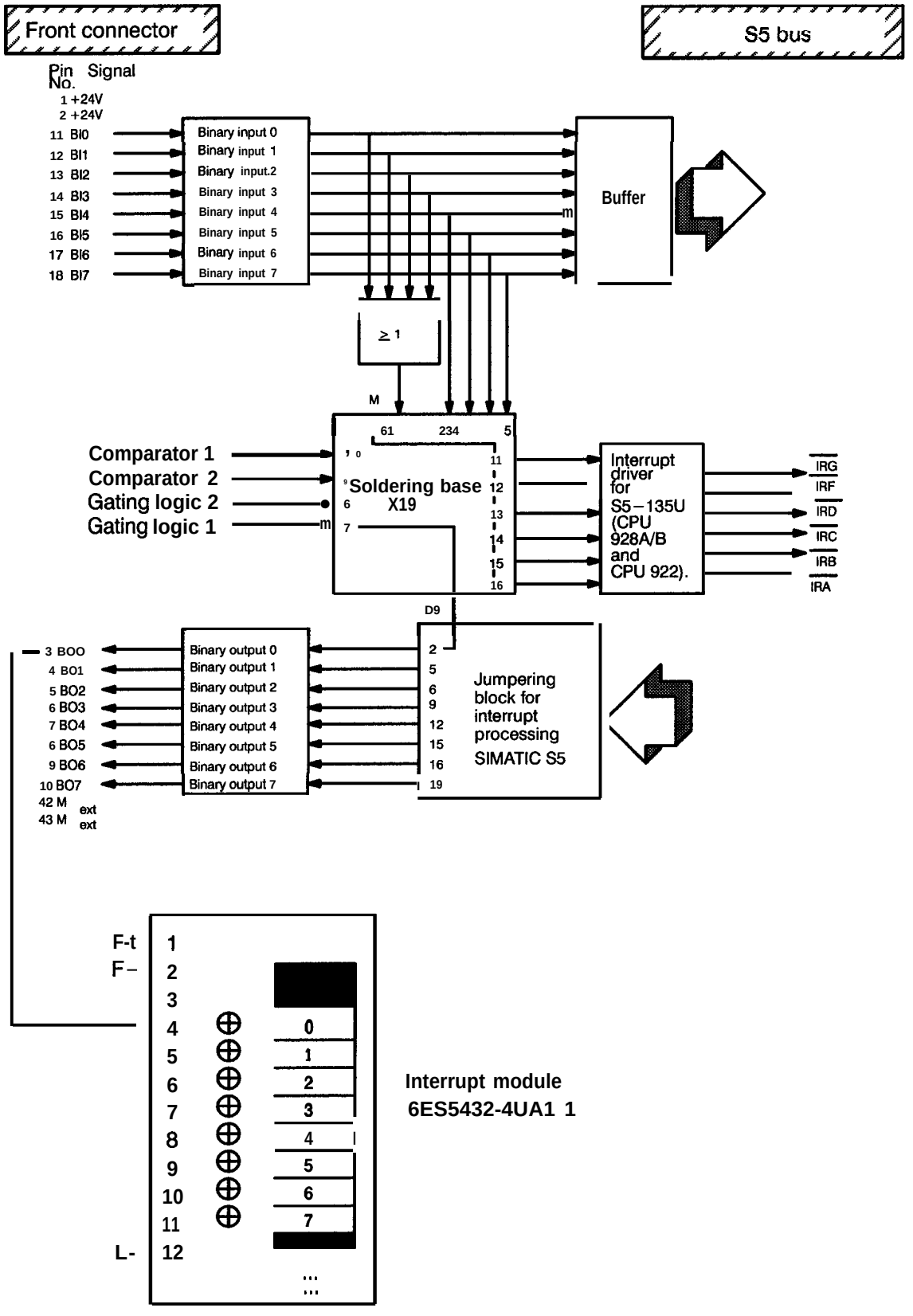
Example:
In the S5–135U with CPU 922the two analog input values AIOand All are applied to the difference amplifier. The amplifier output runs to +comp. and is compared with –comp. which is connected to the input AI6. If the value at the AI6 channel exceeds the output voltage at the difference amplifier, an interrupt is generated and a value which was previously filed in FW 120 is output at A02 via DAC2. The module address is given as 160; parameterization is for falling edge.

Analog signal jumpering:



Diff. amp. = Difference amplifier
Comp. = Comparator
Chan. = Channel

Binary signal interrupt jumpering:



On the interrupt module6ES5432-4UA1 1 various presetting are required. For the relevant input in this case the setting “rising edge” was selected. The module address is given as 128. For a more detailed description of interrupt procedures, see the appropriate equipment manual. Simplified user program for scanning the interrupt inputs:

OB 1

```
NETWORK 1        0000          OB 1 for CPU 921
0000         :
0001         :L    KM 1 1XXXXXX   Enable interrupt (“STROBE” = 1) and
0003         :T    PY167          Reaction to falling edge
0004         :                    (“LOG” = 1)
0005         :
0006         :BE
```

OB 2

```
NETWORK 1        0000          Interrupt OB for CPU 921
0000         :JU   FB  X         Save scratchpad flag
0001 NAME    :SAVE
0002         :
0003         :L    PW 128        Read in interrupt module
0004         :T    FW 114
0005         :L    Pw 130        Read in interrupt module
0006         :T    FW 116
0007         :L    PY 165        Load comparator states
0008         :T    FW 110
0009         :AN   F  110.1      Evaluate parameter bit “B”
000A         :A    F  114.0      Evaluate interrupt input
000B         :JC FB  Z           Interrupt reaction (CPU 922)
000C NAME    :INTERRUPT 922
000D         :
000E         :JU   FB  Y         Load scratchpad flags
000F NAME    :LOAD
0010         :BE
```

FB Z

```
NETWORK 1
NAME :INTERRUPT 922              Interrupt reaction (CPU 922)

0005         :L    FW 120        Write DAC2
0006         :T    PW 162
0007         :BE
```

In addition, system organization blocks OB 190 to OB 193 are available in CPUS 922 and 928A/B for saving and loading the scratchpad flags.

4.4.2 Interrupt Processing in the S5–150U/S

The systems S5–150U/S have no interrupt lines. In this case an interrupt signal is only possible via evaluation of the peripheral byte O. For details of this procedure seethe appropriate equipment manual.

An interrupt OB is allocated to each bit of the input byte O, as follows:

10.0 – OB 2
10.1 – OB3
10.2 – OB 4
10.3 – OB 5
10.4 – OB 6
10.5 – OB 7
10.6 – OB 8
10.7 – OB 9

In case of a signal change for a bit of IBO, a branch to the correlated interrupt block takes place. Generally an interrupt module is used for interrupt generating (for theS5–150U this is the module 6ES5432–4UA1 1, and for the S5–150S it is the module6ES5432–3BA11). See the appropriate equipment manual for specifications and operation.

On the IP 243 itself, the memory latch D9 must be replaced by the soldering base D9. The interrupt–generating outputs of the gating logic are connected with the binary outputs BOO to B07 via the soldering base D9. Then the outputs are externally connected with the inputs of a binary input. The solder connections on soldering base Xl 9 remain in their original delivery state (all interrupt lines to grounding M).

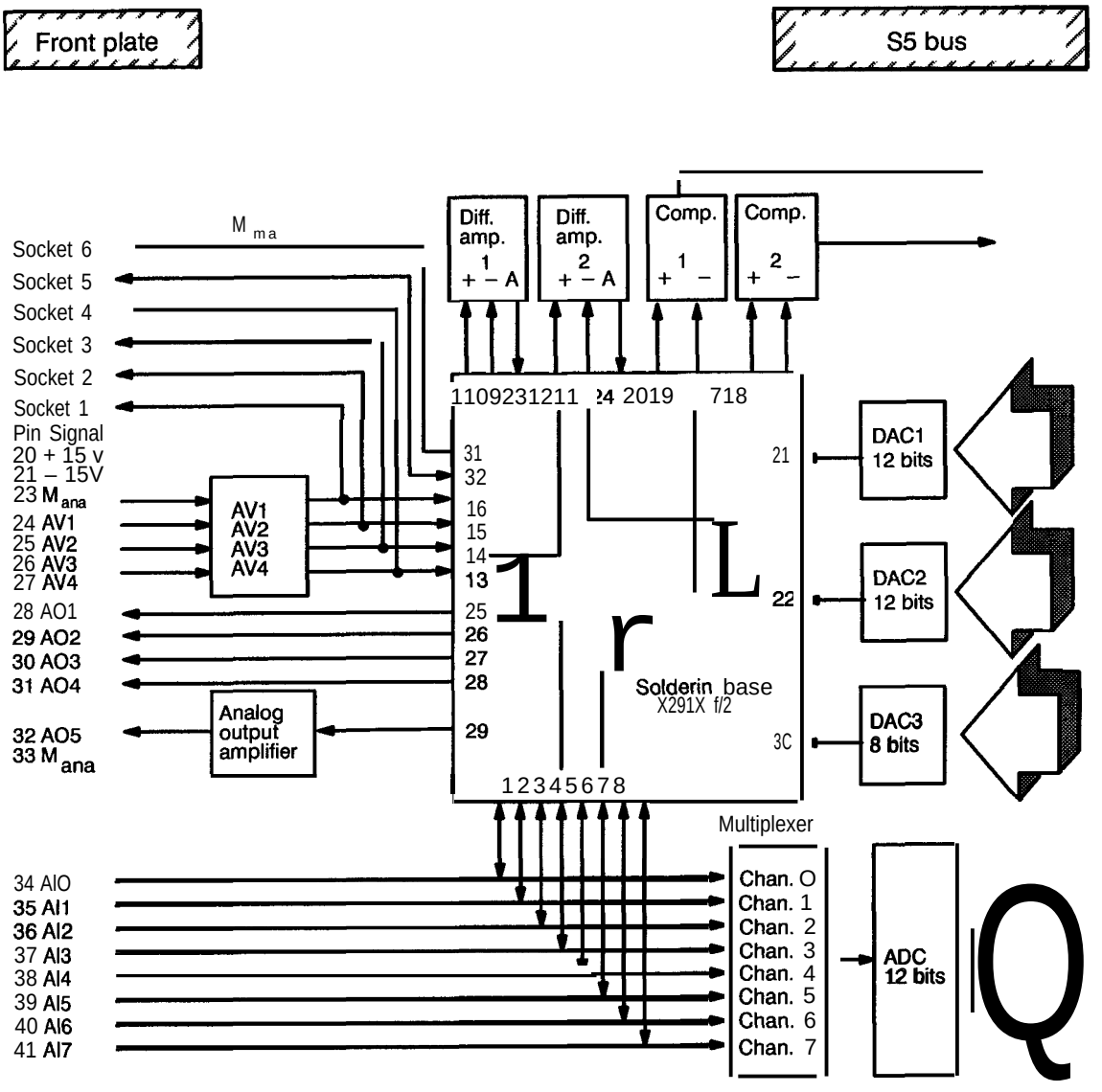
> **Attention:** With the systems S5–150U/S, interrupt processing is only possible in an expansion rack. The same applies to the use of IPs.

All interrupt–generating modules must be located in the same expansion rack.

Example:

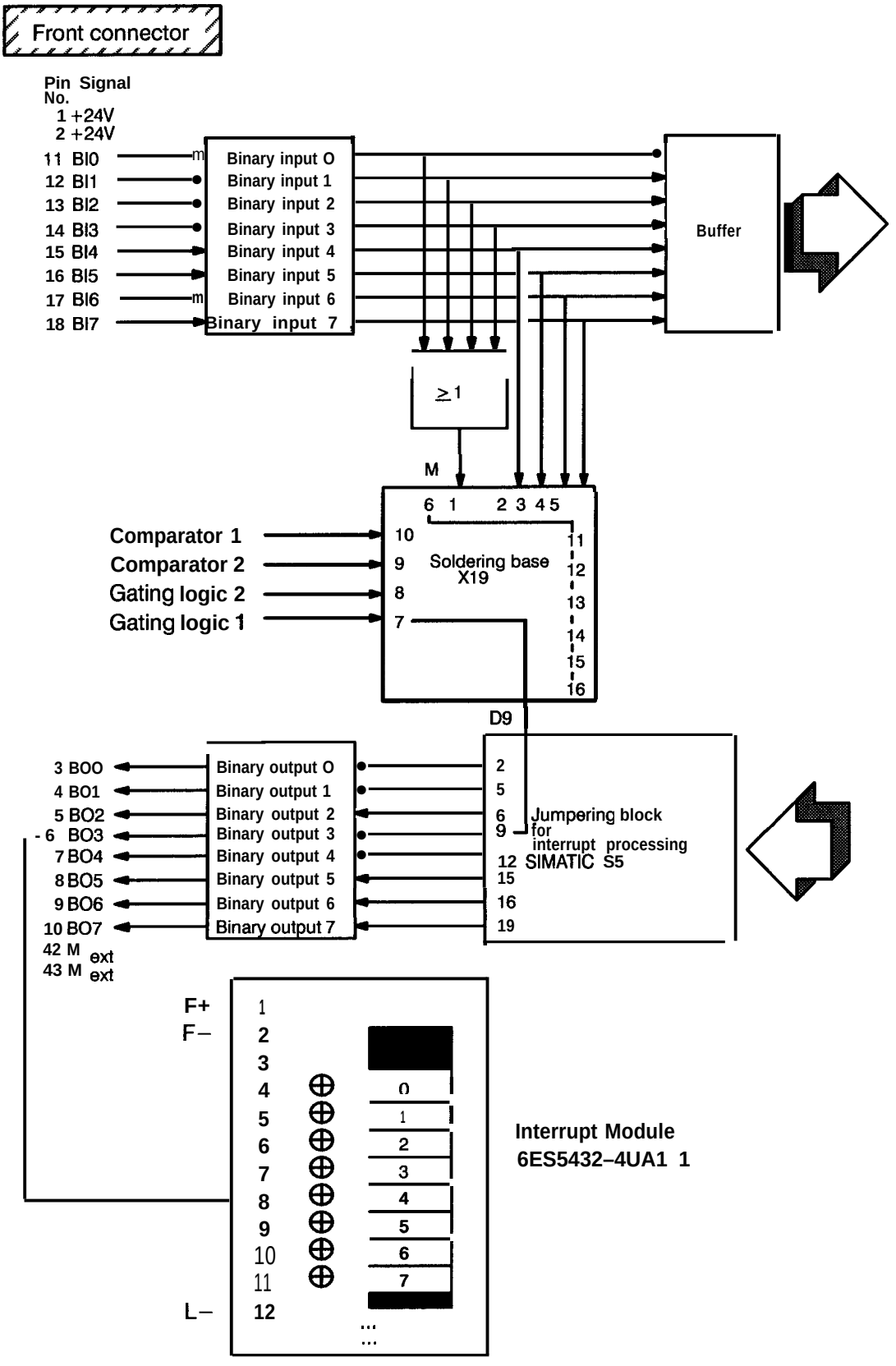
In theS5–150U an IP 243 is operated under the following conditions:
A value stored in FW 78 is output on DAC2 and stored on the difference amplifier. Difference + is connected with AV3. The amplifier output value is compared with the analog input channel AI5 at comparator 1, whereby AI5 is also read in on ADC. If AI5 is less than the value of the signal at +comp, AI2 is first converted three times, then AV4 twice on the ADC. The module address is given as 240; parameterization is for rising edge.A6ES5432-4UA11 interrupt module is used and parameterized accordingly.

Analog signal jumpering:



Diff. amp. = Difference amplifier
Comp. = Comparator
Chan. = Channel

Binary signal/interrupt jumpering:



User Program

OB 1

```
NETWORK 1        0000          OB 1 for S5-150U/S
0000         :
0001         :L    KM O1XXX1O1  Enable interrupt ("STROBE"= 1) and
0003         :T    PY 247       Reaction to rising edge
0004         :                  ("LOG' '= O); selection of channel A15
0005         :T    PY 246       Convert ADC
0006         :L    PW 246       Read ADC
0007         :     FW 90        Store converted value
0008         :
0009         :L    FW 78        Load value to be converted
000A         :T    PY 242       Write DAC2
000B         :
000C         :BE
```

OB 6

```
NETWORK 1        0000          Interrupt OB for S5- 150U/S
0000         :JU   FB  X        Save scratchpad flag
0001 NAME    :SAVE
0002         :
0003         :L    PY 245       Load comparator states
0004         :T    FY 120
0005         :AN   F  120.0     Evaluate parameter bit "A"
0006         :JC   FB  Z        Interrupt reaction (S5–150U)
0007 NAME    :INTERRUPT 150
0008         :
0009         :JU   FBY          Load scratchpad flag
000A NAME    :LOAD
000B         :BE
```

FB Z

```
NETWORK 1        0000
NAME :INTERRUPT 150          Interrupt reaction S5–1 50U/S

0005    :L   KM O1XXXO1O     Select channel AI2 at the ADC
0007    :T   PY 247
0008    :T   PY 246          Convert AI2
0009    :L   PW 246          Read AI2
000A    :T   FW 70           Store converted value
000B    :T   PY 246          Convert AI2
000C    :L   PW 246          Read AI2
000D    :T   FW 72           Store converted value
000E    :T   PY 246          Convert AI2
000F    :L   PW 246          Read AI2
0010    :T   FW 74           Store converted value
0011    :L   KM 01)()()(011  Select channel 3 (AV4) at the ADC
0013    :T   PY 247
0014    :T   PY 246          Convert AI3
0015    :L   PW 246          Read AI3
0016    :T   FW 76           Store converted value
0017    :T   PY 246          Convert AI3
0018    :L   PW 246          Read AI3
0019    :T   FW 78           Store converted value
OOIA    :BE
```

4.4.3 Interrupt Processing in the S5–155U/H

With the S5–155U, the evaluation of interrupts is accomplished the same way as with the S5–150U/S (i.e., by scanning the input byte O [S5–150U mode]). The S5–155U system offers the additional possibility of interrupt requests via interrupt lines, but it cannot be put to use directly in connection with the IP 243, as the hardware interrupts operate in level–triggered mode.

Proceed as described in section 4.3.2 when using a CPU 922 or a CPU 928A/B (edge–triggered) in PLC S5–155U.

Indirect operation via the interrupt lines is possible, if the parameters in DX O were assigned accordingly. This is only possible with an interrupt–capable, digital–input module to which the desired IP 243 signals are routed externally. The blocks OB 2 to OB 5 are defined as interrupt blocks (S5-150U/S mode).

If interrupt evaluation in this manner is desired, see the S5–155U or S5–155H equipment manual.

The evaluation of the input byte O is accomplished in the same way as in the S5–150U/S systems; for each bit of input byte O, an interrupt OB is allocated where the respective interrupt reaction is filed.

A process interrupt is always initiated by a binary input (e.g., from the interrupt module 6ES5 432–4UA11. Again, this input is set by one of the binary outputs of the IP 243. On the IP 243, the memory latch D9 must be exchanged for the soldering base D9 (included with delivery), which serves as a connecting link between the binary signal/interrupt jumpering and the binary outputs.

The jumpers between the interrupt–line pins and the grounding contact M may not be altered from their factory-delivered condition.

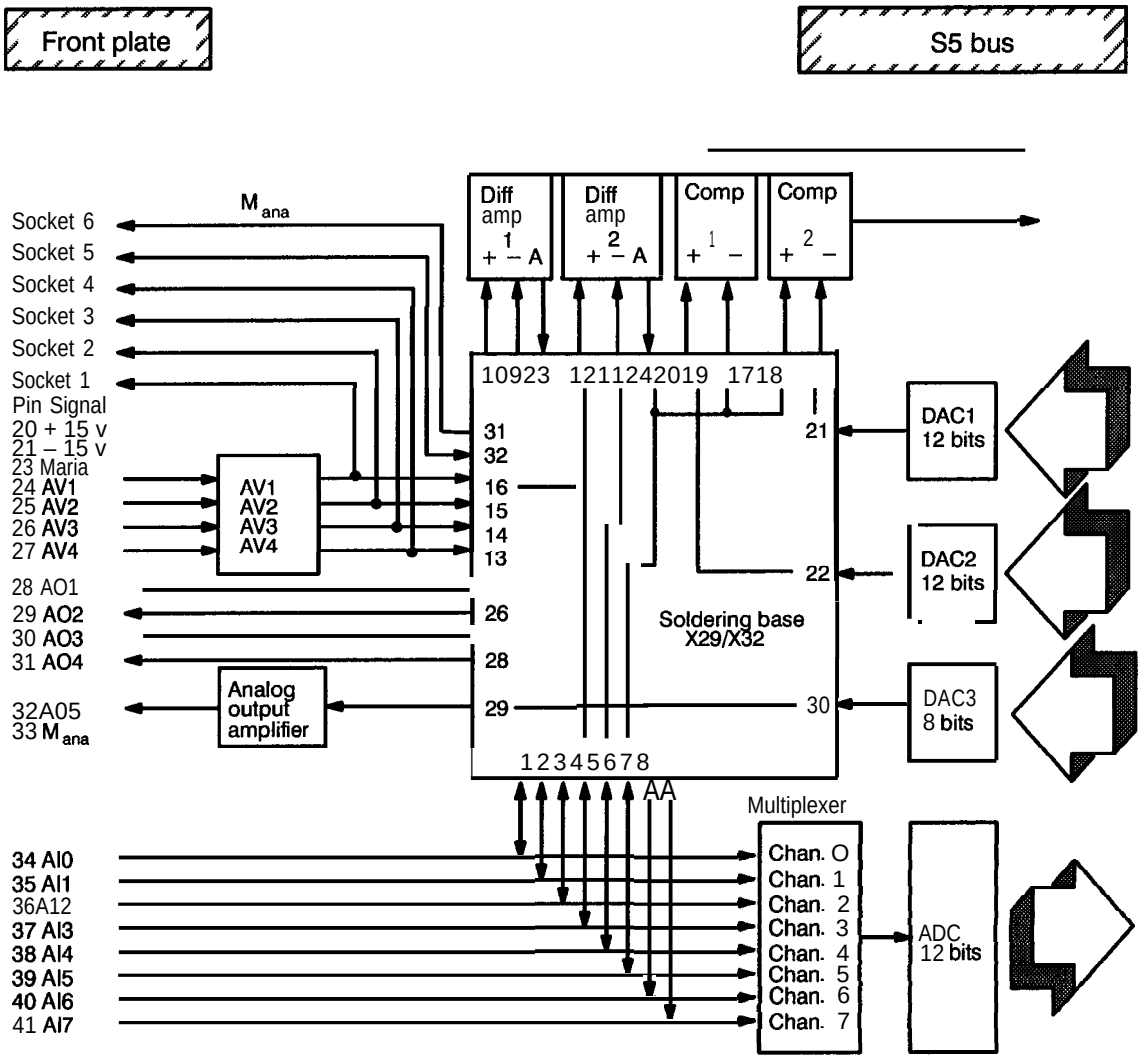
Attention: Operation of the IP 243 and of the interrupt module 432-4 is possible in the central or expansion rack. The IP 243 and the interrupt module can also be located in different module racks.

Example:

In the S5–155U system, the difference amplifier 2 of an IP 243 is connected to a conditioned analog value AV1 and to the analog input channel A15. The output of the difference amplifier is checked for exceeding or dropping below certain values. If the output exceeds a value furnished by DAC2, previously filed in FW 190, then the output of the difference amplifier and the input channel AV1 are read in at the ADC and stored in the flag area. Depending on the signal status of the binary input B12, either KF = +800 (status “O”) or KF = +1000 (status “I”) is active at DAC1. If the respective value drops too low, a voltage of 5.85 V is output at DAC3. The module address is given as 176; parameterization is for falling edge.

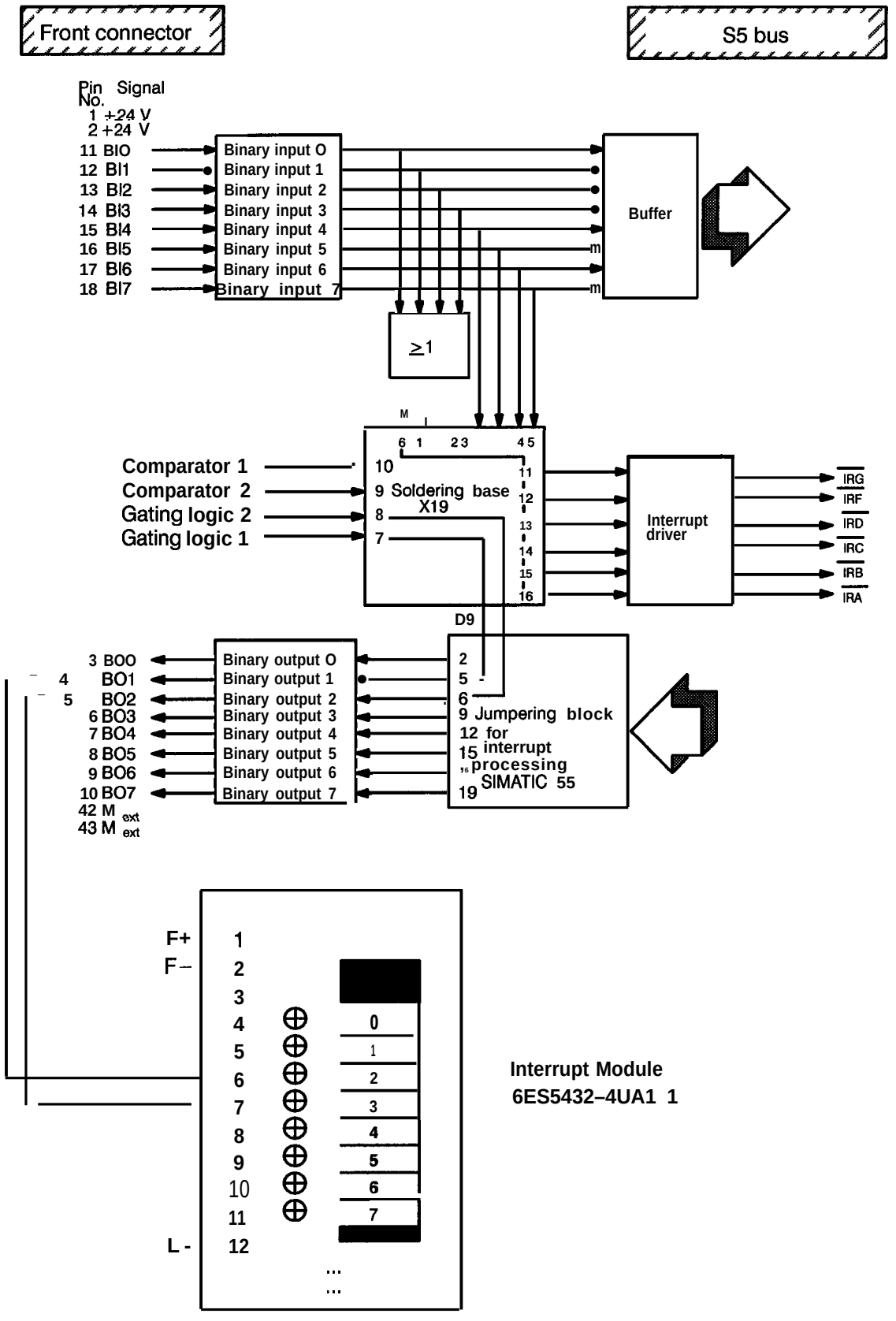
On the module 432–4, the presetting must be set according to the operating instructions.

Analog signal jumpering:



Diff. amp. = Difference amplifier
Comp. = Comparator
Chan. = Channel

Binary signal/interrupt jumpering:



Interrupt Module
6ES5432–4UA1 1

OB 1

```
NETWORK 1       0000                    OB 1 for S5-155U

0000      :
0001      :L    KM 11XXXXXX             Enable interrupt ("STROBE"=1) and
0003      :T    PY 183                  Reaction to falling edge
0004      :                             ("LOG"=1)
0005      :L    FW 190                  Load stored value
0006      :T    PW 178                  Write DAC2
0007      :L    PY 180                  Read binary inputs
0008      :T    FY 192
0009      :A    F  192.2                Scan BI2
000A      :JU   FB  A                   Value for BI2 = "1"
000B NAME :SIGNAL 1
000C      :AN   F  192.2                Scan BI2
000D      :JU   FB  B                   Value for BI2 = "O"
000E NAME :SIGNAL 0
000F      :BE
```

FB A

```
NETWORK 1       0000
NAME :SIGNAL 1                        Value for BI2 = "1"

0005      :L    KF  +1000               Load KF=+1OOO if BI2 = "I"
0007      :T    PW 176                  Write DAC1
0008      :BE
```

FB B

```
NETWORK 1       0000
NAME :SIGNAL O      Value for BI2 = "O"

0005      :L    KF  +800                Load KF=+800 if BI2 = "O"
0007      :T    PW 176                  Write DAC1
0008      :BE
```

OB 4

```
NETWORK 1       0000                    Interrupt OB(S5–155U) at value drop
0000      :JU   FBX                     Save scratchpad flag
0001 NAME :SAVE
0002      :
0003      :L    PY 181                  Load comparator states
0004      :T    FY 194
0005      :AN   F  194.3                Evaluate parameter bit "D"
0006      :JC   FB  Z2                  Interrupt reaction at value drop
0007 NAME :INTERRUPT 2
0008      :
0009      :JU   FB  Y                   Load scratchpad flag
000A NAME :LOAD
```

```
000B        :BE
```

OB 5

```
NETWORK 1       0000        Interrupt OB (S5– 155U) at excess value
0000        :JU  FB  X      Save scratchpad flag
0001 NAME :SAVE
0002        :
0003        :L   PY 181     Load comparator states
0004        :T   FY 196
0005        :AN  F  196.1   Evaluate parameter bit "B"
0006        :JC  FB  Z1     Interrupt reaction at excessive value
0007 NAME :INTERRUPT 1
0008        :
0009        :JU  FB  Y      Load scratchpad flag
000A NAME :LOAD
000B        :BE
```

FB Z1

```
NETWORK 1       0000
NAME :INTERRUPT 1           Excess value: Diff > DAC2

0005        :L   KM 1IXXX101    Enable interrupt ("STROBE"=l )
0007        :T   PY 183         and select channel 5 at the ADC
0008        :T   PY 182         Convert output difference 2
0009        :L   PW 182         Read output difference 2
000A        :T   FW 200         Store value in FW 200
000B        :L   KM 1 1XXX011   Select channel 3 at the ADC
000D        :T   PY 183
000E        :T   PY 182         Convert AV1
000F        :L   PW 182         Read AV1
0010        :T   FW 202         Store value in FW 202
0011        :BE
```

FB Z2

```
NETWORK 1
NAME :INTERRUPT 2           Value drop: Diff < DAC1

0005        :L   KM 10010110    Load 5.85 V =150 units
0007        :T   PY 180         Write DAC3
0008        :BE
```

5 Putting into Operation

5.1 Basic Connector

Any of the three IP 243 versions (i.e., with full or part configuration) has a basic connector which provides the link to the SIMATIC S5 bus, and the S5 bus, respectively. This connector is located on the upper half of the module.

	d	b	z
2		M	+5 V
4		PESP	
6		AB O	CPKL
8		AB 1	$\overline{\text{MEMR}}$
10		AB 2	$\overline{\text{MEMW}}$
12		AB 3	$\overline{\text{RDY}}$
14	$\overline{\text{IRA}}$	AB 4	DB0
16	$\overline{\text{IRB}}$	AB 5	DB1
18	$\overline{\text{IRC}}$	AB 6	DB2
20	$\overline{\text{IRD}}$	AB 7	DE33
22		AB 8	DB4
24	$\overline{\text{IRF}}$	AB 9	DB5
26	$\overline{\text{IRG}}$	AB 10	DB6
28		AB 11	DB7
30			
32		M	

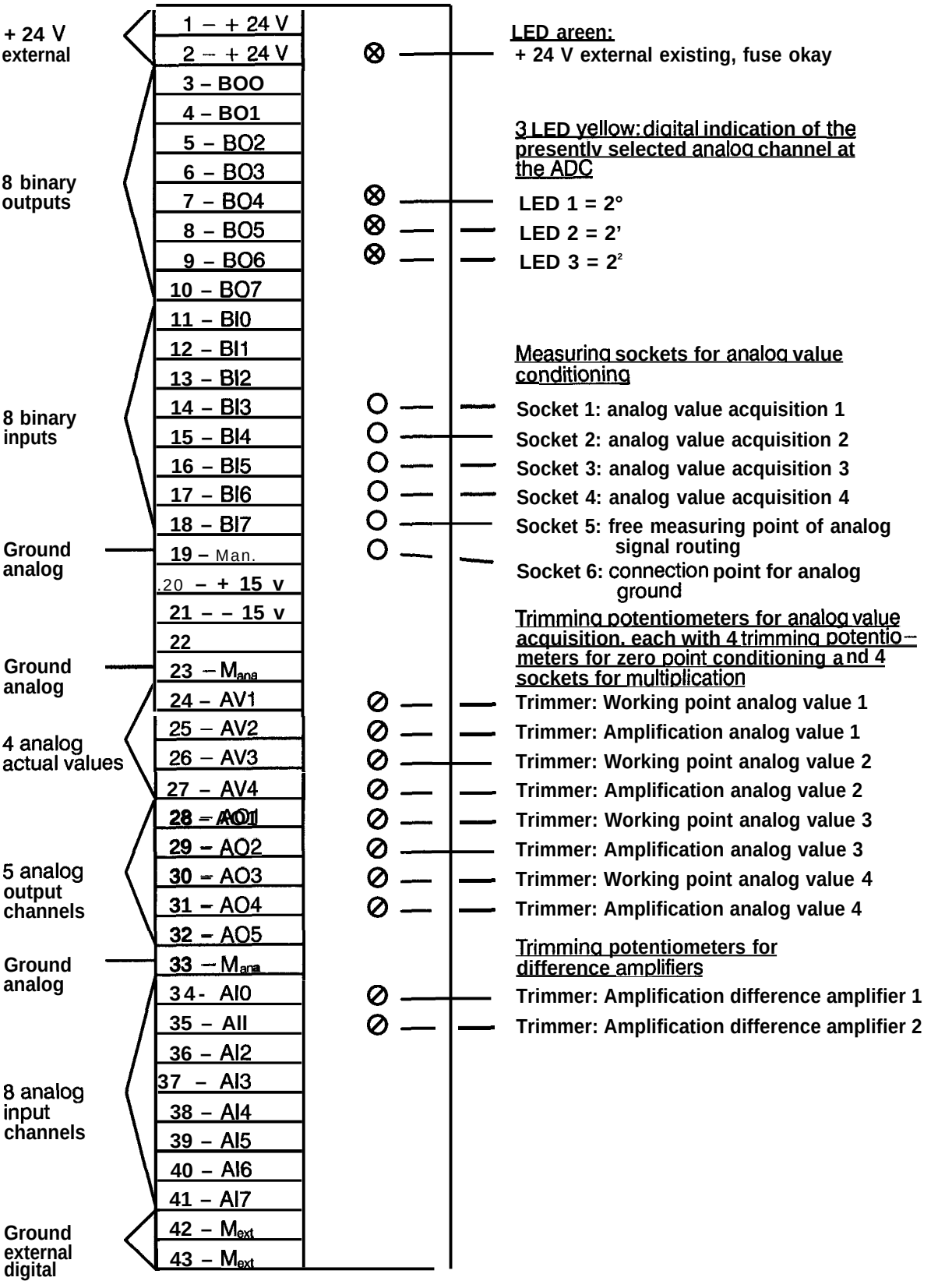
Basic connector pin assignment

5.2 Front Plate and Front Connector

The required 43-way front connector is available in versions for crimp connection or screw connection:

– Crimp connection: Order No. 6XX3068
– Screw connection: Order No. 6XX3081

Schematic diagram of the front connector:



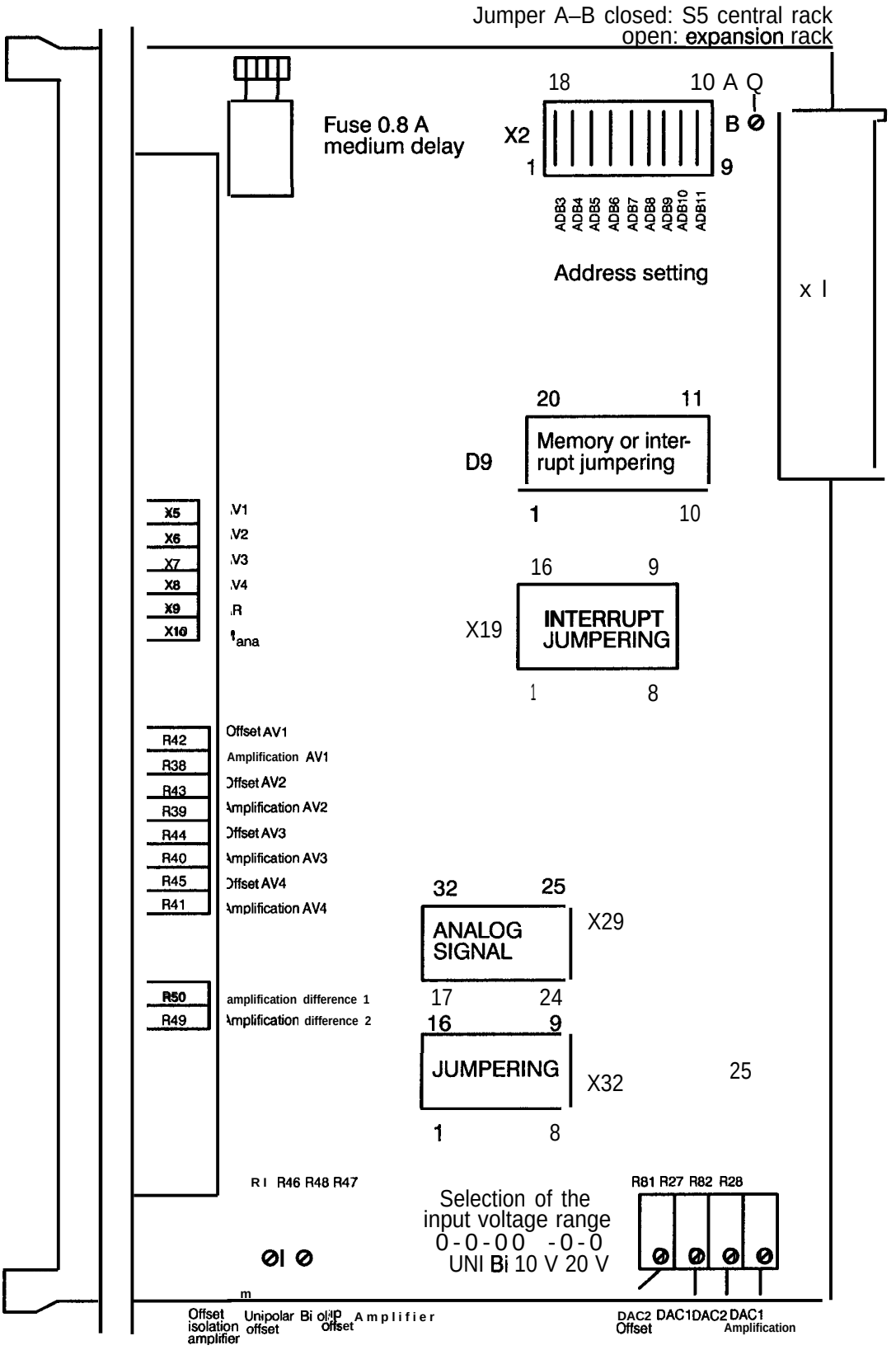
5.3 Explanation of the Signal Names and Abbreviations

+24 V	Supply voltage +24 V DC
M_{ext}	O V reference potential (M from +24 V supply)
M_{ana}	O V reference potential (analog)
BOO to 607	Binary outputs O to 7
BI0 to BI7	Binary inputs O to 7
AV1 to AV4	Analog input channels 1 to 4 with analog value condition
AO1 to A05	Analog output channels 1 to 5
AI0 to A17	Analog input channels O to 7
&15 V	Sensor power supply

Attention: No load should be hooked up to the sensor power supply of ±15 V unless it is ensured that the supply voltage doesn't exceed U_p = +24 V ±10% and that the consumption does not exceed 50 mA with a fully configured system and 70 mA with a partly configured version. If these maximum values are not observed, this can cause an overload of the DC/DC converter and thus a function breakdown of the module.

Attention: Do not connect Maria and M_{ext}, since a separation between the analog and the digital section must be maintained.

5.4 Layout of Setting Elements and Jumpers

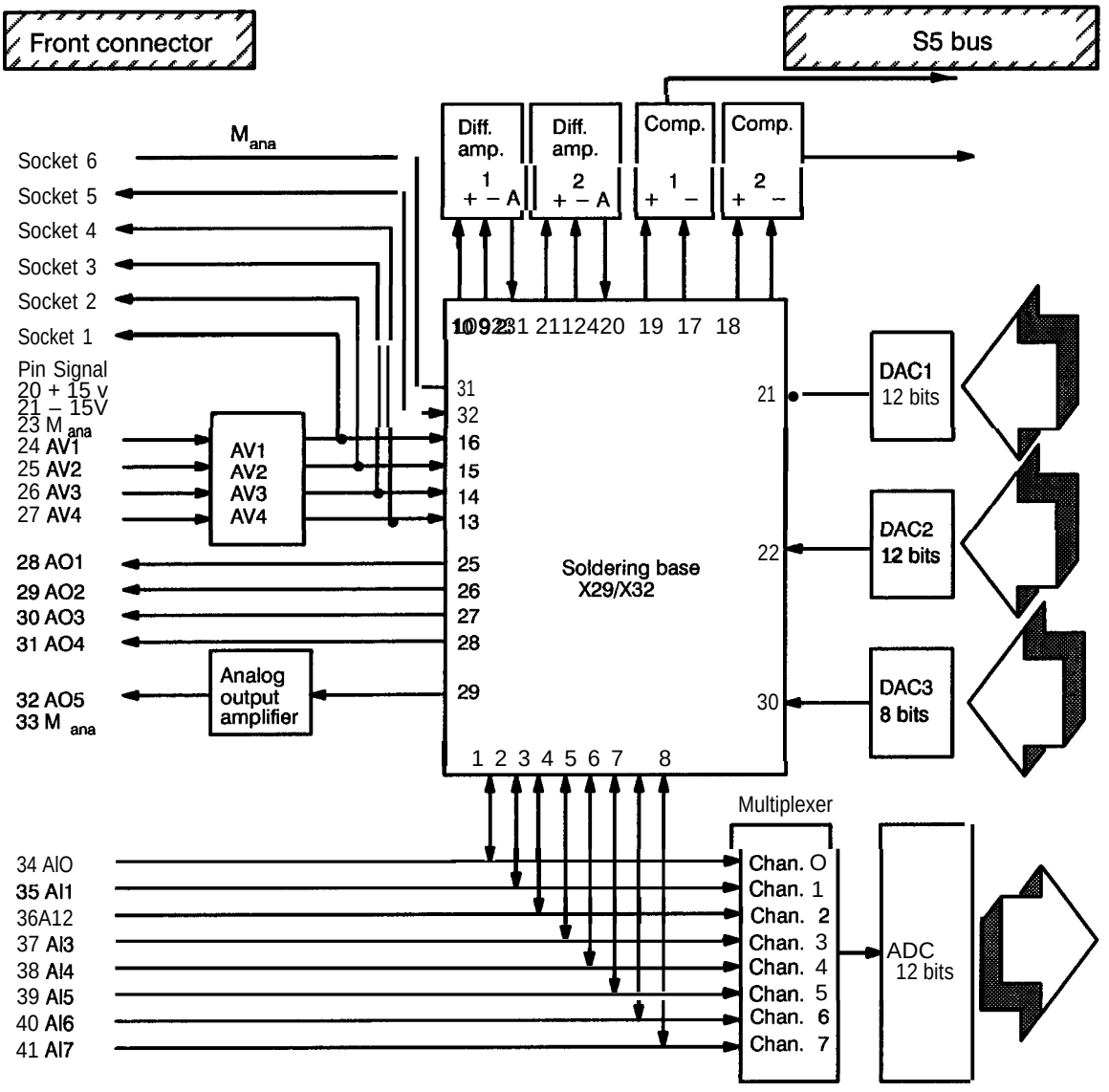


5.5 Jumpering of the Analog Signals

5.5.1 Circuitry of the Analog Signal Jumpering

The two soldering bases X29 and X32 (see section 5.1) form the basis for the jumpering of the analog signals. Via these bases, by means of soldering in jumpers, the required analog signals or the different internal module components can be connected in a user–specific way.

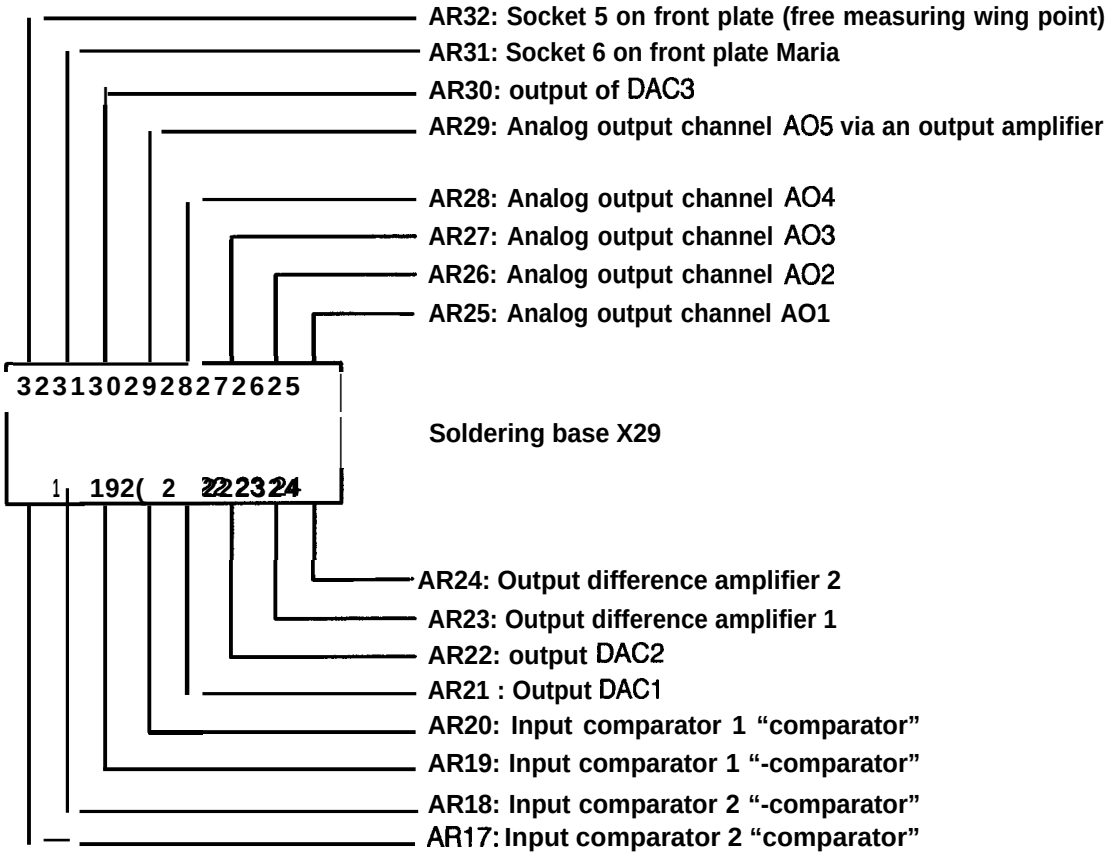
The following diagram shows all signals on the jumpering base which can be combined.

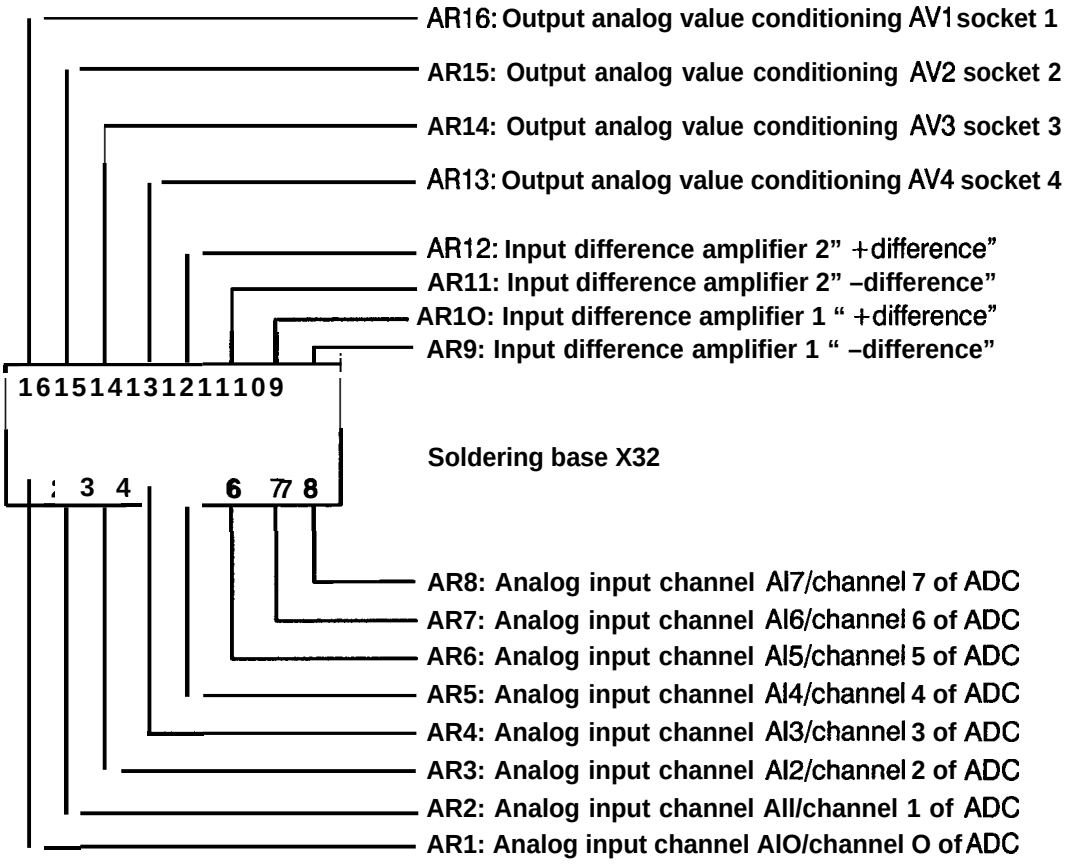


Diff.amp. = **Difference amplification**
Comp. = **Comparator**
Chan. = **Channel**

5.5.2 Soldering Base Pin Assignment

The analog signal jumpering comprises the two 16–way soldering base X29 and X32 (see section 5.4, Layout of Setting Elements and Jumpers). The available 32 pins of the soldering bases have the following signal assignment:

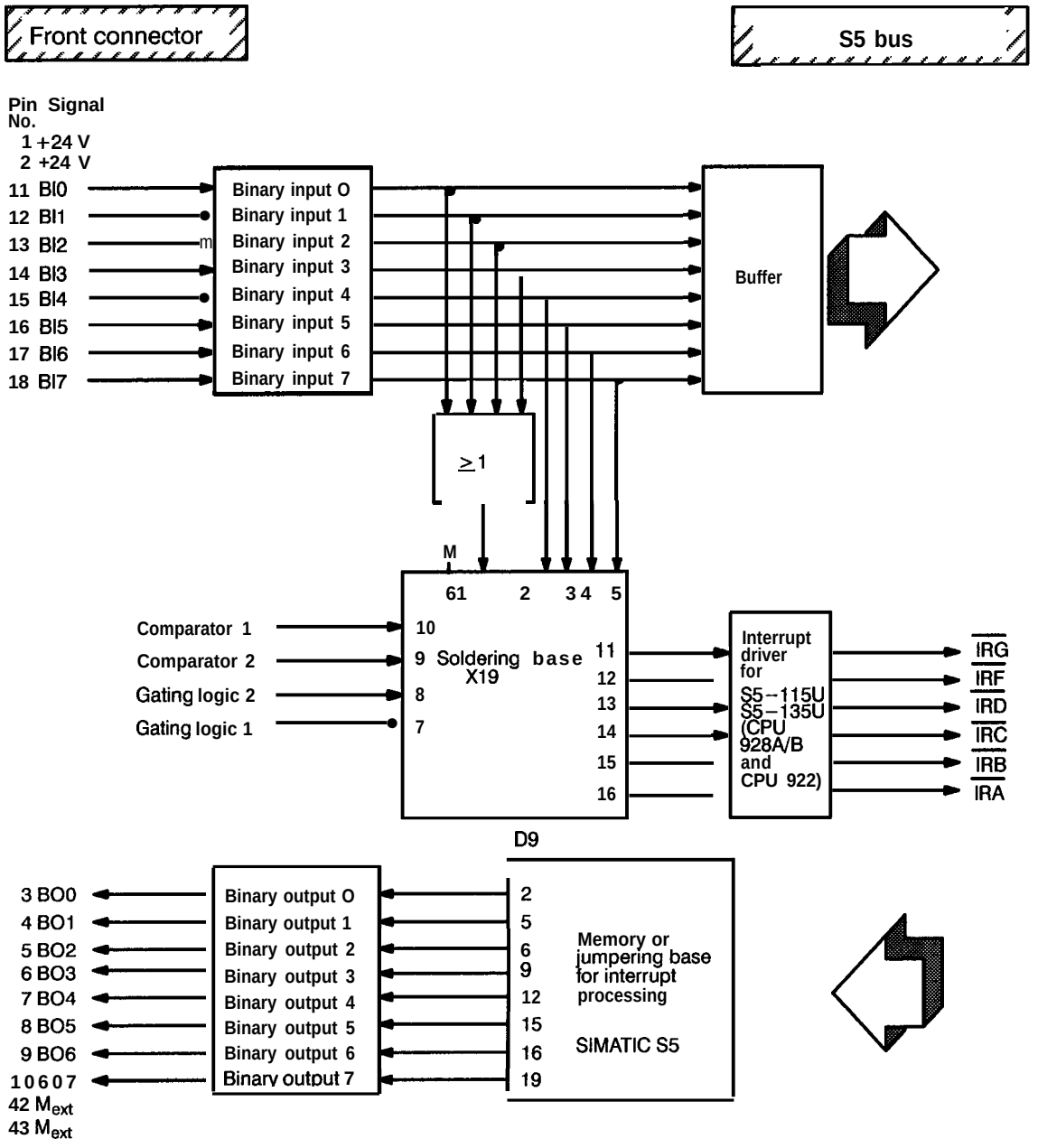




All analog components are designed in a way that the signals at the analog signal jumpering are standardized in the ranges O V to1O V or ±1O V.

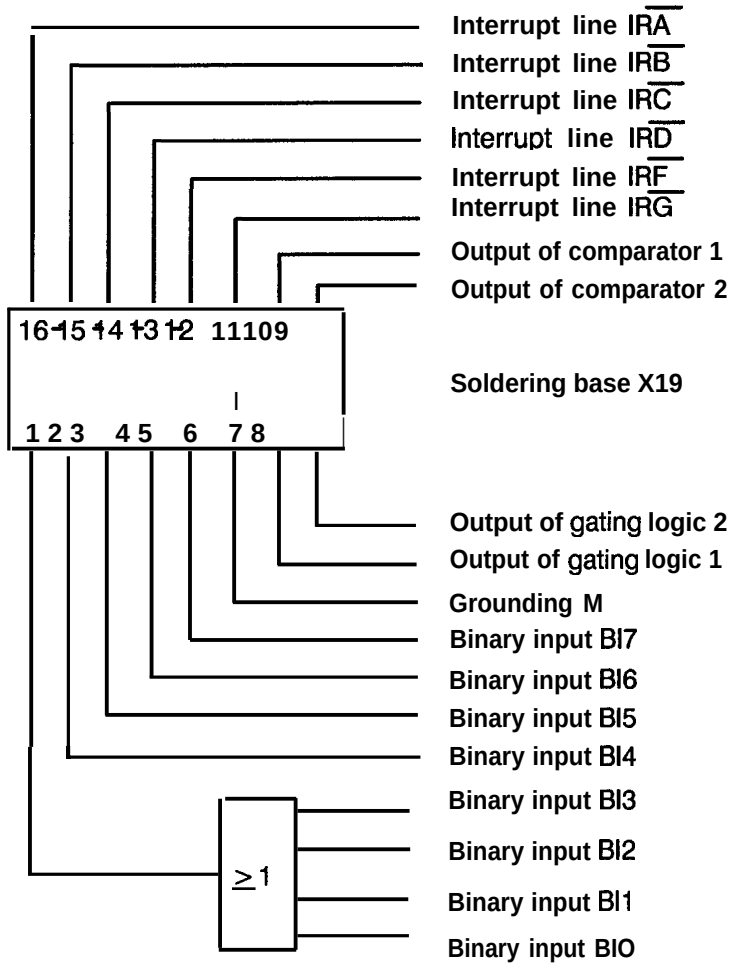
5.6 Jumpering of the Binary Signals

The binary signals are also conducted via a soldering base and can be interswitched in auser-specific way. If desired, the interrupt evaluation is also activated via the binary signal jumpering. The digital inputs and outputs can be directly read in or read out via the bus. For interrupt processing, however, jumpers must be installed on the soldering base X19. The following diagram shows the structure of the binary signal jumpering:



5.7 Interrupt Jumpering

If an interrupt evaluation is intended, this is possible with the programmable controllersS5–11 5U/H and S5–135U with CPU 928A/B or CPU 922 (or same CPUS in PLC S5–155U) via direct bus access to the interrupt lines. All other control devices require an additional binary input module with process interrupt generation and external wiring. In this case, the intermediate memory latch D9 must be replaced with the soldering base D9, included in the delivery. A detailed description of the procedures for interrupt processing with the IP 243 is given in section 4. Here, reference is made only to the pin assignment of the soldering base relevant to the jumpering of interrupts.



Attention: At delivery, the jumpers are installed as shown in the diagram:

$\overline{IRA}$ - $\overline{IRB}$ - $\overline{IRC}$ - $\overline{IRD}$ - $\overline{IRF}$ - $\overline{IGR}$ - M (Pins 16-15-14-13-11 -6)

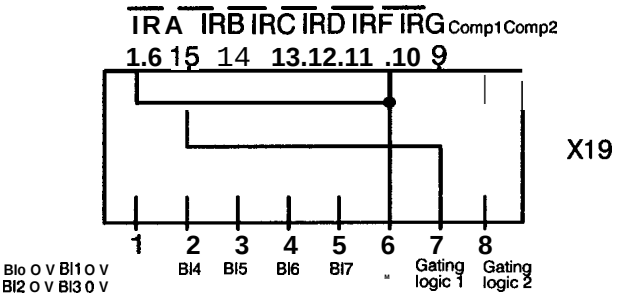
If the IP 243 is used in SIMATIC S5 systems with level–tri gered interrupt processing, these jumpers must not be changed.

If, however, the module is operated with a different programmable controller which allows interrupt processing directly via the bus, then the corresponding pins of the interrupt lines must be free from their soldered connections. All unused interrupt lines must retain their jumper connection with grounding M.

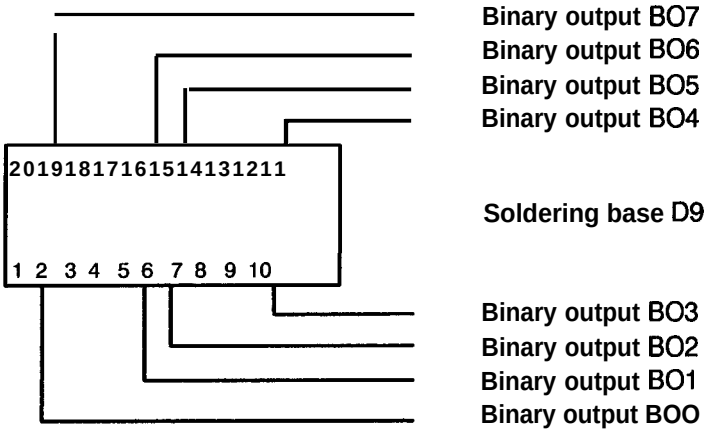
E

In the programmable controllerS5–115U, an interrupt is activated on interrupt line B via gating logic 1.

The following jumpers must be established on the soldering base:



As already mentioned, for interrupt jumpering in SIMATIC S5 units without direct bus access, memory latch D9 must be replaced by the soldering base D9. This soldering base has the following pin assignment:



Attention: To evaluate interrupts with an additional interrupt module, the interrupt–generating outputs of the comparators or the gating logic must be connected by jumpers from the soldering base XI 9 to base D9 to the binary outputs of the IP 243. These outputs are then connected externally to the binary input module with process–interrupt generation.

5.8 Setting the Module Address

The module address is set via the DIP FIX switch on the soldering base X2 (see the layout of setting elements in section 5.4). Addressing in the 1/0 area is between the starting addresses 128 and 248. The address displacement is 8 (i.e., a maximum of 16 modules can be addressed).

Example: First starting address 144
Second starting address 152

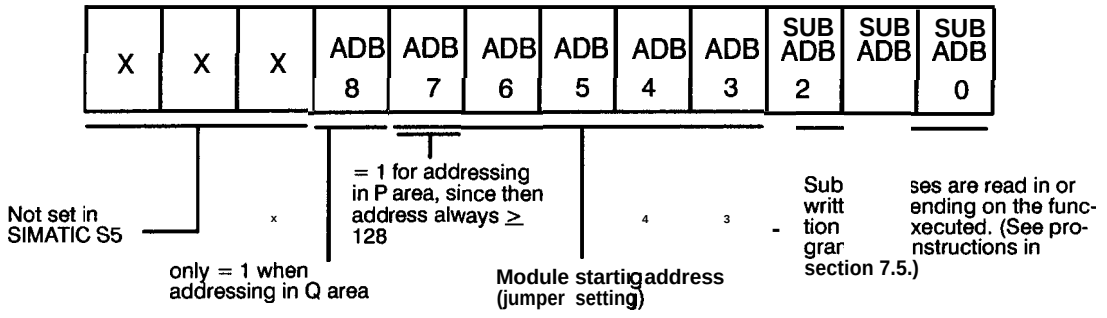
It should be noted that when the IP 243 is used in a central rack (S5–115U/H, S5–135U or S5–155U/H), the jumper A–B must be closed. In an expansion device, the jumper A–B must remain open.

The soldering base X2 appears as follows:

Address bit	Jumper	Address	
ADB 3	1–18	2^3 = 8	
ADB 4	2–17	2^4 = 16	
ADB 5	3–16	2^5 = 32	
ADB 6	4–15	2^6 = 6 4	
ADB 7	5–14	2^7 = 128	This jumper must always be installed in the P area as the module address is always ≥ 128.
ADB 8	6–13	2^8 = 256	With SIMATIC S5, this jumper is only installed when the module is addressed in Q area.
ADB 9	7–12	2^9 = 512	With SIMATIC S5 these jumpers are always open.
ADB 10	8–1 1	2^{10} = 1024	
ADB 11	9–Io	2^{11} = 2048	

Attention: Only the programmable controllers S5–135U, S5–150U/S and S5–155U/H are capable of addressing the Q area. The module must be inserted in an expansion rack. The Q area comprises the start adresses 0 to 248.

Addressing at the SIMATIC S5 system bus appears as follows:



Example: Setting of module address 144

10 – – – – – – –O 18
20 ———— —— 0 17
30 – – – – – – –O 16
40 – – – – – – –0 15
50 ———— - 0 14
60 – – – – – – –O 13
70 – – – – – – –0 12
80 – – – – – – –O 11
90 – – – – – – –0 10

ADB 3 = 2^3 Jumper 2 - 17 -t 2^4 = 16 and
ADB 4 = 2^4 Jumper 5 – 14 → 2^7 = 128 installed
ADB 5 = 2^5 corresponds to the setting module
ADB 6 = 2^6 address 144 (in the P areea)
ADB 7 = 2^7
ADB 8 = 2^8
ADB 9 = 2^9
ADB 10 = 2^{10}
ADB 11 = 2^{11}

Base X2 assignment

6 Technical Specifications

Binary Inputs:

Rated Input Voltage 24VDC
Number ofInputs 8
Galvanic Isolation ..... no
Input Voltage Corresponding to:
"O" Signal ..... open–circuitedor −5 V to 5.1V
"I" Signal , ... 12.7 V to 30 V
InputResistance ..... typically 10 kΩ
Input Current (''I'' Signal) ..... typically 2.5 mA
DelayTime ..... typically 2.7 msec
Polarization Protection ..... yes
Maximum Permissible Cable Lengths:
– Unshielded 400m
–Shielded ..... 1000 m
Interrupt–Generating Inputs (Optional)

Binary Outputs:

NumberofOutputs 8
Outputvoltage
– Nominal Value 24V
– For Signal "0" ..... maximum of 3 V
– For Signal "1" ..... minimum of–I.9V
Output Current for Signal "1"
– Nominal Value ..... 200 mA
– Permissible range 2t0200mA
Residual Current for Signal "O" ..... maximum of 250 μA
Total Switching Current maximumof600mA
Switching FrequencywithoutLoad ..... maximum of 1 kHz
Galvanic Isolation ..... no
Fuse (Externa124VSupply) ..... 0.8 A, medium slow
Short-CircuitProtection ..... fuse
Maximum Permissible Cable Lengths:
–Unshielded 400m
–Shielded ..... 1000 m

Analog Inputs:

Input Signal Ranges . . . . . ±5 V
. . . . . ±10 V
. . . . . 0 V to +10 V
Number of Inputs 8
Digital Representation of Input Signal 11 bits and sign or 12 bits
Measuring Principle . . . . . successive approximation
Galvanic Isolation . . . . . no
Conversion Time . . . . . .35 µsec.[1]
Input Resistance . . . . . approximately 1MΩ
Permissible Voltage between Input
and Earth (Destruction Limit) . . . . . ±35 V
Maximum Permissible Voltage between
Two Inputs (Destruction Limit) . . . . . ±35 V
Linearity Error. . . . . ≤ $\pm 3.10^{-4}$
Zero Error . . . . . ≤ $\pm 5.10^{-4}$
Temperature Error . . . . . ≤ $\pm 3.10^{-5}$ pro Kelvin
Basic Error Limit (DIN 43745) . . . . . ≤ ±0.6‰
Operational Error Limit
(between 0° C and +55° C) (DIN 43745) . . . . . ≤ ±1.2‰
Maximum Permissible Cable Length
–Shielded . . . . . 20 m

12-Bit Analog Output:

Input Signal Range . . . . . ±10 V, bipolar
Number of Outputs 2
Digital Representation of Output Signal . . . . . 11 bits and sign
Galvanic Isolation . . . . . no
Output Current . . . . . ±5 mA
Burden Resistance . . . .22 kΩ
Burden Connection . . . . . burden connected to OV
Short-Circuit Protection . . . . . yes
Short-Circuit Current . . . . . approximately 25 mA
Settling Time to 99% of Rated Output
Value for a Cable Length of 20 M . . . .5 µsec.
Linearity Error. . . . . ≤ *3.1 0^{-4}
Zero Error . . . . . ≤ $\pm 5.10^{-4}$
Temperature Error . . . . . <*2.1 0^{-6} pro Kelvin
Basic Error Limit (DIN 43745) . . . . . ≤ ±0.6‰
Operational Error Limit
(between 0° C and +55° C DIN 43745) . . . . . ≤ ±0.85‰
Maximum Permissible Cable Length
–Shielded . . . . . 20 m

[1] Thecommand processing times for the selection of measuring points and the start of coding are not included here.

8–Bit Analog Output:
Output Signal Range . . . .0 V to +10 V, unipolar
Number of Outputs 1
Digital Representation of
Output Signal . . . .8 bits
Galvanic Isolation . . . . . no
Output Current . . . . . ±5 mA
Burden Resistance . . . . . .>2 kΩ
Burden Connection . . . . . burden connected to O V
Short-Circuit Protection . . . . . temporary
Short-Circuit Current . . . . . undefined
Settling Time to 99% Of
Rated Output Value for a
Cable Length of 20 M . . . . . 10 µsec.
Basic Error Limit (DIN 43765) . . . . . ≤ ±2%
Operational Error Limit
(between 0° C and +55° C) (DIN 43765) . . . . . ≤ ±4%
Maximum Permissible Cable Length
–Shielded . . . . . 20 m

Analog Output Amplifier
Output Signal Range . . . . . ±10 V, bipolar
Number of Outputs 1
Galvanic Isolation . . . . . no
Output Current . . . . . ±5 mA
Burden Resistance . . . .22 kΩ
Burden Connection . . . . . burden connected to O V
Short-Circuit Protection . . . . . yes
Short-Circuit Current . . . . . approximately 20 mA
Maximum Permissible Cable Length
–Shielded . . . . . 20 m

8–Bit Analog Output with Analog Amplifier Series:
Output Signal Range . . . .0 Vto 10 V, unipolar
Number of Outputs 1
Digital Representation . . . . . 8 bits
Galvanic Isolation . . . . . no
Output Current . . . . . ±5 mA
Burden Resistance . . . .22 kΩ
Burden Connection . . . . . burden connected to O V
Short-Circuit Protection . . . . . yes
Short-Circuit Current . . . . . approximately 20 mA
Settling Time to 99% of Rated Output
Value for a Cable Length of 20 M . . . . . 10 µsec.
Error Limit at 25° C . . . . . ≤ ±0.2%
Error Limit between 0° C and +55° C ≤ ±0.4%
Maximum Permissible Cable Length
–Shielded . . . . . 20 m

Analog Value Conditioning Circuits:

Input Signal Range . . . . . ±10 V
Number of Inputs 4
Galvanic Isolation . . . . . no
Input Resistance . . . . . typically 200 kΩ
Input Time Constant . . . . . typically 110 µsec.
Setting Range for Zero Displacement –2 Vto +2 V
(Operating Point)
Amplification . . . . . 0.5 to 5
Voltage between Input and
0 V Connection (Destruction Limit) . . . . . maximum .&35 V

Difference Amplifier (P controller):

Input Signal Range . . . . . ±10 V
Output Signal Range . . . . . ±10 V
Number of Controllers 2
Galvanic Isolation . . . . . no
Output Current . . . . . &5mA
Amplification. . . . . 1.1 to 20
Input Time Constant . . . . . typically 500 µsec.
Input Resistance . . . . . typically 1 MΩ
Burden Resistance . . . . . ≥ 2 kΩ
Short-Circuit Protection . . . . . yes
Short-Circuit Current . . . . . approximately 50 mA
Voltage between Two Inputs
(Destruction Limit) . . . . . ±35 V
Voltage between input and
0 V connection (Destruction Limit) . . . . . ±35 V

Comparators:

Input Signal Range . . . .0 V to +10 V
Number of Inputs 2
Input Time Constant . . . . . typically 250 µsec.
Input Resistance . . . . . typically 44 kΩ
Voltage between Two Inputs
(Destruction Limit) . . . . . maximum ±35 V
Voltage between Input and
0 V Connection (Destruction Limit) . . . . . ±35 V
Interrupt–Generating Option

Power Supply Voltage UP:
Rated value 24VDC
Ripple U_{ss} . . . . . maximum 3.6 V
Permissible Range (Including Ripple) .. . .20 Vto 30 V DC
Value for t < 0.5 sec. . . . . maximum 35V

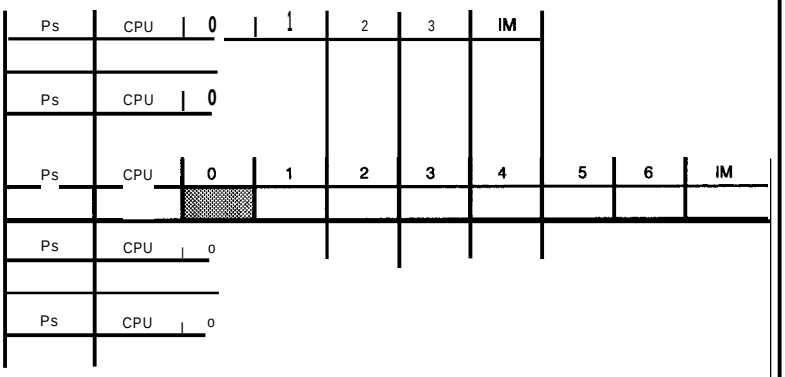
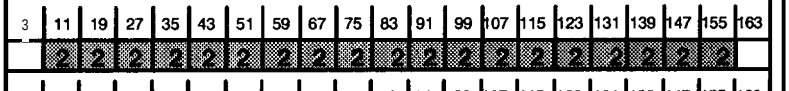
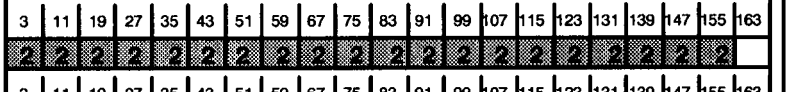
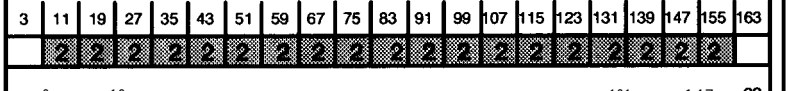
Current Consumption:
Internal +5 V Supply . . . . . typically 600 mA
External +24 V Supply
(without Sensor Power Supply
and Total Switching Current) . . . . . typically 270mA
External Supply Voltage . . . . . +20 V DC to +30 V
Power Loss
–Full Configuration . . . . . 11.8 W
(6ES5243-lAA1 1)
–Part Configuration, Al Only .. ..4.6 W
(6ES5243-IAB1l)
–Part Configuration, AO Only .. ..6.1 W
(6ES5243-lACI 1)

Mechanical Data:
Dimensions (W x H x D) . . . . . 20 mm x 244 mm x 202 mm
Mounting Width . . . . . 1–1/3 SPS = 1 module slot

Weight . . . . . .approximately 0.46 kg (6ES5243-lAA11)
. . . . . .approximately 0.38 kg (6ES5243–lAB11)
. . . . . .approximately 0.39 kg (6ES5 243–1AC11)

Ambient Conditions:
Operating Temperature . . . . . 0° to +55° C
Storage and Transport Temperature . . . . . –40° to +70° C

6.1 In Which Slots Can the IP 243 Analog Module Be Used ?

Programmable Controller in Module Rack		Slot Designa- ▒ ≙ Operation of IP 243 in this slot possible
Central Controller S5–115U	CR 700–0LA	
	CR 700–OLB	
	CR 700–1	
	CR 700–2	
	CR 700–3	
Expansion Device	ER 701–3 ①	
Central Controller S5–135U		
Central Controller S5–155U		
Expansion Device S5–183U		
Expansion Device S5– 1841		
Expansion Device S5– 1851		
Expansion Device ① S5–186U		

The IP 243 analog module cannot be inserted in central unit S5–150U/S or expansion devices ER 701 –1, ER 701 –2, and 187U.

1. Interrupts can be processed in expansion devices starting at release 6ES5 701–31A13 when optical fiber links 6ES5307–3UAI 1 and 6ES5317–3UA11 are used.
2. Functionality very restricted since no interrupt lines available
3. Functionality restricted since not all interrupt lines available
4. Changing of jumpers on the bus PCB is required.

7 Programming Instructions

7.1 Overview

These programming instructions describe the following standard function blocks:

FB 160 (PER:ANL) "Read analog module"

FB 161 (PER:ANS) "Write analog module"

The function blocks, together with the

IP 243 analog module,

are used in the following programmable controllers.

FB 160	FB 161	PLC/CPU
x	x	S5-115U (CPU 941A/B to CPU 944A/B)
x	x	S5-115H (CPU 942-7UH...)
x	x	S5-135U (CPU 922, CPU 928A/B)
x	x	S5-150U/S
x	x	S5-155U/H

These programming instructions require users to be familiar with sections 1 through 6 and with the programmable controllers they are using.

The following example shows a test assembly (with the analog module IP 243) for easily testing the jumper assignments and functions. This test program can also be used as the basis for a future automation task.

The S5-DOS floppy disk contains the files of the function blocks with example, and the English and French commentary blocks for the respective programmable controllers.

PLC S5-	File		
	Function Block	Commentary Block	
	German	English	French
	S5MxxxST.S5D	ECMxxxST.S5D	FCMxxxST.S5D
115U/H	S5MA50ST.S5D	ECMA50ST.S5D	FCMA50ST.S5D
135U	S5MB22ST.S5D	ECMB22ST.S5D	FCMB22ST.S5D
15ou/s	S5MA40ST.S5D	ECMA40ST.S5D	FCMA40ST.S5D
155 U/H[1)]	S5MA60ST.S5D	ECMA60ST.S5D	FCMA60ST.S5D

Copy the commentary block to the S5MxxxST.S5D file to obtain the commentary in your language when the example is printed out. Use the S5MxxxDR.INI for the printout.

The appropriate title block file are:

S5MxxxF1.INI
ECMxxxF1.INI
FCMXXXF1.INI

1) Use the xxMB22ST.S5D files when a CPU 922 or 928A/B is used in PLC S5-155U.

7.2 Function Block FB 160 (PER:ANL)

7.2.1 Function Description

The function block “Read analog module” (when the module is outfitted accordingly) accepts the selected analog value and outputs it either as a bit pattern, the way it arrives from the module, or as a 16–bit fixed point numeral, standardized to the respective nominal value.

Furthermore, the binary inputs and the comparator outputs can be read with this function block. Prior to reading the comparator outputs, the gating logic is switched over.

Function

FB 160 reads the analog and binary inputs, switches over the gating logic and reads the comparator outputs.

7.2.2 Calling the Function Block

In the STL (statement list):

S5-115U/H

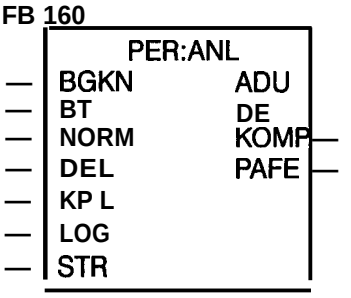
```
        :JU FB160
NAME    :PER:ANL
BGKN
BT
NORM
DEL
KP L
LOG
STR
ADU
DE
KOMP
PAFE
```

S5–135U
S5–150U/S
S5–155U/H

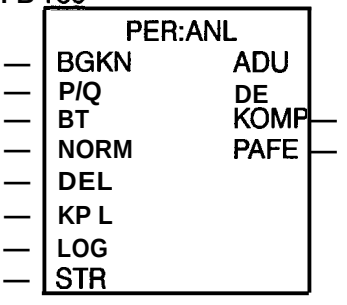
```
        :JU FB160
NAME    :PER:ANL
BGKN    :
P/Q     :
BT      :
NORM    :
DEL     :
KP  L   :
LOG     :
STR     :
ADU     :
DE      :
KOMP    :
PAFE    :
```

In the LAD/CSF (Ladder diagram/ control system flowchart)

FB 160



FB 160



7.2.3 Explanation of Parameters

NAME	CLASS	TYPE	DESIGNATION
BGKN	D	K Y	Specification of the module address and channel number
P/Q	D	KS	Specification of I/O area [1]
BT	D	F	Specification of module type (nominal range)
NORM	I	BI	Switch over to input of standardized values
DEL	I	BI	Read digital inputs
KPL	I	BI	Read comparator outputs
LOG	I	BI	Switching over the gating logic
STR	1	BI	Enable signal for comparator interrupt
ADU	Q	W	Analog value output
DE	Q	BY	Outputting the digital inputs
KOMP	Q	B Y	Outputting the comparator outputs
PAFE	Q	BI	Parameterization error

[1] This parameter is not available on the S5–115U/H programmable controller. It can only be addressed in the P area.

7.2.4 Parameter Assignment

BGKN : KY = x, y x = Module address
128< x ≤ 248 for P/Q : KS=P
0< x ≤ 248 for P/Q: KS=Q

y = Channel number
0 ≤ y ≤ 7

P/Q : KS = P Normal 1/0 area
KS = Q Expanded 1/0 area

BT : KF = X Module type; Specification of the nominal range
x = O unipolar O V to 10 V
x = 1 bipolar –10 V to +10 V
x = 2 bipolar –5 V to +5 V

PAFE : In case of illegal parameterization the signal status is"1". The recog–nized error is then shown by the assignment of the flag byte FY 255:

F 255.0 The module address is outside of the specified area or is not within the 8–bit grid pattern (first part of parameter BGKN)

F 255.1 The parameter P/Q is not set with 'P-' or 'Q-'. (Does not apply to programmable controller S5-115U/H.)

F 255.2 –

F 255.3 –

F 255.4 QVZ, no module found under this address. (first part of parameter BGKN) (only set with S5–155U/H)

F 255.5 –

F 255.6 The channel number is outside the specified range (second part of parameter BGKN)

F 255.7 The parameter BT is outside the specified range.

7.2.5 Data Area Assignment

No data blocks are addressed.

Addressing the Module in S5–155/H

For proper operation of the function block, the analog module 1P 243 must be addressed in the address range from KH = FF080 to KH = FF1FF. This corresponds to the 1/0 area from KH = FF080 to KH = FFOFF (byte number 128 to 255) and to the Q range from KH = FF1OO to KH = FF1FF (byte number O to 255).

7.2.6 Technical Specifications

Block no.	160			
Block name	PER:ANL			
PLC S5–	115U	135U	15ou/s	155U
Library no. P71200–S...	51 60–A–2	9160–A–1	4160–A–1	61 60–6–1
Call length (in words)	13	14		
Block length (in words)	165	180		222
Processing time (in msec)				
	CPU 941A/B	CPU 922		
Without standardization	8.2/4.9	1.8	0.4	0.69
With standardization	11.115.9	2.1	0.5	0.74
	CPU 942A/B	CPU 928A/B		
Without standardization	5.4/4.9	1 .1/1.0		
With standardization	6.4/5.9	1 .2/1.1		
	CPU 943A/B			
Without standardization	3.3/4.1			
With standardization	4.5/5.5			
	CPU 944A/B			
Without standardization	0.5/0.3			
With standardization	2.1/1 .7			
Nesting depth	1	0		
Blocks called	FB 242 (integrated in PLC)	None		
Data areas used	–			
Flag areas used	FY 238 to FY 255	FY 244 to FY 255		
System instructions	None			
Other	1)	–		2)

1) Interruptions (interrupts and wake–up alarms) are temporarily disabled in the block with the AS/AF commands. This cancels out any “AS” command which you may have programmed.

2) All interruptions (process alarms, interrupts and wake–up alarms) are disabled in the block for approximately 42 pee.

7.2.7 Function Block Application

The module basic address and the channel number for the analog value are specified by parameter BGKN. Depending on the channel number, the function block reads an analog value from the module and outputs it at parameter ADC.

The representation of the analog value depends on the NORM parameter:

NORM = “O”:

The analog value read at the module is output unchanged at parameter ADC (as a bit pattern according to the description in the operating instructions).

NORM = “1“

The analog value read at the module is converted to the nominal range. The nominal range is defined by the values at parameter BT. The conversion formulas are:

for BT = O (Nominal range O V to 10 V):

$$\text{ADC} = \text{rough value} \times \frac{20000}{8192}$$

for BT = 1 (Nominal range –10 Vto +10 V):

$$\text{ADC} = \text{rough value} \times \frac{20000}{4096}$$

for BT = 2 (Nominal range –5 V to +5 V):

$$\text{ADC} = \text{rough value} \times \frac{20000}{8192}$$

The analog value is output as a 16–bit fixed–point numeral for the unit mV.

When parameter DE–L has the signal status”1”, the binary module inputs are read and then output at parameter DE. If the module has no binary inputs, signal status “O” is output to all bits.

When parameter KP–L has the signal status”1”, the comparator outputs of the module are read and then output at parameter KOMP. The bits now required, LOG and STR, are set in accordance with the parameters LOG and STR, and they are transferred to the module during channel selection.

7.3 Function Block FB 161 (PER:ANS)

7.3.1 Function Description

The function block "Write analog module" either transfers a specified bit pattern or a 16–bit fixed–point numeral, standardized to the nominal value, to the module. The function block can also control the binary outputs if the module is outfitted accordingly.

Function

FB 161 outputs an analog value and the 8 binary outputs.

7.3.2 Calling the Function Block

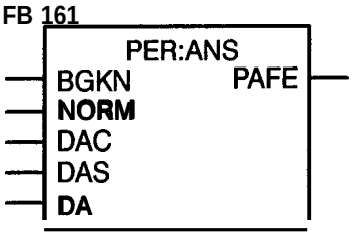
In the STL (statement list):

S5-115U/H

```
        :JU FB161
NAME    :PER:ANS
BGKN    :
NORM    :
DAC     :
DAS     :
DA      :
PAFE    :
```

In the LAD/CSF (Ladder diagram/ control system flowchart):

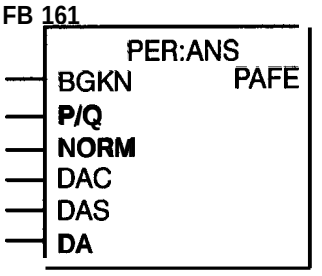
FB 161



S5–135U, S5–150U/S, S5–155U/H

```
        :JU FB161
NAME    :PER:ANS
BGKN    :
P/Q     :
NORM    :
DAC     :
DAS     :
DA      :
PAFE    :
```

FB 161



7.3.3 Explanation of Parameters

NAME	CLASS	I/TYPE	DESIGNATION
BGKN	D	KY	Specification of the module address and channel number
P/Q	D	KS	Specification of 1/0 area
NORM	I	BI	Switch over to input of standardized values
DAU		W	Specification of the 1/0 area [1]
DAS		BI	Write digital outputs
DA		BY	Specification of the digital outputs
PAFE	Q	BI	Parameterization error

[1] This parameter is not available on the S5–115U/H programmable controller. It can only be addressed in the P area.

7.3.4 Parameter Assignment

BGKN : KY = x, y

x = Module address
128< x ≤ 248 for P/Q : KS=P
O ≤ x ≤ 248 for P/Q: KS=Q

y = Channel number
0 ≤ y ≤ 7

P/Q :

KS = P Normal 1/0 area
KS = Q Extended 1/0 area

PAFE :

In the event of illegal parameterization, the signal status is"1". There-cognized error is then indicated by the assignment of the flag byte FY 255:

F 255.0 The module address is outside the specified area or not within the 8–bit grid pattern. (first part of parameter BGKN)

F 255.1 The parameter is not set with 'P-' or 'Q–'. (Does not apply to programmable controllerS5-115U/H)

F 255.2 –

F 255.3 –

F 255.4 QVZ, no module found under this address. (first part of parameter BGKN) (only set with S5–155U/H)

F 255.5 –

F 255,6 The channel number is outside the specified range (second part of parameter BGKN)

F 255.7 –

7.3.5 Data Area Assignment

No data blocks are addressed.

Addressing the Module (S5–155U/H)

For proper operation of the function block, the analog module 1P 243 must be addressed in the address range from KH = FF080 to KH = FF1 FF. This corresponds to the 1/0 area from KH = FF080 to KH = FFOFF (byte number 128 to 255) and to the Q range from KH = FF1OO to KH = FF1FF (byte number O to 255).

7.3.6 Technical Specifications

Block no.	161			
Block name	PER:ANS			
PLC S5–	115U	135U	150U/S	155U
Library no. P71200–S...	5161 –A–O	9161 –A–1	4161 –A–O	6161 –B–1
Call length (in words)	8	9		
Block length (in words)	158	170		195
Prcessing time (in msec)				
	CPU 941A/B	CPU 922		
Without standardization	5.9/3.2	1.4	0.2	0.59
With standardization	9.6/3.5	1.7	0.3	0.64
	CPU 942A/B	CPU 928A/B		
Without standardization	3.3/3.2	0.7/0.2		
With standardization	4.4/3.5	1 .0/0.3		
	CPU 943A/B			
Without standardization	2.8/2.6			
With standardization	3.1/2.8			
	CPU 944A/B			
Without standardization	0.3/< 0.1			
With standardization	1.811.6			
Nesting depth	1	0		
Blocks called	FB 242 (integrated in PLC)	None		
Data areas used	–			
Flag areas used	FY 238 to FY 255	FY 248 to FY 255		
System instructions	None			
Other	–			

7.3.7 Function Block Application

The module basic address and the channel number of the analog value to be written are specified at parameter BGKN. The value at parameter DAU is transferred to DAC1, DAC2, or DAC3 according to the channel number.

The representation of the analog value DAC depends on the signal status at parameter NORM:

NORM = “O”:

The bit pattern at parameter DAC (in the case of channel 3, the left byte) is transferred to the module unchanged (bit assignment as shown in the operating instructions).

NORM = “1“:

The value at the parameter is interpreted as a standardized 16–bit fixed–point number (nominal range with KN = 1 or 2: ± 10000 mV; with KN = 3: O to 10000 rev). Depending on the channel number KN, the analog value is computed according to the following formula:

For channel number 1 or 2:

$$\text{Analog value} = \text{DAC} \times \frac{13422}{65536}$$

For channel number 3:

$$\text{Analog value} = \text{DAC} \times \frac{1678}{65536}$$

If the value is outside the currently valid nominal range, it is limited to an extreme value.

If the parameter DA-S has signal status”1”, the value at parameter DA is transferred to the binary module outputs. If the module has no binary outputs, the command is ineffective.

7.4 Example

This example shows the operation of the analog module 1P 243. By means of a simulator the individual functions can be selected (via binary inputs). The signal states can be displayed via binary outputs. The display shows how an analog value applied to the module can be read and how an analog value can be output via the module.

This example also shows the necessary jumper settings and wiring requirements for the mo-dule. Therefore, it can also be used as a test program to check the jumper settings and functions of the module.

7.4.1 Device Configuration

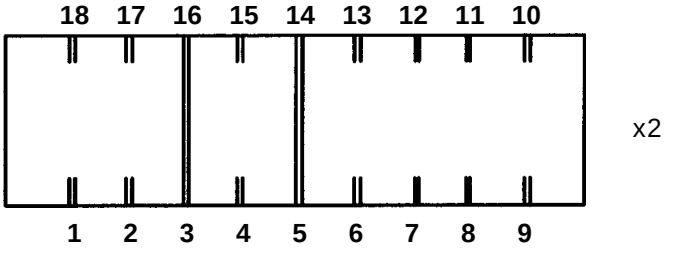
For a test of the analog module IP 243, the following devices can be used:

- One of the listed programmable controllers
- Programmer (e.g., PG 750)
- Analog module 1P 243 (6ES5 243–IAA11) in full configuration: front connector K with screw mounting (6)(X3 081)
- Digital input module; front connector with screw mounting
- Digital output module; front connector with screw mounting
- 2 simulators (6ES5788–0L412)
- Voltage source for two analog signals
- Voltmeter

7.4.2 Jumper Assignment of the Analog Module

Module Address (Basic Address 160):

DIP switch S2: ABD 5 ON (Jumper 3–13) = 2^5 = 32
ABD 7 ON (Jumper 5–14) = 2^7 = 128
Module address = 160



Analog routing:

Soldering bases X32 and X29:

Analog value 1 (PIN 16)	**– >**	**Channel O –> (PIN 2)**	**Comparator 1 + (PIN 20)**
Analog value 2 (PIN 15)	**– >**	**Channel 1 –>** (PIN 2)	**Comparator 1 – (PIN 19)**

DAC1 (PIN 21)	– >	AQ1 (PIN 25)
DAC2 (PIN 22)	–>	AQ2 (PIN 26)
DAC3 (PIN 30)	– >	AQ3 (PIN 27)

7.4.3 Assignment of the Inputs and Outputs

The program is designed in a way that allows easy adaptation to different input and output assignments. The program block (PB 243) that contains the test program works with flags only. The inputs and outputs to be used are allocated to these flags by organization block OB 1.

In the example the flags are the input word IW4 and the output word QW4 or the input word IW4 and the output word QW8 for theS5–115U.

I 4.0	F 4.0	NORM	Standardize analog value (convert)
I 4.1	F 4.1	DE_L	Read binary inputs
14.2	F 4.2	KP_L	Read comparator outputs
I 4.3	F 4.3	LOG	Switch over gating logic
I 4.4	F 4.4	STR	Enable signal for comparator interrupt
I 4.5	F 4.5	–	–
14.6	F 4.6	DA-S	Write binary outputs
I 4.7	F 4.7		Reset all binary outputs and flags
IB5	FY 5	DA	Binary outputs for output via the analog module
QB4/QB8	FY 8	DE	Binary inputs read by the analog module
QB5/QB9	FY 9	KOMP	Comparator outputs read by the analog module
Q 6. O/Q 10.0	F 14.0	PAFE	Parameterization error bit of FB 160
Q 6.1/Q 10.1	F 14.1	PAFE	Parameterization error bit of FB 161
–	FW 10	ADU	Analog value read by the module
–	FW 12	DAU	Analog value output via the module
–	FY 16		Error flag byte (FY 255) of FB 160
–	FY 17		Error flag byte (FY 255) of FB 161

7.4.4 Turn-On, Start-Up Behavior

The program is loaded entirely from the floppy disk to the user memory of the programmable controller.

During start-up there is no need to supply any data to the analog module. Its ready state is indicated by the green LED on the front panel. The LED lights up when an external 24 V voltage is applied.

If at the time the programmable controller is turned on, all simulator inputs are in switch position "O", no outputs maybe set after the start-up of the programmable controller.

If one of the outputs Q 6. O/Q 10.0 (flag F 14.0) or Q 6.1/Q 10.1 (flag F 14.1) is set, a para-meterization error was made. The exact error cause can be identified at flag byte FY 16 (for the parameterization error shown for output Q 6. O/Q 10.0) or at flag byte FY 17 (for the parameterization error shown for output Q 6.1/Q 10.1). Both flag bytes are set in accordance with the error bytes FY 255 of the standard function blocks FB 160 and FB 161.

7.4.5 Reading the Binary Inputs

If input 14.1 is brought to switch position"1", the binary inputs connected to the analog module are displayed at output byte QB4/QB8. If the signal status of these inputs is modified, the display on the simulator is modified accordingly.

7.4.6 Reading the Analog Value

The channel numbers from O to 7 are specified via the parameter BGKN of function block FB 160. The LEDs on the module's front plate indicate the currently selected channel as a bit pattern.

The analog value read in the example is transferred to the module through the front panel connector via input IW1 (contact 24) and the appropriate potential contact (contact 23). It can be measured simultaneously at sockets 1 (IW1) and 6 (M_{ana}). The output for analog value acquisition AV1 (Pin 16) must be brought to channel O of the ADC (Pin 1) via analog valuejumpering.

The analog value read by function block FB 160 is output in flag word FW 10. Via the programmer function "Control Variable", the actual value can be displayed directly.

If input 14.0 ("NORM") is brought to switch position"1", the analog value is displayed in mV given in binary code (ranging from –1 0000 to +10000). Otherwise it is given as a bit pattern, the way it arrives from the module.

Via the two potentiometers "Work point AV1" and "Amplification AV1", the analog value can be changed. In order to check whether the module reproduces the applied value in correct form, the amplification should be set to value"1" and the work point to "O". For this purpose a firm value (e.g., 2 V) should be specified at the analog value input AV1. Then a reading should be taken at the sockets and the amplification changed until the input value matches the end value. The work point is set by zero adjustment (i.e., the applied and the measured voltages are both zero). Via soldered jumpers the individual voltage ranges can be set as follows:

UNI – 10 V (BT = O: Voltage range from O V to 10 V)

BI – 20 V (BT = 1: Voltage range from -10 Vto +10 V)

BI – 10 V (BT = 2: Voltage range from -5 V to +5 V)

7.4.7 Checking the Comparators

If routing of analog values has not been completed, the output for analog value acquisition AV1 (Pin 16) must be connected with the "+" input of comparator 1 (Pin 20). Furthermore, the output for analog value acquisition AV2 (Pin 15) must be connected with channel 1 of the ADC (Pin 2) and with the "-" input of comparator 1 (Pin 19).

Channel O is set to 2 V. Depending on whether the analog value measured at channel 1 is below or above 2 V, there will be different states of the comparator outputs (in this case A and B for comparator output 1).

The function KP–L "Read comparator outputs" is switched on via input 14.2. Depending on the status of the LOG bit (I 4.3), the following signal states will result for comparator output 1:

LOG (1 4.3)	= "0"	= "1"
Channel 1<2 V	A = "O", B = "1"	A = "1"j B = "l"
Channel 1>2 V	A = "l", B = "1"	A = "1", B = "O"

The comparator outputs are conducted to the output byte QB5/QB9 and are displayed there. In this case "A" corresponds to output Q 5. O/Q 9.0 and "B" corresponds to Q 5.1/Q 9.1. After turning off the function "Read comparator outputs", the outputs at the simulator remain active. Via input I 4.7 (flag F 4.7) the outputs can be reset.

7.4.8 Writing the Binary Outputs

When the function "DA-S Write binary outputs" (1 4.6) is activated, the binary outputs of the analog module, connected to the simulator, are indicated by LEDs on the simulator.

The binary outputs are entered at input byte IB5.

7.4.9 Writing the Analog Value

When the analog routing operations have been performed in single steps so far, they now must be supplemented by the following jumpers:

DAC1	– >	AO1
(PIN 21)		(PIN 25)
DAC2	–>	AO2
(PIN 22)		(PIN 26)
DAC3	– >	AO3
(PIN 23)		(PIN 27)

Via the programmer function “Control variable” a value can be specified via flag word FW 12 which is output as an analog value. If input 14.0 (NORM) has signal status”1”, the value can be output in mV in binary form (ranging from –1 0000 to +10000). Otherwise the bit pattern is required and is then directly transferred to the module.

In order to determine the written analog value, it is measured at the contacts in the front connector of the analog module (e.g., pin 28 for AO1 and pin 33 for potential).

7.5 Programming Without FB

7.5.1 Address Assignment

For read and write operations the 1P 243 requires an 8–byte address area. These eight bytes are assigned as follows:

	ADR	READ MSB							LSB	
Starting address	0	–	–	–	–	–	–	–	–	(READY-Delay)
Starting address + 1	1	–	–	–	-	–	–	-	-	(READY-Delay)
Starting address + 2	2	–	–	–	–	–	–	–	–	(READY-Delay)
Starting address + 3	3	–	–	–	-	–	–	–	–	(READY-Delay)
Starting address + 4	4	7	6	5	4	3	2	1	0	DIGITAL INPUT
Starting address + 5	5	1	1	1	1	D	C	B	A	COMPARATORS
Starting address + 6	6	2'1	2'?	29	2^8	2^7	2^6	2^5	2^4	HIGH–BYTE ADC
Starting address + 7	7	2^3	2^2	2^1	2^0	0	0	0	0	LOW–BYTE ADC

	ADR	WRITE MSB							LSB	
Starting address	0	S	X	X	X	X	2^{10}	29	2^8	HIGH–BYTE DAC1
Starting address + 1	1	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LOW–BYTE DAC1
Starting address + 2	2	S	X	X	X	X	2^{10}	2^9	2^8	HIGH–BYTE DAC2
Starting address + 3	3	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LOW–BYTE DAC2
Starting address + 4	4	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DAC3
Starting address + 5	5	7	6	5	4	3	2	1	0	BINARY OUTPUT
Starting address + 6	6	X	X	X	X	X	X	X	X	ADC convert
Starting address + 7	7	LOG	STR	X	X	X	2^2	2^1	2^0	Comparators/ ADC channel select

ADR = Address byte
MSB = Most significant bit
LSB = Least significant bit

Attention:

Although the four bytes ADR O to 3 are not set for READ and no READY is generated, no input module maybe addressed in this area, as the data bus driver of the module is “turned on” in this area also.

7.5.2 Reading and Writing the Inputs and Outputs

The descriptions of the individual 1P 243 hardware components also refer to software handling. With an example, this section summarizes the programming commands for the respective accesses.

Example for module address 128 with SIMATIC S5

Function	Data D7 D6 D5 D4 D3 D2 D1 DO	Subaddresses 2^2 2^1 2^0	STEP 5 Statement
BI Read	7 6 5 4 3 2 1 0	1 0 0 ≙ Mod. adr. + 4	LPY 132
BO Write	7 6 5 4 3 2 1 0	1 0 1 ≙ Mod. adr. + 5	TPY 133
DAC1 Write	VZ X X X X 2^{10} 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0	O 0 0 ≙ Mod. adr. + O 0 0 1 ≙ Mod. adr. + 1	TPY 128 TPY 129 0 TPW 128
DAC2 Write	VZ X X X X 2^{10} 2^9 2^8 2^7 2^6 2^5 2^6 2^3 2^2 2^1 2^0	O 1 0 ≙ Mod. adr. + 2 0 1 12 Mod. adr. + 3	TPY 130 TPY 131 0 TPW 130
DAC3 Write	2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0	1 0 0 ≙ Mod. adr. + 4	TPY 132
Read Comparators	1 1 1 1 D C B A	1 0 1 ≙ Mod. adr. + 5	LPY 133
Write ADC selection	L S X X X 2^2 2^1 2^0	1 1 1 ≙ Mod. adr. + 7	TPY 135
Write ADC conversion	X X X X X X X X	1 1 0 ≙ Mod. adr. + 6	TPY 134
ADC Read	2^1 1 2^0 2^9 2^6 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0 0 0 0 0	1 1 0 ≙ Mod. adr. + 6 1 1 1 ≙ Mod. adr. + 7	LPY 134 LPY 135 0 LPW 134

The propagation times for these three commands must be added to the converting times of a maximum of 35 µsec. per channel to obtain the time required for reading in an analog input channel. If the same channel is converted in repeated sequence, the command "ADC channel select" can be omitted, as the selected channel remains active after the call until it is overwritten.

Attention:

Not only the channel, which is selected by the multiplexer and then converted by the ADC, is stored in byte "subaddress 7" but also the desired states of the "LOG" and "STROBE" bits. When writing the data, make sure that no other functions are overwritten.