SIEMENS

Technical Description
Order number: 6AR1930-4AA06-2AA0 **April 2003**

SMP16-SFT251

Order number: 6AR1304-0EA00-0AA0

Counter board with two 32-bit incremental/pulse counters

SICOMP Industrial Microcomputer

(4)J31069-D2090-U001-A1-7618

Product History of the Technical Description

Revision [1)]	Record of Changes	Date
A0	First edition	03/00
A1	Control Register 1 and 2, Chapter 6.4.3 and 6.4.4	04/03

1) Corresponds to the 4th block of digits of the drawing number in the footer

Explanation of Notation

* An asterisk behind the signal name indicates a low-active signal (e.g., IOR*).

/ A slash between two signal names separates two level-dependent functions of one signal. Example: C/D* means Command for high level and Data for low level.

x Bits marked with an x in the register descriptions are irrelevant.

– Connections indicated with a dash in a connector assignment table are reserved (i.e., bus or I/O interface).

Signal Special signals not included in these specifications are indicated in bold print in the signal assignment tables and then explained (e.g., **AMSEOP**).

Safety Notes for SICOMP Boards

ESD protection measures

Caution

When handling boards and other components carrying this symbol, always adhere to ESD protection guidelines (**E**lectrostatic **S**ensitive **D**evices).

- Never touch the boards unless required work makes this absolutely necessary.
- When working with the boards, use a conductive and grounded work surface.
- Wear a grounding bracelet.
- Never touch the pins, connections or printed circuits of the boards.
- Never permit the boards or components to be touched by chargeable objects (e.g., synthetic materials).
- Keep the boards or components at least 10 cm away from CRT units and television sets.
- Leave the boards in their special packaging until they are needed. When registering boards, etc. do not remove the boards from their packaging or touch them.
- Boards may only be installed or removed when the voltage is off.

Wiring of Bus Backplanes

System-related signal wiring on SICOMP board systems is performed with wrap connections. The power supply cables are bundled together with cable binders. These cables are equipped with plug-in or screw connections.

Caution:
All signal wiring (the interrupt signal lines in particular) must be of the appropriate design and kept as short as possible. When longer interrupt signal lines cannot be avoided, twisted pair wiring must be used.

Related SICOMP SMP16 Literature

For more information on installing and handling SICOMP boards, see "SICOMP IMC system manual".

Table of Contents

1 Initial Startup

The primary steps involved in the initial startup of the board are listed below.

1. Software configuration. See chapters 1.1 and 4 for more information.

   Attention:
   Chip select channel 0 must be **enabled** for the board.The other channels can be enabled or disabled depending on the particular application. The ASBIC channel must be **disabled**.

2. Wiring I/O devices. See chapter 1.2 or 2.8 for more information.

1.1 Preparing for Software Configuration

The configuration of the board with the SMP16-AKO auto configuration software (see chapter 2.8) can be performed directly in the target system or in a separate generation system. In addition, the configuration can be performed in a separate system, but the board can still be configured in the target system.

In all cases, the board must be installed in an SMP16 bus system with daisy chain connection at the time of programming.

Configuration in the target system

	Requirements on the Target System
Required hardware	• SICOMP IMC AT CPU • SMP16 bus backplane with daisy chain
Required software	• Windows 95 • SMP16-AKO V2.0

Configuration in the target system, generation of the configuration in separate system

	Requirements on the Target System	**Requirements on the Generation System**
Required hardware [1)]	• SICOMP IMC AT CPU • SMP16 bus backplane with daisy chain	• PC-AT (e.g., workplace computer or laptop)
Required software	• RMOS or MS-DOS • AKO start program	• Windows 95 or Windows NT • SMP16-AKO V2.0

1) In addition, there must be a way to transfer the generated configuration file (i.e., STARTUP.SKD) to the target system. Some examples are listed below.
- Serial connection via zero modem cable (is supported by AKO start program)
- Floppy disk drives on both systems
- LAN connection

Configuration in a separate generation system

The board is installed in the generation system for configuration and then returned to the target system afterwards.

	Requirements on the Generation System
Required hardware	• SICOMP IMC AT CPU • SMP16 bus backplane with daisy chain
Required software	• Windows 95 • SMP16-AKO V2.0

Daisy chaining for configuration via software

With SMP16-SYS403 bus backplanes with 5 or more slots, the daisy change connection is already implemented electronically.

With the other bus backplanes, the slots of the software-configurable boards must be wired as shown below.

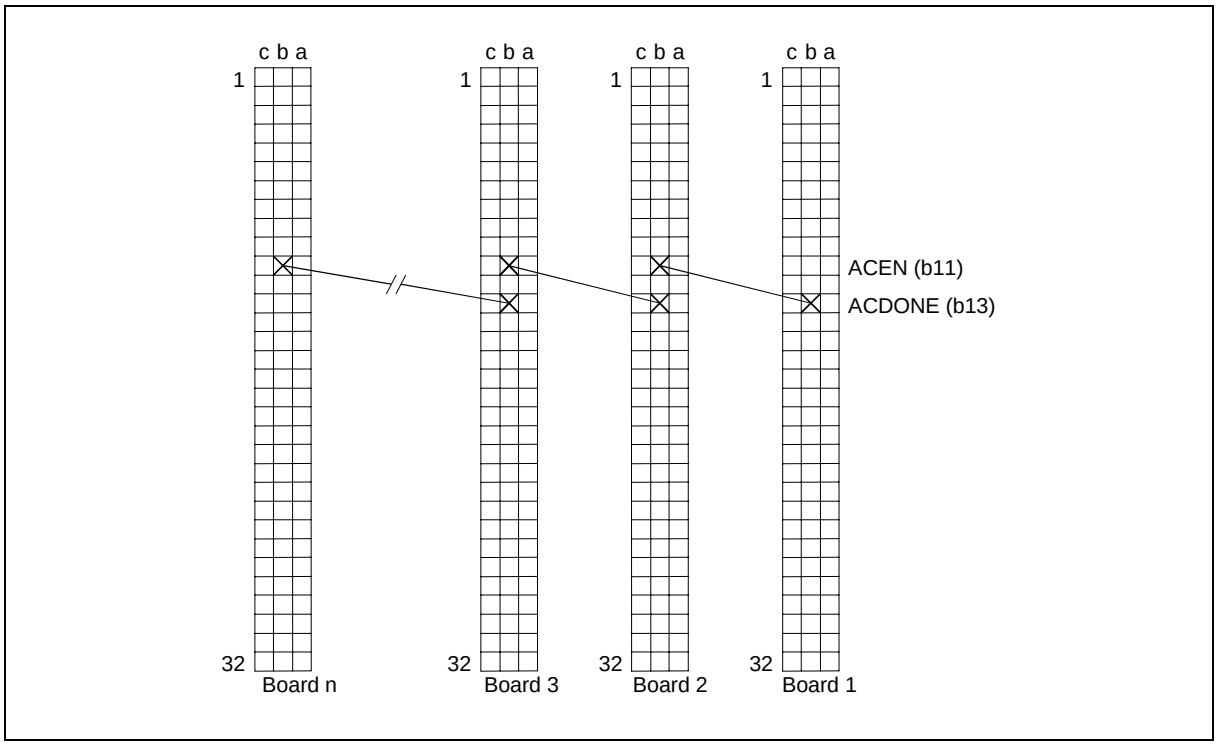


Figure 1.1 Daisy chaining on the SMP16 bus backplane for configuration via software

The ACEN input of the first software configurable board in the chain of configuration remains open as does the ACDONE output of the last board. All other ACDONE outputs must be connected with the ACEN input of the next board. See chapter 3.2.1.

1.2 Wiring the I/O

The differential control lines must be twisted in pairs (see chap. 3.3). The single-ended control lines must be twisted with the related ground.

The shield must be applied (for HF) to both the board and the addressed I/O. To prevent equalizing currents on the shield, an equipotential bonding conductor should be installed parallel to the signal line.

Never install your control lines near strong interference (e.g., motors, relays, high-voltage or power lines, thyristor controllers, power inverters and transmitters).

Also adhere to the information on electromagnetic compatibility contained in the SICOMP IMC system manual under the chapter on ambient conditions.

2 Features

2.1 Characteristics

The SMP16-SFT251 is a counter board with two 32-bit counters. Its software is compatible with the SMP-E251. It should be used instead of the SMP-E251.

The board has the following characteristics.

General

- Two 15-pin, sub D socket strips for connection of the I/O
- Free-convection ventilation
- EEPROM for identification and parameterization of the board
- Automatic configuration with "auto configuration" (see chap. 4)
- 5 V encoder power drawn from bus voltage (via fuse)

Functions per channel

- Position acquisition with connection of a two-track incremental encoder (single, double or quadruple edge evaluation, max. track frequency of 2 MHz)
- One zero-marking-pulse latch register and 3 extra latch registers (can be triggered by digital inputs) one of which can also be used as a comparator register
- Three digital, single-ended inputs (24 V) for triggering the extra latch registers or for generating interrupts
- One digital, single-ended input (24 V) for resetting the counter or for triggering interrupts
- A comparator register can be used to trigger an alarm (interrupt, status bit) when a certain counter state is reached and/or to reset the counter.
- Both the shaft encoder signals and the digital inputs of channel 0 can be assigned to channel 1. This makes it possible to run both counters parallel to each other.
- Frequency or pulse width measurement with frequencies up to 4 MHz. Either level or edge-control can be used to start the counter.
- The counting signals (A track and B track) and the zero marking pulse (N track) can be set with DIP switches for either 24 V technology or for RS 422.
- The operating modes can be set separately for each channel.

The following block circuit diagram shows the logical organization of the board.

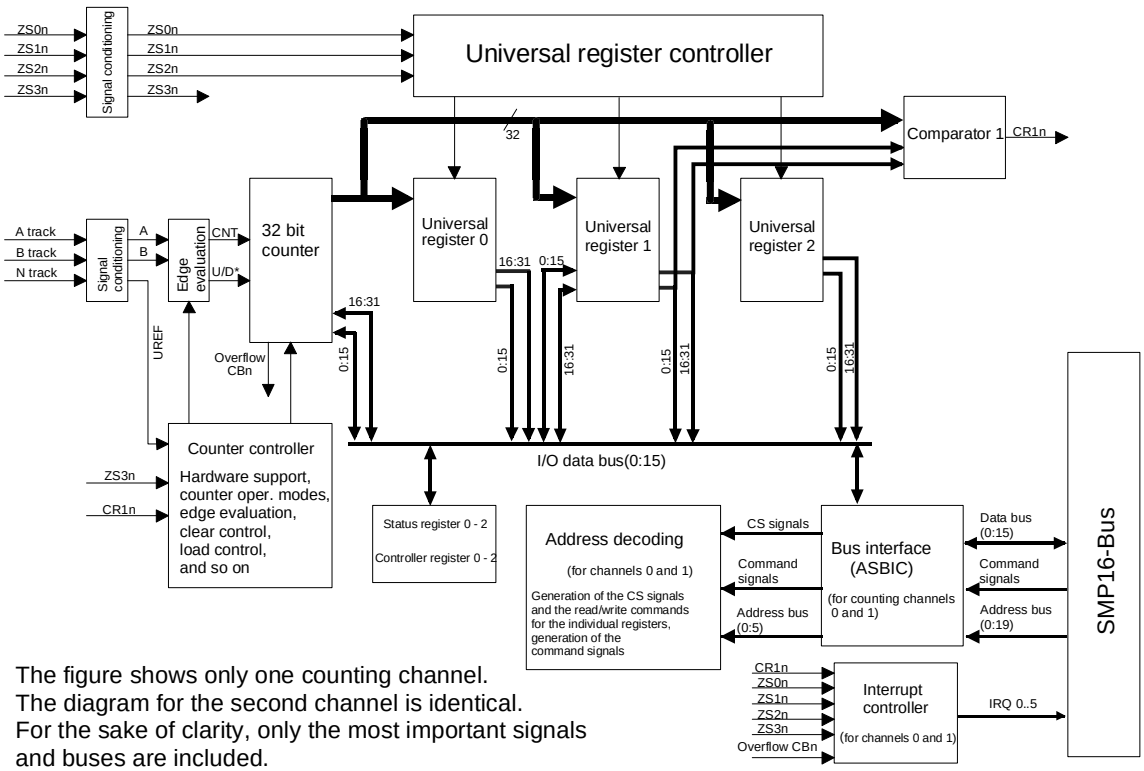
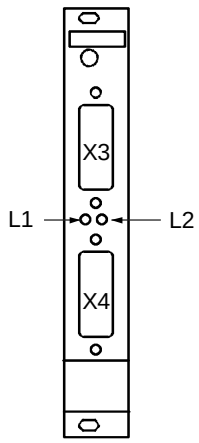


Figure 2.1 Block circuit diagram of the SMP16-SFT251

2.2 Front LEDs

The two front LEDs (L1 and L2) show the direction of rotation of the shaft encoder for channel 0 or channel 1 during position acquisition.
These LEDs are irrelevant for "frequency and pulse width measurement" mode.



Channel 0:

Direction of Rotation	Status - LED L1
Up	On
Down	Off

Channel 1:

Direction of Rotation	Status - LED L2
Up	On
Down	Off

2.3 Operational Values

System portion	
Voltage supply (from SMP16 bus)	+5 V ±5%
Current consumption with nominal voltage (without encoder power)	Max. of 400 mA
Counter inputs	
Number of channels	2
Counter size	32 bits
Interfaces: encoder inputs A, B, and N (zero marking pulse)	24 V technology, opto-decoupled (single-ended or differential) or RS 422
Operational values with 24 V technology:	
Differential	±13 V to ±30 V
Differential, max. ratings	±34 V
Single-ended, low level	–3 V to +5 V
Single-ended, high level	+13 V to +30 V
Single-ended, max. ratings	±34 V
Input current with 24 V technology (U_{in} = 24 V) (U_{in} = 30 V)	11.4 mA (typ.) 15.1 mA (max.)
See RS 422 specifications for operational values with RS 422.	
Input frequency for incremental encoders:	2 MHz (max.)
Input frequency with frequency/gate time measurement	4 MHz (max.)
Extra inputs	
Number	4 per channel
Interfaces	24 V technology
Input voltage, low level	–3 V to +5 V
Input voltage, high level	+13 V to +30 V
Input voltage, max. ratings	±34 V
Input current with high level (U_{in} = 24 V) (U_{in} = 30 V)	11.4 mA (typ.) 15.1 mA (max.)
5 V encoder power	
Encoder voltage	5 V (typ.) Depends on the power supply of the SMP16 system and the voltage drops on the board (typically 0.2 V)
Total current	720 mA (max.)
Short-circuit immunity	Yes (with SMD safety fuse)

Notes on 24 V interface

The 24 V interface offers extra immunity to interference. The physical characteristics of this interface (high voltage swings with currents > 10 mA) restrict its use with high-speed applications.
For this reason, encoders with the RS 422 interface should be used for encoder applications with track frequencies > 500 kHz. Otherwise, the encoder signals might not be transferred accurately which would cause counting errors in the system.

2.4 Physical Characteristics of the Encoder Signals

Encoders can be connected to the board with an RS 422 or 24 V interface. The desired physical characteristics must be selected with the two DIP switches (S1 and S2) on the board. See chapter 3.4.

Caution

Since setting the wrong interface may destroy the board, make sure that all DIP switches required for selection of the interface are set correctly.

2.5 Time Requirements for the Input Signals

2.5.1 Encoder Signals

The two track signals (A and B) of the encoder must be displaced by 90° to each other.

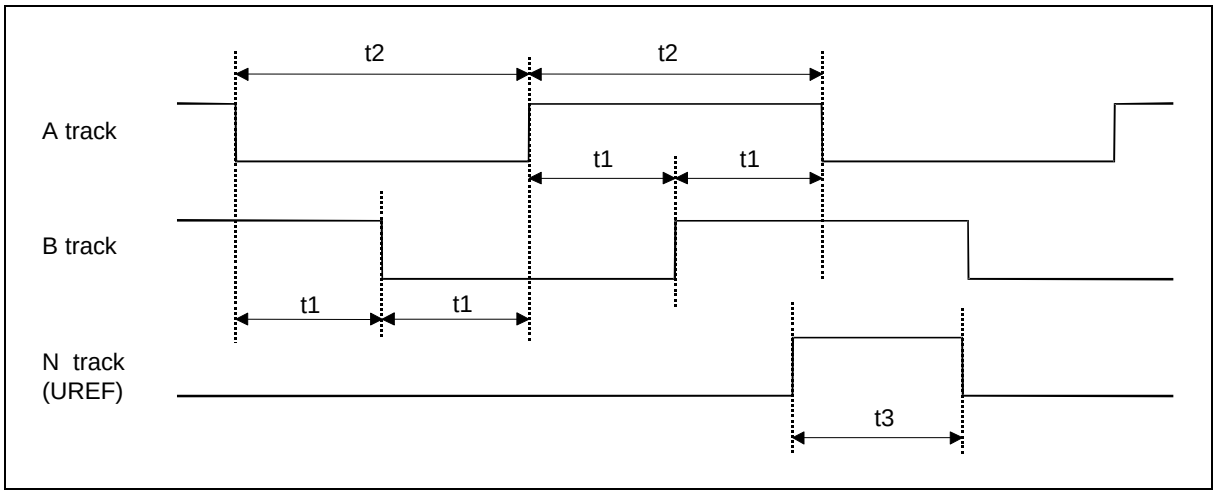


Figure 2.2 Time relationships of the encoder signals

t1	A edge to B edge	125 nsec (min.)
t2	Pulse width, A/B track	250 nsec (min.)
t3	Pulse width, N track	125 nsec (min.)

2.5.2 Frequency and Pulse Width Measurement

With frequency and pulse width measurement, the reference gate signal must be at least twice as long as the maximum expected cycle duration of the frequency to be measured.

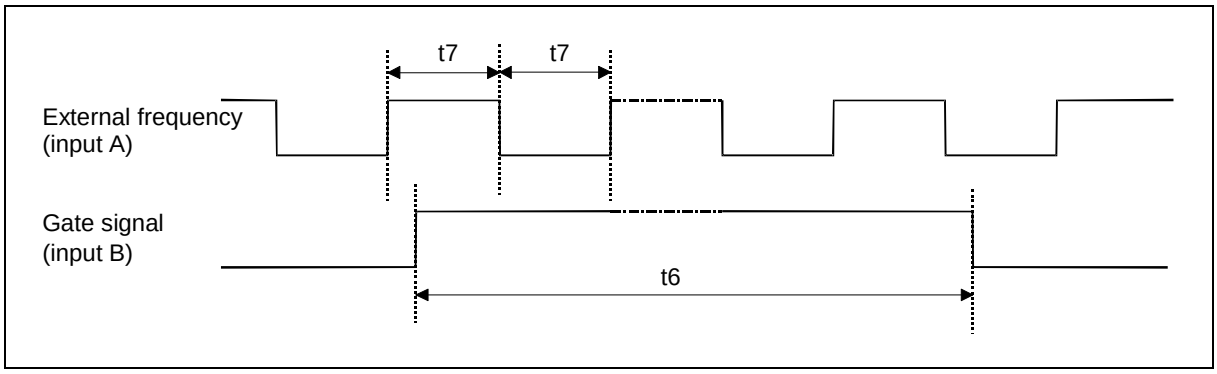


Figure 2.3 Time relationships with frequency and pulse width measurement

t7	Clock pulse high/low time	125 nsec (min.)
t6	Gate time when the external clock pulse is used	2 x t7 (min.)
t6	Gate time when the internal clock pulses are used	t8 (min.)
t8	Cycle time of the internal clock pulses: 1.25 MHz 2.5 MHz 2.0 MHz 4.0 MHz	 800 nsec 400 nsec 500 nsec 250 nsec

2.5.3 Special Signals

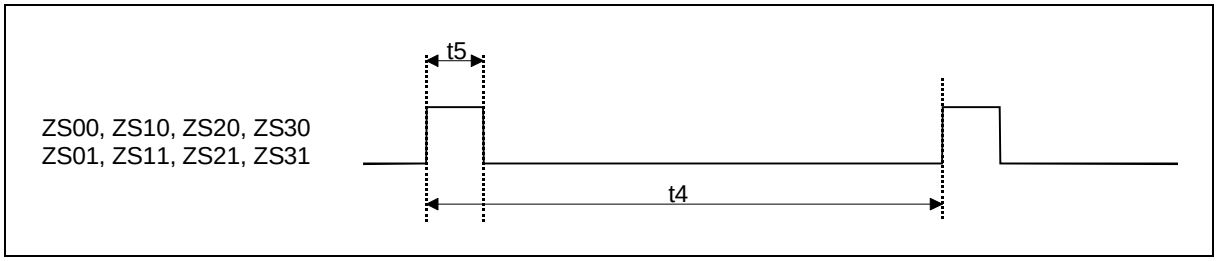


Figure 2.4 Time relationships of the special signals

t4	High edge to high edge	400 nsec (min.)
t5	Pulse width	250 nsec (min.)

2.6 Time Relationships of the 24 V Interface

The following signal runtimes apply to the 24 V interface.

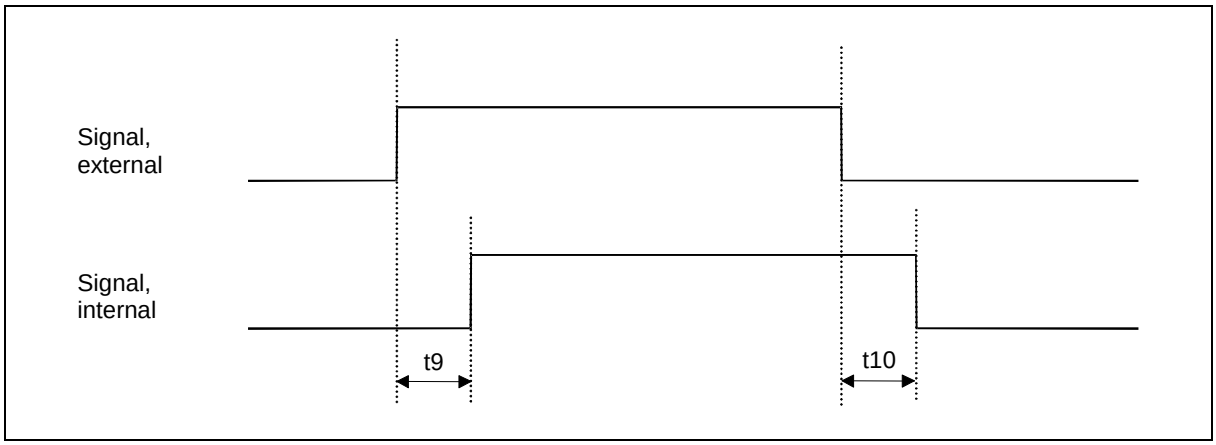


Figure 2.5 Signal runtimes for the 24 V interface

t9	Time from Low → High	500 nsec (typ.)
t10	Time from High → Low	400 nsec (typ.)

These signal runtimes apply to 24 V outputs with push-pull clock pulse technology. Other runtimes may apply when other technologies are used.

2.7 Ambient Conditions

	Operation	Transportation and Storage
Temperature	0° C to 55° C	–40° C to +70° C
Relative humidity (RH)	10% to 90%	10% to 90%
Permissible air pressure	450 hPa to 1100 hPa	
Permissible temperature fluctuation	10° C/30 min. (without condensation) or 0.5° C/min.	
Vibrations in acc. w. IEC 68-2-6 Test FC, 20 cycles in 3 axes, approx. 11 min. per cycle	10 Hz to 61 Hz: 0.2 mm amplitude 61 Hz to 500 Hz: 2 g	5 Hz to 8 Hz: 7.5 mm amplitude 8 Hz to 500 Hz: 1 g
Shock	IEC 68-2-27 Test E/A 3 times per axis 2 directions per axis total of 18 impacts 15 g/11 msec	IEC 68-2-29 per 1000 impacts at 6 levels 25 g/6 msec

2.8 Recommended Accessories

SMP16-AKO

Auto-configuration software for MS-DOS and Windows for setting the SMP16 bus interface

Order number: 6AR1400-0FA10-3AA0

The product includes online help with a detailed description of the function and handling of the configuration software.

The files (SFT251.BGB and SFT251.BGT) which are required to set the board are available on the Internet under:
http://www.ad.siemens.de/sicomp/html_76/hotline.htm

SMD safety fuse

Order number: R451.750 (the Littlefuse company)

Figure 3.1 shows where the two fuses are located on the board.

3 Interfaces

3.1 Overview of the Interfaces

Pin	Design	Use
X1	Socket strip, 20-pin	Reserved
X2	Multi-point terminal strip, 96-pin	SMP16 bus interface
X3	Sub D socket, 15-pin	Input, counting channel 0
X4	Sub D socket, 15-pin	Input, counting channel 1
S1	DIP switch, 8-pin	Switch, 24 V technology ↔ RS 422, channel 0
S2	DIP switch, 8-pin	Switch, 24 V technology ↔ RS 422, channel 1

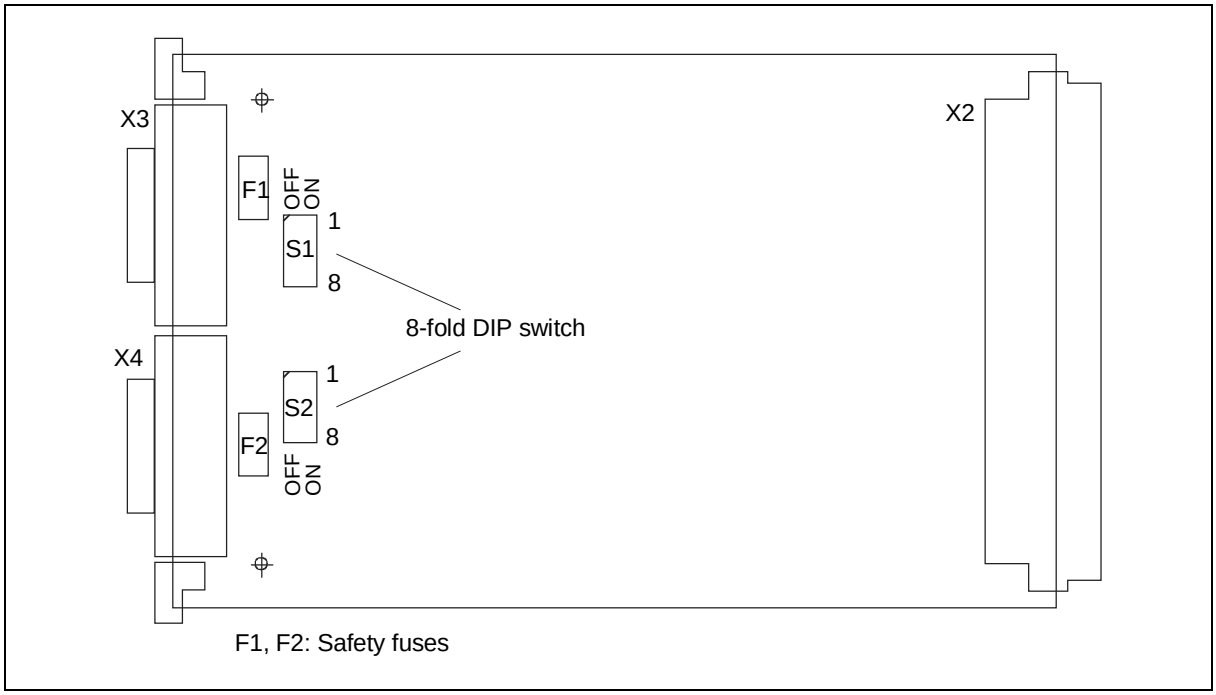


Figure 3.1 Overview of the connection and setting elements

3.2 Pin Connector X2 to SMP16 Bus

The following table shows the bus signals used by the board.

Pin	a	b	c
1	–	A16	–
2	–	A17	GND
3	–	**AEN**	+5 V
4	–	–	MMIO*
5	MEMCS16*	–	A12
6	RESET*	–	A0
7	–	–	A13
8	MEMR*	–	A1
9	RESIN*	–	A14
10	MEMW*	–	A2
11	–	**ACEN**	A15
12	RDYIN	–	A3
13	BUSEN	**ACDONE**	**INT0oNMI***
14	DB0	–	A4
15	–	+5 V	**INT1***
16	DB1	GND	A5
17	–	GND	**BS**
18	DB2	–	A6
19	–	–	**INT2***
20	DB3	–	A7
21	IOCS16*	–	**INT3***
22	DB4	DB8	A8
23	–	DB9	**INT4***
24	DB5	DB10	A9
25	–	DB11	**INT5***
26	DB6	DB12	A10
27	–	DB13	**INT0***
28	DB7	DB14	A11
29	–	DB15	**NMI***
30	IOW*	BHEN	IOR*
31	–	A18	GND
32	+5 V	A19	–

3.2.1 Signals for the Daisy Chain

ACEN,
ACDONE

Input (b11)
Output, open collector (b13)

The ACEN input signals a board that it has been selected for configuration of the ASBIC chip. Using the ACDON output, it indicates that it has finished its own configuration and the next board can be configured. See chapter 1.1.

3.2.2 Other Special Signals

AEN Address Enable, input (b3)

Control signal for PC compatible bus accesses, must be connected with AEN (b3) to the CPU slot for PC-I/O addressing (up to 3FFh).

BS "Board Select," input, TTL level (c17)
When low, this signal deactivates the board. However, the interrupts of the board still remain active.

Interrupts of the counting channels and extra inputs

INT0* Interrupt output, open collector (c27)
INT1* Interrupt output, open collector (c15)
INT2* Interrupt output, open collector (c19)
INT3* Interrupt output, open collector (c21)
INT4* Interrupt output, open collector (c23)
INT5* Interrupt output, open collector (c25)

INT0oNMI* Interrupt output, open collector (c13)
Interrupt INT0* is located here so that it is compatible with the SMP-E251. This interrupt is identical to the INT0* signal. Modern applications sometimes use this pin as NMI*. When, for instance, the SMP16-COM595 bus coupler and the SMP16-SFT251 are installed in the same slot for this reason, the INT0* signal must be switched off from this pin. See chapter 6.4.5. INT0* can always be taken from pin c27.

NMI* "Non Maskable Interrupt," output, open collector (c13)
Characteristics: low: 0.4 V/8 mA

Signalizes a hardware error of the ASBIC chipc or of the board.

3.3 I/O Connectors X3 and X4

The following table shows the assignment of the 15-pin, sub D socket strips X3 and X4.

Pin	Assignment	Pin	Assignment
1	VCC	9	An
2	VCC	10	GND
3	Bn*	11	ZS1n
4	An*	12	ZS0n
5	Nn	13	ZS3n
6	GND	14	ZS2n
7	Nn*	15	GNDn
8	Bn		

n = Channel number (0 or 1)

VCC 5 V encoder power (via 750 mA fine fuse from the system power supply)

GND Ground connection for shaft encoder signals

An Uninverted input of track A of channel n

An* Inverted input of track A of channel n

Bn Uninverted input of track B of channel n

B0* Inverted input of track B of channel n

Nn Uninverted input of track N of channel n

Nn* Inverted input of track N of channel n

ZS0n, ZS1n, ZS2n, ZS3n Extra inputs for channel n (see chapter 6.3.8 for a description)

GNDn Ground connection for the extra inputs of channel n (summation point)
This ground can be connected to system ground (GND) with switch S1.8.

Note:
The differential control lines (e.g., An and An*) must be twisted in pairs.

When single-ended connection of a shaft encoder with a 24 V interface is to be used, the inverted inputs (An*, Bn* and Nn*) of each signal (A, B, and N) must be connected to GND. The lines with the signals (An, Bn and Nn) must be twisted in pairs with the corresponding grounding line.

The lines of the extra inputs must be twisted in pairs with the corresponding grounding line.

3.4 Interface Switches S1 and S2

These two switches (S1 and S2) can be used to select the physical interface of the shaft encoder signals A, B and N for each channel. S1 is the selection switch for counting channel 0. S2 is the selection switch for counting channel 1.

Counting Channel 0		**Counting Channel 1**	
24 V technology	RS 422	24 V technology	RS 422
S1.1 to S1.7 = OFF	S1.1 to S1.7 = ON	S2.1 to S2.7 = OFF	S2.1 to S2.7 = ON

The two switches (S1.8 or S2.8) can be used to connect the grounding connection (GND0 or GND1) of the extra inputs of both counting channels to board ground.

Counting Channel 0	**Counting Channel 1**
Connect GND0 with GND	Connect GND1 with GND
S1.8 = ON	S2.8 = ON

Note:
This connection is provided for already existing applications with SMP-E251 for which pin 15 of plug connectors X3 and X4 was used as the grounding connection. In all other applications, this connection should be open.

4 Configuration with Software

The configuration data of the SMP16-SFT251 are stored by the ASBIC chip on the serial EEPROM of the board. The tables below show the default settings of the values which can be changed by the automatic configuration software SMP16-AKO.

Note:
The configuration data must be adjusted each time a system is changed by inserting or removing a board or module since the board or the module may not be able to be addressed otherwise.

Required settings in the "chip select channel 0 to 3" dialog fields

Channel	**0 (w)**	**1 (x)**	**2 (y)**	**3 (z)**
Setting	Enabled [1)]	**Enabled [1)]**	**Enabled [1)]**	**Enabled [1)]**
Address mode	**SMP-I/O**	**SMP-I/O**	**SMP-I/O**	**SMP-I/O**
Base address	**400 hex**	**420 hex**	**430 hex**	**440 hex**
Address range	32 bytes	8 bytes	16 bytes	16 bytes
Function	E251 function	Expanded function	Universal register, channel 0	Universal register, channel 1

Sample values shown in ***bold*** *type can be changed to meet the particular requirements.*

1) Default setting: Disabled

The base addresses must be whole-number multiples of the address area (e.g., for channel 0: 400h, 420h, 440h and so on).

Default settings in the "ASBIC channel settings" dialog field

Parameter	**Default Setting**
ASBIC channel	Disabled
Address mode	SMP-I/O
Base address	200 hex

Default settings in the "general" dialog field

Parameter	**Default Setting**
Parallel Output Port (POP)	0011 0000 bin
Memory address range	Includes MMIO range

Settings on the parallel output port

Bit	7	6	5	4	3	2	1	0	**Meaning:**
									Counting frequency, channel 0 (for frequency and pulse width measurement) 0: 2.5 or 4 MHz (depending on the operating mode) 1: 1.25 or 2 MHz (depending on the operating mode)
									Counting frequency, channel 1 (for frequency and pulse width measurement) 0: 2.5 or 4 MHz (depending on the operating mode) 1: 1.25 or 2 MHz (depending on the operating mode)
									Clock pulse supplied externally, channel 0 (With frequency and pulse width measurement, the counting clock pulse can be supplied externally.) 0: Internal 1: External
									Clock pulse supplied externally, channel 1 (With frequency and pulse width measurement, the counting clock pulse can be supplied externally.) 0: Internal 1: External
									Ext. strobe, channel 0 Enable N track (zero marking pulse) input. Otherwise ignore zero marking signals. 0: Switch off N track 1: Switch on N track (default)
									Ext. strobe, channel 1 Enable N track (zero marking pulse) input. Otherwise ignore zero marking signals. 0: Switch off N track 1: Switch on N track (default)
									Ext. clear, channel 0 Pulse on track N (zero marking pulse) resets the counter. 0: Function off 1: Function on
									Ext. clear, channel 1 Pulse on track N (zero marking pulse) resets the counter. 0: Function off 1: Function on

For more details on how to handle these settings, see chapter 6.3.

5 Compatibility with SMP-E251

The SMP-E251-compatible registers and functions are located on the SMP-SFT251 in the address area of ASBIC channel 0. Since the address assignment is the same as that of the SMP-E251, software compatibility between the SMP16-SFT251 and the SMP-E251 is ensured.
This compatibility is always ensured after a power-up or a hardware reset.

This address assignment can be changed with the BG_Mode board-mode bit in control register 0 (bit 4). For the new address assignment, see chapter 6.1. This address assignment was selected to permit the registers of ASBIC channel 0 to be addressed with faster 16-bit accesses. However this means that, although the functions of the SMP-E251 are retained, the address assignment is no longer compatible with the SMP-E251.

When replacing an SMP-E251 with an SMP16-SFT251, remember that the SMP16 board no longer has jumpers. The addresses and various board modes are set with the SMP16-AKO auto-configuration software. See chapter 2.8.
In addition, the physical design of the shaft encoder inputs is not the same as that of the SMP-E251. Switch S1 or S2 can be used to choose between RS 422 and 24 V technology. In contrast to the SMP-E251, the 24 V inputs of the SMP16-SFT251 require more current due to the optical decoupling. See chapter 2.3.

6 Programming the Board

6.1 Register Overview

The SMP16 bus-ASIC ASBIC can be used to implement 4 channels with different base addresses (base addresses w to z). Remember that the base addresses must be multiples of the length of the corresponding address area.

Example:
Base address w includes 32 bytes (1Fh) ⇒ Addresses 400h, 420h, 440h, etc. can be used for base address w.

ASBIC channel 0

There are two different address assignments for the registers of ASBIC channel 0. The "BG_Mode" board-mode bit in control register 0 (bit 4) can be used to run the board as compatible with the SMP-E251 or to use expanded functions (SMP-E251 or SMP16-SFT251 mode). The board is always in SMP-E251 mode (BG_Mode = "0") after power-up or a hardware reset.
When SMP-E251 is selected, ASBIC channel 0 (base address w) can only be addressed with 8-bit accesses. The resulting address assignment of ASBIC channel 0 is shown below.

Address Assignment (Hex)	**I/O Unit**	**Function**	
		Write	**Read**
Base Address w	Counter 0	SW strobe command [1)]	Interrupt register (counter 0)
w + 1		Counter byte 0 [1)]	Zero-marking-pulse buffer, byte 0
w + 2		Counter byte 1 [1)]	Zero-marking-pulse buffer, byte 1
w + 3		Counter byte 2 [1)]	Zero-marking-pulse buffer, byte 2
w + 4		Counter byte 3 [1)]	Zero-marking-pulse buffer, byte 3
w + 5		Mode register [1)]	Reserved
w + 6	Board control counters 0 and 1	Control register 0	Status register 0
w + 7		Reset alarm bits	Status register 1
w + 8	Counter 1	SW strobe command [1)]	Interrupt register (counter 1)
w + 9		Counter byte 0 [1)]	Zero-marking-pulse buffer, byte 0
w + A		Counter byte 1 [1)]	Zero-marking-pulse buffer, byte 1
w + B		Counter byte 2 [1)]	Zero-marking-pulse buffer, byte 2
w + C		Counter byte 3 [1)]	Zero-marking-pulse buffer, byte 3
w + D		Mode register [1)]	Reserved
w + E	Counter 0	SW clear command [1) 2)]	Reset zero-marking-pulse latch
w + F	Counter 1	SW clear command [1) 2)]	Reset zero-marking-pulse latch
w + 10	Board control	SW strobe command for both channels	Reserved
w + 11	Counter 0	Enable one-time counter [2)]	Cancel counter write protection [2)3)]
w + 12	Counter 1	Enable one-time counter [2)]	Cancel counter write protection [2)3)]
w + 13	Counters 0 and 1	Reserved	Disable one-time counter
w + 14	Board control	Enable zero-marking-pulse inputs	Reserved

Address Assignment (Hex)	I/O Unit	Function	
		Write	**Read**
w + 15	Counter 0	SW reload command [1]	Reserved
w + 16	Counter 1	SW reload command [1]	Reserved
w + 17 to 1F		Reserved	Reserved

1) Not possible when write protection is set

2) The access triggers the function. Use the value "00H" for write accesses. Use any value for read accesses.

3) When hardware support is activated, an arriving zero-marking-pulse signal triggers write protection. See chapter 6.3.4.

When expanded mode (BG_Mode = 1) is used, the registers in channel 0 can only be addressed with 16-bit accesses. The address assignment is shown below.

Address Assignment (Hex)	I/O Unit	Function	
		Write	**Read**
Base address w	Counter 0	Command register, low byte	Interrupt register (counter 0)
w + 1	Counter 1	Command register, high byte	Interrupt register (counter 1)
w + 2	Counter 0	Counter byte 0 [1]	Zero-mark.-pulse buffer, byte 0
w + 3		Counter byte 1 [1]	Zero-mark.-pulse buffer, byte 1
w + 4	Counter 0	Counter byte 2 [1]	Zero-mark.-pulse buffer, byte 2
w + 5		Counter byte 3 [1]	Zero-mark.-pulse buffer, byte 3
w + 6	Counter 1	Counter byte 0 [1]	Zero-mark.-pulse buffer, byte 0
w + 7		Counter byte 1 [1]	Zero-mark.-pulse buffer, byte 1
w + 8	Counter 1	Counter byte 2 [1]	Zero-mark.-pulse buffer, byte 2
w + 9		Counter byte 3 [1]	Zero-mark.-pulse buffer, byte 3
w + A	Control counter 0	Mode register [1], channel 0	Status register 0
w + B	Control counter 1	Mode register [1], channel 1	Status register 1
w + C	Board control	Control register 0	Reserved
w + D		"00000000b"	
w + E to 1F		Reserved	Reserved

1) Not possible when write protection is set

Caution

Some of the reserved addresses of ASBIC channel 0 are used for testing and factory settings. Never write access these areas since this might render the board useless.

ASBIC channel 1

Address Assignment (Hex)	I/O Unit	Function	
		Write	Read
Base address x	Board control	Control register 1 (low byte)	Control register 1 (low byte)
x + 1		Control register 1 (high byte)	Control register 1 (high byte)
x + 2	Board control	Control register 2 (low byte)	Control register 2 (low byte)
x + 3		Control register 2 (high byte)	Control register 2 (high byte)
x + 4	Board control	Interrupt mask (low byte)	Interrupt mask (low byte)
x + 5		Interrupt mask (high byte)	Interrupt mask (high byte)
x + 6	Board control	Clear register (low byte)	Status register 2 (low byte)
x + 7		Clear register (high byte)	Status register 2 (high byte)

ASBIC channel 2

Address Assignment (Hex)	I/O Unit	Function	
		Write	Read
Base address y	Channel 0 Universal register 0		UREG_00, byte 0
y + 1			UREG_00, byte 1
y + 2			UREG_00, byte 2
y + 3			UREG_00, byte 3
y + 4	Channel 0 Universal register 1	UREG_10, byte 0	UREG_10, byte 0
y + 5		UREG_10, byte 1	UREG_10, byte 1
y + 6		UREG_10, byte 2	UREG_10, byte 2
y + 7		UREG_10, byte 3	UREG_10, byte 3
y + 8	Channel 0 Universal register 2		UREG_20, byte 0
y + 9			UREG_20, byte 1
y + A			UREG_20, byte 2
y + B			UREG_20, byte 3
y + C to F		Reserved	Reserved

ASBIC channel 3

Address Assignment (Hex)	I/O Unit	Function	
		Write	**Read**
Base address z	Channel 1 Universal register 0		UREG_01, byte 0
z + 1			UREG_01, byte 1
z + 2			UREG_01, byte 2
z + 3			UREG_01, byte 3
z + 4	Channel 1 Universal register 1	UREG_11, byte 0	UREG_11 byte 0
z + 5		UREG_11, byte 1	UREG_11, byte 1
z + 6		UREG_11, byte 2	UREG_11, byte 2
z + 7		UREG_11, byte 3	UREG_11, byte 3
z + 8	Channel 1 Universal register 2		UREG_21, byte 0
z + 9			UREG_21, byte 1
z + A			UREG_21, byte 2
z + B			UREG_21, byte 3
z + C to F		Reserved	Reserved

Note:
ASBIC channels 1 to 3 can be addressed with both 8-bit and 16-bit accesses. With 8-bit accesses, the low byte must first be written to/read from the lower address and then the high byte written to/read from the higher address.

6.2 Reset Reactions

The board can be reset with a hardware reset via the SMP16 bus.

Status after reset/initialization

- All registers are cleared. Both counters are reset to "00000000hex."
- The front LEDs are off.

6.3 Function Description

6.3.1 Reading the Counter Status

The counter states cannot be read directly from the counter. Before the counter status can be read, it must be saved in a register. The "zero-marking-pulse-buffer" registers and the universal registers are used for this purpose. See chapter 6.1.

The counter status is transferred to the zero-marking-pulse buffer when a zero-marking pulse arrives or an SW-strobe occurs. Depending on the status of the BG_Mode bit, the buffer can then be read with byte or word-accesses (see chapter 6.1). The read sequence is unimportant.

Note:
SW strobe will only work with operating mode "position acquisition with hardware support" when write protection of the particular channel is disabled (see chapter 6.3.4).

Chapters 6.3.8 and 6.3.9 explain how the universal registers function.

6.3.2 Loading the Counters

Both counters can be preloaded with start values. A counter-load register is assigned to each counter for this purpose. The data that will be loaded to the counter are intermediately stored in this register until the next loading procedure occurs. Actual loading of the counter differs depending on the status of the BG_Mode board mode bit (see also chapter 6.4.2).

BG_Mode = "0"

In this case, the counter can only be addressed with 8-bit accesses as described in chapter 6.1. Each byte is loaded directly to the counter. The order in which the bytes are written to the counter is unimportant.

Note:
In this board mode, the counters should only be loaded when no counting signals are queued on the inputs. Otherwise, the counter states may no longer be consistent.

BG_Mode = "1"

In this board mode, ASBIC channel 0 can only be addressed with 16-bit accesses (see chapter 6.1). The data must be written to the address of the counters in the following order: high word first (counter bits 16 to 31) and low word second (counter bits 0 to 15). The high word is first stored intermediately in the counter-load register. Not until the low word is loaded to the counter is the counter synchronously loaded with all 32 bits. This type of counter loading ensures that all four counter bytes arrive at the counter at the same time and that all four bytes are available simultaneously for the counting procedure. This makes it possible to load the counter synchronously even during running operation.

Note:
Loading the counters will only work with operating mode "position acquisition with hardware support" when write protection of the particular channel is disabled (see chap. 6.3.4).

6.3.3 Position Acquisition via Shaft Encoder Edge Evaluation

A two-track incremental shaft encoder with zero-marking track can be connected to each channel (see also chapter 2.5.1). The counting impulses and counting direction are determined from the signals of the A and B tracks. This is done by evaluating the edges of the individual tracks.
The following figure illustrates this principle.

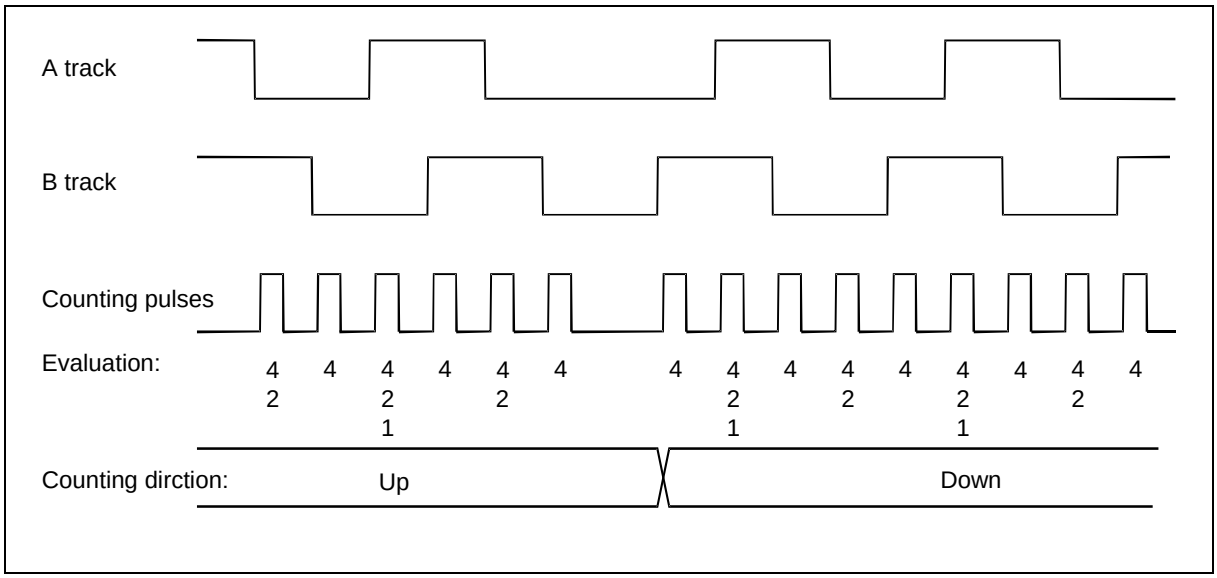


Figure 6.1 Shaft encoder edge evaluation

The counting direction is determined by the relationship of the A track to the B track. The number of counting pulses depends on which type of edge evaluation was set in the mode registers of the counters (see chapter 6.4.1).

- Quadruple edge evaluation counts each edge on the A and the B tracks.
- Double edge evaluation only counts the change in edge on the A track.
- Single edge evaluation only counts the rising edge of the A track.

Note:
With single edge evaluation, the counter may drift off slowly in one counting direction (due to operating mode) even the shaft encoder axis is at a standstill. This occurs when vibrations from the plant cause the shaft encoder to always have an edge change on the A track.

The hysteresis function which can be activated in the mode registers of the counters (see also chap. 6.3.11) can be used to counteract this behavior and suppress the first counting pulse after a reverse in the direction of rotation. The following figure illustrates use of the hysteresis function.

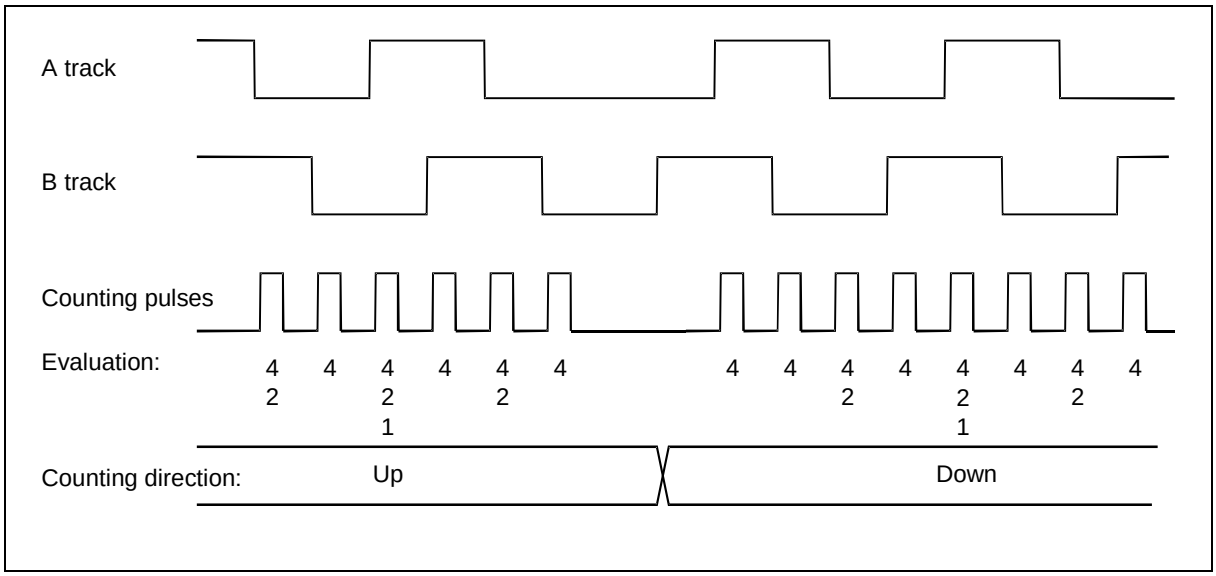


Figure 6.2 Shaft encoder edge evaluation with the hysteresis function

6.3.4 Position Acquisition with Hardware Support

In this mode, the board offers the user support in processing the registers. The zero-marking-pulse input of the respective channel plays an important role. An arriving zero marking pulse triggers the following events on the board.

- The current counter status is stored in the zero-marking-pulse buffer where it can then be read.
- Counter write protection is set so that the zero-marking-pulse buffer cannot be overwritten by an event. (It cannot be overwritten by a zero-marking-pulse signal or SW strobe.) The counter itself is also protected from write accesses or "clear" events (see chapter 6.3.10). Write protection can be reset with the "cancel counter write protection" command (see chapter 6.3.7).
- The following status bits are set for each of the two counting channels.

Status Bits, Counting Channel 0	**Status Bits, Counting Channel 1**
SCH0 (status register 0, bit 3)	SCH1 (status register 0, bit 2)
REF0 (status register 0, bit 0)	REF1 (status register 0, bit 1)
Q0 (status register 1, bit 6)	Q1 (status register 1, bit 7)
INT (interrupt register, counting channel 0)	INT (interrupt register, counting channel 1)

The meaning of these signals is described in chapter 6.4.

The "one-time" and "cyclic" modes

When hardware support is activated, you can choose between "one-time" and "cyclic" mode. With one-time mode (control register 0, bit 3 = "0" for counting channel 0 or bit 1 = "0" for counting channel 1) the one-time counter is set when a zero marking pulse arrives. This prevents (also with counter write protection disabled) additional zero-marking pulses from being registered and overwriting the zero-marking-pulse buffer.The zero-marking-pulse input is enabled again with the "enable one-time counter" command for the particular counting channel.
Only zero-marking-pulse signals are disabled while the one-time counter is set. Write accesses to the counter and commands (SW strobe, SW clear, etc.) can continue to be performed if counter write protection is canceled.

The one-time counter is not used during cyclic mode and is also not set.

Note:
Hysteresis can be used for the zero-marking-pulse logic (see chapter 6.3.11).

6.3.4.1 Preparing for Position Acquisition with Hardware Support

- The "ext. strobe channel n" bit of the respective channel must be set on the parallel output port of the ASBIC. For default settings, see chapter 4.
- The zero-marking-pulse inputs must be enabled with the appropriate command (see chapter 6.3.7).

These measures enable the zero-marking-pulse signals of the shaft encoder for the logic.

- Counter write protection must then be disabled with a command afterwards (see chapter 6.3.7).
- Control register 0 must be programmed (see chapter 6.4.2).
  – Enable or disable interrupts INT0 or INT1.
  – Specify board mode.
  – Select one-time or cyclic mode for each channel.
  – Enable hardware support for each channel.
- The mode registers of the two channels must be programmed (see chapter 6.4.1).
  – Set position acquisition.
  – Enable/disable hysteresis function.
  – Select edge evaluation.
- When hardware support is activated, the one-time counter must be enabled with a command (see chapter 6.3.7).

Note:
Shaft encoders trigger the zero-marking pulse once for each revolution. The same number of counting pulses are always supplied between two zero-marking pulses. For instance, when quadruple edge evaluation is used, a shaft encoder that supplies 5000 pulses on the A and B tracks per revolution would increment or decrement the counter by 20,000 counting pulses for each revolution. Since the board synchronizes all external signals, the counter difference between two zero-marking pulses may vary by ± 1 increment (i.e., in the above example, the difference of the counter states between two zero-marking pulses may fluctuate between 19,999 and 20,001). However, these fluctuations cancel each other out when all pulses are added together.

6.3.5 Position Acquisition without Hardware Support

The primary difference between this mode and "position acquisition with hardware support" mode is that the arrival of a zero-marking pulse does not trigger write protection. This means that the counter and the zero-marking-pulse buffer can still be modified with write accesses or commands (e.g., SW strobe) even after a zero-marking pulse has arrived.

The arrival of a zero-marking pulse triggers the following events.

- The current counter state is stored in the zero-marking-pulse buffer.
- The following status bits are set in each of the two counting channels.

Status Bits, Counting Channel 0	Status Bits, Counting Channel 1
REF0 (status register 0, Bit 0)	REF1 (status register 0, bit 1)
Q0 (status register 1, bit 6)	Q1 (status register 1, bit 7)
INT (interrupt register, counting channel 0)	INT (interrupt register, counting channel 1)

The meaning of these signals is described in chapter 6.4.

To be able to receive zero-marking pulses again, the zero-marking-pulse latch of the respective channel must be reset with the "reset zero-marking-pulse latch" command.

Note:
Hysteresis can be used for the zero-marking-pulse logic (see chapter 6.3.11).

6.3.5.1 Preparing for Position Acquisition without Hardware Support

Since this mode does not require an evaluation of the zero-marking pulse, the following two steps (activation of the zero-marking-pulse inputs) are not absolutely necessary.

- The "ext. strobe channel n" bit of the particular channel must be set (for default setting, see chapter 4) on the parallel output port of the ASBIC.
- The zero-marking-pulse inputs must be enabled with the appropriate command (see chapter 6.3.7).

These measures enable the zero-marking-pulse signals of the shaft encoders for the logic.

- Counter write protection must then be canceled with a command afterwards (see chapter 6.3.7).
- Control register 0 must be programmed (see chapter 6.4.2).
  – Enable or disable interrupts INT0 or INT1.
  – Specify the board mode.
  – Disable hardware support for each channel.
- The mode registers of both channels must be programmed (see chapter 6.4.1).
  – Set position acquisition.
  – Enable/disable hysteresis function.
  – Select edge evaluation.

Note:
The shaft encoders trigger the zero-marking pulse once with each revolution. The same number of counting pulses is always supplied between two zero-marking pulses. For instance, a shaft encoder that supplies 5000 pulses to the A and B tracks for each revolution increments or decrements the counter by 20,000 counting pulses when quadruple edge evaluation is used. Since the board synchronizes all external signals, the counter difference between two zero-marking pulses may vary by ± 1 increment (i.e., in the example above, the difference of the counter states between two zero-marking pulses may fluctuate between 19,999 and 20,001). However, these fluctuations cancel each other out when all increments are added up.

6.3.6 Frequency and Pulse Width Measurement

The counters of the SMP16-SFT251 can measure frequencies or pulse widths. This operating mode can be set for each counter in the appropriate mode register (see chapter 6.4.1).

Frequency measurement

A gate (differential) is applied on the B input of the counter. The counter is ready to count while this gate is open (logical "1"). The frequency to be measured is applied (differential) to the A input of the counter. If the time during which the gate is open is known (t_B), the frequency of A can be determined from the counter state which was counted while the gate was open.

f_A = Counter state / t_B

Pulse width measurement

During pulse width measurement, the pulse to be measured is applied (differential) on the B input. The counter is ready to count as long as the pulse is active (logical "1"). The counter can be clock-pulsed for this with the internal counting frequencies. The width of this pulse can be determined from the values of the counting frequency (f) and the counter status.

t_B = Counter status * f

6.3.6.1 Preparing for Frequency and Pulse Width Measurement

The counter requires a clock-pulse signal and a gate signal for this application.

- The gate signal must be a differential signal. It is connected to the B input of the counting channel.
- An external or internal clock-pulse signal can be used. When an external clock pulse is used, connection of the clock-pulse signal to the A connections of the respective counting channel must be differential (see also chapter 2.5.2). Bit 2 (counting channel 0) or bit 3 (counting channel 1) must be set for this on the parallel output port of the ASBIC (see chapter 4). When the internal clock pulses are used, four different internal clock pulses are available. These clock pulses vary depending on the BG_Mode bit in control register 0 (see chapter 6.4.2) and the configuration bits "counting frequency, channel 0" (counting channel 0) or "counting frequency, channel 1" (counting channel 1) on the parallel output port of the ASBIC.

BG_Mode	"Counting Frequency, Channel n" = "0"	"Counting Frequency, Channel n" = "1"
0	2.5 MHz	1.25 MHz
1	4 MHz	2 MHz

Frequency measurement The frequency to be measured is supplied externally. A reference gate signal with the desired accuracy must be provided on the gate input.

Pulse width measurement The pulse to be measured corresponds to the gate signal. As already described above, either an external source or the internal clock pulse can be used as the measuring frequency.

6.3.6.2 Gating

The gate can be generated differently depending on the TOR_MD bit (gate mode, see chapter 6.4.1).

TOR_MD = "0" (level-controlled)

The gate is active as long as the gate input is high. Pulse width measurement should only use this mode.

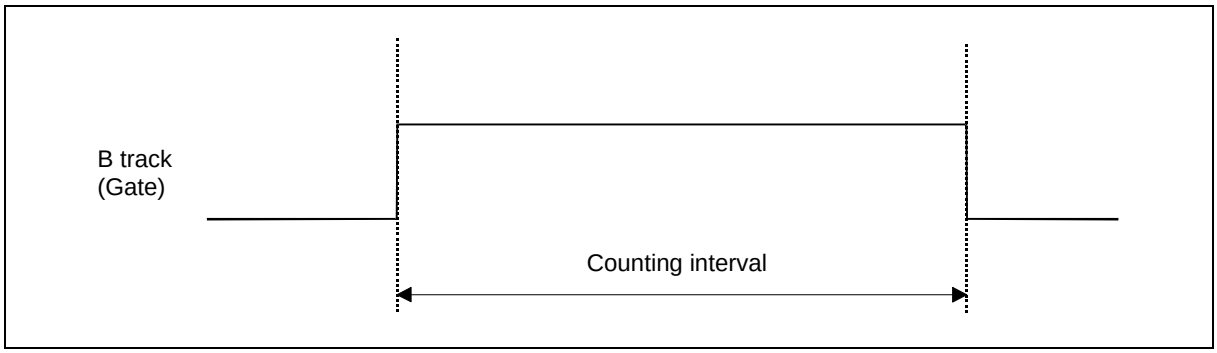


Figure 6.3 Gating with TOR_MD = "0"

TOR_MD = "1" (edge-controlled)

A rising edge on the gate input activates the gate. An additional rising edge on the gate input deactivates the gate again.

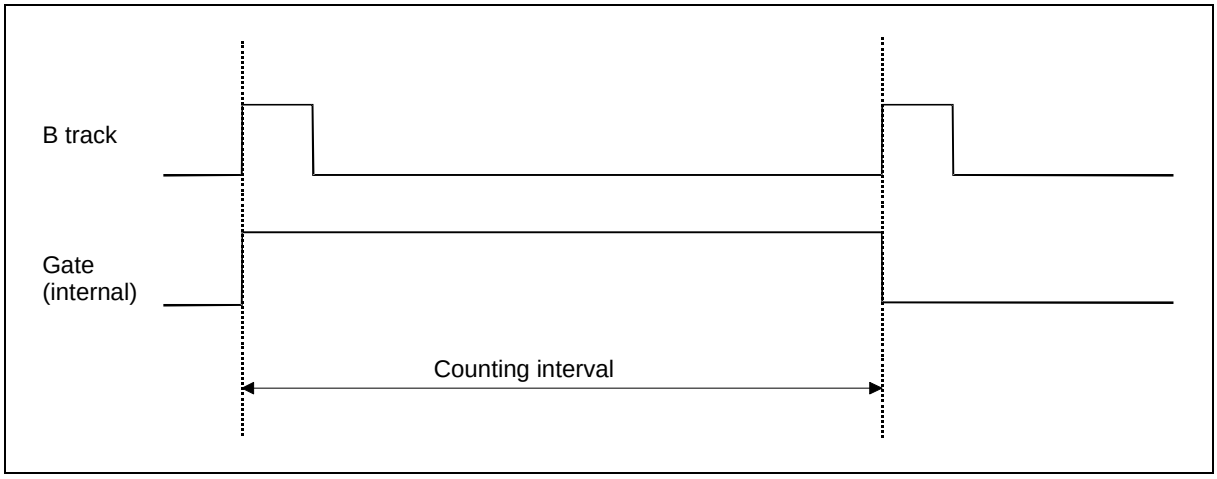


Figure 6.4 Gating with TOR_MD = "1"

While the gate is active, status bit TOR0 or TOR1 is set in status registers 1 or 2.

6.3.6.3 How Frequency and Pulse Width Measurement Is Handled

The impulses of the external or internal clock pulse are counted during gate time (see chapter 6.3.6.2). An open gate is indicated by the "TOR0" status bit in status register 1 (counting channel 0) or the "TOR1" status bit in status register 2 (counting channel 1). At the end of the gate, the counter status can be transferred with a rising edge on the zero-marking-pulse input or an SW strobe in the zero-marking-pulse buffer.

With use of the zero-marking-pulse input

If the zero-marking pulse signal is to be used to save the counter status at the end of the measurement, the applicable counting channel can be used as with the "position acquisition with hardware support" mode (see chapter 6.3.4). Only the "frequency and pulse width measurement" mode needs to be set in the mode register.

In addition, the reset functions of the zero-marking pulse of the respective counting channel can be activated on the parallel output port ("ext. clear channel n"). In this case, the arrival of a zero-marking pulse would first store the counter state in the zero-marking-pulse buffer and then reset the counter (see chapter 4). This function is recommended for frequency or pulse width measurement.

The zero-marking-pulse input must be connected differently to the gate signal depending on which gate mode is set.

- For TOR_MD = "0"
  Connection of the gate signal to the zero-marking-pulse input is inverted (i.e., the uninverted input of B must be connected to the inverted input of N, and the inverted B input must be connected to the uninverted N input).
- For TOR_MD = "1"
  The gate signal must be connected parallel to the zero-marking-pulse input.

TOR_MD = "0": The rising edge on the zero-marking-pulse input at the end of the gate causes the counter state to be saved in the zero-marking-pulse buffer. Counting write protection is set at the same time for the applicable counting channel. If desired, the counter can be reset after its state has been saved in the zero-marking-pulse buffer.

TOR_MD = "1": A rising edge is generated on the zero-marking-pulse input with both the start impulse and the stop impulse. After the start impulse, the counter write protection triggered by this impulse must be canceled immediately so that the rising edge can be detected on the zero-marking-pulse input when the stop impulse occurs. The counter state after the stop impulse is the measuring result, and the counter state after the start impulse is ignored.

Program processing for this mode is the same as that of the "position acquisition with hardware support" mode (see chapter 6.3.4).

Without use of the zero-marking-pulse input

Another way to perform the measurement is to scan gate status bit TOR0 or TOR1. It must be ensured that the counter is reset at the beginning of the measurement. The TOR0 or TOR1 bits can then be polled to determine whether the gate on the respective B input is still open or is already closed. When the gate is closed, the counter state can be transferred to the zero-marking-pulse buffer with an SW strobe and then read.

6.3.7 Overview of the Commands

The following commands can be sent to the board controller with ASBIC channel 0.

Command	Function
Enable zero-marking-pulse inputs (chan. 0 and chan. 1)	The zero-marking-pulse inputs of both counting channels are activated and remain active until the next hardware reset or power-up.
Enable one-time counter (channel 0 or channel 1)	An arriving zero-marking pulse disables the one-time counter during one-time mode. All other zero-marking pulses are then ignored. This command re-enables the one-time counter.
Disable one-time counter (chan. 0 and chan. 1)	The one-time counter is disabled, and the zero-marking-pulse signals are then ignored.
Cancel counter write protection (channel 0 or channel 1)	Cancels counter write protection for the respective channel (see chapter 6.3.4).
SW strobe (chan. 0 or chan. 1 or both at the same time)	The contents of the counter of the respective counting channel are transferred to the zero-marking-pulse buffer from where the counter state can be read. The command is only effective when counter write protection of the respective channel is not active.
Reset zero-marking-pulse latch (channel 0 or channel 1)	Arrival of a zero-marking pulse sets the zero-marking-pulse latch. The latch can be canceled (separately for each counting channel) with this command.
SW clear (channel 0 or channel 1)	Reset the counter status to "00000000hex" The command is only effective when counter write protection of the respective channel is not active.
SW reload (channel 0 or channel 1)	Resets the counter status to the contents of the applicable counter load register (see chapter 6.3.2) The command is only effective when counter write protection of the respective channel is not active.
Reset alarm bits	Resets status bits ZS00, ZS20, ZS01, ZS21, Q1, Q0, CB1, and CB0 (see chapter 6.4.10)

The address of ASBIC channel 0 varies with the status of the BG_mode board mode bit (control register 0, bit 4).
This also applies to the commands listed above.

- When BG_Mode = "0," the commands are called with read or write accesses to certain addresses in the ASBIC channel 0 area. For more information, see chapter 6.1.
- When BG_Mode = "1," the commands are generated by write accesses to the command register (ASBIC channel 0, base address w). Each data bit has a special meaning. See table below.

Data Bit	Command
0	Enable zero-marking-pulse inputs
1	Reserved
2	Reset zero-marking-pulse latch for channel 0
3	Reset zero-marking-pulse latch for channel 1
4	Enable one-time counter for channel 0
5	Enable one-time counter for channel 1
6	Disable one-time counter
7	Reset alarm bits
8	SW clear, channel 0
9	SW clear, channel 1
10	SW reload, channel 0
11	SW reload, channel 1
12	Cancel counter write protection for channel 0
13	Cancel counter write protection for channel 1
14	SW strobe, channel 0
15	SW strobe, channel 1

Note:
This type of command generation permits several commands to be executed simultaneously. Commands for one channel can be called at the same time as commands for the other channel since the channels are not dependent on each other. Several commands can also be executed simultaneously within one channel. However, caution is required since the sequence of the commands is then undefined. This applies particularly to the commands "SW strobe," "SW clear," "SW reload," and "cancel counter write protection." These commands should never be executed together with other commands of the same channel.

6.3.8 Extra Inputs ZS00 to ZS30 (Counting Channel 0) or ZS01 to ZS31 (Counting Channel 1)

The functions of the signals are programmed in control register 1 or control register 2 (see chapter 6.4.3 or chapter 6.4.4). The functions are listed in the following table.

Signal	Interrupt Function	Counter Function
ZS00	Signal can trigger INT1 request.	Save counter state in universal register UREG_00
ZS10	Signal can trigger INT2 request.	Save counter state in universal register UREG_10
ZS20	Signal can trigger INT1 request.	Save counter state in universal register UREG_20
ZS30	Signal can trigger INT2 request.	Reset counter of channel 0 (see also chapter 6.3.10)
ZS01	Signal can trigger INT1 request.	Save counter state in universal register UREG_01
ZS11	Signal can trigger INT3 request.	Save counter state in universal register UREG_11
ZS21	Signal can trigger INT1 request.	Save counter state in universal register UREG_21
ZS31	Signal can trigger INT3 request.	Reset counter of channel 1 (see also chapter 6.3.10)

The types of functions can be set individually for each signal.

For reasons of compatibility, status signals ZS00, ZS20 or ZS01, ZS21 are located in status register 1, and the INT1 trigger can be enabled/disabled in control register 0 (bit 5, LAX).

6.3.9 The Universal Registers

In addition to the 32-bit, zero-marking-pulse buffer, the SMP16-SFT251 contains three more 32-bit universal registers for each channel.

The following table lists the functions of the registers (see also chapter 6.3.8).

Register	Comparator Function	Counter Function
UREG_00		Accept counter status of counter 0 at ZS00 trigger
UREG_10	Comparator function with counter of channel 0	Accept counter status of counter 0 at ZS10 trigger
UREG_20		Accept counter status of counter 0 at ZS20 trigger
UREG_01		Accept counter status of counter 1 at ZS01 trigger
UREG_11	Comparator function with counter of channel 1	Accept counter status of counter 1 at ZS11 trigger
UREG_21		Accept counter status of counter 1 at ZS21 trigger

The registers UREG_10 and UREG_11 provide the comparator function in addition to the counting buffer function. The contents of the registers are continuously compared (using a comparator) with the current counter status of the related counter. When equal, an appropriate bit is set in status register 2 (bit 3 CR_10 for channel 0, bit 11 CR_11 for channel 1 - see chapter 6.4.9). In addition, an INT4 interrupt can be triggered for channel 0, and an INT5 interrupt can be triggered for channel 1. The comparator output can also be used to reset the related counter (see chapter 6.3.10). This makes it possible to have a counter always count within a specified range.

Registers UREG_10 and UREG_11 can also be written with certain values for the comparator function.

Note:
Hysteresis can be used for the comparator function (see chapter 6.3.11).

6.3.10 The Clear Functions

Various mechanisms can be used to reset the counter of a channel. The CLR_MD0 control bits in control register 1 or the CLR_MD1 control bits in control register 2 can be used to select whether the arrival of a reset event is to set the counter to "00000000h" ("set counter to zero") or to a certain value which is stored intermediately ("reload for clear") in the counter load register (see chapter 6.3.2).

The following table provides information on how to trigger a reset function and the modes which can be set.

Trigger	**Activation**	**Available Function Mode**	
		"Set Counter to Zero"	**"Reload for Clear"**
Arriving zero-marking pulse of the shaft encoder	Bit 6 (channel 0) or bit 7 (channel 1) on the parallel output port of the ASBIC	Bit 10 (CLR_MD) = "0" in control register 1 or 2	Bit 10 (CLR_MD) = "1" in control register 1 or 2
Counter equal to universal register UREG_10 (channel 0) or UREG_11 (channel 1)	Bit 9 (CR1n_CLR) in control register 1 or 2 [1)]	Bit 10 (CLR_MD) = "0" in control register 1 or 2	Bit 10 (CLR_MD) = "1" in control register 1 or 2
Special signal ZS30 (channel 0) or ZS31 (channel 1)	Bit 8 (ZS3n_CLR) in control register 1 or 2 [1)]	Bit 10 (CLR_MD) = "0" in control register 1 or 2	Bit 10 (CLR_MD) = "1" in control register 1 or 2
SW clear (channel 0 or 1)	Always active	Sets the counter to "00000000"	-------
SW reload (channel 0 or 1)	Always active	-------	Loads the counter with the contents of the counter load register

1) n = channel number (0 or 1)

6.3.11 The Hysteresis Functions

If the shaft encoders are subjected to vibration, this vibration may cause counting pulses or zero-marking-pulse signals to be generated even when the shaft encoder axis is at a standstill. To correct this situation, three different hysteresis functions are available for use on each channel.

1. Hysteresis for reversal of direction of rotation
   When this hysteresis is activated, the first counting pulse is suppressed when the direction of rotation is reversed. This minimizes fluctuation around a counter status when the shaft encoder axis is at a standstill.

2. Zero-marking-pulse hysteresis
   This hysteresis does not enable the zero-marking-pulse logic again until the counter status has moved two counting pulses in one direction after a zero-marking pulse has arrived. This type of hysteresis is recommended when the zero-marking-pulse signal is used to trigger interrupts. Otherwise, if the shaft encoder came to a stop precisely on the zero-marking pulse and vibration caused zero-marking-pulse signals to be triggered continuously, this could then result in an avalanche of interrupts.
   This hysteresis can only be activated together with the hysteresis for reversal of the direction of rotation.

3. Comparator hysteresis
   This hysteresis does not enable the comparator logic again until the counter status has moved two counting pulses in one direction after the comparator value has been reached. This type of hysteresis is recommended when the comparator is used to trigger interrupts. Otherwise, if the shaft encoder stopped when the counter status was exactly the same as the comparator value, vibration might continuously trigger comparator interrupts.
   This type of hysteresis can only be activated together with the hysteresis for reversal of the direction of rotation.

The hysteresis cannot be activated in "frequency and pulse width measurement" mode.

The following table shows how to activate the individual hysteresis functions.

Hysteresis Function	**Activation**
Hysteresis for reversal of the direction of rotation	Set bit 5 (HZ) in the mode register of the applicable channel. See chapter 6.4.1.
Zero-marking-pulse hysteresis	Set bit 5 (HZ) in the mode register of the applicable channel. See chapter 6.4.1. Set bit 12 (REF0_HYST) in control register 1 (counting channel 0), or set bit 12 (REF1_HYST) in control register 2 (counting channel 1). See chapter 6.4.3 or 6.4.4.
Comparator hysteresis	Set bit 5 (HZ) in the mode register of the applicable channel. See chapter 6.4.1. Set bit 11 (KOMP0_HYST) in control register 1 (counting channel 0), or set bit 11 (KOMP1_HYST) in control register 2 (counting channel 1). See chapter 6.4.3 or 6.4.4.

6.3.12 Switching the Two Counting Channels in Parallel

The two counters can be switched in parallel (i.e., track signals A, B and N of counting channel 0 can be switched to the counter of counting channel 1). However, this leaves the track signals of counting channel 1 without any function. This setting requires that bit K02K1 be set in control register 2 (bit 7). See chapter 6.4.4.
Special signals ZS00, ZS10 and ZS20 of counting channel 0 can be connected to counting channel 1. This can then be used to trigger the universal registers of counting channel 1 with the special signals of channel 1 and channel 0. For the assignment of signals ZS00 to ZS20 to the individual universal registers and the activation of this parallel circuit, see the description of control register 2 (chapter 6.4.4).

6.3.13 Interrupts

The following interrupts are available.

Interrupt	Source	Reset [1)]	Masking	Status Bits
INT0	Zero-marking pulse of channel 0 or channel 1	Read the applicable zero-marking-pulse buffer Or in the clear register: Bit 0 (CLR_INT0_0) = "1" or Bit 8 (CLR_INT0_1) = "1"	Bit 7 (channel 0) and Bit 6 (channel 1) in control register 0	Bit 0 of the INT registers of channel 0 or channel 1 or bit 0 (channel 0) and bit 1 (channel 1) in status register 0
INT1	Rising edge on ZS00, ZS20, ZS01 or ZS21	"Reset alarm bits" command Or in clear register: Bit 1 (CLR_INT1_00) = "1," Bit 2 (CLR_INT1_20) = "1," Bit 9 (CLR_INT1_01) = "1," or Bit 10 (CLR_INT1_21) = "1"	Bit 5 (LAX) of control register 0 (for all signals)	Bits 4 to 7 in status register 0
INT2	Rising edge on ZS10 or ZS30 or Overflow CB0 of counter channel 0	In clear register: Bit 3 (CLR_INT2_10) = "1," Bit 4 (CLR_INT2_30) = "1," or Bit 5 (CLR_INT2_CB0) = "1"	Bits 0 to 2 in interrupt mask	Bits 0 to 2 in status register 2
INT3	Rising edge on ZS11 or ZS31 or Overflow CB1 of counter channel 1	In clear register: Bit 11 (CLR_INT3_11) = "1," Bit 12 (CLR_INT3_31) = "1," or Bit 13 (CLR_INT3_CB1) = "1"	Bits 8 to 10 in interrupt mask	Bits 8 to 10 in status register 2
INT4	Comparator of counting channel 0	In clear register: Bit 6 (CLR_INT4_CR0) = "1"	Bit 3 in interrupt mask	Bit 3 in status register 2
INT5	Comparator of counting channel 1	In clear register: Bit 14 (CLR_INT5_CR1) = "1"	Bit 11 in interrupt mask	Bit 11 in status register 2

1) The clear register is described in more detail in chapter 6.4.10.

6.4 Description of the Registers

6.4.1 Mode Registers, Channel 0 and Channel 1

The mode registers have different addresses depending on the status of the BG_Mode bit in control register 0 (bit 4).

BG_Mode	Address Mode Register, Counting Channel 0	Address Mode Register, Counting Channel 1
0	w + 5	w + D
1	w + A	w + B

Bit	7	6	5	4	3	2	1	0
Name	PD	TOR_MD	HZ	0	Edge evaluation			

PD Operating mode
- 0 Position acquisition (shaft encoder evaluation)
- 1 Frequency and pulse width measurement

TOR_MD Gate mode for frequency and pulse width measurement
- 0 Counter continues running as long as the gate input is active.
- 1 Counter starts at rising gate edge and stops with the next one.

HZ Specifies whether the hysteresis is enabled for position acquisition
The direction of counting is specified for frequency and pulse width measurement.
- 0 Hysteresis off/counting up
- 1 Hysteresis on/counting down

Edge evaluation For position acquisition
- 0000 Quadruple edge evaluation
- 0001 Double edge evaluation
- 0101 Single edge evaluation

6.4.2 Control Register 0

Control register 0 has a different address depending on the BG_Mode bit in control register 0 (bit 4).

BG_Mode	Address, Control Register 0	Remarks
0	w + 6	
1	w + C	Fill bits 8 to 15 with "00hex"

Bit	7	6	5	4	3	2	1	0
Name	REFI0	REFI1	LAX	BG_Mode	EPB0	HWU0	EPB1	HWU1

REFI0 Masks out the counter interrupt of channel 0 from group interrupt INT0

0 Counter interrupt channel 0 disabled

1 Counter interrupt channel 0 enabled

REFI1 Masks out the counter interrupt of channel 1 from group interrupt INT0

0 Counter interrupt channel 1 disabled

1 Counter interrupt channel 1 enabled

LAX Simultaneously masks out the interrupt requests of inputs ZS00, ZS20, ZS01, and ZS21 from group interrupt INT1

0 INT1 disabled

1 INT1 enabled

BG_Mode Board mode
Switches the board to SMP16-SFT251 mode. In this mode, the board is no longer compatible with the SMP-E251. This mode provides an increased scope of functions.
The address location of ASBIC channel 0 differs depending on the status of this bit.

0 SMP16-SFT251 mode off

1 SMP16-SFT251 mode on

EPB0 One-time/cyclic operation of the hardware support, channel 0

0 One-time operation

1 Cyclic operation

HWU0 Hardware support, channel 0

0 With hardware support

1 Without hardware support

EPB1 One-time/cyclic operation of the hardware support, channel 1

0 One-time operation

1 Cyclic operation

HWU1 Hardware support, channel 1

0 With hardware support

1 Without hardware support

6.4.3 Control Register 1 (16-Bit Register, Addresses x and x+1)

Control register 1 can be read and written with both 16-bit and 8-bit accesses. The special signals and functions of channel 0 can be set in this register. The functions of this register are more extensive than the functions of the SMP-E251.

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	x	x	x	x	x	TR20	TR10	TR00
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	x	x	x	REF0_HYST	KOMP0_HYST	CLR_MD0	CR10_CLR	ZS30_CLR

TR00 Activates the trigger function of ZS00. This can be used to load the current counter status to register UREG_00 when a rising edge occurs on ZS00.

0 Trigger function off

1 Trigger function on

TR10 Activates the trigger function of ZS10. This can be used to load the current counter status to register UREG_10 when a rising edge occurs on ZS10.

0 Trigger function off

1 Trigger function on

TR20 Activates the trigger function of ZS20. This can be used to load the current counter status to register UREG_20 when a rising edge occurs on ZS20.

0 Trigger function off

1 Trigger function on

ZS30_CLR Activates the reset function of ZS30. A rising edge on ZS30 resets the counter of channel 0.

0 Reset function disabled

1 Reset function enabled

CR10_CLR Activates the reset function of the comparator of channel 0
The counter can be reset with this when the contents of register UREG_10 match the current counter status of channel 0.

0 Reset function of comparator CR10 disabled

1 Reset function of comparator CR10 enabled

CLR_MD0 Specifies the reset mode of channel 0 (see chapter 6.3.10)

0 When a reset event occurs, the counter is set to "00000000."

1 When a reset event occurs, the counter is loaded with the contents of the counter-load register.

KOMP0_ HYST Activates the hysteresis of comparator CR10 (only works when the hysteresis of channel 0 in mode register 0 is active: HZ = "1")

0 Comparator hysteresis off

1 Comparator hysteresis on

REF0_ HYST Activates the hysteresis of the zero-marking-pulse logic of channel 0 (only works when the hysteresis of channel 0 in mode register 0 is active: HZ = "1")

0 Zero-marking-pulse hysteresis off

1 Zero-marking-pulse hysteresis on

6.4.4 Control Register 2 (16-Bit Register, Addresses x+2 and x+3)

Control register 2 can be read and written with both 16-bit and 8-bit accesses. The special signals and functions of channel 1 can be set in this register.

Bit	7	6	5	4	3	2	1	0
Name	K02K1	x	TR20_P	TR10_P	TR00_P	TR21	TR11	TR01

TR01 Activates the trigger function of ZS01. This can be used to load the current counter status to register UREG_01 when a rising edge occurs on ZS01.

0 Trigger function off

1 Trigger function on

TR11 Activates the trigger function of ZS11. This can be used to load the current counter status to register UREG_11 when a rising edge occurs on ZS10.

0 Trigger function off

1 Trigger function on

TR21 Activates the trigger function of ZS21. This can be used to load the current counter status to register UREG_21 when a rising edge occurs on ZS21.

0 Trigger function off

1 Trigger function on

TR00_P Activates the trigger function of ZS00 for register UREG_01 of channel 1. This can be used to load the current counter status to register UREG_01 when a rising edge occurs on ZS00. The setting is not dependent on the status of TR01. If both bits are active, the two signals (ZS00 and ZS01) are evaluated in parallel.

0 Trigger function off

1 Trigger function on

TR10_P Activates the trigger function of ZS10 for register UREG_11 of channel 1. This can be used to load the current counter status to register UREG_11 when a rising edge occurs on ZS10. The setting is not dependent on the status of TR11. If both bits are active, the two signals (ZS10 and ZS11) are evaluated in parallel.

0 Trigger function off

1 Trigger function on

TR20_P Activates the trigger function of ZS20 for register UREG_21 of channel 1. This can be used to load the current counter status to register UREG_21 when a rising edge occurs on ZS20. The setting is not dependent on the status of TR21. If both bits are active, the two signals (ZS20 and ZS21) are evaluated in parallel.

0 Trigger function off

1 Trigger function on

K02K1 Switches shaft encoder inputs A, B and N from channel 0 to channel 1. This can be used to deactivate the shaft encoder inputs of channel 1.

0 Rerouting off

1 Rerouting on

Bit	15	14	13	12	11	10	9	8
Name	x	x	x	REF1_HYST	KOMP1_HYST	CLR_MD1	CR11_CLR	ZS31_CLR

ZS31_CLR Activates the reset function of ZS31. A rising edge on ZS31 resets the counter of channel 1.

0 Reset function disabled

1 Reset function enabled

CR11_CLR Activates the clear function of the comparator of channel 1.
When register UREG_11 equals the current counter status of channel 1, this can be used to reset the counter.

0 Reset function of comparator 1 (CR11) disabled

1 Reset function of comparator 1 (CR11) enabled

CLR_MD1 Specifies the reset mode for channel 1. See chapter 6.3.10.

0 When a reset event occurs, the counter is set to "00000000."

1 When a reset event occurs, the counter is loaded with the contents of the counter-load register.

KOMP1_ HYST Activates the hysteresis of comparator CR11 (only works when the hysteresis of channel 1 in mode register 1 is active). HZ = "1")

0 Comparator hysteresis off

1 Comparator hysteresis on

REF1_ HYST Activates the hysteresis of the zero-marking-pulse logic of channel 1 (only works when the hysteresis of channel 1 in mode register 1 is active). HZ = "1")

0 Zero-marking-pulse hysteresis off

1 Zero-marking-pulse hysteresis on

6.4.5 Interrupt Mask (16-Bit Register, Addresses x+4 and x+5)

The interrupt mask can be read and written with both 16-bit and 8-bit accesses. The interrupts of the SMP16-SFT251 can be masked in this register. This register does not contain interrupts INT0 and INT1. For SMP-E251 compatibility's sake, these interrupts are contained in control register 0.

Bit	7	6	5	4	3	2	1	0
Name	x	x	x	INT0_C13*	CR10_INT	ZS30_INT	ZS10_INT	CB0_INT
Bit	15	14	13	12	11	10	9	8
Name	x	x	x	x	CR11_INT	ZS31_INT	ZS11_INT	CB1_INT

CB0_INT Masks out the overflow of counting channel 0 from the INT2 interrupt request
- 0 INT2 disabled when overflow occurs
- 1 INT2 enabled when overflow occurs

ZS10_INT Masks out the ZS10 signal from the INT2 interrupt request
- 0 INT2 request disabled
- 1 INT2 request enabled

ZS30_INT Masks out the ZS30 signal from the INT2 interrupt request
- 0 INT2 request disabled
- 1 INT2 request enabled

CR10_INT Masks out comparator 1 of channel 0 (CR10) from group interrupt INT4
- 0 INT4 function of CR10 disabled
- 1 INT4 function of CR10 enabled

INT_C13* Switches off interrupt INT0 on bus plug-connector pin c13
- 0 INT0 on pin c13 enabled
- 1 NT0 on pin c13 disabled

CB1_INT Masks out the overflow of the counter of channel 1 from the INT3 interrupt request
- 0 INT3 disabled when overflow occurs
- 1 IINT3 enabled when overflow occurs

ZS11_INT Masks out the ZS11 signal from the INT3 interrupt request
- 0 INT3 request disabled
- 1 INT3 request enabled

ZS31_INT Masks out the ZS31 signal from the INT3 interrupt request
- 0 INT3 request disabled
- 1 IINT3 request enabled

CR11_INT Masks out comparator 1 of channel 1 (CR11) from group interrupt INT5
- 0 INT5 function of CR11 disabled
- 1 INT5 function of CR11 enabled

6.4.6 Interrupt Register, Channel 0 and Channel 1

With the interrupt registers of the counter blocks of channel 0 and channel 1, an arriving zero-marking pulse sets bit 0 to "1." Reading a zero-marking-pulse buffer resets the bit on the particular channel.

The address of the interrupt register of channel 1 varies depending on the status of the BG_Mode bit in control register 0 (bit 4).

BG_Mode	Address Interrupt Register, Counting Channel 0	Address Interrupt Register, Counting Channel 1
0	w	w + 8
1	w	w + 1

Bit	7	6	5	4	3	2	1	0
Name	x	x	x	x	x	x	x	INT

INT Zero-marking-pulse signal arrived at the counter. (Counter status was stored in the zero-marking-pulse buffer.)

0 Interrupt flag not set

1 Interrupt flag set

6.4.7 Status Register 0

The addresses of the two status registers (0 and 1) vary depending on the status of the BG_Mode bit in control register 0 (bit 4).

BG_Mode	Address, Status Register 0	Address, Status Register 1
0	w + 6	w + 7
1	w + A	w + B

Bit	7	6	5	4	3	2	1	0
Name	EX0	AL0	EX1	AL1	SCH0	SCH1	REF1	REF0

EX0 INT1 request by ZS00
0 No INT1 request
1 INT1 request triggered

AL0 INT1 request by ZS20
0 No INT1 request
1 INT1 request triggered

EX1 INT1 request by ZS01
0 No INT1 request
1 INT1 request triggered

AL1 INT1 request by ZS21
0 No INT1 request
1 INT1 request triggered

SCH0 Write protection for counting channel 0
0 Set
1 Not set

SCH1 Write protection for counting channel 1
0 Set
1 Not set

REF1 INT0 request of counting channel 1 (same as counter-interrupt flag in the interrupt register)
0 No INT0 request
1 INT0 interrupt of channel 1 is queued.

REF0 INT0 request of counting channel 0 (same as counter-interrupt flag in the interrupt register)
0 No INT0 request
1 INT0 request of channel 0 is queued.

6.4.8 Status Register 1

The addresses of the two status registers (0 and 1) vary depending on the status of the BG_Mode bit in control register 0 (bit 4).

BG_Mode	Address, Status Register 0	Address, Status Register 1
0	w + 6	w + 7
1	w + A	w + B

Bit	7	6	5	4	3	2	1	0
Name	Q1	Q0	REFE1	REFE0	ZR1	ZR0	CB1	CB0

Q1 Intermediately stored zero-marking-pulse signal of channel 1 (is reset with the "cancel counter write protection" or "reset zero-marking-pulse latch" command)

0 Not set

1 Set

Q0 Intermediately stored zero-marking-pulse signal of channel 0 (is reset with the "cancel counter write protection" or "reset zero-marking-pulse latch" command)

0 Not set

1 Set

REFE1 Current state of the zero-marking-pulse signal of channel 1 (not stored intermediately)

0 Not set

1 Set

REFE0 Current state of the zero-marking-pulse signal of channel 0 (not stored intermediately)

0 Not set

1 Set

ZR1 Counting direction of channel 1

0 Down

1 Up

ZR0 Counting direction of channel 0

0 Down

1 Up

CB1 Intermediately stored overflow indication of channel 1 (can be reset with the "reset alarm bits" command)

0 No overflow

1 Overflow

CB0 Intermediately stored overflow indication of channel 0 (can be reset with the "reset alarm bits" command)

0 No overflow

1 Overflow

6.4.9 Status Register 2 (16-Bit Register, Addresses x+6 and x+7)

Both 16-bit and 8-bit accesses can be used for status register 2.

Bit	7	6	5	4	3	2	1	0
Name	x	x	x	TOR0	CR_10	ZS30	ZS10	CB0

CB0 Intermediately stored overflow indication of channel 0 (can be reset with the "reset alarm bits" command)

0 No overflow

1 Overflow

ZS10 Status bit for the INT2 request of signal ZS10 (regardless of the ZS10_INT setting in control register 1). ZS10 is stored intermediately and is reset by the CLR_INT2 bit in the clear register.

0 No INT2 request by ZS10

1 INT2 request by ZS10

ZS30 Status bit for the INT2 request of signal ZS30 (regardless of the ZS30_INT setting in control register 1. ZS30 is stored intermediately and is reset by the CLR_INT2 bit in the clear register.

0 No INT2 request by ZS30

1 INT2 request by ZS30

CR_10 Indicates whether or not the counter status of channel 0 and the contents of UREG_10 are equal. The bit is stored intermediately and is reset by the CLR_INT4 bit in the clear register.

0 Counter status of channel 0 not equal to UREG_10

1 Counter status of channel 0 equals UREG_10 (INT4 request).

TOR0 Status of the gate of channel 0 (only valid when "frequency and pulse width measurement" is activated in mode register 0 of channel 0. PD = "1")

0 Gate closed. No clock pulses are being counted.

1 Gate open. Clock pulses are being counted.

Bit	15	14	13	12	11	10	9	8
Name	x	x	x	TOR1	CR_11	ZS31	ZS11	CB1

CB1 Intermediately stored overflow indication of channel 1 (can be reset with the "reset alarm bits" command)

0 No overflow

1 Overflow

ZS11 Status bit for INT3 request of signal ZS11 (regardless of the ZS_11_INT setting in control register 2). ZS11 is stored intermediately and is reset by the CLR_INT3 bit in the clear register.

0 No INT3 request by ZS11

1 INT3 request by ZS11

ZS31 Status bit for the INT3 request of signal ZS31 (regardless of the ZS31_INT setting in control register 2). ZS31 is stored intermediately and is reset by bit CLR_INT3 in the clear register.

0 No INT3 request by ZS31

1 INT3 request by ZS31

CR_11 Indicates whether or not the counter state of channel 1 equals UREG_11. The bit is stored intermediately and is reset with bit CLR_INT5 in the clear register.

0 Counter state of channel 1 not equal UREG_11

1 Counter state of channel 1 equals UREG_11 (INT5–request).

TOR1 Status of the gate of channel 1 (only valid when "frequency or pulse width measurement" is activated in mode register 1 of channel 1. PD = "1")

0 Gate closed. No clock pulses are being counted.

1 Gate open. Clock pulses are being counted.

6.4.10 Clear Register (16-Bit Register, Addresses x+6 and x+7)

The clear register can be used to reset waiting interrupt or status signals. This function is executed when the register, in which the appropriate bits of the signals to be deleted are set, is write-accessed.

Bit	7	6	5	4	3	2	1	0
Name	x	CLR_INT4_CR0	CLR_INT2_CB0	CLR_INT2_30	CLR_INT2_10	CLR_INT1_20	CLR_INT1_00	CLR_INT0_0

CLR_INT0_0 Deletes the INT0 request of channel 0. Functions like the read-access to the appropriate counting register.

0 No effect

1 Reset INT0 request of channel 0 and the Q0 status signals in status register 1

CLR_INT1_00 Deletes the INT1 request of the ZS00 signals and resets the related status bits

0 No effect

1 Reset the INT1 request of special signal ZS00 and status signal EX0 in status register 0

CLR_INT1_20 Deletes the INT1 request of the ZS20 signals and resets the related status bits

0 No effect

1 Reset the INT1 request of special signal ZS20 and status signal AL0 in status register 0

CLR_INT2_10 Deletes the INT2 request of the ZS10 signals and resets the related status bits

0 No effect

1 Reset the INT2 request of special signal ZS10 and status signal ZS10 in status register 2

CLR_INT2_30 Deletes the INT2 request of the ZS30 signals and resets the related status bits

0 No effect

1 Reset the INT2 request of special signal ZS30 and status signal ZS30 in status register 2

CLR_INT2_CB0 Deletes the INT2 request of the counter overflow of channel 0

0 No effect

1 Reset the INT2 request of the overflow of channel 0

CLR_INT4_CR0 Deletes the INT4 request of the comparison register of channel 0, including the related CR10 status bit in status register 2

0 No effect

1 Reset the INT4 request of the comparison register

Bit	15	14	13	12	11	10	9	8
Name	x	CLR_INT5_CR1	CLR_INT3_CB1	CLR_INT3_31	CLR_INT3_11	CLR_INT1_21	CLR_INT1_01	CLR_INT0_1

CLR_INT0_1 Deletes the INT0 request of channel 1. Functions the same as reading out the applicable counting register.

0 No effect

1 Resets the INT0 request of channel 1 and the Q1 status signals of status register 1

CLR_INT1_01 Deletes the INT1 request of the ZS01 signals and resets the related status bits

0 No effect

1 Reset the INT1 request of special signal ZS01 and status signal EX1 in status register 0

CLR_INT1_21 Deletes the INT1 request of the ZS21 signals and resets the related status bits

0 No effect

1 Reset the INT1 request of special signal ZS21 and status signal AL1 in status register 0

CLR_INT3_11 Deletes the INT3 request of the ZS11 signals and resets the related status bits

0 No effect

1 Reset the INT3 request of special signal ZS11 and status signal ZS11 in status register 2

CLR_INT3_31 Deletes the INT3 request of the ZS31 signals and resets the related status bits

0 No effect

1 Reset the INT3 request of special signal ZS31 and status signal ZS31 in status register 2

CLR_INT3_CB1 Deletes the INT3 request of the counter overflow of channel 1

0 No effect

1 Reset the INT3 request of the overflow of channel 1

CLR_INT5_CR1 Deletes the INT5 request of the comparison register of channel 1, including the related CR11 status bit in status register 2

0 No effect

1 Reset the INT5 request of the comparison register

6.5 Times

6.5.1 Read/Write Accesses

Read/write accesses require a minimum command time of 100 nsec. No recovery time is required between two commands.

6.5.2 Board Commands

BG_Mode = "0"

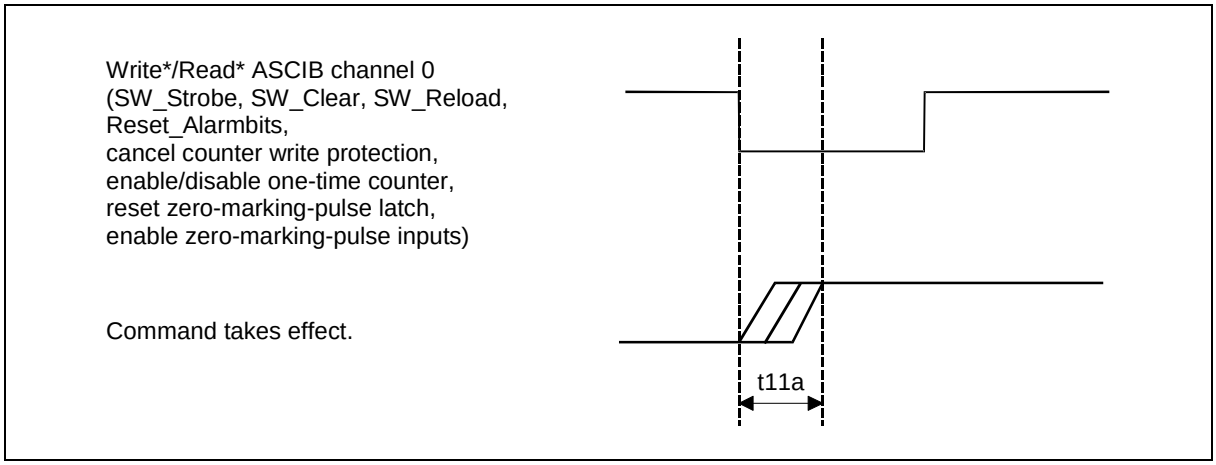


Figure 6.5 Times of the board commands with BG_Mode = "0"

BG_Mode = "1"

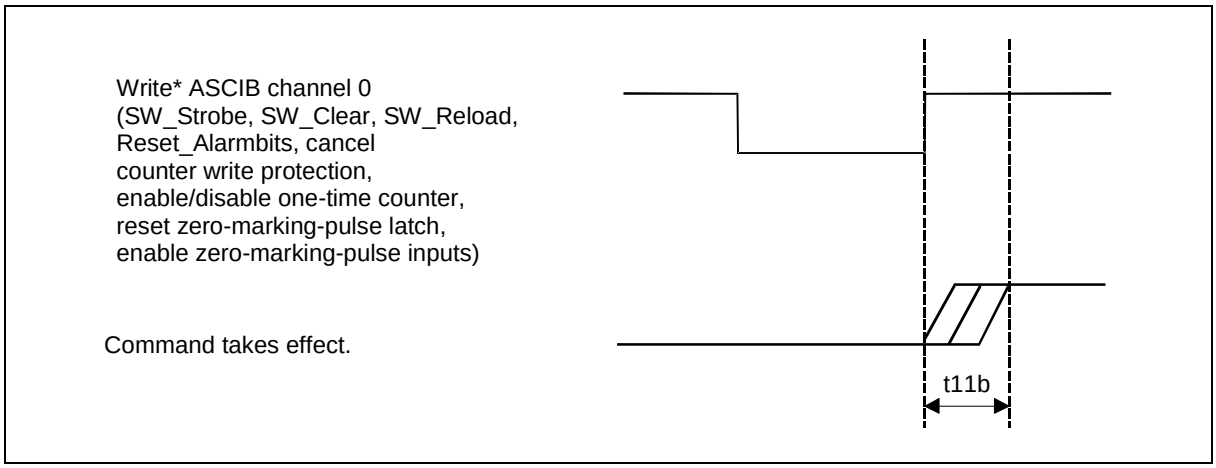


Figure 6.6 Times of the board commands with BG_Mode = "1"

t11a	Command → effect	Max. of 125 nsec
t11b	Command → effect	Max. of 160 nsec

Time interval t11b is ensured by an onboard-ready controller which delays all later commands up to 250 nsec after the rising edge of the write signal.

7 Sample Programs

7.1 Position Acquisition with Hardware Support (BG_Mode = "0")

Prerequisites:

- Base address for ASBIC channel 0 = 400hex
- The "ext. strobe channel n" bits must be activated on the parallel output port of the ASBIC.

```
/*******************************************************
** Initialize board:
*******************************************************/
// Enable zero-marking-pulse inputs
outportb (0x414,0x00);

// Cancel counter write protection for counting channel 0
dummy = inportb(0x411);

// Specify mode register for counting channel 0
// Position acquisition without hysteresis. Quadruple edge evaluation.
outportb(0x405,0x00);

// Cancel counter write protection for counting channel 1
dummy = inportb(0x412);

// Specify mode register for counting channel 1
//Position acquisition without hysteresis. Double edge evaluation.
outportb(0x40D,0x01);

// Setting the operating mode:
// Counting channel 0: Activate hardware support, with one-time counter
// Counting channel 1: Activate hardware support, without one-time counter
// Interrupts are disabled
// Board mode BG_MODE = 0
outportb(0x406,0x02);

// Enable one-time counter for counting channel 0
outportb(0x411,0x00);

// Initialize counter (e.g., by setting to "00000000" with SW-CLEAR):
outportb(0x40E,0x00);
outportb(0x40F,0x00);

/*************************************************************
** Main program
*************************************************************/

// The status registers can be scanned cyclically in a loop to determine
// whether a zero-marking pulse has arrived on one of the counting channels.
// Zero-marking pulse arrived on channel 0?
Q0 = inportb(0x407) & 0x40;
```

```
// If yes, then execute instructions
if (Q0)
{
   // Cancel counter write protection for channel 0
   inportb(0x411);

   // Enable one-time counter for channel 0
   outportb(0x411,0x00);

   // Read counter with byte-accesses
  CNT00 = inportb(0x401);
  CNT01 = inportb(0x402);
  CNT02 = inportb(0x403);
  CNT03 = inportb(0x404);
}

// Zero-marking pulse arrived on channel 1?
Q1 = inportb(0x407) & 0x80;

// If yes, then execute instructions
if (Q1)
{
   // Cancel counter write protection for channel 1
   inportb(0x412);

   // Read counter with byte-accesses
  CNT10 = inportb(0x409);
  CNT11 = inportb(0x40A);
  CNT12 = inportb(0x40B);
  CNT13 = inportb(0x40C);
}
```

The determined counter states can now be processed further.

The counter status can also be scanned with SW strobe commands. Just keep in mind that the SW strobe only works when the write protection of the respective channel is not set.

```
// Example: SW strobe for channel 0
 outportb(0x400,0x00);
// Read counter with byte-accesses
 CNT00 = inportb(0x401);
 CNT01 = inportb(0x402);
 CNT02 = inportb(0x403);
 CNT03 = inportb(0x404);
```

7.2 Position Acquisition without Hardware Support (BG_Mode = "1")

Prerequisites:

- Base address for ASBIC channel 0 = 400hex
- The "ext. strobe, channel n" bits are deactivated on the parallel output port of the ASBIC.

```
/*******************************************************
** Initialize board:
*******************************************************/

// Switch board mode:
 outportb(0x406,0x10);

// Cancel counter write protection for counting channels 0 and 1
 outport(0x400,0x3000);

// Specify mode register for counting channels 0 and 1
// Channel 0:  Position acquisition without hysteresis. Quadruple edge evaluation.
// Channel 1:  Position acquisition without hysteresis. Double edge evaluation.
outport(0x40A,0x0100);

// Set the operating mode:
// Counting channel 0:  Deactivate hardware support
// Counting channel 1:  Deactivate hardware support
// Interrupts are disabled
// Board mode BG_MODE = 1
outport(0x40C,0x0015);

// Initialize counter (e.g., set to "00000000" with SW-CLEAR)
outport(0x400,0x0300);

/*************************************************************
** Main program
*************************************************************/

// The counter states can be read cyclically in a loop.

// SW strobe for channels 0 and 1
 outport(0x400, 0xC000);

// Read counter 0 with word-accesses
 CNT00 = inport(0x402);
 CNT01 = inport(0x404);

// Read counter 1 with word-accesses
 CNT10 = inport(0x406);
 CNT11 = inport(0x408);
```

The determined counter states can now be processed further.

7.3 Frequency and Pulse Width Measurement without Using the Zero-Marking-Pulse Input

The example illustrates a measurement with counting channel 0.

Prerequisites:

- Base address for ASBIC channel 0 = 400hex, for ASBIC channel 1 = 420hex
- The "ext. strobe, channel 0" bit is deactivated on the parallel output port of the ASBIC.
- The board is run in expanded mode (BG_MODE = "1").

```
/*******************************************************
** Initialize board:
*******************************************************/
// Switch board mode:
 outportb(0x406,0x10);

// Cancel counter write protection for counting channel 0
 outport(0x400,0x1000);

// Specify mode register for counting channel 0
// Channel 0: Frequency/pulse width measurement, gate is level-controlled, counting direction is up
outport(0x40A,0x0080);

// Set the operating mode:
// Counting channel 0: Deactivate hardware support
// Interrupts are disabled
// Board mode BG_MODE = 1
outport(0x40C,0x0014);

// Initialize counter (set to "00000000" with SW-CLEAR)
outport(0x400,0x0100);

/*************************************************************
** Main program
*************************************************************/
// Wait in a loop for the gate to open
// (by scanning status bit TOR0 in status register 2)
while (!GATE)
   GATE = inport(0x426) & 0x0010;

// When the gate is open, wait until it closes again.
while (GATE)
   GATE = inport(0x426) & 0x0010;

// At the end of the gate, the counter status can be stored in the zero-
// marking-pulse buffer with an SW strobe.
outport(0x400, 0x4000);

// Read counter 0 with word-accesses
 CNT00 = inport(0x402);
 CNT01 = inport(0x404);
```

When the gate width is known, the counter status can then be used to determine the desired frequency. When the frequency is known, the counter status can then be used to determine the desired gate width.